# Si2163

## DVB-C Demodulator

## Description

The Si2163 is a compact, standalone DVB-C digital TV demodulator ideally matching Silicon Labs' Si2170/1/2 new hybrid silicon tuner product family. The analog front-end consists of two ADCs with wide dynamic range (12-bit) to allow operation with standard IF (~36 MHz), Low-IF, or Zero-IF inputs. This enables the use of the Si2163 with any TV tuner, either metal can or silicon tuner based. The Si2163 supports ITU J.83 annex A/C and DVB-C (EN 300 429) and accepts symbol rates from 1 to 7.2 MSymbol/s.

The Si2163 includes a user-configurable 31-tap equalizer for optimum reception even in case of difficult network conditions, such as long echoes.

Serial or parallel master MPEG TS output modes are supported. Furthermore, a TS slave parallel mode is available via a GPIF port and provides glue less interface to Silicon Labs' MCU devices with embedded USB interface. The user can optionally program a 32-PID hardware filter to reduce the output TS bit rate (or add more TS security for Pay-TV channels).

The Si2163 supports ultra-fast channel scanning operations for VHF/UHF digital cable channels, thanks to an embedded DSP. For supported tuners, the complete algorithm for fast channel scan, *QuickScan*, is provided as a downloadable patch file. *QuickScan* runs on the embedded DSP to limit the host CPU / MPEG decoder software burden.

An internal $I^2C$ pass-through logic switch acts as an $I^2C$ repeater and provides a "quiet" $I^2C$ bus to the RF front end.

A maximum of six general-purpose inputs/outputs are available; three GPIOs also feature Δ/Σ and interrupt output capabilities.

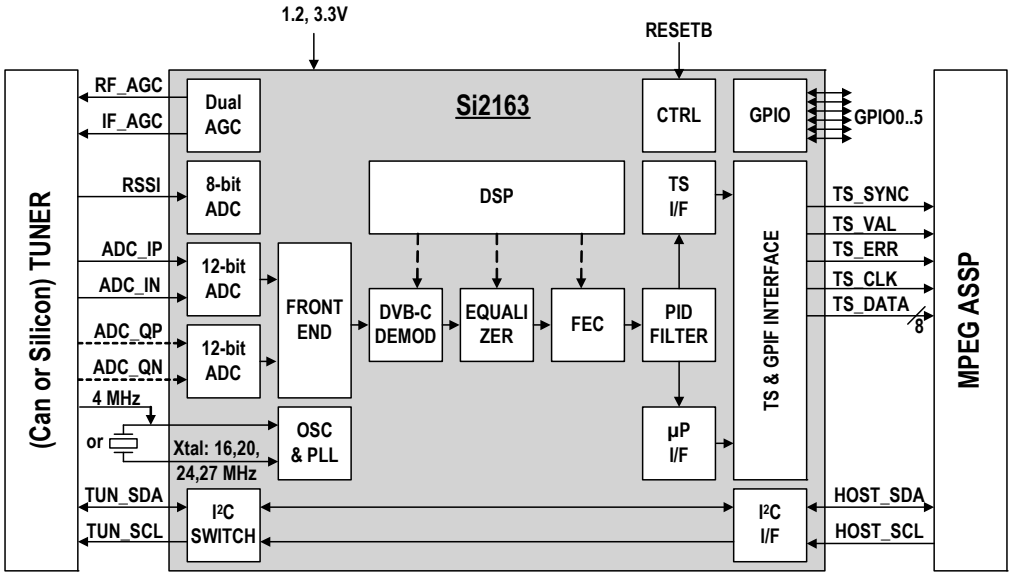
Best-in-class demodulation performance is achieved while still maintaining very low-power operation. The Si2163 guarantees a low-cost system implementation due to its minimal BOM and very small package footprint. The Si2163 remains pin-to-pin compatible with Si2161 (DVB-T) and Si2165 (DVB-T/C) devices.

## Features

- ITU J.83 Annex A/C and DVB-C (EN 300 429) compliant
- NorDig Unified 2.0 and C-Book compliant
- Suitable for low power design: 120 mW (typical, 36 MHz IF normal sampling mode)
- Dual 12-bit ADCs: accept 1st IF, low IF, or zero-IF inputs.
- Symbol rate from 1 to 7.2 MBaud
- Independent AGC controls (for IF & RF), plus RSSI measurement
- On-chip ACI filtering: fixed 8 MHz SAW filter even for low symbol rates
- Ultra fast, DSP controlled, automatic UHF/VHF band scanning (*QuickScan*)
- Master TS output modes, parallel or serial (with tri-state function)
- Slave TS parallel output: external device polls data from an embedded FIFO, providing a seamless interface to any USB controller.
- On-chip PID filtering to reduce TS output bit rate
- Up to six GPIOs
- Two 5 V tolerant $I^2C$ control buses (host-side, tuner-side) with on-chip $I^2C$ logic switch.
- 4, 16, 20, 24, or 27 MHz clock/crystal reference
- 3.3 and 1.2 V power supplies only
- Very compact QFN-36, 5 x 6 mm, RoHS compliant package

## Applications

- Digital cable STB, NIM, and iDTV set
- Cable enabled Personal Video Recorder (DVD or HDD-based)
- Digital cable PC-TV card or peripheral

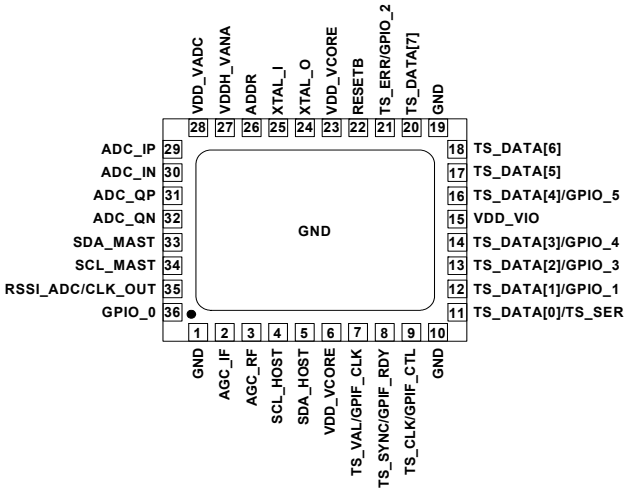


## Selected Electrical Specifications

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| **General** | | | | |
| Ambient Temperature | 0 | 25 | 85 | °C |
| Power-up Time | — | — | 10 | ms |
| $I^2C$ Speed (Host side) | <1 | — | 400 | kHz |
| Input Clock or Supported Xtal Frequency | — | 4*/16/20/24/27 | — | MHz |
| VDD_VCORE Supply | 1.14 | 1.2 | 1.26 | V |
| VDD_VIO Supply** | 1.62 | 1.80 to 3.30 | 3.60 | V |
| VDD_VADC | 1.14 | 1.2 | 1.26 | V |
| VDDH_VANA | 3.00 | 3.30 | 3.60 | V |
| **Input ADC (2 x 12-bits)** | | | | |
| Input Differential Voltage Range | — | 1 | — | Vpp |
| IF Oversampling Mode Clock | 37 | 48 | 60 | MHz |
| IF Sub-sampling Mode Clock | 18.5 | 27 | 32.5 | MHz |
| ZIF Mode Sampling Clock | 18.5 | 48 | 60 | MHz |
| System Clock | — | — | 85 | MHz |
| **TS Output Rates** | | | | |
| Serial Mode Clock | — | — | 65 | MHz |
| **Power Consumption** | | | | |
| DVB-C, 6.9 MBaud, 256 QAM (adc_clk @ 56 MHz), Parallel TS | — | 120 | — | mW |
| Total Stand-by Power Consumption | — | 13 | — | mW |

***Note:** Clock only.
****Note:** 5 V tolerant $I^2C$ bus requires VDD_VIO supply set @ 3.3 V.

## Pin Assignments




## 5 x 6 mm SLP QFN-36 Package Information