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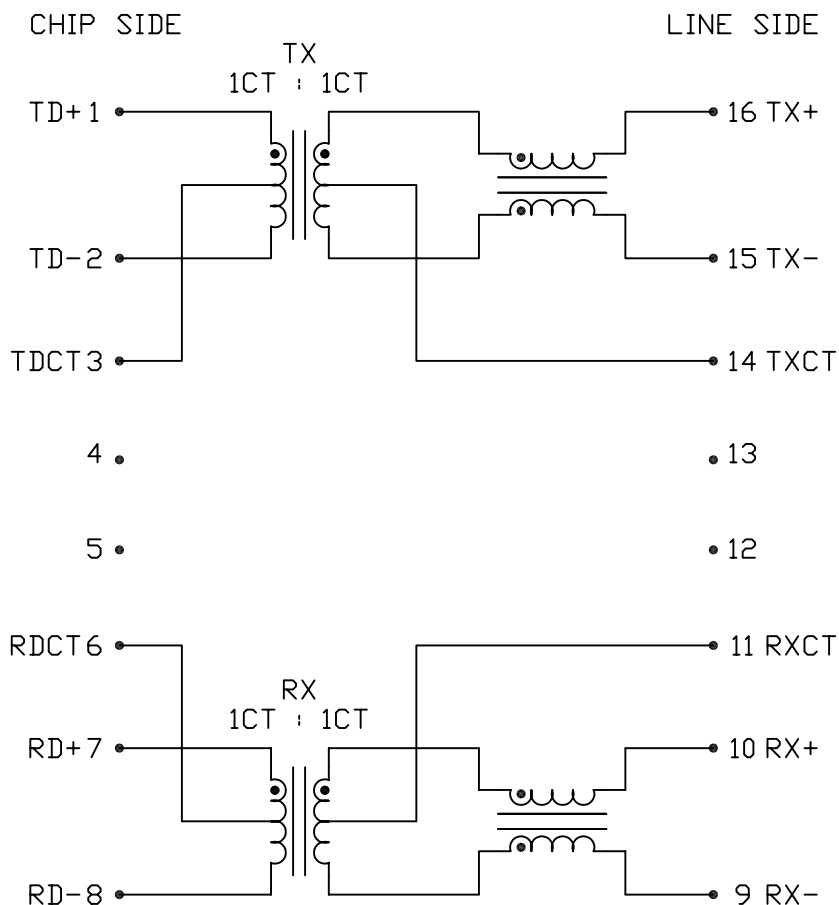
PRELIMINARY

ELECTRICAL CHARACTERISTICS @ 25°C

RoHS



SCHEMATIC



URNS RATIO

Tx (1-3-2) : (16-14-15)
Rx (7-6-8) : (10-11-9)

1CT : 1CT
1CT : 1CT

POLARITY

PER DOT CONVENTION

DCL

1-2 = 7-8

350μH MIN
@100kHz, 100mV W/8mA DC BIAS

LEAKAGE INDUCTANCE, Le
CHIP SIDE WITH LINE SIDE SHORT

0.4μH MAX
@1MHz, 20mV

INTERWINDING CAPACITANCE, Cw/w
CHIP SIDE TO LINE SIDE

25pF MAX
@1MHz, 20mV

DC RESISTANCE
(1-2) = (7-8)

1.3Ω MAX

INSERTION LOSS
@100kHz TO 80MHz

1.0dB MAX

RETURN LOSS (UNDER 100Ω ±15% ENVIRONMENT)
@0.5 TO 30 MHz
@30 TO 60 MHz
@60 TO 80 MHz

16dB MIN
16-20LOG(f/30MHz) dB MIN
10dB MIN

COMMON TO COMMON MODE ATTENUATION
@0.1 TO 80 MHz
@80 TO 125 MHz
@125 TO 250 MHz

38dB MIN
30dB MIN
10dB MIN

CROSSTALK
@0.1 TO 80 MHz
@80 TO 125 MHz
@125 TO 250 MHz

38dB MIN
30dB MIN
10dB MIN

COMMON TO DIFFERENTIAL MODE ATTENUATION
@0.1 TO 80 MHz
@80 TO 125 MHz
@125 TO 250 MHz

38dB MIN
30dB MIN
10dB MIN

HIPOT

1500Vrms

OPERATING TEMPERATURE -40°C TO +85°C

ORIGINATED BY	DATE	TITLE	PART NO. / DRAWING NO.	STANDARD DIM. TOL. IN INCH	[] METRIC DIM. AS REFERENCE
CH Chan	2013-05-03	10/100BASE-T MODULE S558-5999-W2-F	X5585999W2-F	.X	UNIT : INCH [mm] REV. : PB
DRAWN BY	DATE		FILE NAME	.XX	SCALE : N/A SIZE : A4
ZC Guo	2013-05-03		X5585999W2FPB.DWG	.XXX	PAGE : 2

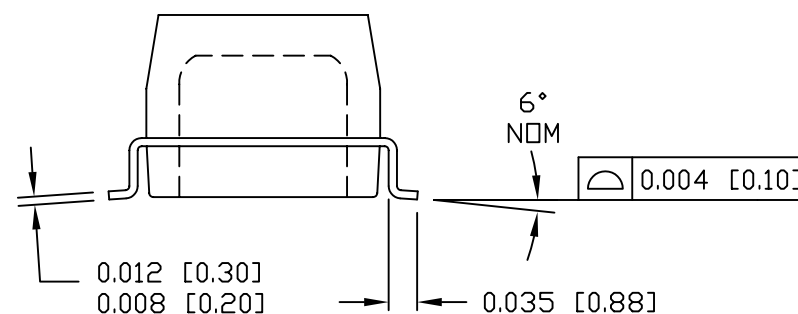
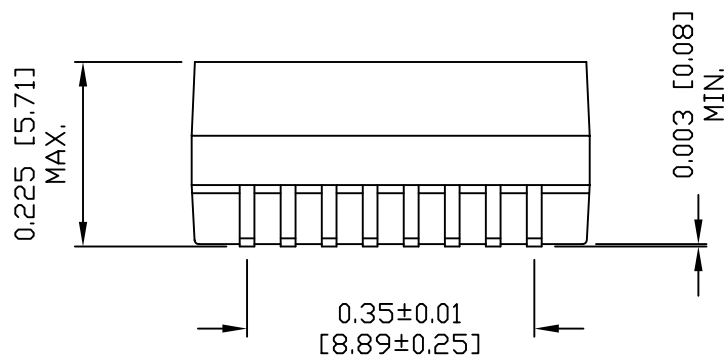
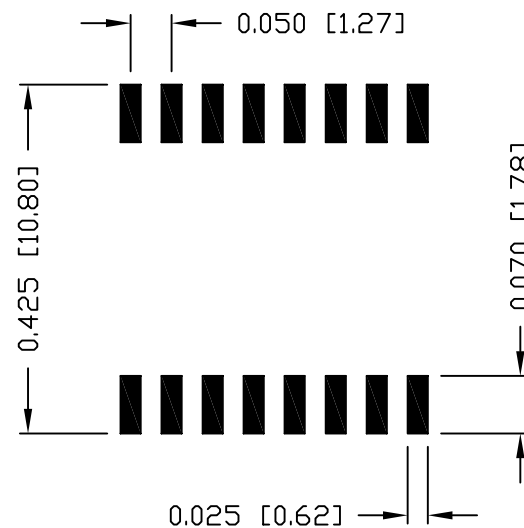
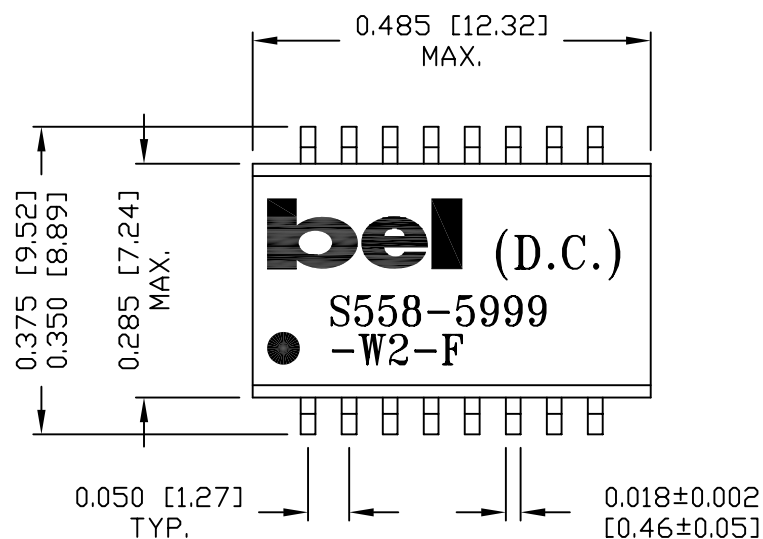


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PRELIMINARY

SUGGESTED PCB PAD LAYOUT

RoHS



NOTES:

1. STANDARD MARKING REFER TO DOC. HAND-WORK-04.
2. PACKAGE CODE: "QBS001".

ORIGINATED BY	DATE	TITLE	PART NO. / DRAWING NO.	STANDARD DIM.		[] METRIC DIM. AS REFERENCE	
				TOL.	INCH	UNIT : INCH [mm]	REV. : PB
Lawrence Tsang	2013-05-03	MECHANICAL DRAWING	X5585999W2-F	.X		SCALE : N/A	SIZE : A4
DRAWN BY	DATE	S558-5999-W2-F	FILE NAME	.XX	±0.01		PAGE : 3
				.XXX	±0.005		
ZC Guo	2013-05-03		X5585999W2FPB.DWG				

