S70FL01GS

1 Gbit (128 Mbyte) MirrorBit® Flash Non-Volatile Memory
CMOS 3.0 Volt Core
Serial Peripheral Interface with Multi-I/O

Data Sheet *(Preliminary)*

Notice to Readers: This document states the current technical specifications regarding the Spansion product(s) described herein. Each product described herein may be designated as Advance Information, Preliminary, or Full Production. See *Notice On Data Sheet Designations* for definitions.

Publication Number S70FL01GS_00 **Revision** 02 **Issue Date** April 25, 2013

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***Data Sheet** (Preliminary)*

Features

- **Serial Peripheral Interface (SPI)**
  - SPI Clock polarity and phase modes 0 and 3
  - Double Data Rate (DDR) option
  - Extended Addressing: 32-bit address
  - Serial Command set and footprint compatible with S25FL-A, S25FL-K, and S25FL-P SPI families
  - Multi I/O Command set and footprint compatible with S25FL-P SPI family
- **READ Commands**
  - Normal, Fast, Dual, Quad, Fast DDR, Dual DDR, Quad DDR
  - AutoBoot – power up or reset and execute a Normal or Quad read command automatically at a preselected address
  - Common Flash Interface (CFI) data for configuration information
- **Programming (1.5 Mbytes/s)**
  - 512-byte Page Programming buffer
  - Quad-Input Page Programming (QPP) for slow clock systems
- **Erase (0.5 Mbytes/s)**
  - Uniform 256-kbyte sectors
- **Cycling Endurance**
  - 100,000 Program-Erase Cycles on any sector typical
- **Data Retention**
  - 20 Year Data Retention typical

Security Features

- **One Time Program (OTP) array of 1024 bytes**
- **Block Protection**
  - Status Register bits to control protection against program or erase of a contiguous range of sectors.
  - Hardware and software control options
  - Advanced Sector Protection (ASP)
  - Individual sector protection controlled by boot code or password
- **Spansion 65 nm MirrorBit Technology with Eclipse™ Architecture**
- **Core Supply Voltage: 2.7V to 3.6V**
- **I/O Supply Voltage: 1.65V to 3.6V**
- **Temperature Range:**
  - Industrial (-40°C to +85°C)
  - Automotive In-Cabin (-40°C to +105°C)
- **Packages (all Pb-free)**
  - 16-lead SOIC (300 mils)

General Description

This document contains information for the S70FL01GS device, which is a dual die stack of two S25FL512S die. For detailed specifications, please refer to the discrete die data sheet:

Document	Publication Identification Number (PID)
S25FL512S Data Sheet	S25FL512S_00

Publication Number S70FL01GS_00 **Revision** 02 **Issue Date** April 25, 2013

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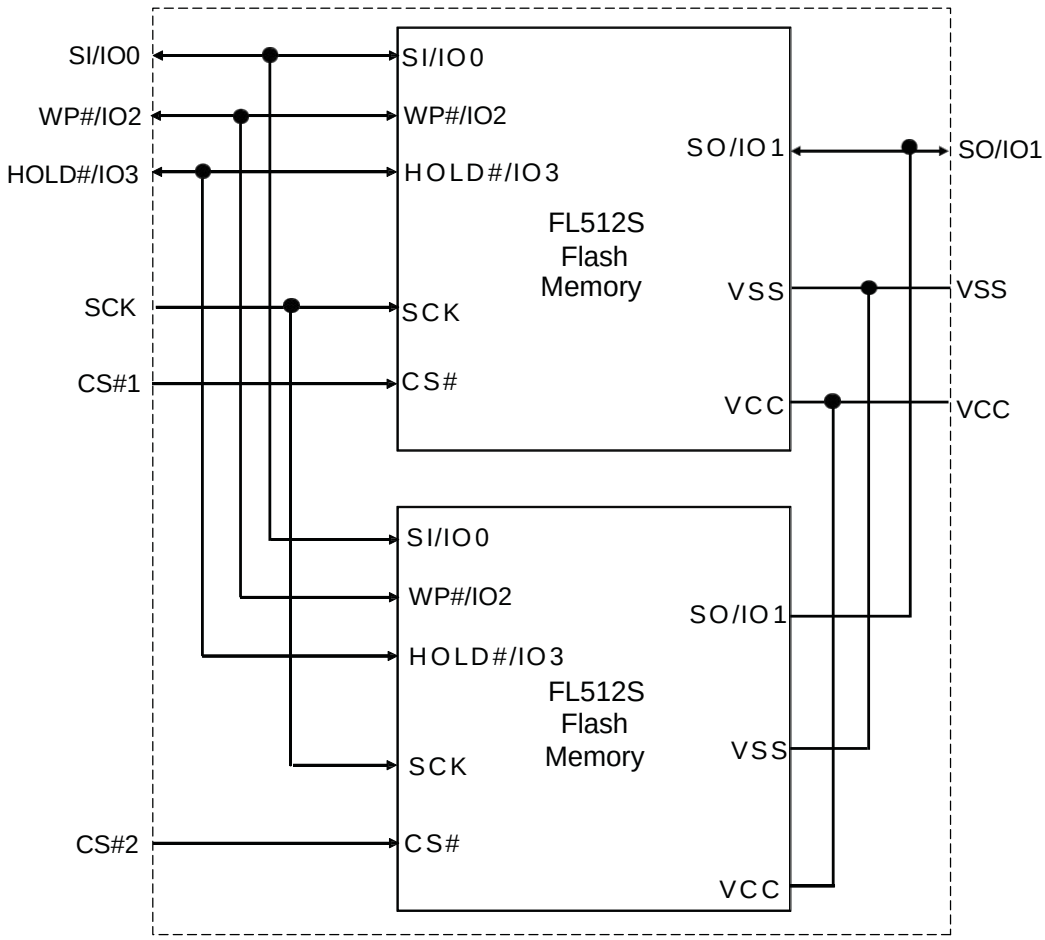
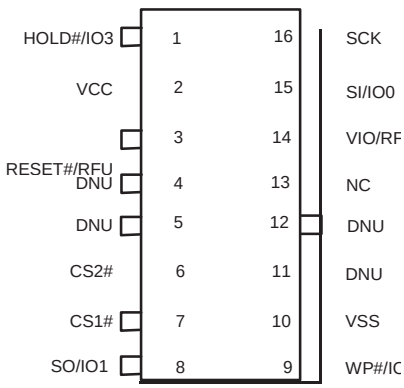


2. Connection Diagrams

Figure 2.1 16-pin Plastic Small Outline Package (SO)



Note:

1. V_{IO} (pin 14) is not supported in the S70FL01GS device and is RFU. Refer to Section 8. for more details.

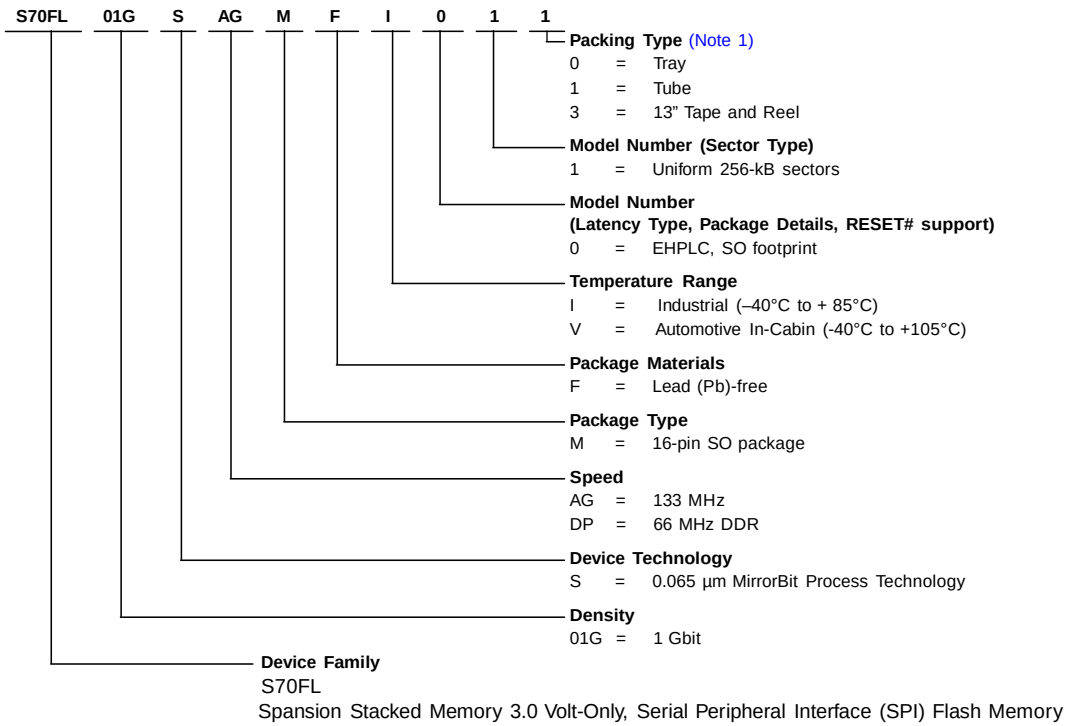
3. Input/Output Summary

Table 3.1 Signal List

Signal Name	Type	Description
RESET#	Input	**Hardware Reset:** Low = device resets and returns to standby state, ready to receive a command. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used.
SCK	Input	**Serial Clock.**
CS#	Input	**Chip Select.**
SI / IO0	I/O	**Serial Input** for single bit data commands or IO0 for Dual or Quad commands.
SO / IO1	I/O	**Serial Output** for single bit data commands. IO1 for Dual or Quad commands.
WP# / IO2	I/O	**Write Protect** when not in Quad mode. IO2 in Quad mode. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad commands.
HOLD# / IO3	I/O	**Hold** (pause) serial transfer in single bit or Dual data commands. IO3 in Quad-I/O mode. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad commands.
V_{CC}	Supply	**Core Power Supply.**
V_{IO}	Supply	**Versatile I/O Power Supply. Note:** V_{IO} is not supported in the S70FL01GS device. Refer to Section 8. for more details.
V_{SS}	Supply	**Ground.**
NC	Unused	**Not Connected.** No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a Printed Circuit Board (PCB). However, any signal connected to an NC must not have voltage levels higher than V_{CC}.
RFU	Reserved	**Reserved for Future Use.** No device internal signal is currently connected to the package connector but there is potential future use of the connector for a signal. It is recommended to not use RFU connectors for PCB routing channels so that the PCB may take advantage of future enhanced features in compatible footprint devices.
DNU	Reserved	**Do Not Use.** A device internal signal may be connected to the package connector. The connection may be used by Spansion for test or other purposes and is not intended for connection to any host system signal. Any DNU signal related function will be inactive when the signal is at V_{IL}. The signal has an internal pull-down resistor and may be left unconnected in the host system or may be tied to V_{SS}. Do not use these connections for PCB signal routing channels. Do not connect any host system signal to this connection.

4. Ordering Information

The ordering part number is formed by a valid combination of the following:



Notes:

1. *EHPLC = Enhanced High Performance Latency Code table.*
2. *Uniform 256-kB sectors = All sectors are uniform 256-kB with a 512B programming buffer.*

4.1 Valid Combinations

Table 4.1 lists the valid combinations configurations planned to be supported in volume for this device.

Table 4.1 S70FL01GS Valid Combinations Table

S70FL01GS Valid Combinations					
Base Ordering Part Number	**Speed Option**	**Package and Temperature**	**Model Number**	**Packing Type**	**Package Marking (1)**
S70FL01GS	AG	MFI	01	0, 1, 3	FL01GS+A+(temp)+F+(Model Number)
S70FL01GS	DP				FL01GS+D+(temp)+F+(Model Number)

Note:

1. *Package Marking omits the leading "S70" and package type.*

5. Device Operations

5.1 Programming

Each Flash die must be programmed independently due to the nature of the dual die stack.

5.2 Simultaneous Die Operation

The user may only access one Flash die of the dual die stack at a time via its respective Chip Select.

5.3 Sequential Reads

Sequential reads are not supported across the end of the first Flash die to the beginning of the second. If the user desires to sequentially read across the two die, data must be read out of the first die via CS1# and then read out of the second die via CS2#.

5.4 Sector/Bulk Erase

A sector erase command must be issued for sectors in each Flash die separately. Full device Bulk Erase via a single command is not supported due to the nature of the dual die stack. A Bulk Erase command must be issued for each die.

5.5 Status Registers

Each Flash die of the dual die stack is managed by its own Status Registers. Reads and updates to the Status Registers must be managed separately. It is recommended that Status Register control bit settings of each die are kept identical to maintain consistency when switching between die.

5.6 Configuration Register

Each Flash die of the dual die stack is managed by its own Configuration Register. Updates to the Configuration Register control bits must be managed separately. It is recommended that Configuration Register control bit settings of each die are kept identical to maintain consistency when switching between die.

5.7 Bank Address Register

It is recommended that the Bank Address Register bit settings of each die are kept identical to maintain consistency when switching between die.

5.8 ASP Register, Password Register, PPB Lock Register, PPB Access Register, DYB Access Register, DDR Data Learning Registers

It is recommended that the bit settings for all of the above registers in each die are kept identical to maintain consistency when switching between die.

5.9 Block Protection

Each Flash die of the dual die stack will maintain its own Block Protection. Updates to the TBPROT and BPNV bits of each die must be managed separately. By default, each die is configured to be protected starting at the top (highest address) of each array, but no address range is protected. It is recommended that the Block Protection settings of each die are kept identical to maintain consistency when switching between die. In addition, any update to the FREEZE bit must be managed separately for each die. If the FREEZE bit is set to a logic 1, it cannot be cleared to a logic 0 until a power-on-reset is executed on each die that has the FREEZE bit set to 1.

6. Read Identification (RDID)

The Read Identification (RDID) command outputs the one-byte manufacturer identification, followed by the two-byte device identification and the bytes for the Common Flash Interface (CFI) tables. Each die of the FL01GS dual die stack will have identical identification data as the FL512S die, with the exception of the CFI data at byte 27h, as shown in Table 6.1.

Table 6.1 Product Group CFI Device Geometry Definition

Byte	Data	Description
27h	1Bh	Device Size = 2^N byte

7. RESET#

Note that the hardware RESET# input (pin 3) is bonded out and active for the S70FL01GS device. For applications that do NOT require use of the RESET# pin, it is recommended to not use RESET# for PCB routing channels that would cause the RESET# signal to be asserted Low (V_{IL}). Doing so will cause the device to reset to standby state. The RESET# signal has an internal pull-up resistor and may be left unconnected in the host system if not used.

8. Versatile I/O Power Supply (V_{IO})

Note that the Versatile I/O (V_{IO}) power supply (pin 14) is not supported and pin 14 is RFU (Reserved for Future Use) in the standard configuration of the S70FL01GS device. Contact your local sales office to confirm availability with the V_{IO} feature enabled.

9. DC Characteristics

This section summarizes the DC Characteristics of the device.

Table 9.1 DC Characteristics

Symbol	Parameter	Test Conditions	Min	Typ (1)	Max	Unit
V_{IL}	Input Low Voltage		-0.5		0.2 x V_{CC}	V
V_{IH}	Input High Voltage		0.7 x V_{CC}		V_{CC}+0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA, V_{CC} = V_{CC} min			0.15 x V_{CC}	V
V_{OH}	Output High Voltage	I_{OH} = –0.1 mA	0.85 x V_{CC}			V
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max, V_{IN} = V_{IH} or V_{IL}			±4	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max, V_{IN} = V_{IH} or V_{IL}			±4	µA
I_{CC1}	Active Power Supply Current (READ)	Serial SDR @ 50 MHz Serial SDR @ 133 MHz Quad SDR @ 80 MHz Quad SDR @ 104 MHz Quad DDR @ 66 MHz Outputs unconnected during read data return (2)			18 36 50 61 75	mA
I_{CC2}	Active Power Supply Current (Page Program)	CS# = V_{CC}			100	mA
I_{CC3}	Active Power Supply Current (WRR)	CS# = V_{CC}			100	mA
I_{CC4}	Active Power Supply Current (SE)	CS# = V_{CC}			100	mA
I_{CC5}	Active Power Supply Current (BE) (3)	CS# = V_{CC}			100	mA
I_{SB} (Industrial)	Standby Current	RESET#, CS# = V_{CC}; SI, SCK = V_{CC} or V_{SS}, Industrial Temp		70	200	µA

Notes:

1. *Typical values are at T_{AI} = 25°C and V_{CC} = 3V.*
2. *Output switching current is not included.*
3. *Bulk Erase is on a per-die basis, not for the whole device.*

10. AC Test Conditions

Figure 10.1 Input, Output, and Timing Reference Levels

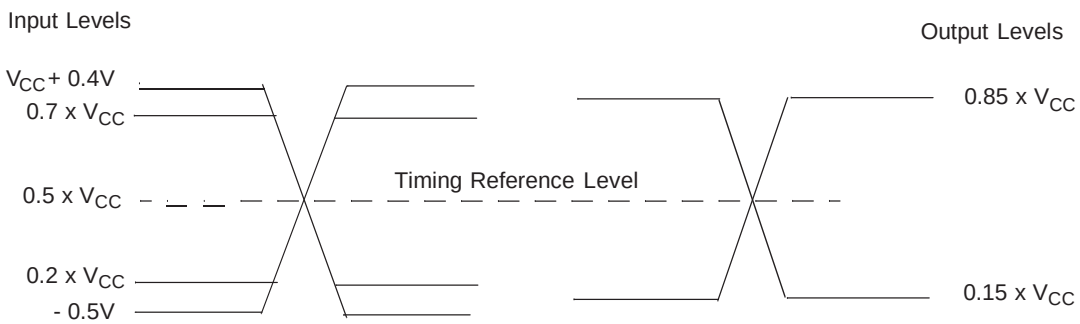


Figure 10.2 Test Setup

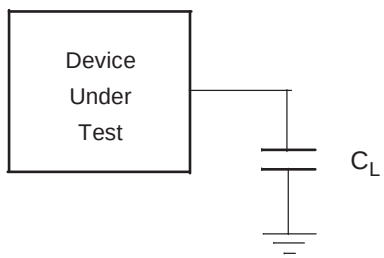


Table 10.1 AC Measurement Conditions

Symbol	Parameter	Min	Max	Unit
C_L	Load Capacitance		30 15 (4)	pF
	Input Rise and Fall Times		2.4	ns
	Input Pulse Voltage	0.2 x V_{CC} to 0.8 V_{CC}		V
	Input Timing Ref Voltage	0.5 V_{CC}		V
	Output Timing Ref Voltage	0.5 V_{CC}		V

Notes:

1. *Output High-Z is defined as the point where data is no longer driven.*
2. *Input slew rate: 1.5 V/ns.*
3. *AC characteristics tables assume clock and data signals have the same slew rate (slope).*
4. *DDR Operation.*

11. SDR AC Characteristics

Table 11.1 SDR AC Characteristics (Single Die Package, V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
$F_{SCK, R}$	SCK Clock Frequency for READ and 4READ instructions	DC		50	MHz
$F_{SCK, C}$	SCK Clock Frequency for single commands (4)	DC		133	MHz
$F_{SCK, C}$	SCK Clock Frequency for the following dual and quad commands: DOR, 4DOR, QOR, 4QOR, DIOR, 4DIOR, QIOR, 4QIOR	DC		104	MHz
$F_{SCK, QPP}$	SCK Clock Frequency for the QPP, 4QPP commands	DC		80	MHz
P_{SCK}	SCK Clock Period	1/ F_{SCK}		∞	
t_{WH}, t_{CH}	Clock High Time (5)	45% P_{SCK}			ns
t_{WL}, t_{CL}	Clock Low Time (5)	45% P_{SCK}			ns
t_{CRT}, t_{CLCH}	Clock Rise Time (slew rate)	0.1			V/ns
t_{CFT}, t_{CHCL}	Clock Fall Time (slew rate)	0.1			V/ns
t_{CS} (7)	CS# High Time (Read Instructions) CS# High Time (Program/Erase)	10 50			ns
t_{CSS}	CS# Active Setup Time (relative to SCK)	3			ns
t_{CSH}	CS# Active Hold Time (relative to SCK)	3		3000 (6)	ns
t_{SU}	Data in Setup Time	3			ns
t_{HD}	Data in Hold Time	2			ns
t_V	Clock Low to Output Valid	0		8.0 (2) 7.65 (3) 6.5 (4)	ns
t_{HO}	Output Hold Time	2			ns
t_{DIS}	Output Disable Time	0		8	ns
t_{WPS}	WP# Setup Time	20 (1)			ns
t_{WPH}	WP# Hold Time	100 (1)			ns
t_{HLCH}	HOLD# Active Setup Time (relative to SCK)	3			ns
t_{CHHH}	HOLD# Active Hold Time (relative to SCK)	3			ns
t_{HHCH}	HOLD# Non Active Setup Time (relative to SCK)	3			ns
t_{CHHL}	HOLD# Non Active Hold Time (relative to SCK)	3			ns
t_{HZ}	HOLD# enable to Output Invalid			8	ns
t_{LZ}	HOLD# disable to Output Valid			8	ns

Notes:

1. *Only applicable as a constraint for WRR instruction when SRWD is set to a 1.*
2. *Full V_{CC} range (2.7 - 3.6V) and CL = 30 pF.*
3. *Regulated V_{CC} range (3.0 - 3.6V) and CL = 30 pF.*
4. *Regulated V_{CC} range (3.0 - 3.6V) and CL = 15 pF.*
5. *±10% duty cycle is supported for frequencies ≤ 50 MHz.*
6. *Maximum value only applies during Program/Erase Suspend/Resume commands.*
7. *When switching between die, a minimum time of t_{CS} must be kept between the rising edge of one chip select and the falling edge of the other for operations and data to be valid.*

11.1 DDR AC Characteristics

Table 11.2 DDR AC Characteristics 66 MHz Operation

Symbol	Parameter	Min	Typ	Max	Unit
$F_{SCK, R}$	SCK Clock Frequency for DDR READ instruction	DC		66	MHz
$P_{SCK, R}$	SCK Clock Period for DDR READ instruction	15		∞	ns
t_{crt}	Clock Rise Time (slew rate)	1.5			V/ns
t_{cft}	Clock Fall Time (slew rate)	1.5			V/ns
t_{WH}, t_{CH}	Clock High Time	45% P_{SCK}			ns
t_{WL}, t_{CL}	Clock Low Time	45% P_{SCK}			ns
t_{CS}	CS# High Time (Read Instructions)	10			ns
t_{CSS}	CS# Active Setup Time (relative to SCK)	3			ns
t_{CSH}	CS# Active Hold Time (relative to SCK)	3			ns
t_{SU}	IO in Setup Time	2		3000 (2)	ns
t_{HD}	IO in Hold Time	2			ns
t_V	Clock Low to Output Valid	0		6.5 (1)	ns
t_{HO}	Output Hold Time	0			ns
t_{DIS}	Output Disable Time			8	ns
t_{LZ}	Clock to Output Low Impedance	0		8	ns
t_{IHTU}	Time uncertainty due to variation in V_{IH}			50	ps
t_{ILTU}	Time uncertainty due to variation in V_{IL}			50	ps
t_{IO_skew}	First IO to last IO data valid time			600	ps
t_{IORT}	Output rise time given 3V swing and 2.0 V/ns slew			1.5	ns
t_{IOFT}	Output fall time given 3V swing and 2.0 V/ns slew			1.5	ns
ΔT_V	Clock to data valid jitter			25	ps

Notes:

1. *Regulated V_{CC} range (3.0 - 3.6V) and CL =15 pF.*
2. *Maximum value only applies during Program/Erase Suspend/Resume commands.*

11.2 Capacitance Characteristics

Table 11.3 Capacitance

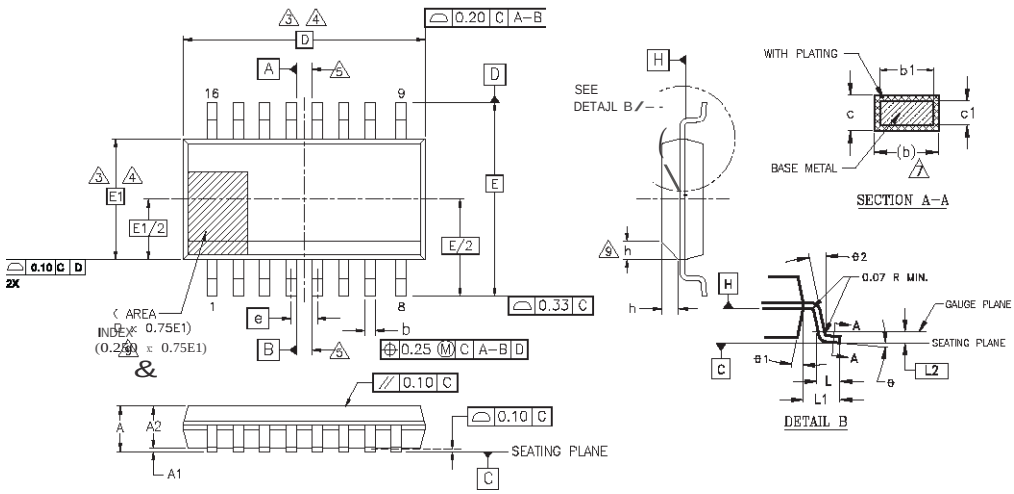
	Parameter	Test Conditions	Min	Max	Unit
C_{IN}	Input Capacitance (applies to SCK, CS#1, CS#2, RESET#)	1 MHz		8	pF
C_{OUT}	Output Capacitance (applies to All I/O)	1 MHz		8	pF

Notes:

1. *For more information on capacitance, please consult the IBIS models.*
2. *Capacitance values correspond to single die FL512S only.*

12. SOIC 16 Physical Diagram

12.1 503016 — 16-pin Wide Plastic Small Outline Package (300-mil Body Width)



PACKAGE	S03016 Onct.)		S03016(mm)	
JEDEC	MS-013(E)M		MS-013(E)M	
SYMBOL	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
A2	0.081	0.104	2.05	2.56
b	0.012	0.020	0.31	0.51
b1	0.011	0.019	0.27	0.48
c	0.00e	0.013	0.20	0.33
c1	0.008	0.012	0.20	0.30
D	0.408BSC		10.30BSC	
E	0.406BSC		10.3DBSC	
E1	0.295BSC		7.50 BSC	
e	0.050BSC		1.27BSC	
L	0.016	0.050	DAD	1.27
L1	0.056 REF		UOREF	
L2	0.010 BSC		0.25BSC	
N	16		16	
h	0.10	0.30	0.25	0.75
II	0·	8'	0·	8'
&1	5'	15'	5'	15'
112	0'	—	0·	—

NOTES:

1. ALL DIMENSIONS ARE IN BOTI-1 INCHES AND MILLMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M- 1994.

ill DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION E1 DOES NOT INCLUDE INTERUEAD FLASH OR PROTRUSION INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM H.

TI-IE PACKAGE TOP MAY BE SMALLER THAN TI-IE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OIJTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERUEAD FLASH. BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF TI-IE PLASTIC BODY.

DATUMS A AND B TO BE DETERMINED AT DATUM H.

6. "N" IS TI-IE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR TI-IE SPECIFIED PACKAGE LENGTH.

TI-IE DIMENSIONS APPLY TO TI-IE FLAT SECTION OF THE UEAD BETWEEN 0.10 T00.25 mm FROM THE UEADTIP.

DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF TI-IE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE UEAD FOOT.

nilS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, TI-IEN A PIN 1 IDENTIFIER MUST BE LOCATED WITI-IIN TI-IE INDEX AREA INDICATED.

10. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.

13. Revision History

Section	Description
Revision 01 (November 6, 2012)	
	Initial release
Revision 02 (April 25, 2013)	
Global	Data sheet designation updated from Advance Information to Preliminary
DC Characteristics	DC Characteristics table: changed Max value of I_{LI}, I_{LO}, I_{CC1}, and I_{SB}

Colophon

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