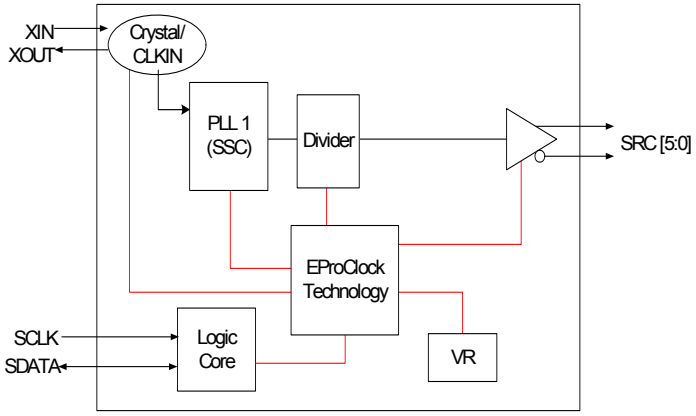
SL28PCIe16

EProClock® PCI Express Gen 2 & Gen 3 Clock Generator

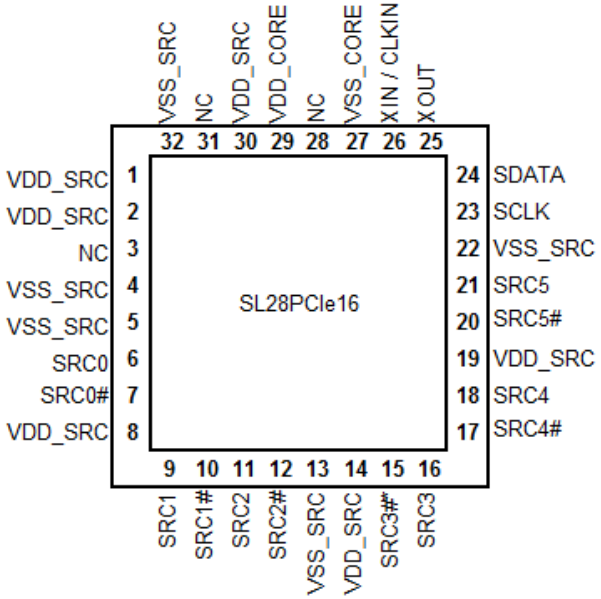
Features

- Optimized 100 MHz Operating Frequencies to Meet the Next Generation PCI-Express Gen 2 & Gen 3
- Low power push-pull type differential output buffers
- Integrated voltage regulator
- Integrated resistors on differential clocks
- Six 100-MHz differential SRC clocks
- Low jitter (<50ps)
- 25MHz Crystal Input or Clock input
- EProClock® Programmable Technology
- I^2C support with readback capabilities
- Triangular Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction
- Industrial Temperature -40°C to 85°C
- 3.3V Power supply
- 32-pin QFN package

Block Diagram



Pin Configuration



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32-QFN Pin Definitions

Pin No.	Name	Type	Description
1	VDD_SRC	PWR	3.3V Power Supply
2	VDD_SRC	PWR	3.3V Power Supply
3	NC	NC	No Connect.
4	VSS	GND	Ground
5	VSS	GND	Ground
6	SRC0	O, DIF	100MHz True differential serial reference clock
7	SRC0#	O, DIF	100MHz Complement differential serial reference clock
8	VDD_SRC	PWR	3.3V Power Supply
9	SRC1	O, DIF	100MHz True differential serial reference clock
10	SRC1#	O, DIF	100MHz Complement differential serial reference clock
11	SRC2	O, DIF	100MHz True differential serial reference clock
12	SRC2#	O, DIF	100MHz Complement differential serial reference clock
13	VSS_SRC	GND	Ground
14	VDD_SRC	PWR	3.3V Power Supply
15	SRC3#	O, DIF	100MHz Complement differential serial reference clock
16	SRC3	O, DIF	100MHz True differential serial reference clock
17	SRC4#	O, DIF	100MHz Complement differential serial reference clock
18	SRC4	O, DIF	100MHz True differential serial reference clock
19	VDD_SRC	PWR	3.3V Power Supply
20	SRC5#	O, DIF	100MHz Complement differential serial reference clock
21	SRC5	O, DIF	100MHz True differential serial reference clock
22	VSS_SRC	GND	Ground
23	SCLK	I	SMBus compatible SCLOCK
24	SDATA	I/O	SMBus compatible SDATA
25	XOUT	O	25.00MHz Crystal output, *Float XOUT if using only CLKIN (Clock input)*
26	XIN / CLKIN	I	25.00MHz Crystal input or 3.3V, 25MHz Clock Input
27	VSS_CORE	GND	Ground
28	NC	NC	No Connect.
29	VDD_CORE	PWR	3.3V Power Supply
30	VDD_SRC	PWR	3.3V Power Supply
31	NC	NC	No Connect.
32	VSS_SRC	GND	Ground

EProClock® Programmable Technology

EProClock® is the world's first non-volatile programmable clock. The EProClock® technology allows board designer to promptly achieve optimum compliance and clock signal integrity; historically, attainable typically through device and/or board redesigns.

EProClock® technology can be configured through SMBus or hard coded.

Features:

- > 4000 bits of configurations
- Can be configured through SMBus or hard coded
- Custom frequency sets
- Differential skew control on true or compliment or both
- Differential duty cycle control on true or compliment or both
- Differential amplitude control
- Differential and single-ended slew rate control
- Program Internal or External series resistor on single-ended clocks
- Program different spread profiles
- Program different spread modulation rate

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers are individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting at power-up. The use of this interface is optional. Clock device register changes are normally made at system initialization, if any are required. The interface cannot be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, access the bytes in sequential order from lowest to highest (most significant bit first) with the ability to stop after any complete byte is transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code described in *Table 1*.

The block write and block read protocol is outlined in *Table 2* while *Table 3* outlines byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

Table 1. Command Code Definition

Bit	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000'

Table 2. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Byte Count–8 bits	20	Repeat start
28	Acknowledge from slave	27:21	Slave address–7 bits
36:29	Data byte 1–8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
45:38	Data byte 2–8 bits	37:30	Byte Count from slave–8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte /Slave Acknowledges	46:39	Data byte 1 from slave–8 bits
....	Data Byte N–8 bits	47	Acknowledge
....	Acknowledge from slave	55:48	Data byte 2 from slave–8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave / Acknowledge
		....	Data Byte N from slave–8 bits
		....	NOT Acknowledge
		....	Stop

Control Registers

Table 3. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start

Table 3. Byte Read and Byte Write Protocol

8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Data byte–8 bits	20	Repeated start
28	Acknowledge from slave	27:21	Slave address–7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		37:30	Data from slave–8 bits
		38	NOT Acknowledge
		39	Stop

Byte 0: Control Register 0

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	1	Spread Enable	Enable spread for SRC outputs 0=Disable, 1= -0.5%
4	0	RESERVED	RESERVED
3	0	RESERVED	RESERVED
2	0	RESERVED	RESERVED
1	0	RESERVED	RESERVED
0	0	RESERVED	RESERVED

Byte 1: Control Register 1

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	1	SRC0_OE	Output enable for SRC0 0 = Output Disabled, 1 = Output Enabled
5	0	RESERVED	RESERVED
4	0	RESERVED	RESERVED
3	1	SRC1_OE	Output enable for SRC1 0 = Output Disabled, 1 = Output Enabled
2	1	RESERVED	RESERVED
1	0	RESERVED	RESERVED
0	0	RESERVED	RESERVED

Byte 2: Control Register 2

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	0	RESERVED	RESERVED
4	0	RESERVED	RESERVED
3	0	RESERVED	RESERVED
2	0	RESERVED	RESERVED

Byte 2: Control Register 2 (continued)

Bit	@Pup	Name	Description
1	0	RESERVED	RESERVED
0	0	RESERVED	RESERVED

Byte 3: Control Register 3

Bit	@Pup	Name	Description
7	1	SRC4_OE	Output enable for SRC4 0 = Output Disabled, 1 = Output Enabled
6	1	SRC5_OE	Output enable for SRC5 0 = Output Disabled, 1 = Output Enabled
5	0	RESERVED	RESERVED
4	0	RESERVED	RESERVED
3	0	RESERVED	RESERVED
2	0	RESERVED	RESERVED
1	0	RESERVED	RESERVED
0	0	RESERVED	RESERVED

Byte 4: Control Register 4

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	1	RESERVED	RESERVED
4	0	RESERVED	RESERVED
3	0	RESERVED	RESERVED
2	0	RESERVED	RESERVED
1	0	RESERVED	RESERVED
0	0	RESERVED	RESERVED

Byte 5: Control Register 5

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	0	RESERVED	RESERVED
4	1	RESERVED	RESERVED
3	0	RESERVED	RESERVED
2	0	RESERVED	RESERVED
1	0	RESERVED	RESERVED
0	0	RESERVED	RESERVED

Byte 6: Control Register 6

Bit	@Pup	Name	Description
7	0	SRC[5:4]_AMP1	SRC[5:4] amplitude adjustment 00= 700mV, 01=800mV, 10=900mV, 11= 1000mV
6	1	SRC[5:4]_AMP0	

Byte 6: Control Register 6

5	0	SRC[3:1]_AMP1	SRC[3:1] amplitude adjustment 00= 700mV, 01=800mV, 10=900mV, 11= 1000mV
4	1	SRC[3:1]_AMP0	
3	0	RESERVED	RESERVED
2	1	RESERVED	RESERVED
1	0	SRC0_AMP1	SRC0 amplitude adjustment 00= 700mV, 01=800mV, 10=900mV, 11= 1000mV
0	1	SRC0_AMP0	

Byte 7: Vendor ID

Bit	@Pup	Name	Description
7	0	Rev Code Bit 3	Revision Code Bit 3
6	0	Rev Code Bit 2	Revision Code Bit 2
5	0	Rev Code Bit 1	Revision Code Bit 1
4	1	Rev Code Bit 0	Revision Code Bit 0
3	1	Vendor ID bit 3	Vendor ID Bit 3
2	0	Vendor ID bit 2	Vendor ID Bit 2
1	0	Vendor ID bit 1	Vendor ID Bit 1
0	0	Vendor ID bit 0	Vendor ID Bit 0

Byte 8: Control Register 8

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	0	RESERVED	RESERVED
4	0	BC4	Byte count register for block read operation. The default value for Byte count is 9. In order to read beyond Byte 9, the user should change the byte count limit.to or beyond the byte that is desired to be read.
3	1	BC3	
2	1	BC2	
1	1	BC1	
0	1	BC0	

Byte 9: Control Register 9

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	1	SRC3_OE	Output enable for SRC3 0 = Output Disabled, 1 = Output Enabled
5	1	SRC2_OE	Output enable for SRC2 0 = Output Disabled, 1 = Output Enabled
4	0	RESERVED	RESERVED
3	0	RESERVED	RESERVED
2	0	RESERVED	RESERVED
1	0	RESERVED	RESERVED
0	1	RESERVED	RESERVED

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
$V_{DD\_3.3V}$	Main Supply Voltage	Functional	–	4.6	V
V_{IN}	Input Voltage	Relative to V_{SS}	–0.5	4.6	V_{DC}
T_S	Temperature, Storage	Non-functional	–65	150	°C
T_A	Industrial Temperature, Operating Ambient	Functional	–40	85	°C
T_A	Commercial Temperature, Operating Ambient	Functional	0	85	°C
T_J	Temperature, Junction	Functional	–	150	°C
$Ø_{JC}$	Dissipation, Junction to Case	JEDEC (JESD 51)	–	20	°C/W
$Ø_{JA}$	Dissipation, Junction to Ambient	JEDEC (JESD 51)	–	60	°C/W
ESD_{HBM}	ESD Protection (Human Body Model)	JEDEC (JESD 22 - A114)	2000	–	V
UL-94	Flammability Rating	UL (Class)	V–0		

Multiple Supplies: The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
VDD core	3.3V Operating Voltage	3.3 ± 5%	3.135	3.465	V
V_{IH}	3.3V Input High Voltage	Single-Ended Clock	2.0	V_{DD} + 0.3	V
V_{IL}	3.3V Input Low Voltage	Single-Ended Clock	V_{SS} – 0.3	0.8	V
V_{IHI2C}	Input High Voltage	SDATA, SCLK	2.2	–	V
V_{ILI2C}	Input Low Voltage	SDATA, SCLK	–	1.0	V
I_{IH}	Input High Leakage Current	Except internal pull-down resistors, $0 < V_{IN} < V_{DD}$	–	5	µA
I_{IL}	Input Low Leakage Current	Except internal pull-up resistors, $0 < V_{IN} < V_{DD}$	–5	–	µA
V_{OH}	3.3V Output High Voltage (DIFF)		0.7	0.9	V
V_{OL}	3.3V Output Low Voltage (DIFF)		–	0.4	V
I_{OZ}	High-impedance Output Current		–10	10	µA
C_{IN}	Input Pin Capacitance		1.5	5	pF
C_{OUT}	Output Pin Capacitance			6	pF
L_{IN}	Pin Inductance		–	7	nH
$I_{DD\_3.3V}$	Dynamic Supply Current	Differential clocks with 7” traces and 2pF load.	–	65	mA

AC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
Crystal					
L_{ACC}	Long-term Accuracy	Measured at VDD/2 differential	–	250	ppm
Clock Input					
T_{DC}	CLKIN Duty Cycle	Measured at VDD/2	47	53	%
T_R/T_F	CLKIN Rise and Fall Times	Measured between $0.2V_{DD}$ and $0.8V_{DD}$	0.5	4.0	V/ns
T_{CCJ}	CLKIN Cycle to Cycle Jitter	Measured at VDD/2	–	250	ps
T_{LTJ}	CLKIN Long Term Jitter	Measured at VDD/2	–	350	ps
V_{IH}	Input High Voltage	XIN / CLKIN pin	2	VDD+0.3	V
V_{IL}	Input Low Voltage	XIN / CLKIN pin	–	0.8	V
I_{IH}	Input High Current	XIN / CLKIN pin, VIN = VDD	–	35	uA
I_{IL}	Input Low Current	XIN / CLKIN pin, 0 < VIN <0.8	–35	–	uA
SRC at 0.7V					
T_{DC}	SRC Duty Cycle	Measured at 0V differential	45	55	%
T_{PERIOD}	100 MHz SRC Period	Measured at 0V differential at 0.1s	9.99900	10.0010	ns
$T_{PERIODSS}$	100 MHz SRC Period, SSC	Measured at 0V differential at 0.1s	10.02406	10.02607	ns
$T_{PERIODAbs}$	100 MHz SRC Absolute Period	Measured at 0V differential at 1 clock	9.87400	10.1260	ns
$T_{PERIODSSAbs}$	100 MHz SRC Absolute Period, SSC	Measured at 0V differential at 1 clock	9.87406	10.1762	ns
T_{CCJ}	SRC Cycle to Cycle Jitter	Measured at 0V differential	–	50	ps
RMS_{GEN1}	Output PCIe* Gen1 REFCLK phase jitter	BER = 1E-12 (including PLL BW 8 - 16 MHz, ζ = 0.54, Td=10 ns, Ftrk=1.5 MHz)	0	108	ps
RMS_{GEN2}	Output PCIe* Gen2 REFCLK phase jitter	Includes PLL BW 8 - 16 MHz, Jitter Peaking = 3dB, ζ = 0.54, Td=10 ns), Low Band, F < 1.5MHz	0	3.0	ps
RMS_{GEN2}	Output PCIe* Gen2 REFCLK phase jitter	Includes PLL BW 8 - 16 MHz, Jitter Peaking = 3dB, ζ = 0.54, Td=10 ns), Low Band, F < 1.5MHz	0	3.1	ps
RMS_{GEN3}	Output phase jitter impact – PCIe* Gen3	Includes PLL BW 2 - 4 MHz, CDR = 10MHz)	0	1.0	ps
L_{ACC}	SRC Long Term Accuracy	Measured at 0V differential	–	100	ppm
T_R / T_F	SRC Rising/Falling Slew Rate	Measured differentially from ±150 mV	2.5	8	V/ns
V_{HIGH}	Voltage High			1.15	V
V_{LOW}	Voltage Low		–0.3	–	V
V_{OX}	Crossing Point Voltage at 0.7V Swing		300	550	mV
ENABLE/DISABLE and SET-UP					
T_{STABLE}	Clock Stabilization from Power-up		–	1.8	ms
T_{SS}	Stopclock Set-up Time		10.0	–	ns

Test and Measurement Set-up

This diagram shows the test load configuration for the differential clock signals

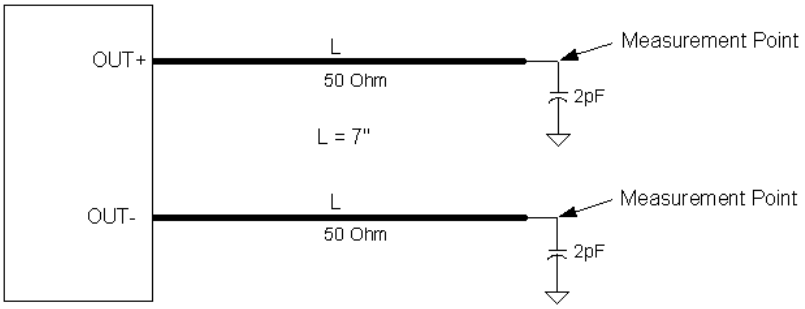


Figure 1. 0.7V Differential Load Configuration

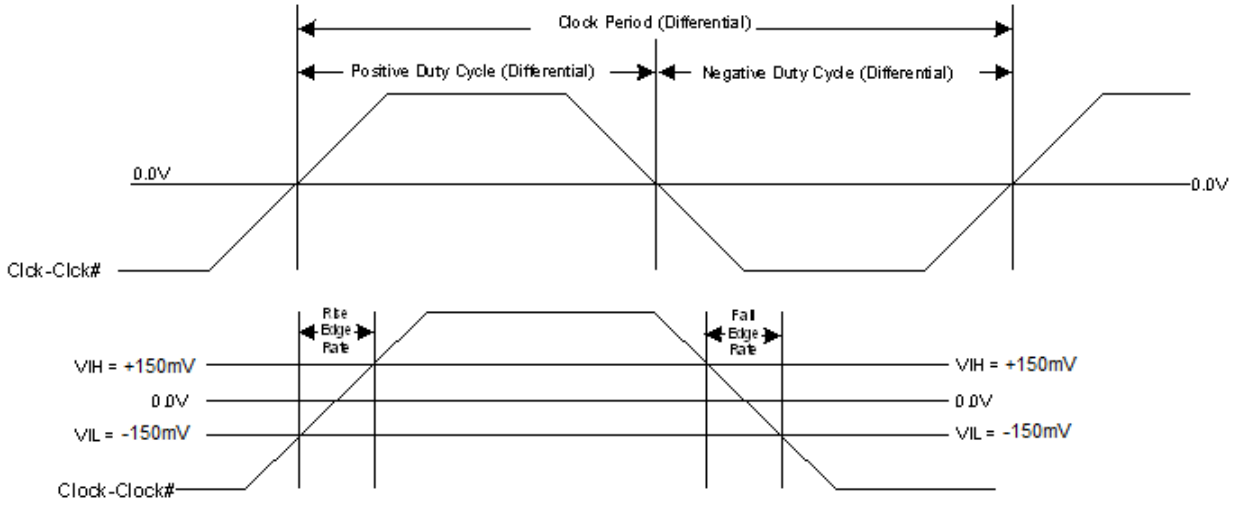


Figure 2. Differential Measurement for Differential Output Signals (for AC Parameters Measurement)

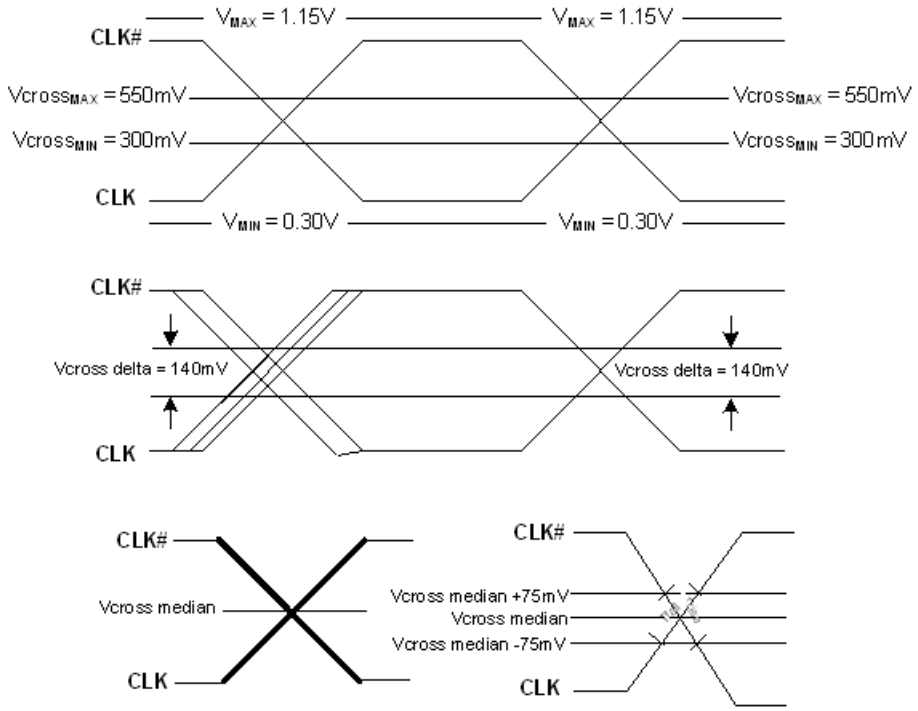


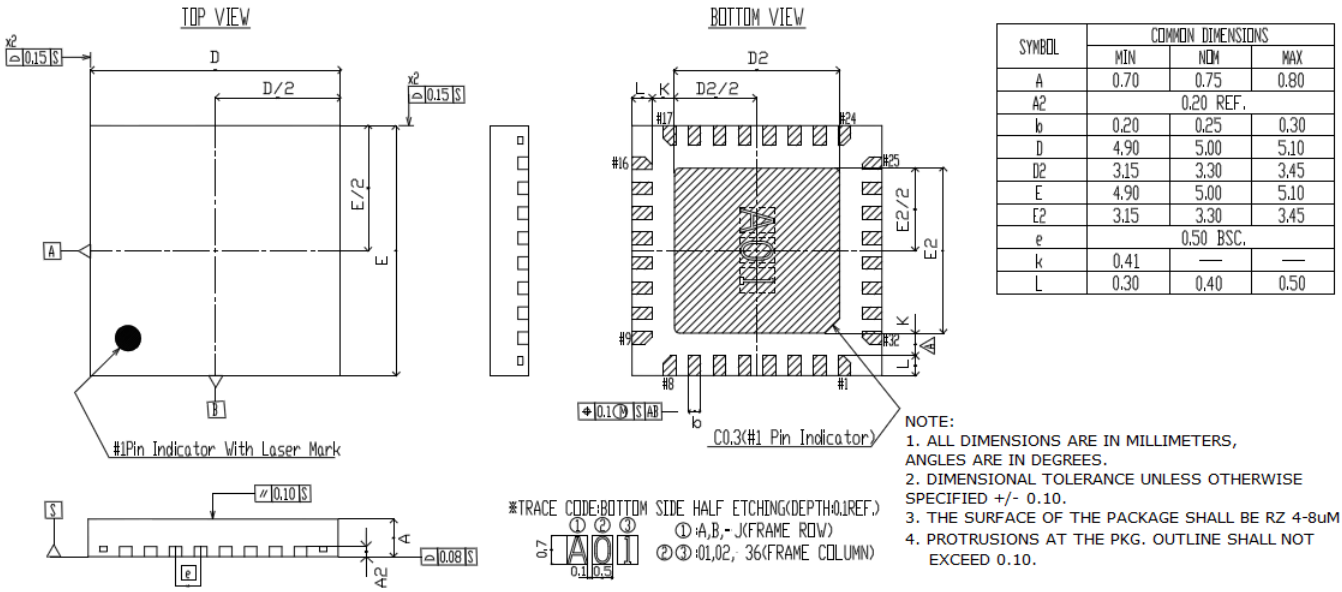
Figure 3. Single-ended Measurement for Differential Output Signals (for AC Parameters Measurement)

Ordering Information

Part Number	Package Type	Product Flow
Lead-free		
SL28PCIe16ALC	32-pin QFN	Commercial, 0° to 85°C
SL28PCIe16ALCT	32-pin QFN–Tape and Reel	Commercial, 0° to 85°C
SL28PCIe16ALI	32-pin QFN	Industrial, -40° to 85°C
SL28PCIe16ALIT	32-pin QFN–Tape and Reel	Industrial, -40° to 85°C

Package Diagrams

32-Lead QFN 5 x 5mm



SYMBOL	COMMON DIMENSIONS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A2		0.20 REF.	
b	0.20	0.25	0.30
D	4.90	5.00	5.10
D2	3.15	3.30	3.45
E	4.90	5.00	5.10
E2	3.15	3.30	3.45
e		0.50 BSC.	
k	0.41	—	—
L	0.30	0.40	0.50

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.
2. DIMENSIONAL TOLERANCE UNLESS OTHERWISE SPECIFIED +/- 0.10.
3. THE SURFACE OF THE PACKAGE SHALL BE RZ 4-8uM
4. PROTRUSIONS AT THE PKG. OUTLINE SHALL NOT EXCEED 0.10.

Document History Page

Document Title: SL28PCIe16 PC EProClock® PCI Express Gen 2 & Gen 3 Clock Generator DOC#: SP-AP-0790 (Rev. 0.3)			
REV.	**Issue Date**	**Orig. of Change**	**Description of Change**
AA	11/15/10	JMA	Initial Release
AA	12/15/10	TRP	1. Updated Control Registers 2. Updated VOH/VOL spec 3. Removed IDD_PD spec 4. Updated foot note
AB	1/13/11	TRP	1. Updated IDD current 2. Updated Byte8 default 3. Removed skew spec