Si4330

ISM Receiver

Description

Silicon Laboratories' Si4330 is a highly-integrated, single chip, wireless ISM receiver that is part of the EZRadioPRO™ family. The EZRadioPRO family includes a complete line of transmitters, receivers, and transceivers that allow RF system designers to choose the optimal wireless part for their application.

The Si4330 offers advanced radio features, including continuous frequency coverage from 240–960 MHz. The Si4330's high level of integration offers reduced BOM cost while simplifying overall system design. The extremely low receive sensitivity (–118 dBm) ensures extended range and improved link performance. Built-in antenna diversity and support for frequency hopping can be used to further extend range and enhance performance. Antenna diversity is completely integrated into the Si4330 and can improve the system link budget by 8–10 dB, resulting in substantial range increases under adverse environmental conditions.

Additional system features, such as an automatic wake-up timer, low battery detector, 64-byte RX FIFO, automatic packet handling, and preamble detection, reduce overall current consumption and allow the use of lower-cost system MCUs. An integrated temperature sensor, general purpose ADC, power-on-reset (POR), and GPIOs further reduce overall system cost and size.

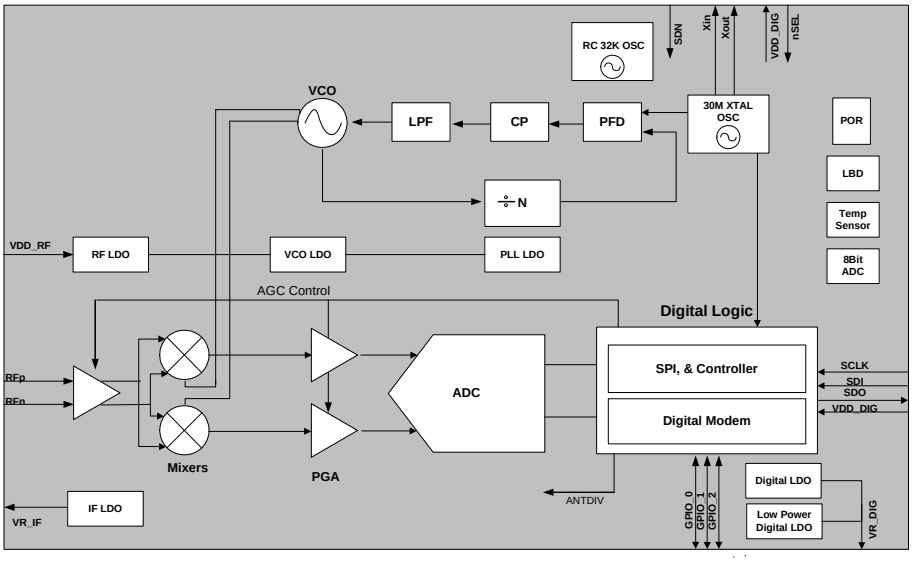
The Si4330 receiver uses a single-conversion architecture to convert the 2-level FSK/GFSK/OOK modulated receive signal to a low IF frequency. Following a programmable gain amplifier (PGA), the signal is converted to the digital domain by a high-performance delta-sigma ADC allowing filtering, demodulation, slicing, error correction, and packet handling to be performed in the built-in DSP, thus increasing the receiver's performance and flexibility versus analog-based architectures. The demodulated signal is then output to the system MCU through a programmable GPIO or via the standard SPI bus by reading the 64-byte RX FIFO. This digital architecture simplifies system design while allowing for the use of lower-end MCUs. The Si4330 is designed to work with an MCU, crystal, and a few passives to create a very low-cost system. Voltage regulators are integrated on-chip, which allows for a wide range of operating supply voltage conditions from +1.8 to +3.6 V.

Features

- Frequency Range = 240–960 MHz
- FSK, GFSK, and OOK modulation
- Sensitivity = –118 dBm
- Low Power Consumption
  - 18.5 mA receive
- Data Rate = 1 to 128 kbps
- Power Supply = 1.8 to 3.6 V
- Ultra low power shutdown mode (10 nA)
- Wake-up timer
- Auto-frequency calibration (AFC)
- Programmable RX BW 2.6–620 kHz
- Programmable packet handler
- Programmable GPIOs
- Embedded antenna diversity algorithm
- RX 64 byte FIFO
- Low battery detector
- Temperature sensor and 8-bit ADC
- Frequency hopping capability
- On-chip crystal tuning
- 20-Pin QFN package
- Low BOM

Applications

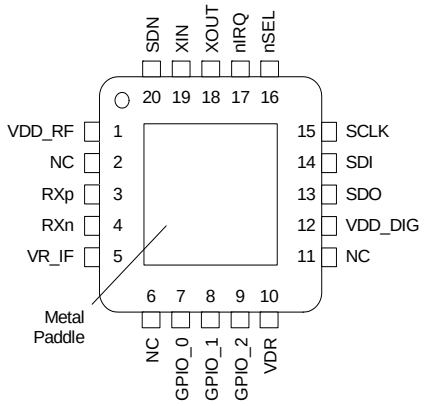
- Remote control
- Home security & alarm
- Telemetry
- Toy control
- Tire Pressure monitoring
- Remote meter reading
- Remote keyless entry
- Home automation
- Industrial control
- Sensor networks
- Health monitors
- Tag readers



Selected Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage Range	V_{dd}		1.8	3.0	3.6	V
Power Saving Modes	$I_{Shutdown}$	RC Oscillator, Main Digital Regulator, and Low Power Digital Regulator OFF	—	10	—	nA
	$I_{Standby}$	Register values retained, Main Digital Regulator, and RC Oscillator OFF	—	400	—	nA
	I_{Sleep}	RC Oscillator ON, Register values retained, and Main Digital Regulator OFF	—	800	—	nA
RX Mode Current	I_{RX}		—	18.5	—	mA
Synthesizer Frequency Range	$F_{SYNTH-LB}$	Low Band	240	—	480	MHz
	$F_{SYNTH-HB}$	High Band	480	—	960	MHz
Synthesizer Frequency Resolution	F_{RES-LB}	Low Band	—	156.25	—	Hz
	F_{RES-HB}	High Band	—	312.5	—	Hz
Synthesizer Settling Time	t_{LOCK}	Measured from leaving Ready mode with XOSC running to any frequency including VCO Calibration	—	200	—	µs
RX Sensitivity	P_{RX_2}	(BER < 0.1%) (2 kbps, GFSK, BT = 0.5, $\Delta f = \pm 5$ kHz)[2]	—	–118	—	dBm
RX Bandwidth	BW		2.6	—	620	kHz
Blocking at 1 MHz	$1M_{BLOCK}$	Desired Ref Signal 3 dB above sensitivity. Interferer and desired modulated with 40 kbps ΔF = 20 kHz GFSK with BT = 0.5	—	–52	—	dB
Blocking at 4 MHz	$4M_{BLOCK}$		—	–56	—	dB
Blocking at 8 MHz	$8M_{BLOCK}$		—	–63	—	dB
Image Rejection	Im_{REJ}	IF=937 kHz	—	–30	—	dB
Operating Ambient Temperature Range	T_A		–40		85	°C

Pin Assignments



20-pin QFN Package Information