Si504

ANY-FREQUENCY 32 KHZ–100 MHZ CMEMS®OSCILLATOR

Features

- Wide frequency range: 32 kHz to 100 MHz
  - Contact Silicon Labs for frequencies above 100 MHz
- ±20/30/50 ppm frequency stability including 10-year aging
- Single wire interface
- LVCMOS output
- Continuous supply voltage range: +1.71 V to +3.63 V
- Low power
- Low period jitter
- User selectable tRise/tFall options
- Glitchless start and stop
- Excellent short-term stability, long-term aging
- Industry standard footprints: 2x2.5, 2.5x3.2, 3.2x5 mm
- RoHS compliant, Pb-free
- Short lead times: <2 weeks
- –20 to +70 °C: Extnd commercial
- –40 to +85 °C: Industrial

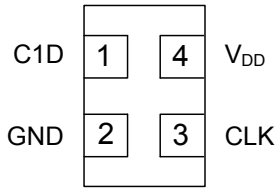
Ordering Information:

See page 20.

Applications

- Storage (SATA/SAS/PCIe)
- General purpose processors
- Industrial controllers
- Embedded controllers
- Motor control
- Flow control
- Office/Home automation
- IP cameras/surveillance
- display and control panels
- Outdoor electronics
- Multi-function printers
- Office equipment

Pin Assignments

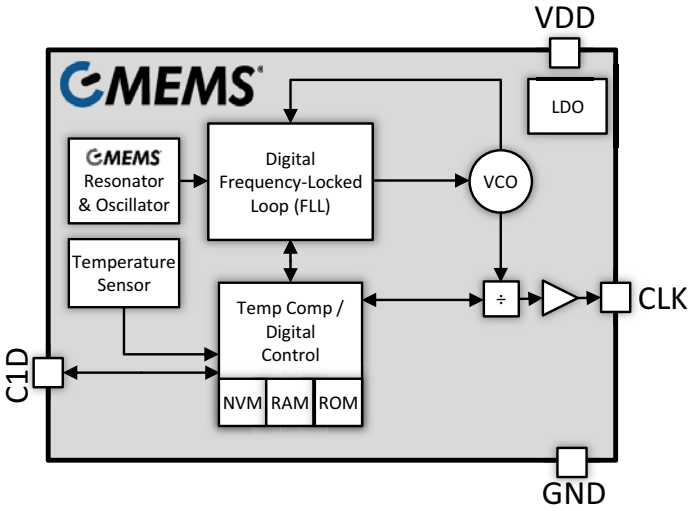


Patents pending

Description

The Si50x CMEMS oscillator family provides monolithic, MEMS-based IC replacements for traditional crystal oscillators. Silicon Laboratories' CMEMS technology combines standard CMOS and MEMS in a single, monolithic IC to provide integrated, high-quality and high-reliability oscillators. Each device is factory tested and configured for guaranteed performance to data sheet specifications across voltage, process, temperature, shock, vibration, and aging. The Si504 programmable CMEMS oscillator provides any frequency and supported feature set from 32 kHz to 100 MHz through a single wire interface.

Functional Block Diagram



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1. Electrical Specifications

Table 1. Recommended Operating Conditions

V_{DD} = 1.71 to 3.63 V, T_A = –40 to 85 °C unless otherwise indicated.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage[1]	V_{DD}		1.71	—	3.63	V
Supply Current	I_{DD1}	C_L=4 pF, 3.3 V_{DD}, F_{CLK}=1.0 MHz, low power option	—	1.7	2.5	mA
		C_L=4 pF, 3.3 V_{DD}, F_{CLK}=100 MHz, low power option	—	5.3	6.5	mA
		C_L=4 pF, 3.3 V_{DD}, F_{CLK}=1.0 MHz, low jitter option	—	3.9	4.9	mA
		C_L=4 pF, 3.3 V_{DD}, F_{CLK}=100 MHz, low jitter option	—	7.6	8.9	mA
Static Supply Current	I_{DD2}	Mode=Stop, low power option F_{CLK}=1 MHz	—	1.7	2.5	mA
		Mode=Stop, low jitter option F_{CLK}=1 MHz	—	3.9	4.9	mA
		Mode=Doze	—	670	890	µA
		Mode=Sleep[2]	—	0.3	1	µA
Input High Voltage	V_{IH}	C1D pin	0.7 x V_{DD}	—	—	V
Input Low Voltage	V_{IL}	C1D pin	—	—	0.3 x V_{DD}	V
Internal Pull-up Resistor	R_I	C1D pin	40	50	60	kΩ
Operating Temperature	T_A	Extended commercial grade	–20	—	70	°C
		Industrial grade	–40	—	85	°C

Notes:
1. The supply voltage range is continuous from 1.71 to 3.63 V.
2. C1D steady state = high.

Table 2. Output Clock Frequency Characteristics[1]

V_{DD} = 1.71 to 3.63 V, T_A = –40 to 85 °C unless otherwise indicated.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency Range	F_{CLK}		0.032	—	100	MHz
Step Size			—	29.8	—	ppb
Clock Period	T_{CLK}	$1/F_{CLK}$	31,250	—	10	ns
Total Stability[2]	F_{STAB}		–20	—	+20	ppm
			–30	—	+30	ppm
			–50	—	+50	ppm
Initial Accuracy	F_I	Measured at 25 °C at the time of shipping	—	±2	—	ppm
Startup Time	T_{SU}	From V_{DD} crossing 1.71 V to first clock output.	—	2.5	4	ms
Resume Time	T_{RUN}	From sleep mode	—	2.5	5	ms
		From doze mode	—	1.7	2.5	ms
		From stop mode	—	—	1.5 x T_{CLK} + 35	ns
Output Disable Time	T_D	To sleep/doze mode, from output running	—	—	225	µs
		To stop, from output running	—	—	1.5 x T_{CLK} + 35	ns
Frequency Update Time	T_{NEW_FREQ}	From end of NewFreq or OriginalFreq command to when new frequency has stabilized.	—	—	5	ms
Offset/Slew Rate Time	T_{SLEW}	From end of Offset Freq command to when offset/slewed frequency has stabilized.	—	600	—	µs

Notes:
1. Refer to Figures 2, 3, and 7 for timing diagrams and additional information.
2. Orderable option. Stability budget consists of 10-year aging, initial tolerance, operating temperature range, rated power supply voltage change, load change, aging, shock, and vibration.

Table 3. Single Wire Interface AC Characteristics*

V_{DD} = 1.71 to 3.63 V, T_A = –40 to 85 °C unless otherwise indicated.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Bit “0” Nominal Duration	T_{ZERO}		0.45	—	5.5	µs
Bit “1” Nominal Duration	T_{ONE}		2.5 x T_{ZERO}	—	16	µs
Bit “0” Tolerance	$T_{ZERO-TOL}$	T_{ZERO} x ± 10%	0.9	—	1.1	
Bit “1” Tolerance	$T_{ONE-TOL}$	T_{ONE} x ± 10%	0.9	—	1.1	
Transaction Reset/Abort Time	T_{RESET}		30	—	—	µs
Byte Write Within Command Sequence Spacing	T_{CBI}		50	—	—	µs
Between Command Sequence Spacing	T_{CI}		1	—	—	ms
Initial/Reset Sequence to 1st Command	T_{RSC}		1	—	—	ms
Sleep Wake Up Pulse Width	T_{WUP}		0.2	—	—	µs

***Note:** Refer to Figures 2, 3, and 7 for timing diagrams and additional information.

Table 4. Output Clock Levels and Symmetry

V_{DD} = 1.71 to 3.63 V, T_A = –40 to 85 °C unless otherwise indicated.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage	V_{OH}	1st ordering option code: A and H I_{OH}=–4 mA	0.90 x V_{DD}	—	—	V
Output Low Voltage	V_{OL}	1st ordering option code: A and H I_{OH}=+4 mA	—	—	0.10 x V_{DD}	V
Rise/Fall Time[1]	tRise / tFall	1st ordering option code[2]: A and H Z_0= 25 Ω @ 3.3V	0.4	0.7	1.2	ns
		1st ordering option code: B and J Z_0= 50 Ω @ 3.3V	1	1.3	1.6	ns
		1st ordering option code: C and K Z_0= 50 Ω @ 2.5V	1	1.3	1.6	ns
		1st ordering option code: D and L Z_0 = 50 Ω @ 1.8V	1	1.3	1.6	ns
		1st ordering option code: E and M Z_0= 110 Ω @ 3.3V	2	3	4	ns
		1st ordering option code: F and N Z_0= 220 Ω @ 3.3V	4	5	7	ns
		1st ordering option code: G and P Z_0= 440 Ω @ 3.3V	7	8	11	ns
Duty Cycle	DC	Drive strength selected such that tRise/tFall (20% to 80%)<10% of period	45	50	55	%

Notes:
1. C_L=15 pF, tRise/tFall (20% to 80%), 3.3 V, unless otherwise stated.
2. Recommended series termination resistor (R_S) = 24.9 Ω for Z_0=50 Ω.

Table 5. Output Clock Jitter and Phase Noise

V_{DD} = 1.71 to 3.63 V, T_A = –40 to 85 °C unless otherwise indicated.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Cycle-to-Cycle Jitter	J_{CCPP}	100 MHz, Low Jitter Option 1st ordering option code: H	—	14	25	ps pk-pk
		100 MHz, Low Power Option 1st ordering option code: A	—	16	26	ps pk-pk
Period Jitter	J_{PRMS}	100 MHz, Low Jitter Option 1st ordering option code: H	—	1	1.6	ps rms
		100 MHz, Low Power Option 1st ordering option code: A	—	1.3	1.9	ps rms
Period Jitter Pk-Pk	J_{PPKPK}	Low Jitter Option 10k samples 1st ordering option code: H	—	9	13	ps pk-pk
		Low Power Option 10k samples 1st ordering option code: A	—	10	16	ps pk-pk
Phase Jitter[1]	ϕ	75 MHz F_{OFFSET}=900 kHz to 7.5 MHz Low Jitter Option 1st ordering option code: H	—	1	1.3	ps rms
		75 MHz F_{OFFSET}=900 kHz to 7.5 MHz Low Power Option 1st ordering option code: A	—	2.5	3.2	ps rms

Notes:

1. Integrated phase jitter exceeds the requirements of some high-performance data communications systems. See AN783 for additional information.

Table 6. Environmental Compliance and Package Information

Parameter	Condition
Mechanical Shock	MIL-STD-883, Method 2002, Cond B. (1,500 g)
Mechanical Shock High g	MIL-STD-883, Method 2002, Cond E. (10,000 g)
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Temperature Cycle	JESD22, Method A104
Resistance to Solder Heat	MIL-STD-883, Method 2036
Contact Pads	Gold over Nickel/Palladium

Table 7. Thermal Characteristics

Parameter	Symbol	Test Condition	MAX	Unit
Thermal Impedance	θ_{JA}	3.2x5 mm, still air	187	°C/W
		2.5x3.2 mm, still air	239	°C/W
		2x2.5 mm, still air	241	°C/W

Table 8. Absolute Maximum Ratings[1]

Parameter	Symbol	Rating	Unit
Maximum Operating Temperature	T_{MAX}	85	°C
Storage Temperature	T_S	–55 to +125	°C
Supply Voltage	V_{DD}	–0.5 to +3.8	V
Input Voltage	V_{IN}	–0.5 to V_{DD} +0.3 V	V
HBM ESD Sensitivity (JESD22-A114)	HBM	2000	V
CDM ESD Sensitivity	CDM	500	V
Soldering Temperature (Pb-free profile)[2]	T_{PEAK}	260	°C
Soldering Time at T_{PEAK} (PB-free profile)[2]	T_P	20–40	s
Junction Temperature	T_J	125	°C

Notes:
1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020.

2. Typical Applications Circuit and AC Waveforms

2.1. Application Circuit

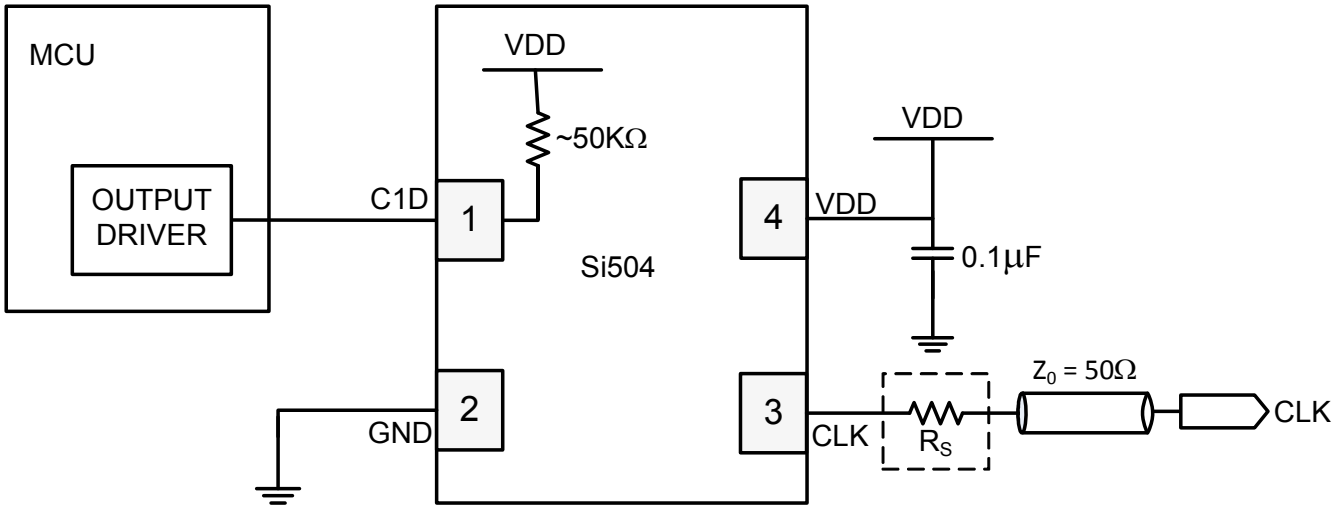


Figure 1. Si504 Application Circuit

Note: Dotted line box is an optional component depending on tRise/tFall configuration option. See Table 4 for R_S recommendations. See Section 5. "Ordering Guide" for configuration options.

2.2. AC Waveforms

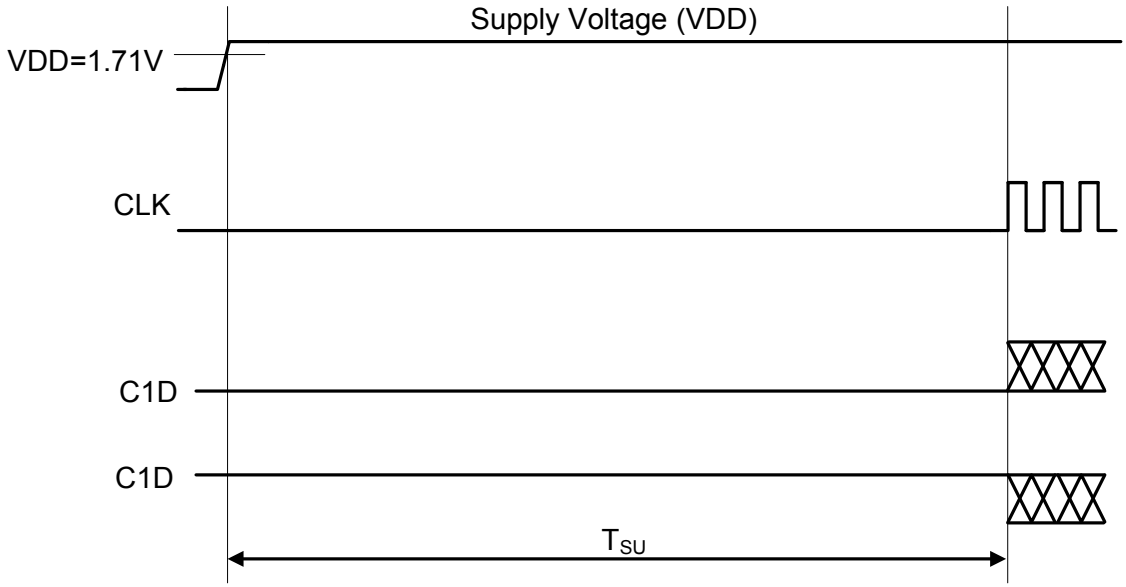


Figure 2. Power-On Timing

Notes:

1. C1D steady state default polarity is set high (C1D=1) with an internal pull-up resistor. User may drive or pull C1D polarity low to change the C1D default steady state, however, the internal pull-up resistor will remain active.
2. Refer to Table 2 and Table 3 for additional information.

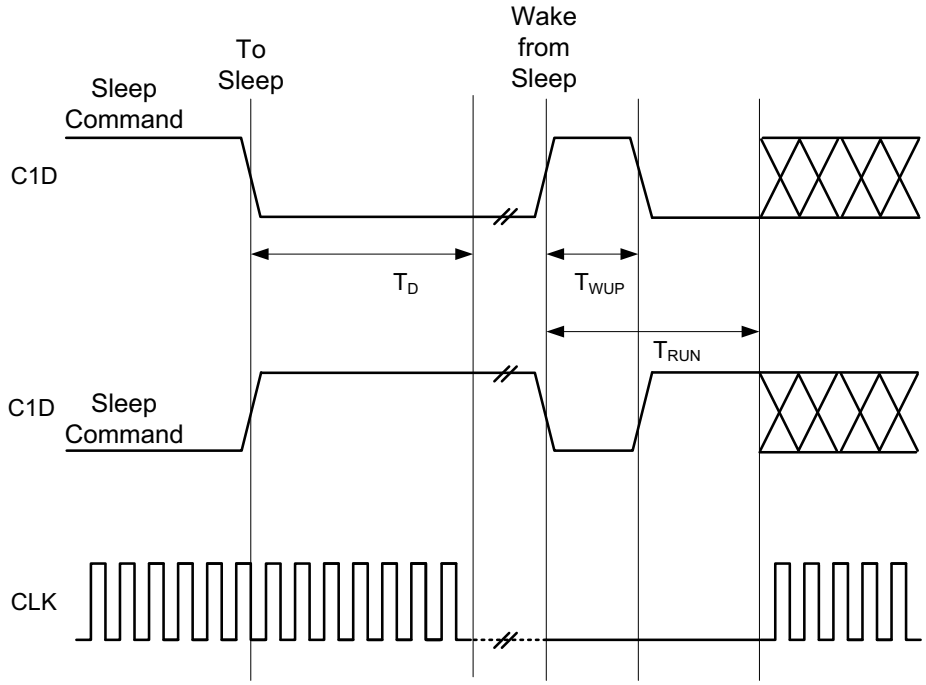


Figure 3. Sleep Timing

Notes:

1. C1D steady state default polarity is set high (C1D=1) with an internal pull-up resistor. User may drive or pull C1D polarity low to change the C1D default steady state; however, the internal pull-up resistor will remain active.
2. Refer to Table 2 and Table 3 for additional information.

3. Functional Description

3.1. Si504 Overview

The Si504 is a fully programmable CMEMS oscillator, capable of adjusting its base output frequency by 29.8 ppb frequency offset steps. The Si504 supports all Si50x CMEMS oscillator functionality through a simple, single wire C1 interface. The C1 interface, its characteristics, and commands are described below. For further details, including C example code, please refer to application note AN752 which is available on the Silicon Labs website.

The Si504 starts up in the user's ordered preconfiguration, as detailed in "5. Ordering Guide", and also available at www.siliconlabs.com/cmems. Depending on the ordered options, some features may be limited such as Frequency Stability, supported Temp Range, and Maximum Anticipated User Frequency. For example, a device that is ordered to support ± 50 ppm, -20 to 70 °C, and 80 MHz as the maximum required output frequency cannot support ± 30 ppm or ± 20 ppm, -40 to 85 °C within spec, or any output frequency above 80 MHz.

From initial power up, the Si504 starts in Run mode with the output frequency and device configuration set to the ordered configuration. There is no option to initially power-up the Si504 in any other mode than Run mode with the ordered configuration. Once the Si504 has completed start-up, the user may reconfigure the Si504 to any supported operating state, operating mode, configuration, or output frequency using C1 commands.

Additional information on the Si50x CMEMS oscillator architecture and CMEMS technology is available in white papers posted on the Silicon Labs website at www.siliconlabs.com/cmems.

3.2. Frequency Adjustment

The Si504 frequency adjustment is seamless and glitchless within the frequency offset (OffsetFreq command) range (±976.4566 ppm). However, if the user is adjusting the output frequency beyond this range (NewFreq command), for example, from 32.768 kHz to 4 MHz, the Si504 adjustment is not seamless since the device momentarily disables the output clock to recalibrate. The momentary blanking is glitchless, disabling and enabling the output clock with no runt pulses, imperfect or partial cycles.

3.3. Operational Modes (Run, Stop, Doze, Sleep)

The Si50x CMEMS series supports four operational output states. If enabled, the Si50x is in Run mode; thus, the clock is output and power is as specified in Table 1. The disable modes are Stop, Sleep, and Doze. Each of these states has a different power consumption profile, as specified in Table 1.

3.3.1. Stop Mode

The Si50x output in Stop mode is high-impedance, also known as High-Z (Hi-Z) or Tri-State. Stop mode disables the output driver, but the digital core and MEMS resonator remain enabled for fast transition to Run mode. The output is stopped and is held at High-Z after completing the last cycle glitch-free. No power saving measure is taken in Stop mode.

3.3.2. Doze Mode

The Si50x output in Doze mode is high-impedance, also known as High-Z (Hi-Z) or Tri-State. Doze mode disables the output driver, the VCO, and the MEMS resonator, but the digital core remains enabled. The output is stopped and is held at High-Z after completing the last cycle glitch-free.

3.3.3. Sleep Mode

The Si50x output in Sleep mode is high-impedance, also known as High-Z (Hi-Z) or Tri-State. Sleep mode disables power to all circuitry except for low-leakage circuitry that retains the last device configuration. The output is stopped and is held at High-Z after completing the last cycle glitch-free.

3.4. Output Rise and Fall Settings

The Si50x clock output is programmable. This enables reduction of electromagnetic interference (EMI) radiation from the clock output and also allows the Si50x to match the rise and fall of existing devices for easy replacement.

The amount of EMI reduction from changing tRise/tFall settings is dependent on the output frequency, the harmonic of interest, and the board layout. Lab results using a 50 MHz FOUT and changing the clock tRise/tFall time from 0.7 ns to 8 ns show up to 14 dB of EMI reduction relative to the fundamental.

The tRise/tFall feature also allows the Si50x to match competing devices' rise and fall times. Crystal oscillator tRise/tFall behavior is largely dependent on the supply voltage. In crystal-based oscillators, a higher supply voltage will generally drive a more rapid tRise/tFall time. The Si50x configuration options match the tRise/tFall to the supply voltage according to the specifications in this data sheet. The Si50x also provides a specified tRise/tFall with a given supply voltage and a 50 Ω trace impedance. See Table 4 for Si50x tRise/tFall specifications.

3.5. Single Wire C1 Interface

The Si504 single wire C1 interface uses Silicon Laboratories' patent-pending Transition Interval Code scheme which uses pulse widths to determine logic states.

IMPORTANT NOTE: The C1 interface supports a beginning C1D polarity of either high (C1D=1) or low (C1D=0). C1D steady state is provisioned as high; however, users can force C1D steady state low; however, the internal pull-up resistor will remain active. Given the above conditions, diagrams below show both C1D polarity options.

3.5.1. Single Wire C1 Interface Overview

1. Transactions start from the steady state value of C1D. C1D default steady state is high (C1D=1), but customers may start C1D low (C1D=0) if they wish.
2. The C1D steady state value can be changed by the user, but the Si504 default steady state will remain high (C1D=1), and C1D must be driven low by the user circuit. Any steady state value change must be followed by a T_{RESET} time during which no C1D changes are allowed.
3. Transactions end with the same C1D value as that with which they started.
4. Bit 0 and bit 1 are valid if they conform to the specified nominal time duration, T_{ZERO} and T_{ONE}, found in Table 3.
5. The timing of bit 0 and bit 1 can vary from T_{ZERO} and T_{ONE} nominal duration by ±10%. For example, if the nominal duration of bit 1 is 1 μs then the longest duration is 1 μs x 1.1 = 1.1 μs, and the shortest duration is 1 μs x 0.9 = 0.9 μs.
6. The minimum nominal duration of bit 1 is 2.5 times the nominal duration of bit 0, with a maximum duration as specified in Table 3.
7. If the C1D value is held steady for T_{RESET} in the middle of a transaction, the transaction will abort and all the data will be discarded.

3.6. C1 Setup/Reset Sequence, Command/Byte Write Transaction and Issuing Commands

3.6.1. Setup/Reset Sequence

The Setup/Reset Sequence is used to set up the C1 interface circuitry to receive commands. This transaction is mandatory after Power-Up and Wake-Up and optional after a command is reset using T_{RESET}. The initial Command Reset Transaction is shown in Figure 4.

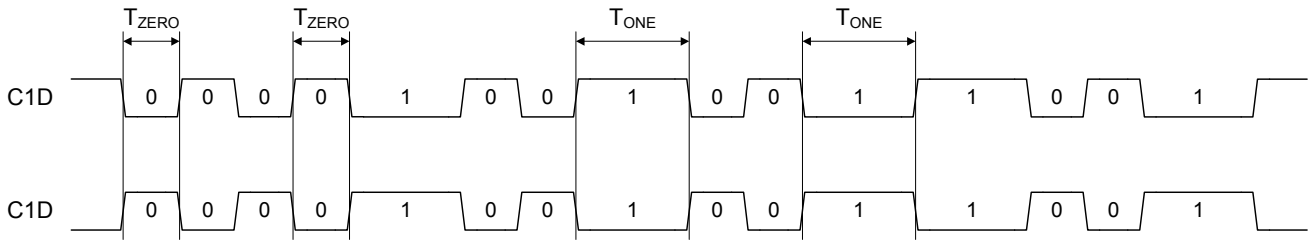


Figure 4. Setup/Reset Sequence

Note: Refer to Table 2 and Table 3 for additional information.

To initialize the C1 interface after Power-Up, the following procedure should be applied:

1. Apply V_{DD}.
2. Wait for T_{SU} to complete.
3. Apply the Setup/Reset Sequence.
4. C1D must be steady state for >T_{RESET}.
5. Wait for T_{RSC} to complete.
6. The device is ready to accept user commands.

To initialize the C1 interface after waking from sleep mode, the following procedure should be applied:

1. C1D activity is not allowed when the device is in Sleep mode. Any C1D edge may wake the device. Therefore, the Si504 does not accept user commands while in Sleep mode.
2. Wake the device by applying a C1D steady state value change or T_{WUP} C1D pulse. Please note that a C1D pulse narrower than the minimum T_{WUP} specification may still wake the device.
3. Wait for T_{RUN} to complete.
4. C1D must be steady state for >T_{RESET}.
5. Apply the Setup/Reset Sequence.
6. Wait for T_{RSC} to complete.
7. The device is ready to accept user commands.

3.6.2. Command/Byte Write Transaction

The Command/Byte Write Transaction is used for the Command Byte and the Data Byte transfer during the command sequence. Each Command/Byte Write Transaction is a 15-bit bit field—a 7-bit preamble (always all 0s), and an 8-bit command/data field. The Command/Byte Write Transaction is shown in Figure 5. (Note that the LSB bit D0 is transferred first during transactions.) The Command Sequence Timing is shown in Figure 6.

3.6.3. Issuing Commands

1. Commands consist of one or more Commands/Byte Write Transactions.
2. Each Command/Byte Write Transaction is a 15-bit bit field—a 7-bit preamble (always all 0s), and an 8-bit command/data field.
3. Commands start with a Command Byte followed by 0 to 4 Data Bytes of the command argument.

4. Command and data write transactions within user commands must be separated by at least T_{CBI} time.
5. Commands are processed after the last argument data byte is sent.
6. Commands with data arguments can be reset and aborted by issuing an Setup/Reset Sequence in place of the data byte. Note that the transferred portion of the user command will be discarded.
7. Transactions must be separated by at least T_{CI} time.
8. After Setup/Reset Sequence, wait at least T_{RSC} time before issuing commands.

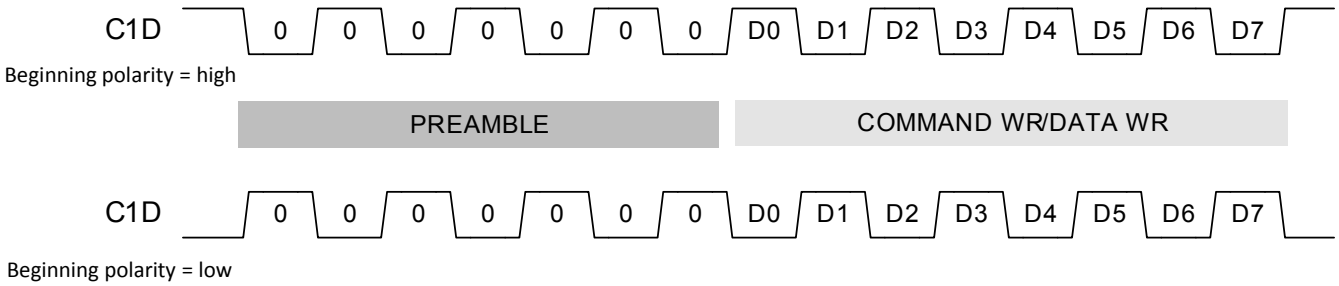
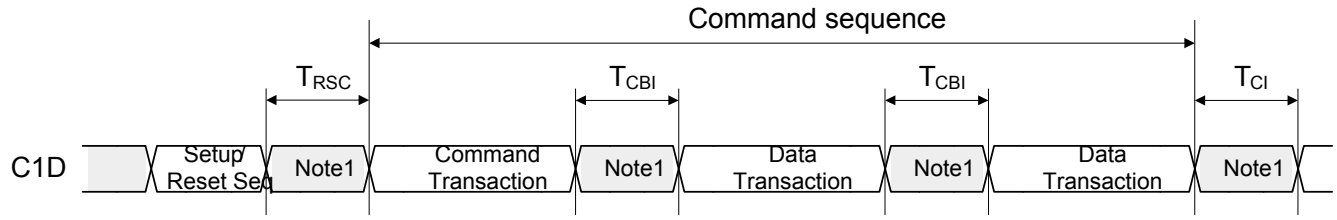


Figure 5. Command/Byte Write Transaction



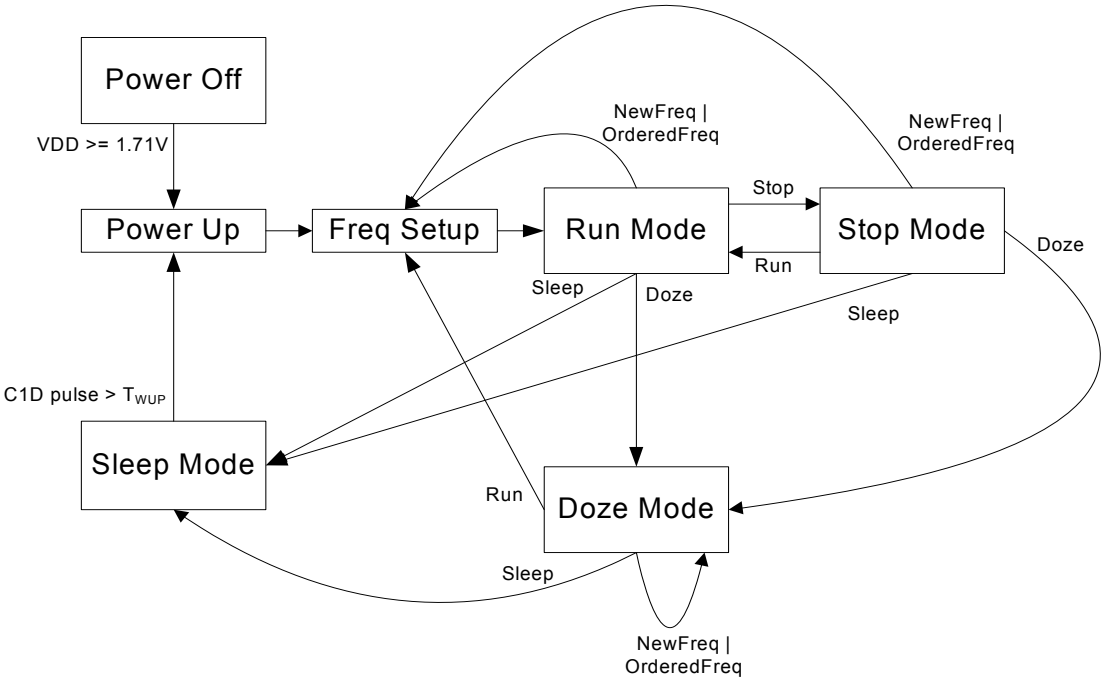
Notes:

1. The C1D value in shaded regions must remain stable for the action to complete. User may change C1D value to assert a C1D steady state change and reset the command.
2. Refer to Table 2 and Table 3 for additional information.

Figure 6. Command Sequence Timing

3.7. Command State Diagram

Figure 7 illustrates the valid operating Si504 modes and transition commands. As illustrated, when the Si504 is in the Frequency Setup state, it can only transition to Run mode. From Run mode, the Si504 can transition to either Stop, Doze, Sleep, or back to Frequency Setup.



Notes:

1. The device can receive C1 commands while it is in Run, Stop, or Doze modes. The device cannot receive C1 command while in Sleep mode.
2. Refer to Table 2 and Table 3 for additional information

Figure 7. Command State Diagram

3.8. Command Byte Table

Table 9. Command Bytes

Command Byte	Name	# Data Byte Arguments	Description
0x50	Run	0	**Run Command.** Transitions the Si504 from any powered down state to Run mode. The Si504 returns to Run mode in its last configuration including base frequency, frequency offsets, and other configurable options.
0x18	Stop	0	**Stop Command.** The output is stopped and is held at Hi-Z/Tri-State after completing the last cycle glitch-free. No power saving measure is taken.
0x20	Doze	0	**Doze Command.** The output is stopped and is held at Hi-Z/Tri-State after completing the last cycle glitch-free. Power savings measures are enabled.
0x30	Sleep	0	**Sleep Command.** The output is stopped and is held at Hi-Z/Tri-State after completing the last cycle glitch-free. Power is discontinued to all circuitry except for low-leakage circuitry which retains the last device configuration.
0x0C	NewFreq	4 (floating point 32-bit IEEE-754 number in Hz, MSB first)	**New Frequency Command.** NewFreq sets a new base frequency for the Si504. If the Si504 is in Run mode, the output clock will stop glitch-free, and then restart at the new base frequency within T_{NEW_FREQ} from the end of the command sequence. If the Si504 is in Stop or Doze mode, the new base frequency is stored and applied when the device is brought out of Stop or Doze mode. Any new base frequency may be overwritten while the device is in Stop or Doze mode. The last programmed new base frequency will be applied. The output clock does not glitch during its transition to the new base frequency. Please note that frequency offsets are cleared.

Table 9. Command Bytes (Continued)

Command Byte	Name	# Data Byte Arguments	Description
0x10	OriginalFreq	0	**Ordered Configuration Frequency.** OrderedFreq returns the Si504 to its original ordered frequency and configuration. If the Si504 is in Run mode, the output clock will stop glitch-free, and then restart at the ordered frequency within T_{NEW_FREQ} from the end of the command sequence. If the Si504 is in Stop or Doze mode, the command is stored and applied when the device is brought out of Stop or Doze mode. The output clock does not glitch during its transition. Please note that all pre-existing frequency offsets are cleared.
0x3A	OffsetFreq	2 (signed integer MSB first)	**Offset Frequency Bytes.** The Si504 slews to the offset frequency from the base frequency specified by OffsetFreq. The offset frequency is in increments of 29.8 ppb (or 2^{-25}). Frequency offset is an absolute frequency shift and is not a cumulative frequency shift. Stated differently, if there is an existing 1 ppm offset and the user requires a 2 ppm offset, the OffsetFreq command should program its value as 2 ppm offset. The original 1 ppm offset will be overwritten. When in Run mode, the offset frequency will be settled on the output as specified by T_{SLEW}. When in Stop or Doze mode, offset will be applied next time the part enters Run mode.

Table 9. Command Bytes (Continued)

<table>
<tr><th>Command Byte</th><th>Name</th><th># Data Byte Arguments</th><th>Description</th></tr>
<tr><td>0x41</td><td>DrvStrength</td><td>1</td><td>Drive Strength Configuration Command.
The output driver strength is selectable as specified in Table 4.

Changing the output driver strength while running may cause glitches.

<table>
<tr><th>Code</th><th>Normalized Output</th><th>Approximate tRise/tFall with V_{DD}</th></tr>
<tr><td>0x0</td><td>1x</td><td>8 ns (3.3V)</td></tr>
<tr><td>0x1</td><td>2x</td><td>5 ns (3.3V)</td></tr>
<tr><td>0x2</td><td>4x</td><td>3 ns (3.3V)</td></tr>
<tr><td>0x3</td><td>8x</td><td>1.3 ns (3.3V)</td></tr>
<tr><td>0x4</td><td>9x</td><td>1.3 ns (2.5V)</td></tr>
<tr><td>0x5</td><td>10x</td><td>1.3 ns (1.8V)</td></tr>
<tr><td>0x6</td><td>11x</td><td>1.3 ns (1.8V)</td></tr>
<tr><td>0x7</td><td>18x</td><td>0.7 ns (3.3V)</td></tr>
</table>
</td></tr>
<tr><td>0x49</td><td>PwrJitter</td><td>1</td><td>Power and Jitter Configuration Command.
The PwrJitter command transitions the device between low power or low jitter modes. The PwrJitter command may be written when the Si504 is in Run, Stop, or Doze mode, but does not take effect until the Si504 moves from one mode to another, thus passing through the Frequency Setup state illustrated in Figure 12. This includes issuing the Run command while the Si504 is in Run mode.

<table>
<tr><th>Code</th><th>Command</th></tr>
<tr><td>0x0</td><td>Low Power Mode</td></tr>
<tr><td>0x1</td><td>Low Jitter Mode</td></tr>
</table>
</td></tr>
<tr><td>0x00</td><td>No Op</td><td>0</td><td>No Operation.</td></tr>
</table>

4. Pin Description

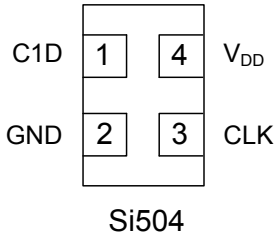


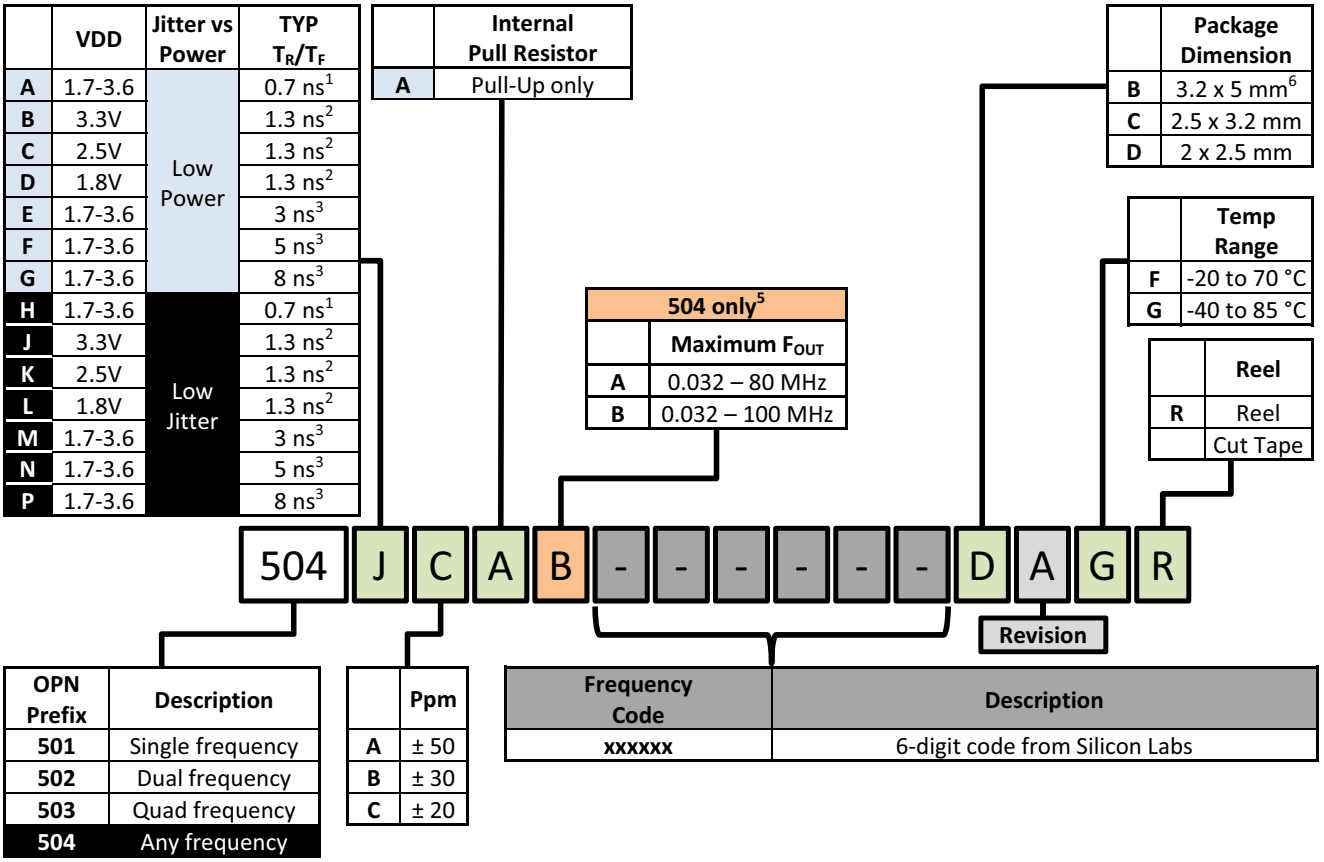
Figure 8. Si504 Pinout

Table 10. Pin Descriptions

Pin	Name	Function
1	C1D	Command Data Input Pin. C1D is the input to the single wire interface.
2	GND	Ground.
3	CLK	Output clock.
4	V_{DD}	Power Supply Pin. Bypass with a 0.1 μF capacitor placed as close to the V_{DD} pin as possible.

5. Ordering Guide

The Si50x family of CMEMS oscillators are highly configurable. Each orderable part number must be specified according to the guidelines below. Each customized part's performance is guaranteed to operate within the data sheet specifications. An online configuration and ordering tool is available at www.siliconlabs.com/cmems.



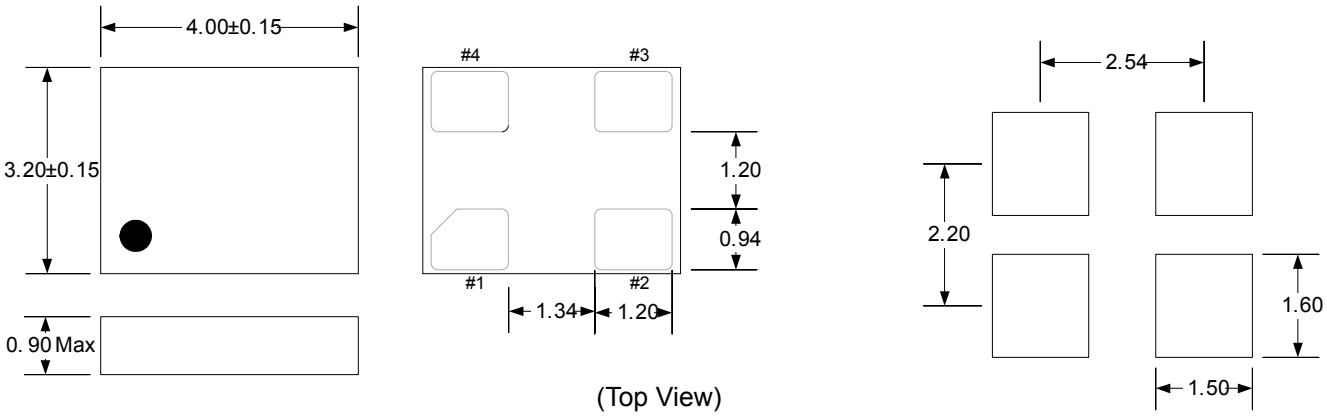
Note:

1. Series termination resistor (R_S) is recommended for this configuration. See Table 4 and Section 2.
2. Series termination resistor is not needed for this configuration. Output impedance is 50 Ω for the indicated supply condition.
3. Series termination resistor is not needed for this configuration. Reduced EMI setting.
4. Please note that the **maximum anticipated frequency** has no lower frequency limit. A device can either be configured to support from 32 kHz up to 80 MHz or from 32 kHz up to 100 MHz.
5. Silicon Labs 3.2 x 5 mm package is delivered as 3.2 x 4 mm and accommodates the industry-standard 3.2 x 5 mm footprint.

Figure 9. Si504 Part Number Syntax

6. Package Dimensions and Land Patterns

6.1. Package Outline: 3.2 x 5 mm 4-pin DFN



Note: The 3.2 x 5 mm package is delivered as a 3.2 x 4 mm package and is drop-in compatible to industry-standard 3.2 x 5 landing patterns.

Figure 10. 3.2 x 5 mm 4-pin DFN

6.2. Package Outline: 2.5 x 3.2 mm 4-pin DFN

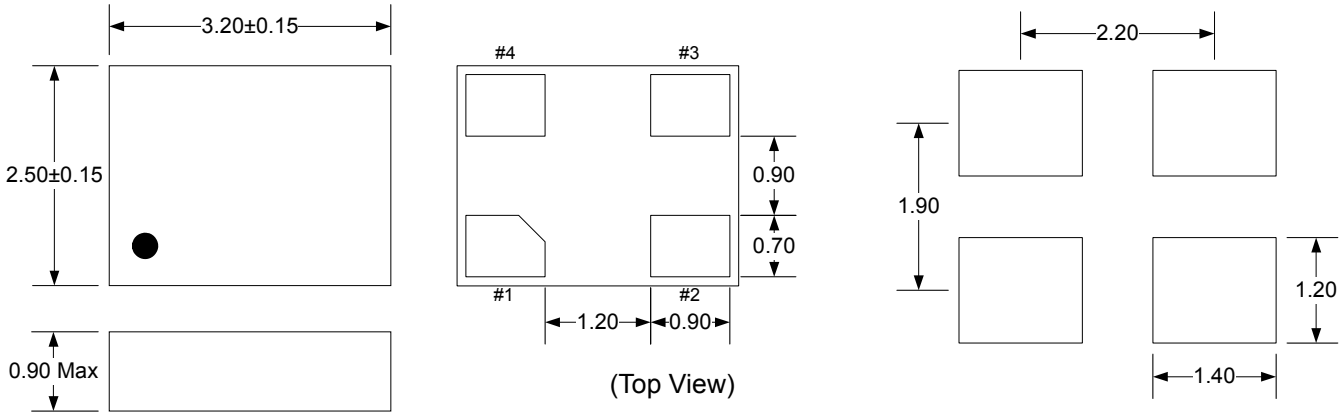


Figure 11. 2.5 x 3.2 mm 4-pin DFN

6.3. Package Outline: 2 x 2.5 mm 4-pin DFN

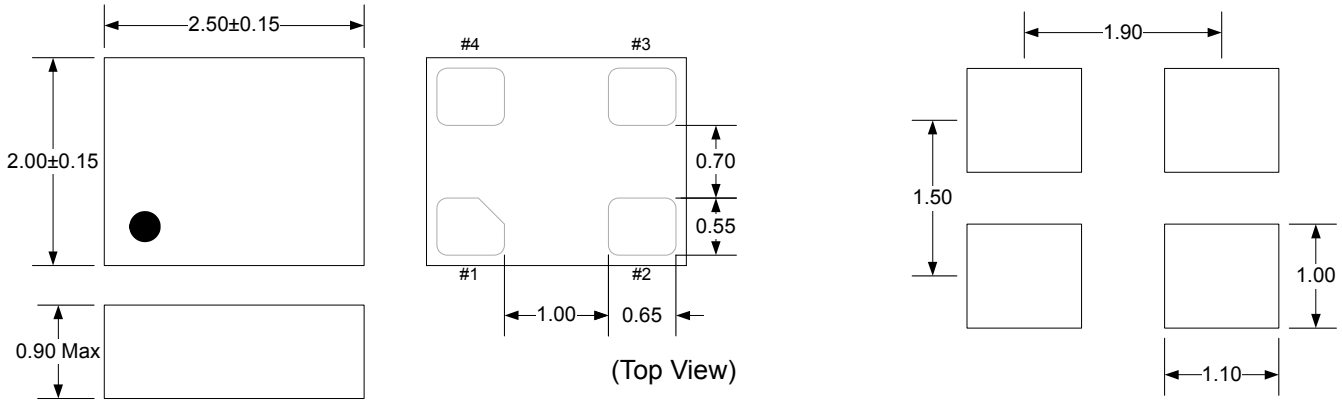
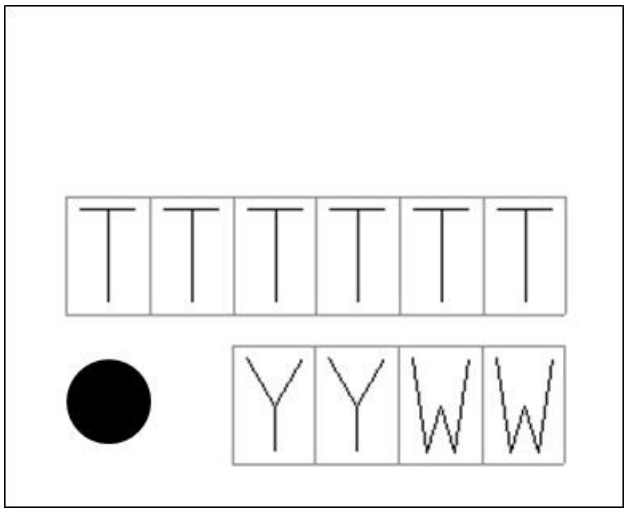


Figure 12. 2 x 2.5 mm 4-pin DFN

7. Top Markings

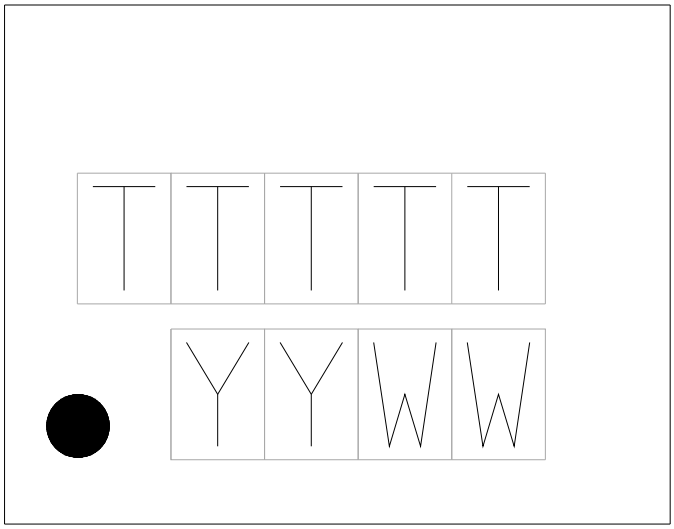
7.1. 3.2 x 5 mm Top Marking



7.2. 3.2 x 5 mm Top Marking Explanation

Mark Method:	Laser	
Font Size:	0.60 mm Right-Justified	
Line 1 Marking:	TTTTTT=Trace Code	Manufacturing Code from the Assembly Purchase Order form.
Line 2 Marking	Circle=0.5 mm Diameter Left-Justified	Pin 1 Indicator
	YY=Year WW=Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the build date.

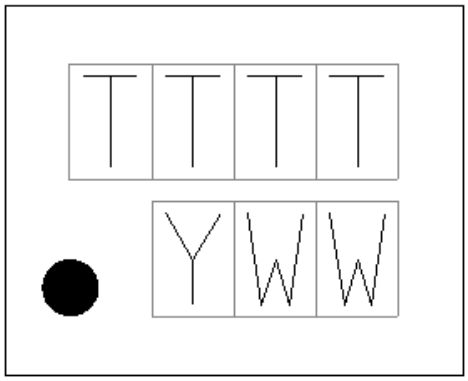
7.3. 2.5 x 3.2 mm Top Marking



7.4. 2.5 x 3.2 mm Top Marking Explanation

Mark Method:	Laser	
Font Size:	0.50 mm Right-Justified	
Line 1 Marking:	TTTTT=Trace Code	Manufacturing Code from the Assembly Purchase Order form.
Line 2 Marking:	Circle=0.3 mm Diameter Left-Justified	Pin 1 Indicator
	Y=Year WW=Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the build date.

7.5. 2 x 2.5 mm Top Marking



7.6. 2 x 2.5 mm Top Marking Explanation

Mark Method:	Laser	
Font Size:	0.50 mm Right-Justified	
Line 1 Marking:	TTTT=Trace Code	Manufacturing Code from the Assembly Purchase Order form.
Line 2 Marking:	Circle=0.3 mm Diameter Left-Justified	Pin 1 Indicator
	Y=Year WW=Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the build date.

Document Change List

Revision 0.21 to Revision 0.4

- Modified Title page.
- Modified Table 1.
- Modified Table 2.
- Modified Table 3.
- Modified Table 4.
- Modified Table 5.
- Modified Table 6.
- Modified Table 7.
- Modified Table 8.
- Modified Section 2.
- Modified Section 3.
- Modified Section 4.
- Modified Section 5.
- Modified Section 6.
- Modified Section 7.

Revision 0.4 to Revision 0.41

- Modified Table 5.

Revision 0.41 to Revision 0.7

- Revised supported frequency range
- Added MIN/MAX figures to all relevant tables

Revision 0.7 to Revision 0.71

- Revised Table 4
- Revised Section 6

Revision 0.71 to Revision 0.72

- Revised Table 2.
- Revised Table 4.
- Revised Table 6.
- Modified Section 2.
- Modified Section 3.
- Modified Section 5.

Contact Information

Silicon Laboratories Inc.

400 West Cesar Chavez
Austin, TX 78701
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Please visit the Silicon Labs Technical Support web page:
https://www.siliconlabs.com/support/pages/contacttechnicalsupport.aspx
and register to submit a technical support request.

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