Si53320

1:5 Low Jitter LVPECL Clock Buffer with 2:1 Input Mux

Features

- 5 LVPECL outputs
- Ultra-low additive jitter: 100 fs rms
- Wide frequency range: 1 to 725 MHz
- Input compatible with LVPECL, LVDS, CML, HCSL, LVCMOS
- 2:1 mux with hot-swappable inputs
- Glitchless input clock switching
- Synchronous output enable
- 20-TSSOP
- Low output-output skew: <50 ps
- Low propagation delay variation: <400 ps
- V_{REF} reference voltage for single-ended input clocking
- RoHS compliant, Pb-free
- Industrial temperature range: –40 to +85 °C
- Footprint-compatible with MC100LVEP14, SY100EP14U, MAX9310

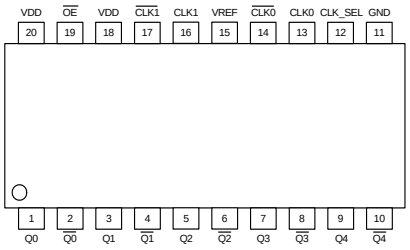
Ordering Information:
See page 17.

Applications

- High-speed clock distribution
- Ethernet switch/router
- Optical Transport Network (OTN)
- SONET/SDH
- PCI Express Gen 1/2/3
- Storage
- Telecom
- Industrial
- Servers
- Backplane clock distribution

Pin Assignments

Si53320



Patents pending

Description

The Si53320 is an ultra low jitter five output LVPECL buffer with synchronous OE. Outputs are enabled/disabled in a low state, ensuring runt pulses are not created when the device is enabled/disabled. The Si53320 features a 2:1 input mux, making it ideal for redundant clocking applications. The Si53320 utilizes Silicon Laboratories' advanced CMOS technology to fanout clocks from 1 to 725 MHz with guaranteed low additive jitter, low skew, and low propagation delay variability. The Si53320 features minimal cross-talk and provides superior supply noise rejection, simplifying low jitter clock distribution in noisy environments.

Functional Block Diagram

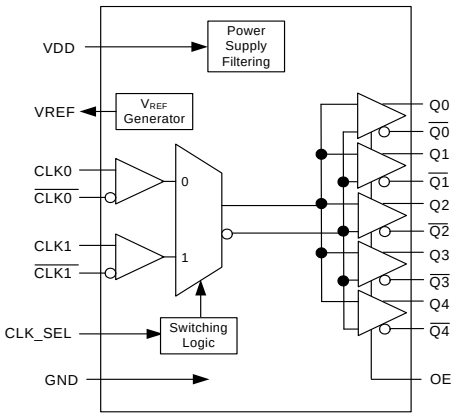


TABLE OF CONTENTS

1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Operating Temperature	T_A		–40	—	85	°C
Supply Voltage Range*	V_{DD}	LVPECL	2.38	2.5	2.63	V
			2.97	3.3	3.63	V

Table 2. Input Clock Specifications

(V_{DD}=2.5 V ± 5%, or 3.3 V ± 10%, T_A=–40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential Input Common Mode Voltage	V_{CM}	VDD = 2.5 V± 5%, 3.3 V± 10%	0.05	—	—	V
Input Swing (single-ended, peak-to-peak)	V_{IN}		0.1	—	1.1	V
Input Voltage High	V_{IH}		VDD x 0.7	—	—	V
Input Voltage Low	V_{IL}		—	—	VDD x 0.3	V
Input Capacitance	C_{IN}		—	5	—	pF

Table 3. DC Common Characteristics

(V_{DD} = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%,T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current	I_{DD}		—	TBD	275	mA
Leakage Current	I_L	Input leakage at all inputs except CLKIN, V_{IN} = 0 V	—	—	TBD	µA
		Input leakage at CLKIN V_{IN} = 0 V	—	—	TBD	µA
Voltage Reference	V_{REF}	V_{REF} pin	—	VDD/2	—	V
Internal Pull-down Resistor	R_{DOWN}	CLK_SEL	—	25	—	kΩ
Internal Pull-up Resistor	R_{UP}	OE	—	25	—	kΩ

Table 4. DC Characteristics—LVPECL

(V_{DD} = 2.5 V ± 5%, or 3.3 V ± 10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage High	V_{OH}	R_L = 50 Ω to V_{DDOX} – 2 V	V_{DDOX} – 1.145	—	V_{DDOX} – 0.895	V
Output Voltage Low	V_{OL}	R_L = 50 Ω to V_{DDOX} – 2 V	V_{DDOX} – 1.945	—	V_{DDOX} – 1.695	V
Output DC Common Mode Voltage	V_{COM}		V_{DDOX} – 1.895	—	V_{DDOX} – 1.425	V
Single-Ended Output Swing	V_{SE}	Terminate unused outputs to R_L = 50 Ω to V_{DDOX}-2 V	0.25	0.60	0.85	V

Table 5. AC Characteristics

(V_{DD} = 2.5 V ± 5%, or 3.3 V ± 10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency	F	LVPECL	1	—	725	MHz
Duty Cycle **Note:** 50% input duty cycle.	D_C	20/80% T_R/T_F<10% of period (Differential)	48	50	52	%
Minimum Input Clock Slew Rate[1]	SR	Required to meet prop delay and additive jitter specifications (20–80%)	0.75	—	—	V/ns
Output Rise/Fall Time	T_R/T_F	LVPECL, LVDS, CML, HCSL, 20/80%			350	ps
Minimum Input Pulse Width	T_W		500	—	—	ps
Additive Jitter (Differential Clock Input)	J	V_{DD} = 2.5/3.3 V, LVPECL, F = 725 MHz, 0.75 V/ns input slew rate	—	60	80	fs
Propagation Delay	T_{PLH}, T_{PHL}	Low to high, high to low Single-ended	TBD	—	TBD	ns
		Low to high, high to low Differential	TBD	—	TBD	ns

Notes:

1. For clock division applications, a minimum input clock slew rate of 30 mV/ns is required.
2. See Figure 4.
3. Defined as skew between outputs on different devices operating at the same supply voltages, temperatures, and equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
4. Measured for 156.25 MHz carrier frequency. Sine-wave noise added to V_{DDOX} (1.8V=50mV_{PP}, 2.5/3.3V=100mV_{PP}) and noise spur amplitude measured. See AN491 for further details.

Table 5. AC Characteristics (Continued)

(V_{DD} = 2.5 V ± 5%, or 3.3 V ± 10%,T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Enable Time[2]	T_{EN}	F = 1 MHz	—	2	—	µs
		F = 100 MHz	—	60	—	ns
		F = 725 MHz	—	50	—	ns
Output Disable Time[2]	T_{DIS}	F = 1 MHz	—	2	—	µs
		F = 100 MHz	—	25	—	ns
		F = 725 MHz	—	15	—	ns
Output to Output Skew	T_{SK}	Identical Configuration, Single-ended (Q_N to Q_M)	—	—	100	ps
		Identical Configuration, Differential (Q_N to Q_M)	—	—	50	ps
Part to Part Skew[3]	T_{PS}	Identical configuration	—	50	—	ps
Power Supply Noise Rejection[4]	PSRR	10 kHz sinusoidal noise	—	–90	—	dBc
		100 kHz sinusoidal noise	—	–90	—	dBc
		500 kHz sinusoidal noise	—	–80	—	dBc
		1 MHz sinusoidal noise	—	–70	—	dBc

Notes:

1. For clock division applications, a minimum input clock slew rate of 30 mV/ns is required.
2. See Figure 4.
3. Defined as skew between outputs on different devices operating at the same supply voltages, temperatures, and equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
4. Measured for 156.25 MHz carrier frequency. Sine-wave noise added to V_{DDOX} (1.8V=50mV_{PP}, 2.5/3.3V=100mV_{PP}) and noise spur amplitude measured. See AN491 for further details.

Table 6. Thermal Conditions

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	Still air	46.2	°C/W
Thermal Resistance, Junction to Case	θ_{JC}	Still air	27.1	°C/W

Table 7. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage Temperature	T_S		–55	—	150	°C
Supply Voltage	VDD		–0.5	—	3.8	V
Input Voltage	V_{IN}		–0.5	—	VDD+ 0.3	V
Output Voltage	V_{OUT}		—	—	VDD+ 0.3	V
ESD Sensitivity	HBM	HBM, 100 pF, 1.5 kΩ	2000	—	—	V
ESD Sensitivity	CDM		500	—	—	V
Peak Soldering Reflow Temperature	T_{PEAK}	Pb-Free; Solder reflow profile per JEDEC J-STD-020	—	—	260	°C
Maximum Junction Temperature	T_J		—	—	125	°C

Note: Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.

2. Functional Description

The Si53320 is a low jitter, low skew 1:5 LVPECL buffer with an integrated 2:1 input mux. The device has a universal input that accepts most common differential or LVCMOS input signals. A clock select pin is used to select the active input clock.

2.1. Universal, Any-Format Input

The Si53320 has a universal input stage that enables simple interfacing to a wide variety of clock formats, including LVPECL, LVCMOS, LVDS, HCSL, and CML. Tables 8 and 9 summarize the various ac- and dc-coupling options supported by the device. Figures 3 and 4 show the recommended input clock termination options.

Table 8. LVPECL, LVCMOS, and LVDS

	LVPECL		LVCMOS		LVDS	
	AC-Couple	DC-Couple	AC-Couple	DC-Couple	AC-Couple	DC-Couple
1.8 V	N/A	N/A	No	Yes	Yes	No
2.5/3.3 V	Yes	Yes	No	Yes	Yes	Yes

Table 9. HCSL and CML

	HCSL		CML	
	AC-Couple	DC-Couple	AC-Couple	DC-Couple
1.8 V	No	No	Yes	No
2.5/3.3 V	No	Yes (3.3 V)	Yes	No

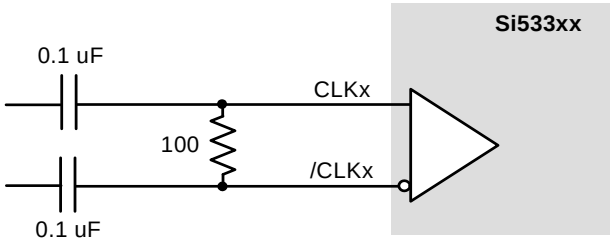


Figure 1. Differential LVPECL, LVDS, CML AC-Coupled Input Termination

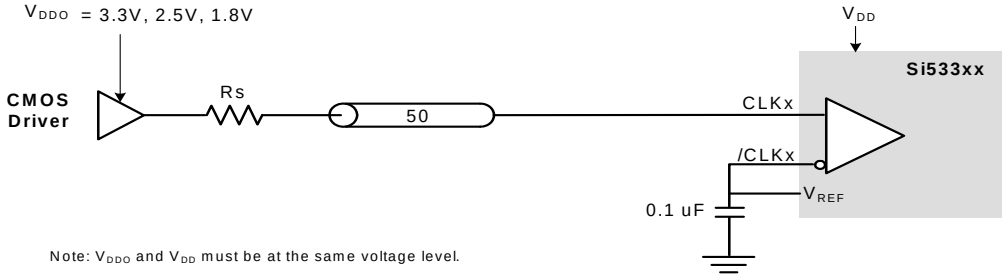
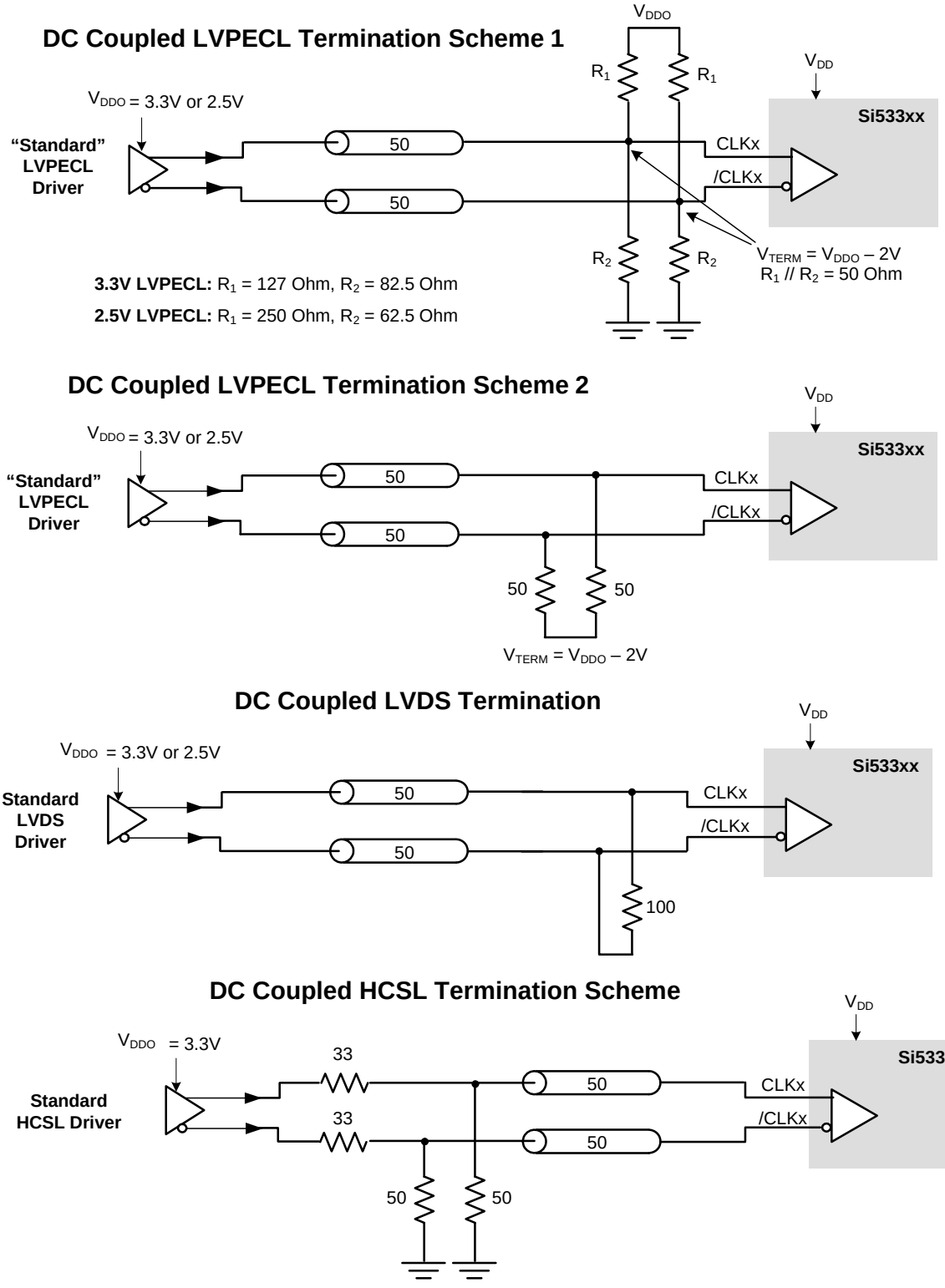


Figure 2. LVCMOS DC-Coupled Input Termination



Note: 33 Ohm series termination is optional depending on the location of the receiver.

Figure 3. Differential DC-Coupled Input Terminations

2.2. Input Bias Resistors

Internal bias resistors ensure a differential output low condition in the event that the clock inputs are not connected. The noninverting input is biased with a 18.75 kΩ pulldown to GND and a 75 kΩ pullup to V_{DD}. The inverting input is biased with a 75 kΩ pullup to V_{DD}.

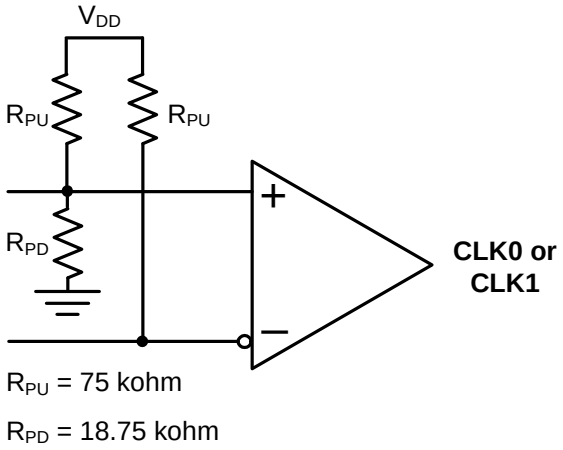
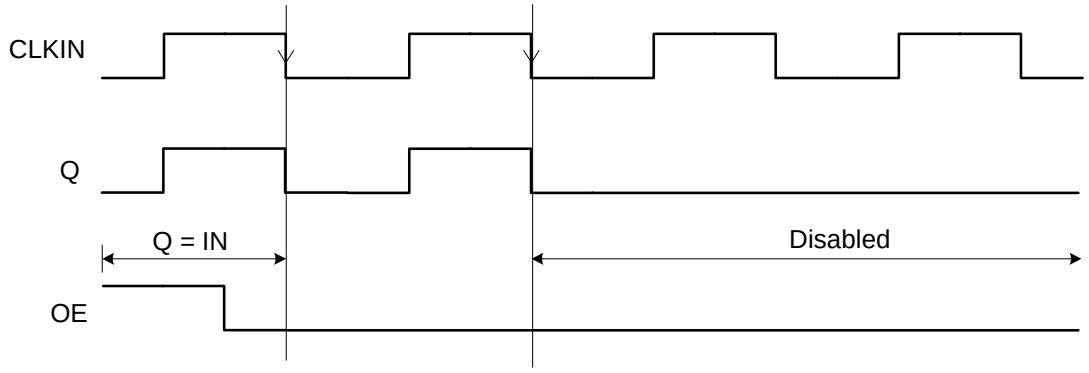


Figure 4. Input Bias Resistors

2.3. Synchronous Output Enable

The Si53320 features a synchronous output enable (disable) feature. Output enable is sampled and synchronized on the falling edge of the input clock. This feature prevents runt pulses from being generated when the outputs are enabled or disabled.



Note 1. Outputs are disabled after 1 to 2 negative edges of the input clock.

Figure 5. Synchronous Output Enable

When OE is low, Q is held low and $\overline{Q}$ is held high for differential output formats.

2.4. Input Mux and Output Enable Logic

The Si53320 provides two clock inputs for applications that need to select between one of two clock sources. The CLK_SEL pin selects the active clock input. The table below summarizes the input and output clock based on the input mux and output enable pin settings.

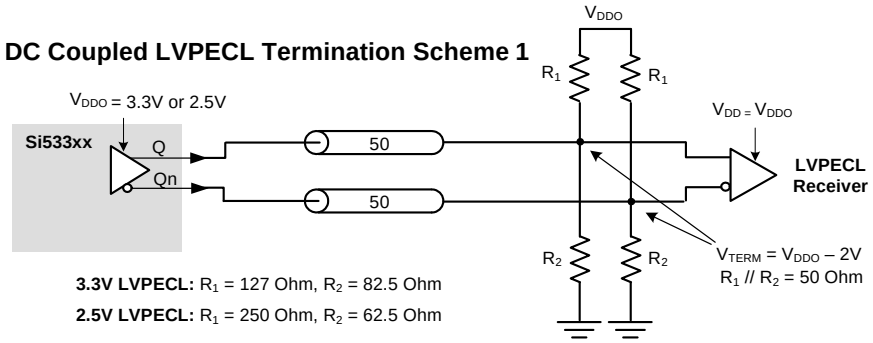
Table 10. Input Mux and Output Enable Logic

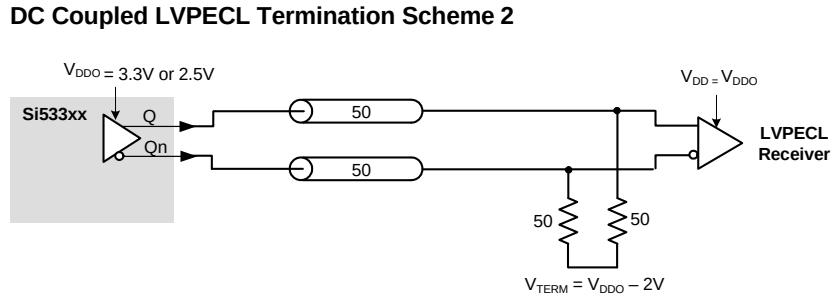
CLK_SEL	CLK0	CLK1	OE[1]	Q[2]
L	L	X	H	L
L	H	X	H	H
H	X	L	H	L
H	X	H	H	H
X	X	X	L	L[3]

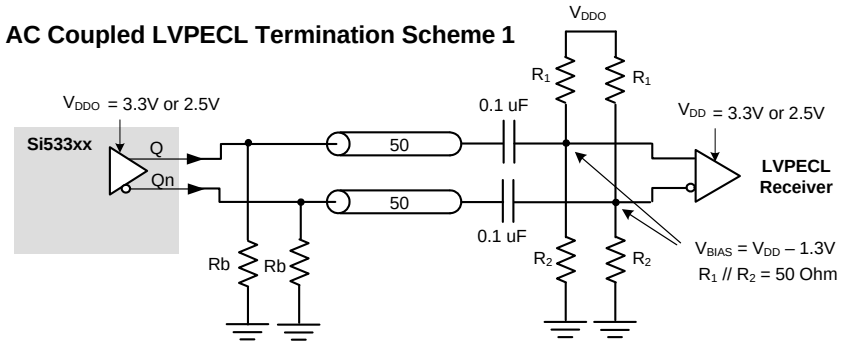
Notes:
1. Output enable active high
2. On the next negative transition of CLK0 or CLK1.
3. Q=low, $\overline{Q}$=high

2.5. Output Clock Termination Options

The recommended output clock termination options are shown below. Unused output clocks should be left floating.







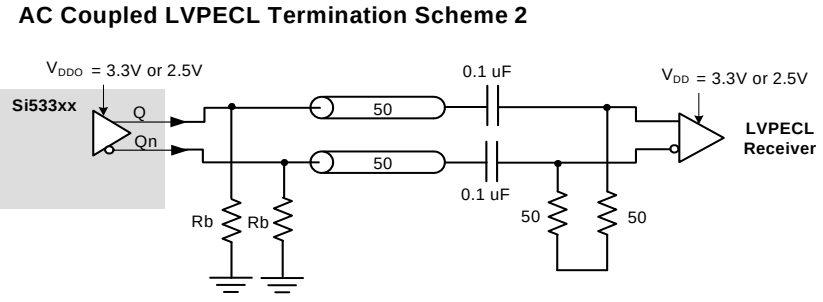


Figure 6. LVPECL Output Termination

2.6. AC Timing Waveforms

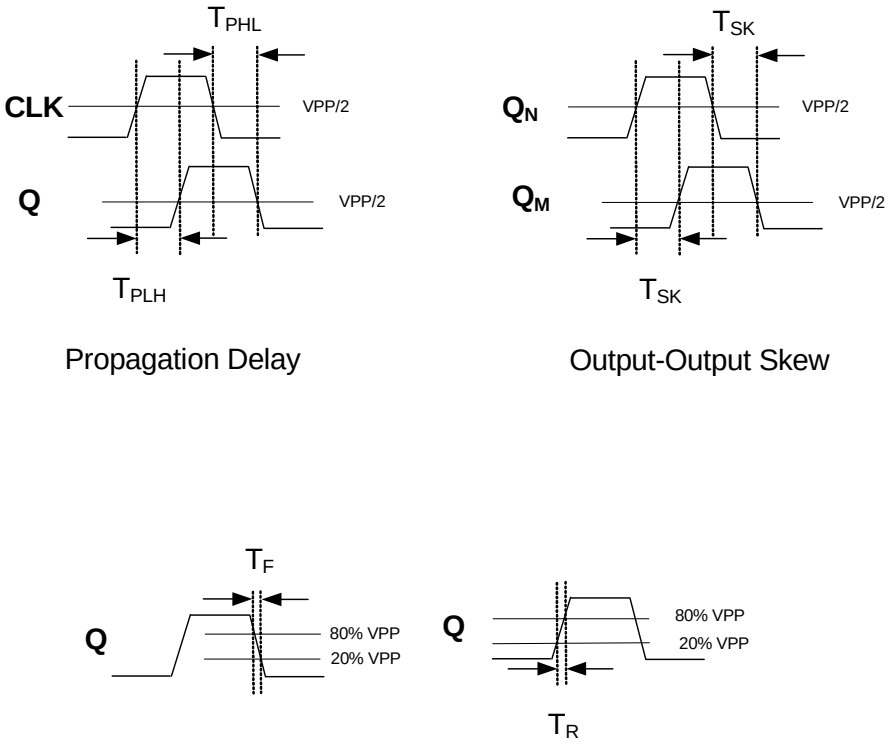
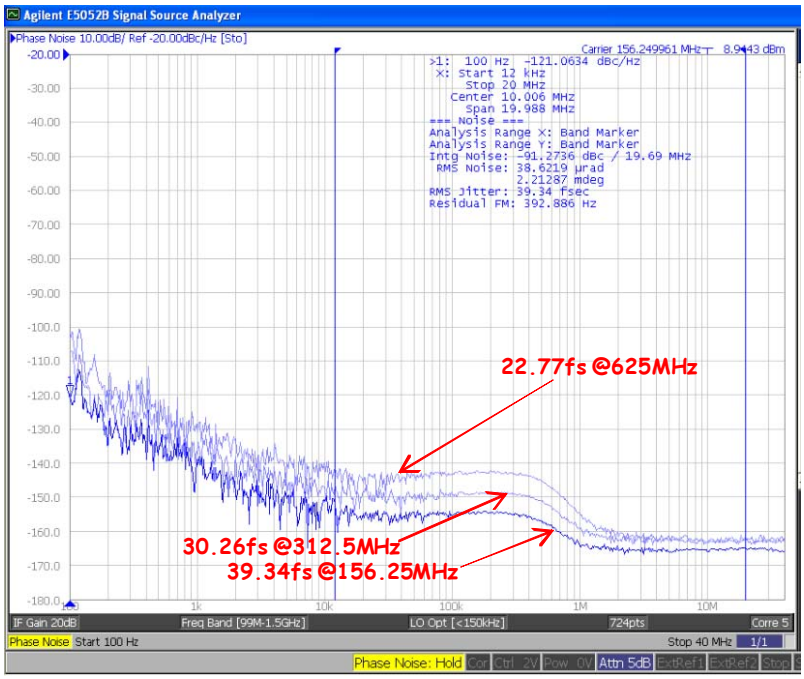
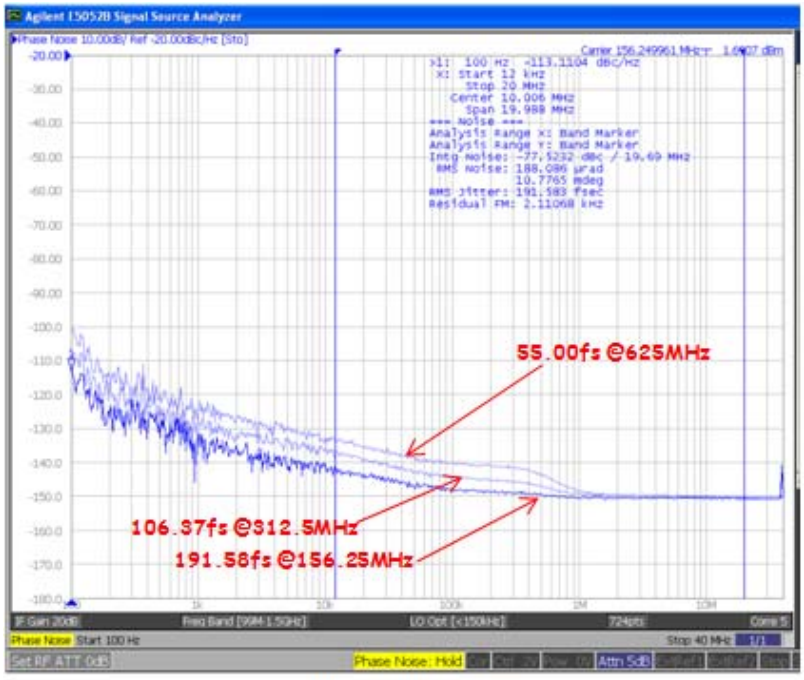


Figure 7. AC Waveforms

2.7. Typical Phase Noise Performance



Source Jitter



Total Jitter

Figure 8. Si53320 Phase Noise

Note: Measured single-endedly.

Table 11. Si53320 Additive Jitter

Frequency (MHz)	Source Jitter (fs)	Total Jitter (fs)	Additive Jitter (fs)
156.25	39.34	191.58	187.50
312.5	30.26	106.37	101.98
625	22.77	55.00	50.07

3. Pin Description: 20-Pin TSSOP

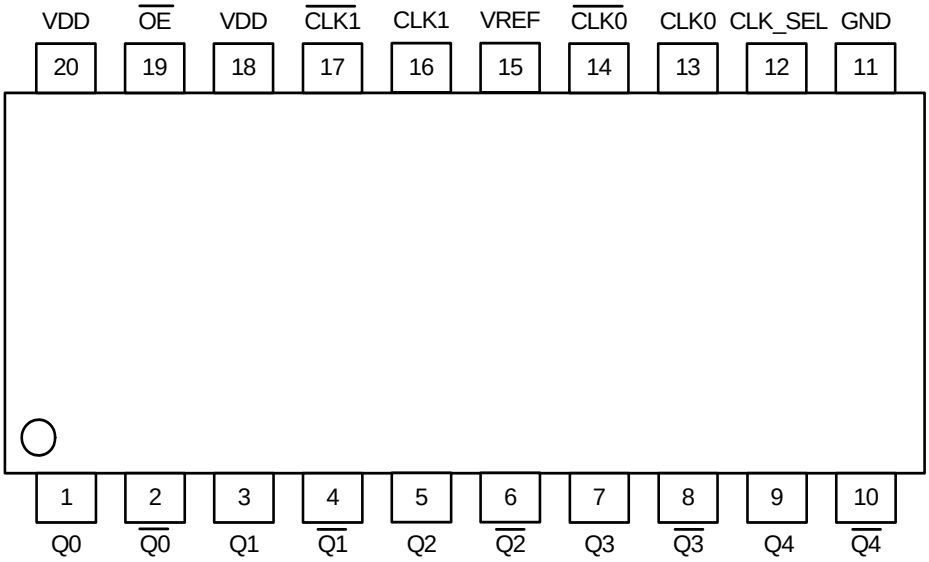


Table 12. Si53320 20-Pin TSSOP Descriptions

Pin #	Name	Description
1	Q0	Output clock 0.
2	$\overline{Q0}$	Output clock 0 (complement).
3	Q1	Output clock 1.
4	$\overline{Q1}$	Output clock 1 (complement).
5	Q2	Output clock 2.
6	$\overline{Q2}$	Output clock 2 (complement).
7	Q3	Output clock 3.
8	$\overline{Q3}$	Output clock 3 (complement).
9	Q4	Output clock 4.
10	$\overline{Q4}$	Output clock 4 (complement).
11	GND	Ground.
12	CLK_SEL	Mux input select pin (LVCMOS). When CLK_SEL is high, CLK1 is selected. When CLK_SEL is low, CLK0 is selected. CLK_SEL contains an internal pull-down resistor.
13	CLK0	Input clock 0. Defaults low when left open.
14	$\overline{CLK0}$	Input clock 0 (complement).

Table 12. Si53320 20-Pin TSSOP Descriptions (Continued)

Pin #	Name	Description
15	V_{REF}	Input reference voltage. When driven by a LVCMOS clock input, connect the unused clock input to V_{REF} and a 0.1µF cap to ground. When driven by a differential clock, do not connect the V_{REF} pin.
16	CLK1	Input clock 1. Defaults low when left open.
17	$\overline{CLK1}$	Input clock 1 (complement).
18	V_{DD}	Core voltage supply. Bypass with 1.0 µF capacitor and place as close to the V_{DD} pin as possible.
19	OE	Output enable. When OE = high, the clock outputs are enabled. When OE = low, Q is held low and $\overline{Q}$ is held high. OE contains an internal pull-up resistor.
20	V_{DD}	Core voltage supply. Bypass with 1.0 µF capacitor and place as close to the V_{DD} pin as possible.

4. Ordering Guide

Part Number	Package	Pb-Free, ROHS-6	Temperature
Si53320-B-GT	20-TSSOP	Yes	–40 to 85 °C

5. Package Outline

5.1. 20-TSSOP Package Diagram

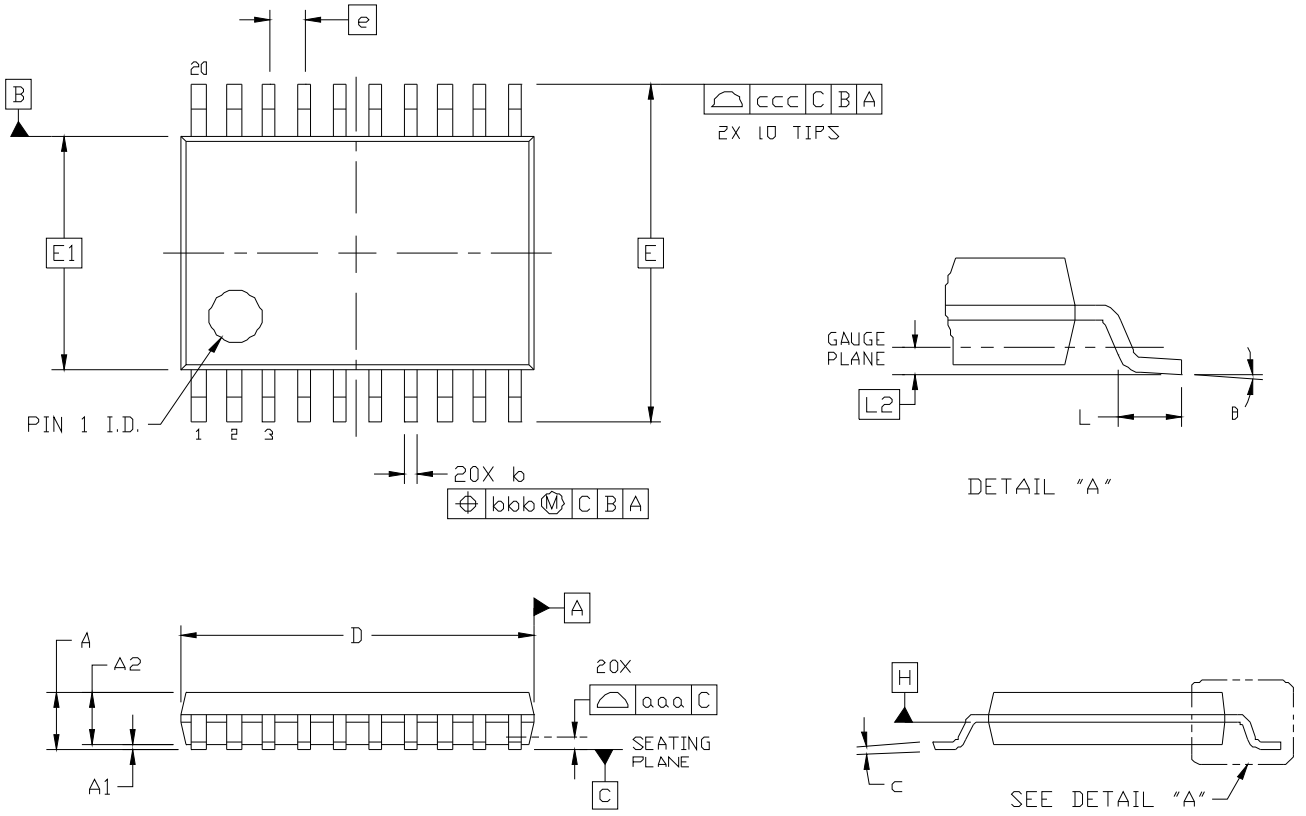


Figure 9. Si53320 20-TSSOP Package Diagram

Table 13. Package Dimensions

Dimension	Min	Nom	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
D	6.40	6.50	6.60
E	6.40 BSC		
E1	4.30	4.40	4.50

Dimension	Min	Nom	Max
e	0.65 BSC		
L	0.45	0.60	0.75
L2	0.25 BSC		
θ	0°	—	8°
aaa	0.10		
bbb	0.10		
ccc	0.20		

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-153, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6. PCB Land Pattern

6.1. 20-TSSOP Package Land Pattern

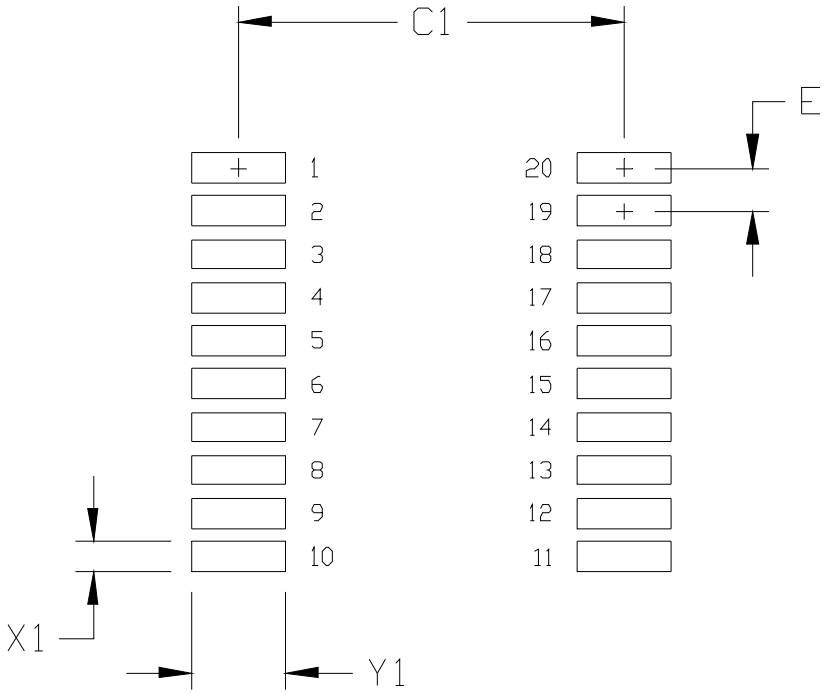


Figure 10. Si53320 20-TSSOP Package Land Pattern

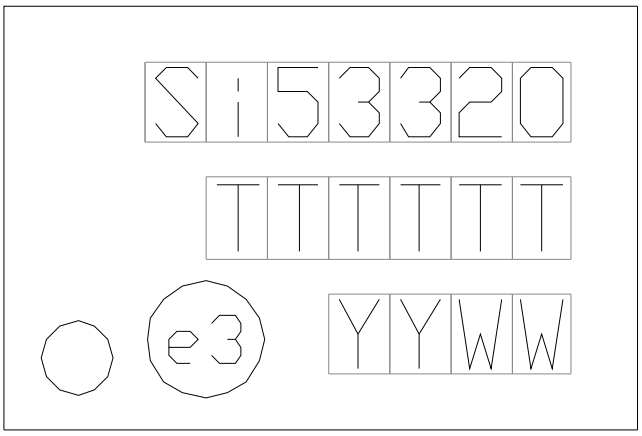
Table 14. PCB Land Pattern

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.80
E	Pad Row Pitch	0.65
X1	Pad Width	0.45
Y1	Pad Length	1.40

Notes:
1. This Land Pattern Design is based on IPC-7351 specifications for Density Level B (Median Land Protrusion)
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

7. Top Marking

7.1. Si53320 Top Marking



7.2. Top Marking Explanation

Mark Method:	Laser	
Font Size:	2.0 Point (0.71 mm) Right-Justified	
Line 1 Marking:	Customer Part Number	**Si53320**
Line 2 Marking:	TTTTTT = Mfg Code	Manufacturing Code from Assembly Purchase Order form.
Line 3 Marking:	Circle = 1.2 mm Diameter	“e3” Pb-Free Symbol
	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to year and work week of the build date.

NOTES:

CONTACT INFORMATION

Silicon Laboratories Inc.

400 West Cesar Chavez
Austin, TX 78701
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Please visit the Silicon Labs Technical Support web page:
https://www.silabs.com/support/pages/contacttechnicalsupport.aspx
and register to submit a technical support request.

Patent Notice

Silicon Labs invests in research and development to help our customers differentiate in the market with innovative low-power, small size, analog-intensive mixed-signal solutions. Silicon Labs' extensive patent portfolio is a testament to our unique approach and world-class engineering team.