TOSHIBA CMOS Integrated Circuit Silicon Monolithic

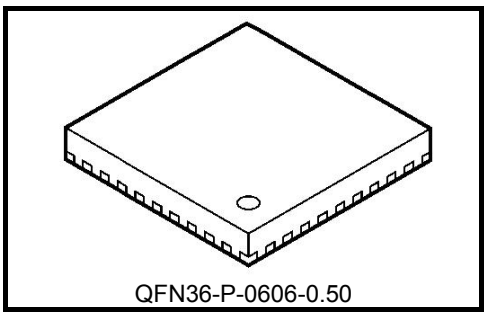
TC32306FTG

Single-Chip RF Transceiver for Low-Power Systems

1. Abstract

The TC32306FTG is a single-chip RF transceiver, which provides many of the functions required for UHF-band transceiver applications. It has the most features transmiting and receiveing the signal.
Furthermore, by digital processing, it can reduce significantly the number of external components and allow fine adjustments.

Various type of applications are supported by this chip as configuring various settings such as supply voltage, frequency, modulation and detection.



Weight: 0.08 g (typ.)

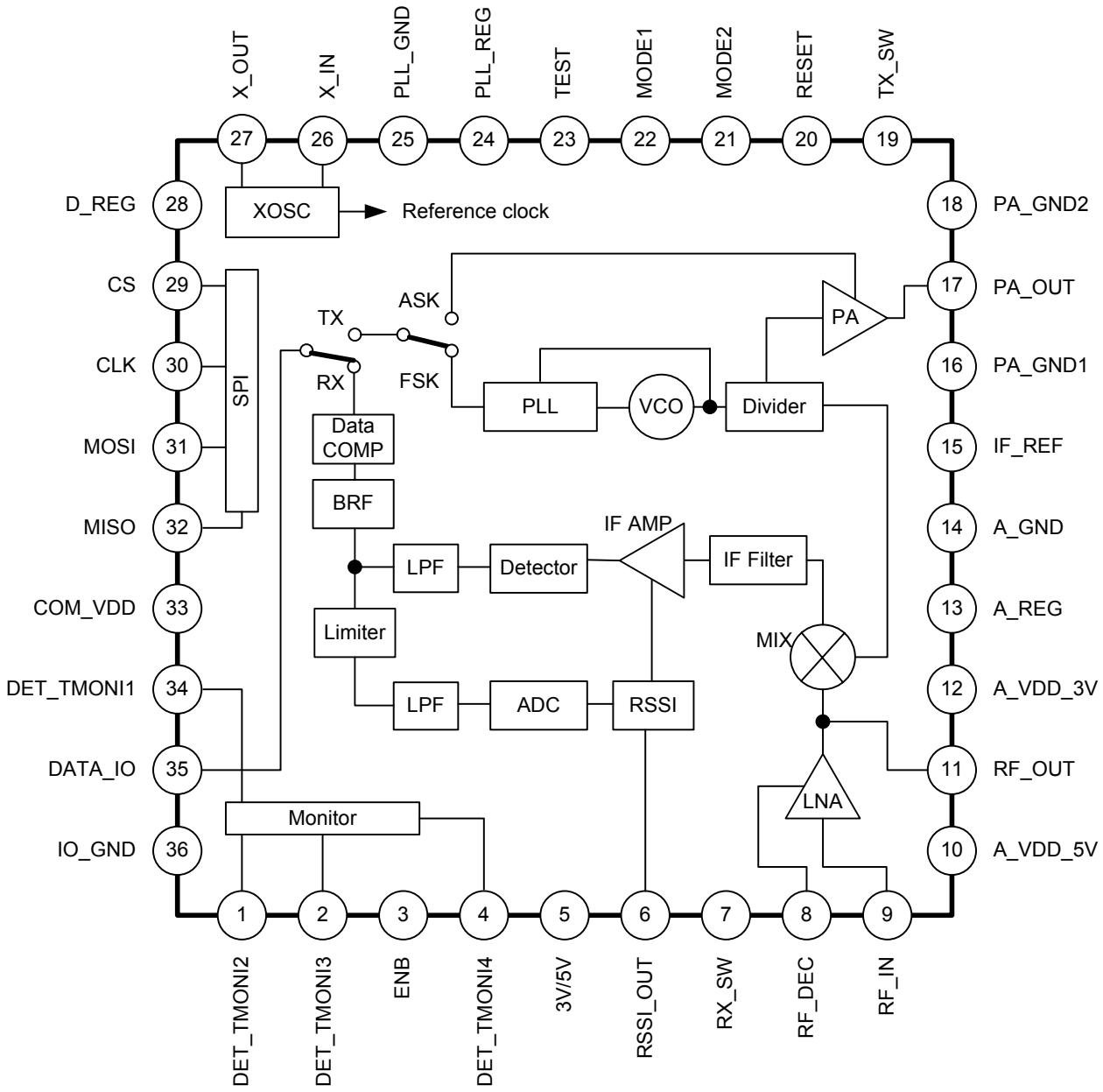
2. Applications

Remote keyless entry (remote door lock / unlock of equipment), automotive equipment applications such as tire pressure monitoring system, and remote controller, etc

3. Features

- Integrates LNA, Mixer, IF Filter, IF AMP, RSSI, Signal Detector, Bit Rate Filter, Data Comparator, PLL, VCO and PA into a single IC.
- Operating voltage range: 2.0 to 3.3 V (For 3V Use), 2.4V to 5.5V (For 5V Use)
- Current consumption: TX 12 mA at +10dBm output level / RX 9.7 mA / Battery Saving 0uA (typ.)
- Use for four RF Band: 315, 434, 868 / 915 MHz
- Supported modulation: ASK / FSK
- Single conversion system
- Two IF Filter bandwidth: wide 320kHz(typ.) at IF = 230kHz / middle 270kHz(typ.) at IF = 280kHz
- Signal Detections: RSSI detection, Noise detection (Only for FSK), Preamble detection
- Receiver sensitivity: under -116dBm (At IF BW = 320kHz, data rate = 600Hz, frequency deviation = +/-40kHz)
- Transmitter power: +10dBm (typ.)
- Serial control (4 wire SPI) / EEPROM control
- Data Comparator Quick Charge / AutoOff Control / Antenna Switch Control

4. Block Diagram



Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

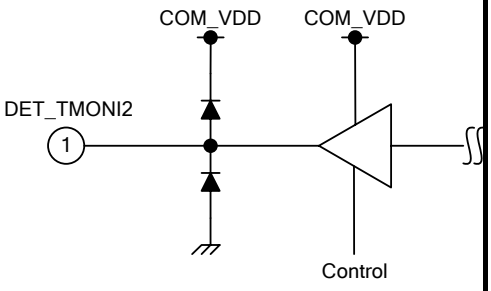
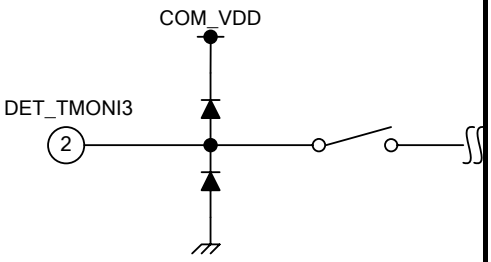
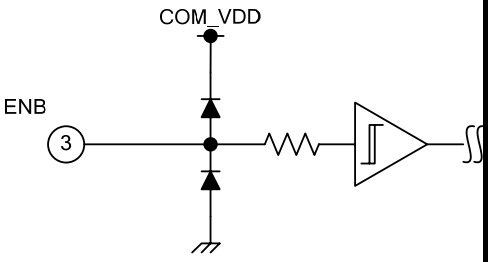
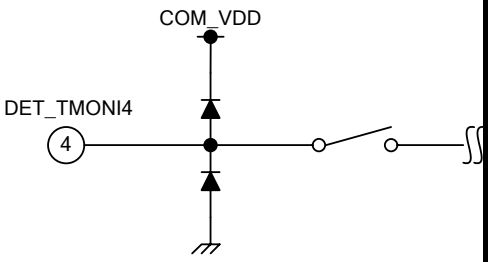
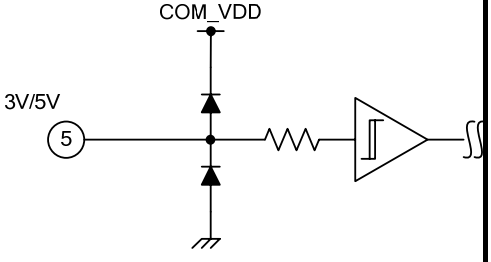
Fig 4-1 Block Diagram

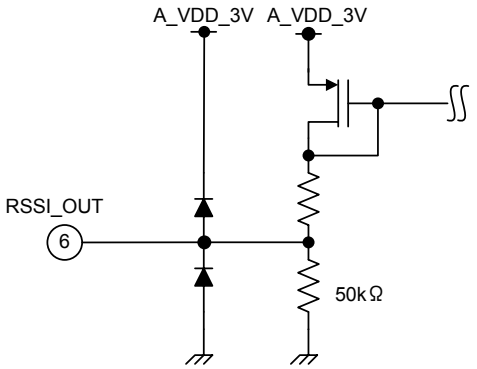
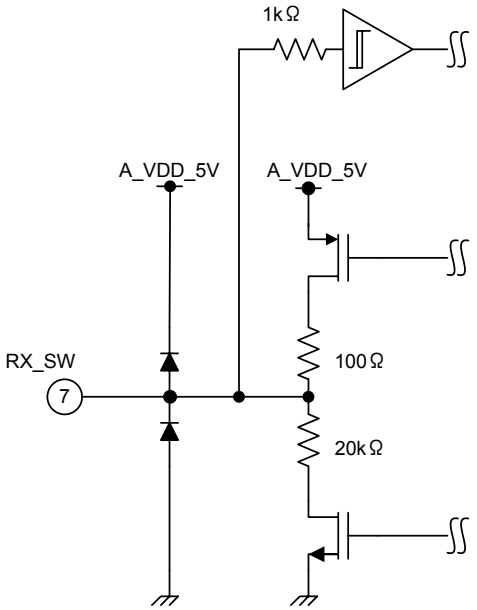
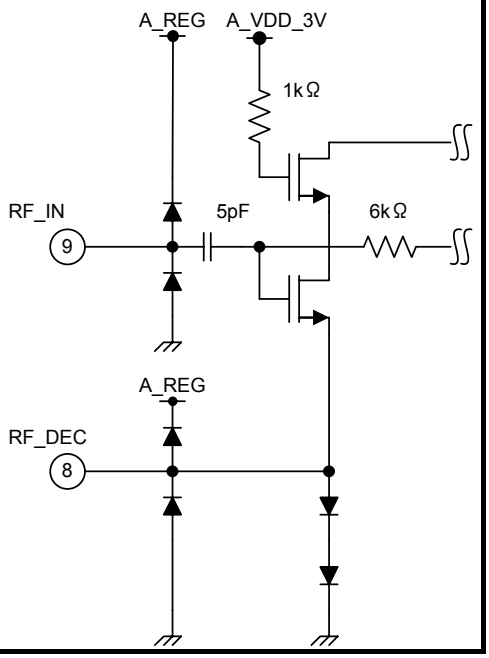
5. Pin Description

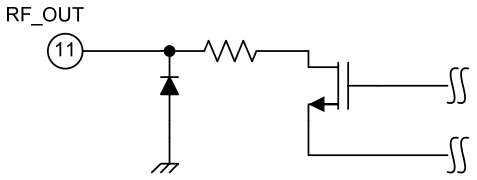
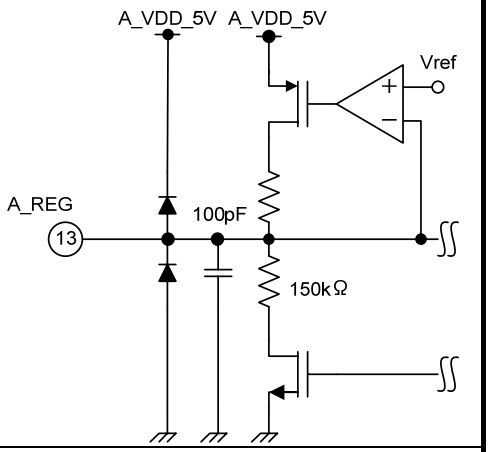
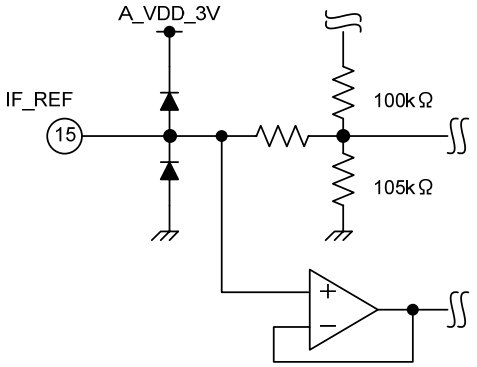
5.1 Equivalent Circuit and Function

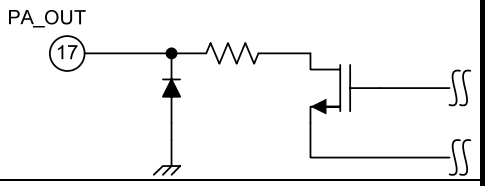
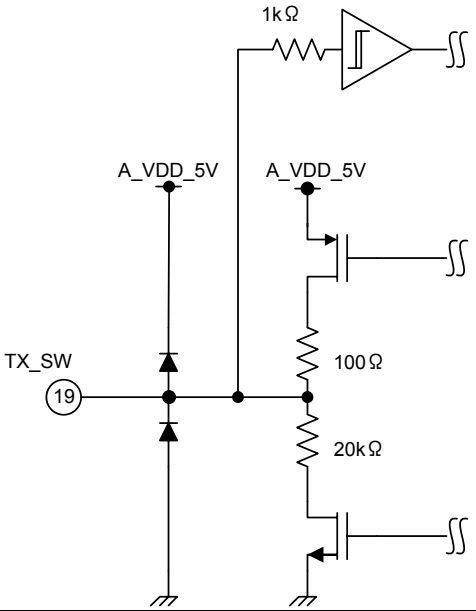
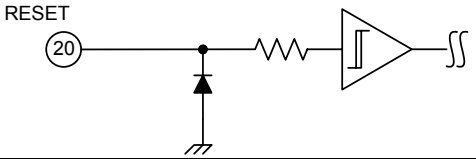
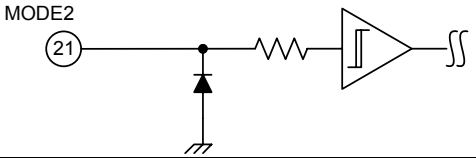
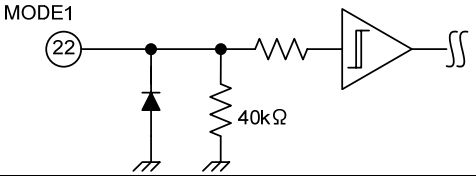
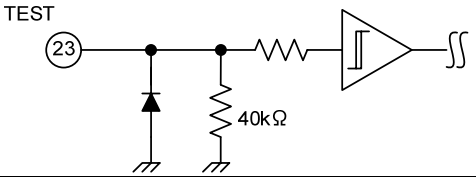
Table 5-1 Pin Description

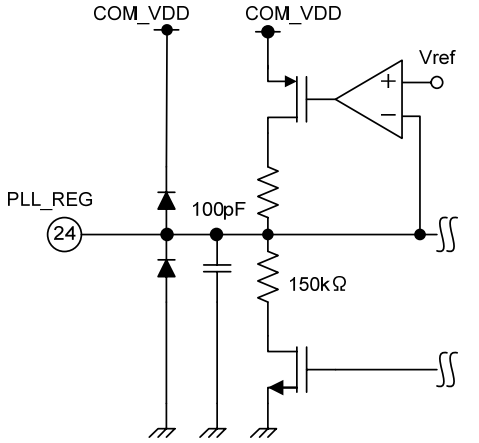
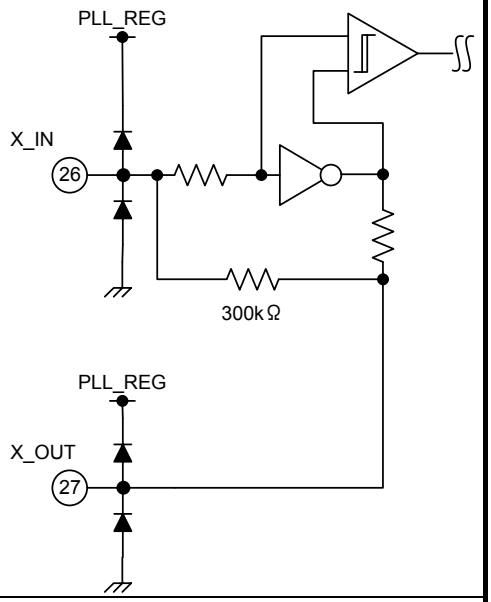
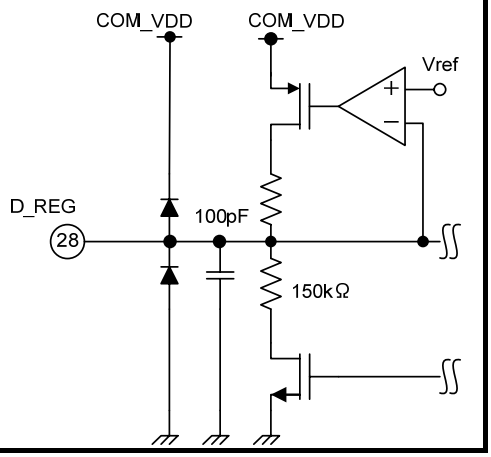
(All the values (resistance, capacity, etc.) shown in the internal equivalent circuit diagram are typical values.)

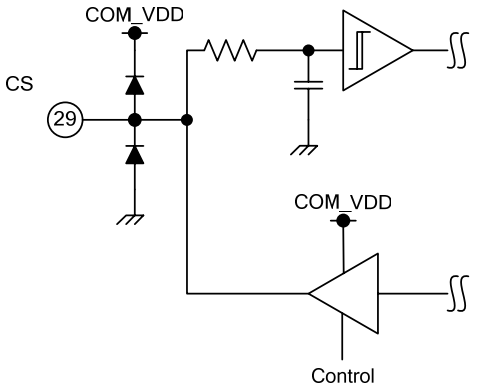
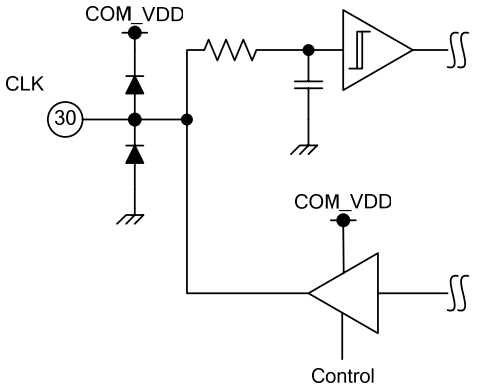
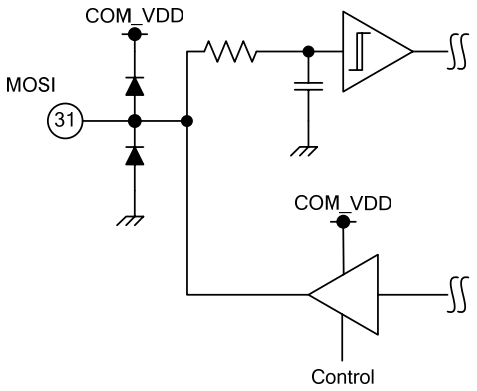
Pin No.	Pin Name	I/O	Description	Internal Equivalent Circuit
1	DET_TMONI2	Output	**Monitor 2** Monitoring internal signals (digital), use for system control At no use, open this pin.	
2	DET_TMONI3	Output	**Monitor 3** Monitoring internal signals (Converted to analog / in User Test) At no use, open this pin. Notice: In User Test, Supply at least 3 V to COM_VDD pin to monitor the signal. Lower voltage supply causes an incorrect monitoring.	
3	ENB	Input	**Enable Pin** Select to enable (In SPI Mode) **Address Setting (In EEPROM Mode)** Set a start address to read memory data. Notice: Do not supply higher voltage than the source in the absence of power supply. That may cause overcurrent.	
4	DET_TMONI4	Output	**Monitor 4** Monitoring internal signals (Converted to analog / in User Test) At no use, open this pin. Notice: In User Test, Supply at least 3 V to COM_VDD pin to monitor the signal. Lower voltage supply causes an incorrect monitoring.	
5	3V/5V	Input	**Supply Voltage Selector** Select supply voltage. Connect power supply for 5V use. / Ground for 3V use. Notice: Do not supply higher voltage than the source in the absence of power supply. That may cause overcurrent.	

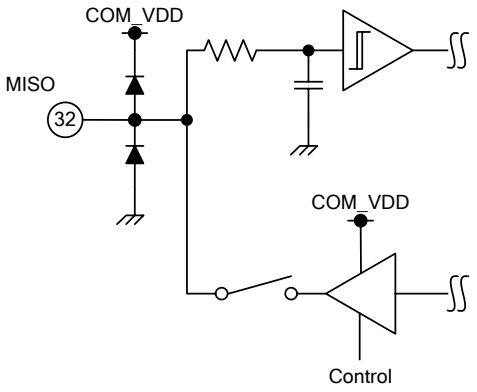
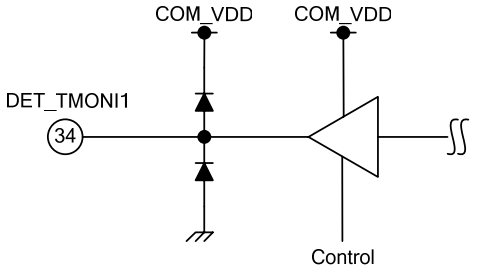
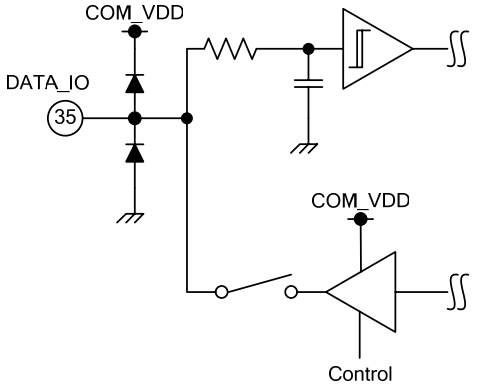
Pin No.	Pin Name	I/O	Description	Internal Equivalent Circuit
6	RSSI_OUT	Output	**RSSI Output** Output RSSI (= Received Signal Strength Indication) voltage. Connect ground via a capacitor. This IC has another RSSI signal for digital processing. At no use, connect ground via a capacitor.	
7	RX_SW	Output	**Antenna Switch Control for RX (In SPI Mode)** At no use, open this pin.	
		Input	**Address Setting (In EEPROM Mode)** Set a start address to read memory data. Notice: Do not supply higher voltage than the source in the absence of power supply. That may cause overcurrent.	
8	RF_DEC	-	**RF Decoupling Pin** Connect a decoupling capacitor. At no use, open this pin.	
9	RF_IN	Input	**RF Input Pin** Do not connect DC voltage. At no use, open this pin.	

Pin No.	Pin Name	I/O	Description	Internal Equivalent Circuit
10	A_VDD_5V	-	**Analog 5V Supply** Supply to mainly analog block. - For 5V use, supply 5V (typ.). - For 3V use, connect A_VDD_3V pin and supply 3V (typ.).	-
11	RF_OUT	Output	**RF Output pin** RF signal output from LNA block, Open drain output. Connect A_VDD_3V pin via a matching circuit. At no use, open this pin.	
12	A_VDD_3V	-	**Analog 3V Supply** - For 3V use, supply 3V (typ.). - For 5V use, voltage regulator output. Connect a bypass capacitor. Do not apply current or voltage on this pin from outside. And do not supply to external circuits except PA_OUT and RF_OUT pin.	-
13	A_REG	Output	**Regulator Output for Analog Block** Supply to mainly analog block. Connect a bypass capacitor. Do not apply current or voltage on this pin from outside. And do not supply to external circuits.	
14	A_GND	-	**Ground (Analog)**	-
15	IF_REF	-	**IF Reference** Connect ground via a capacitor. At no use, open this pin.	
16	PA_GND1	-	**Power Amplifier Ground 1** At no use of PA, connect ground.	-

Pin No.	Pin Name	I/O	Description	Internal Equivalent Circuit
17	PA_OUT	Output	**Power Amplifier Output Stage** Open drain output. Connect A_VDD_3V pin via a matching circuit. At no use, open this pin.	
18	PA_GND2	-	**Power Amplifier Ground 2** At no use of PA, connect ground.	-
19	TX_SW	Output	**Antenna Switch Control for TX (In SPI Mode)** At no use, open this pin.	
		Input	**Address Setting (In EEPROM Mode)** Set a start address to read memory data. Notice: Do not supply higher voltage than the source in the absence of power supply. That may cause overcurrent.	
20	RESET	Input	**Reset** Initialize TC32306FTG.	
21	MODE2	Input	**Mode Control** Select SPI Mode, SPI User Test Mode, EEPROM Mode, EEPROM User Test Mode.	
22	MODE1	Input	**Mode Control** Select SPI Mode, SPI User Test Mode, EEPROM Mode, EEPROM User Test Mode.	
23	TEST	Input	**TEST** Only use for Toshiba test. Connect ground.	

Pin No.	Pin Name	I/O	Description	Internal Equivalent Circuit
24	PLL_REG	Output	**Regulator Output for PLL** Supply to mainly PLL block. Connect a bypass capacitor. Do not supply voltage, and do not supply to an external circuit.	
25	PLL_GND	-	**Ground(Digital)**	-
26	X_IN	Input	**Reference Clock Input** Connect crystal oscillator or external signal generator. Do not apply a DC bias voltage.	
27	X_OUT	Output	**Reference Clock Output** Open this pin except a crystal oscillator use. Do not apply current or voltage on this pin from outside. And do not supply the clock signal to external circuits.	
28	D_REG	Output	**Regulator Output for Digital Block** Supply to mainly digital block. Connect a bypass capacitor. Do not apply current or voltage on this pin from outside. And do not supply to external circuits.	

Pin No.	Pin Name	I/O	Description	Internal Equivalent Circuit
29	CS	Input	**Chip Select Input** In SPI Mode / SPI User Test Mode / EEPROM User Test Mode. Notice: Do not supply higher voltage than the source in the absence of power supply. That may cause overcurrent.	
		Output	**Chip Select Output** In EEPROM Mode.	
30	CLK	Input	**SPI Clock Input** In SPI Mode / SPI User Test Mode / EEPROM User Test Mode. Notice: Do not supply higher voltage than the source in the absence of power supply. That may cause overcurrent.	
		Output	**SPI Clock Output** In EEPROM Mode.	
31	MOSI	Input	**Serial Data Input** In SPI Mode / SPI User Test Mode / EEPROM User Test Mode. Notice: Do not supply higher voltage than the source in the absence of power supply. That may cause overcurrent.	
		Output	**Serial Data Output** In EEPROM Mode.	

Pin No.	Pin Name	I/O	Description	Internal Equivalent Circuit
32	MISO	Output	**Serial Data Output** In SPI Mode / SPI User Test Mode / EEPROM User Test Mode. Notice: Do not supply higher voltage than the source in the absence of power supply. That may cause overcurrent.	
		Input	**Serial Data Input** In EEPROM Mode.	
33	COM_VDD	-	**Common Voltage Supply** Use for 3V and 5V. Supply to mainly control block.	-
34	DET_TMONI1	Output	**Monitor 1** Monitoring internal signals (Digital), use for system control. At no use, open this pin.	
35	DATA_IO	Output	**Data Output** Demodulated signal output at RF-Receiving. Behavior of this pin is different for each state of TC32306FTG reset. See Table 5-2.	
		Input	**Data Input** Signal input for modulation at RF-Transmitting. Behavior of this pin is different for each state of TC32306FTG reset. See Table 5-2. Notice: Do not supply higher voltage than the source in the absence of power supply. That may cause overcurrent.	
36	IO_GND	-	**Ground(I/O Block)**	-

The equivalent circuit diagram for the pin periphery is intended to aid in understanding the connected external circuit design, not to precisely describe the internal circuit.

5.2 Pin Behaviors at Reset and Register Initialized

Several pin behaviors of TC32306FTG depend on setting of Reset, register's initial value, or SPI Mode / EEPROM Mode (including User Test). See Table 5-2

Table 5-2 Pin Behaviors at Reset and Register Initialized

Pin	SPI Mode (TC32306FTG is slave.) (Including SPI User Test Mode)		EEPROM Mode (TC32306FTG is master.)		EEPROM User Test Mode (TC32306FTG is slave.)	
	RESET = "L"	Register's Initial (Battery Saving)	RESET = "L"	Battery Saving	RESET = "L"	Register's Initial (Battery Saving)
MODE2	IN	IN	IN	IN	IN	IN
MODE1	IN	IN	IN	IN	IN	IN
CS	IN	IN	High Output	High Output	IN	IN
CLK	IN	IN	Low Output	Low Output	IN	IN
MOSI	IN	IN	Low Output	Low Output	IN	IN
MISO	Z	Z	Z	Z	Z	Z
ENB	IN	IN	IN	IN	IN	IN
TX_SW	Pull Down	Pull Down	IN	IN	IN	IN
RX_SW	Pull Down	Pull Down	IN	IN	IN	IN
DATA_IO	Z	Low Output	Z	Low Output	Z	Low Output
DET_TMONI1,2	Low Output	Low Output	Low Output	Low Output	Low Output	Low Output
DET_TMONI3,4	Z	Z	Z	Z	Z	Z

Z: High Impedance

Notice: In SPI Mode, TC32306FTG accepts the input of SPI settings at RESET = "L", but will not act.

In Battery Saving Status, DATA_IO pin behavior changes to the value of register:h'0A[D5]RX_TX. Initial value of register:h'0A[D5]RX_TX is "0".

Table 5-3 DATA_IO Pin Behavior in Battery Saving

Pin	h'0A[D5]RX_TX = "0" (RX: Initial)	h'0A[D5]RX_TX = "1" (TX)
DATA_IO	Low Output	Z

Z: High Impedance

In Battery Saving Status, MISO pin changes its behavior at SPI Read when TC32306FTG is slave.

Table 5-4 MISO Pin Behavior in Battery Saving (TC32306FTG is slave.)

Pin	At SPI Read	Except SPI Read
MISO	OUT	Z

Z: High Impedance

6. Functional Description

6.1 Voltage Supply Settings

The voltage supply of TC32306FTG is selectable either 3V or 5V. The supply voltage is selected by setting of 3V/5V pin, and it decides pin connections. At 5V use, connect 3V/5V pin to a voltage supply, then the internal voltage regulator (A_REG30; for analog 3V) outputs the internal 3V (typ.) supply to A_VDD_3V pin.

Table 6-1 Voltage Supply Pins Connection

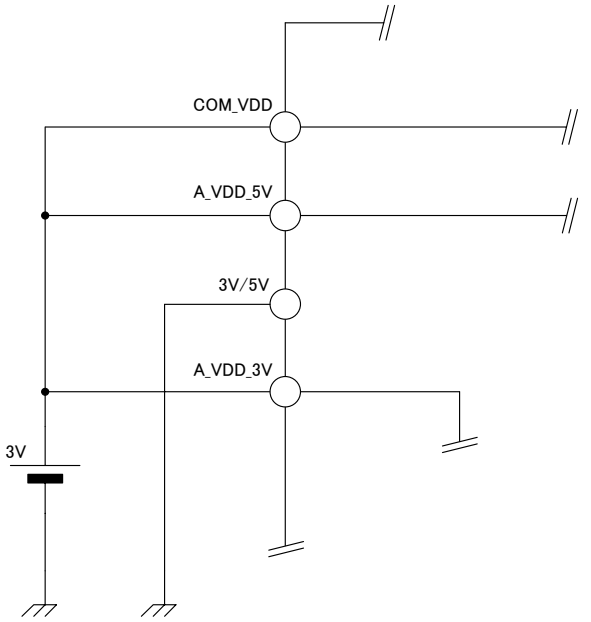
Pin Name	3V Use	5V Use
3V/5V (Behavior of A_REG30 Regulator)	GND (Disable)	5V Supply Input (Enable)
A_VDD_3V	3V Supply Input	Output of A_REG30 Regulator (Do not supply to external circuits.)
A_VDD_5V	3V Supply Input	5V Supply Input
COM_VDD	3V Supply Input	5V Supply Input

6.1.1 3V Use

At 3V use, connect 3V/5V pin to ground. Connect COM_VDD pin, A_VDD_3V pin and A_VDD_5V pin to a stable 3V supply.

Notice:

- Must not operate A_REG30 regulator for 5V use.
- Must not connect COM_VDD pin to voltage supply out of range of $V_{DD(3V)}$ shown as Table 8-1.



(This figure is conceptual. Select bypass capacitors in application circuits.)

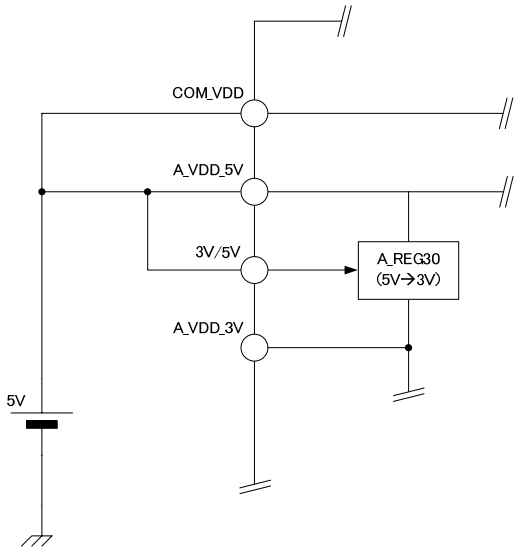
Fig 6-1 Example of Voltage Supply Connection at 3V Use

6.1.2 5V Use

At 3V use, connect 3V/5V pin to the 5V supply. Connect A_VDD_5V pin and COM_VDD pin to a stable 5V supply.

Notice:

- Must not connect A_VDD_3V pin to outside voltage supply.
- Must not connect COM_VDD pin to voltage supply out of range of $V_{DD(5V)}$ shown as Table 8-1.
- Must use a voltage supply from A_VDD_3V pin (output of A_REG30 regulator), for LNA or the matching circuit of PA.



(This figure is conceptual. Select bypass capacitors in application circuits.)

Fig 6-2 Example of Voltage Supply Connection at 5V Use

6.1.3 Supply / Ground Connections

In TC32306FTG supply / ground connections are separated for each functional block. At 5V use, some of analog functional blocks are connected internal 3V regulator (A_REG30 regulator). At 3V use, some of analog functional blocks are connected directly 3V supply, by connecting A_VDD_3V / A_VDD_5V pin.

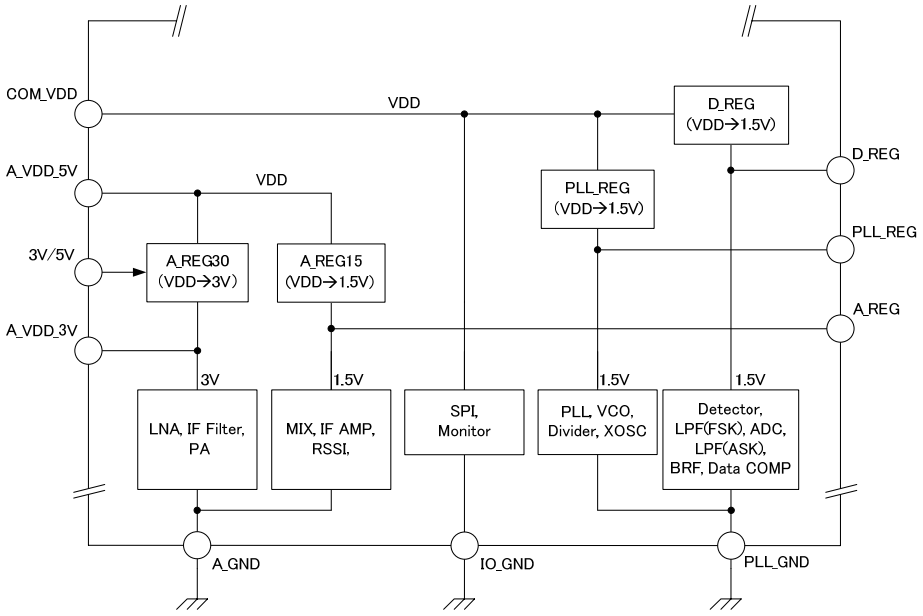


Fig 6-3 Conceptual Supply / Ground Connection to Functional Blocks

(This figure shows main supply / ground lines of functional blocks.)

6.2 Control Mode Settings

TC32306FTG has two control modes, SPI (Serial Peripheral Interface) Mode and EEPROM Mode. The control mode settings are selected by MODE2 pin and User Test Mode in each Control Mode is selected by MODE1 pin.

Table 6-2 Mode of Control

MODE2 Pin	MODE1 Pin	Control Mode Setting
L	L	SPI Mode
L	H	SPI User Test Mode
H	L	EEPROM Mode
H	H	EEPROM User Test Mode

SPI Mode and EEPROM Mode have a difference about an external connection, pin functions and control signal flows. Do not change the control settings in the market products.

Table 6-3 Role of Pin and Control Setting

Control Setting	CS Pin	CLK Pin	MOSI Pin	MISO Pin	ENB Pin	TX_SW Pin	RX_SW Pin
SPI Mode	"Input" This IC is slave by MCU control.			"Output" This IC is slave by MCU control.	"Input" For TC32306FTG status control.	"Output" For antenna switches control.	
SPI User Test Mode							
EEPROM Mode	"Output" This IC is master to control EEPROM.			"Input" This IC is master to read EEPROM data.	"Input" MCU controls EEPROM configuration data area.		
EEPROM User Test Mode	"Input" This IC is slave by MCU control.			"Output Signal" This IC is slave by MCU control.			

6.2.1 SPI Mode Setting and Connection

MCU and TC32306FTG are connected by SPI lines and MCU controls this IC.

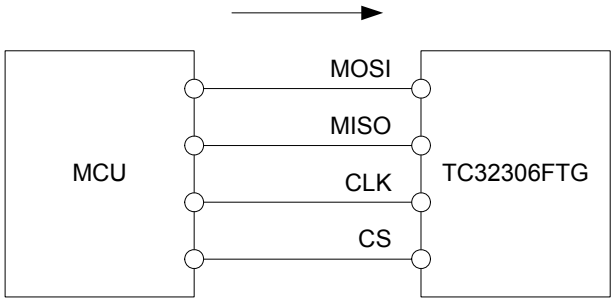


Fig 6-4 Conceptual Connection MCU and TC32306FTG

6.2.2 EEPROM Mode Setting and Connection

EEPROM and MCU, connect via TC32306FTG. This IC is controlled by the register data of EEPROM. Select up to 8 configuration data that are made as registers' modules from "h'0A" to "h'1C", depending on the size of EEPROM. In this mode, use of pins and external connections are different from those of SPI Mode. For example, TX_SW / RX_SW / ENB pin are used to select configuration data of EEPROM.

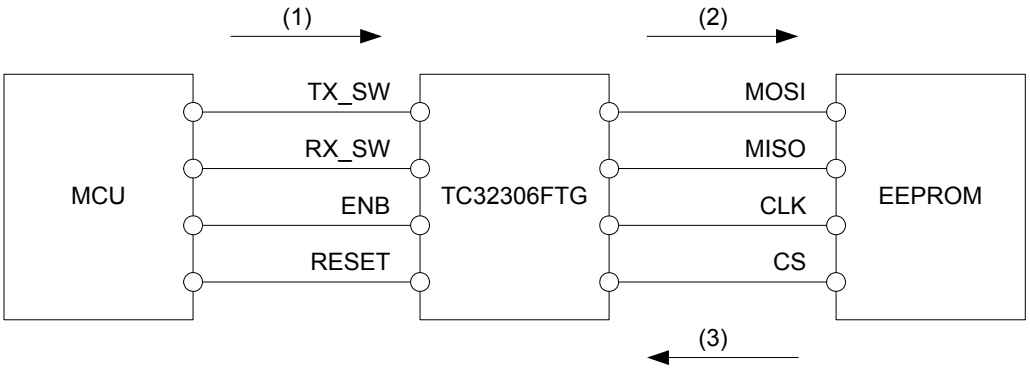


Fig 6-5 Conceptual Connection MCU, EEPROM and TC32306FTG

- In advance, write registers' values to each configuration data area of EEPROM.
- MCU commands this IC for selecting configuration data area of EEPROM. (1)
- This IC read a configuration data from EEPROM by SPI lines at the rising edge of RESET pin signal. (2)
- This IC is operated depending on EEPROM data. (3)

6.3 Universal Functions and Settings

6.3.1 Reset Status

This status initializes the internal condition (such as the register value) of TC32306FTG. For this IC Reset, input "L" signal to RESET pin surely during stable voltage supply. Also releasing Reset of this IC should be operated during stable voltage supply.

Table 6-4 RESET Pin Control

RESET Pin	IC Status
L	Initialize registers and I/O behaviors. Because I/O will be initialized, TC32306FTG does not accept all the settings except some settings. * About I/O behaviors at Reset status, see Table 5-2.
H	Battery Saving / Standby / Run by this IC settings.

* In EEPROM Mode, ENB pin / TX_SW pin / RX_SW pin are available.

Notice:

- Must be reset after voltage supply.
- The value of registers is initialized immediately after reset is released.
- In SPI Mode, TC32306FTG stays Battery Saving from Reset to register setting input, which moves to Run after reset will be released.
- In EEPROM Mode, the internal oscillator circuit for reading EEPROM will start after the reset is released.
- See Table 5-2 of I/O behavior at the register initialized.

- Software Reset

Software Reset will start after write "b'01010101" to register: h'09[D7:D0]RESET7..0. TC32306FTG will be reset as soon as the writing of Software Reset. Then the reset is released by next rising edge of CLK Signal or CS Signal, whichever is earlier. This IC will stay Battery Saving Status till the next Run / Standby command writing.

Table 6-5 Software Reset Command

Software Reset Command
h'09[D7:D0]RESET7..0 = b'01010101

Notice:

- Not available in EEPROM Mode (Except EEPROM User Test Mode)
- At Software Reset, only the register will be reset.
- TC32306FTG will always output "b'00000000" to read the register: h'09[D7:D0]RESET7..0.

6.3.2 Status Control

After reset is released, TC32306FTG has three status, Battery Saving / Standby / Run, then those status are controlled by two registers"h'0A[D7] / h'0A[D6]". In SPI Mode, also use ENB pin.

Table 6-6 IC Status in SPI Mode

MODE2 Pin	ENB Pin	h'0A[D7]ENB	h'0A[D6]ACT	Status	Description
L	L	X	X	Battery Saving	The lowest current consumption status. TC32306FTG only can accept control data (register settings), and stop any other functions. The transition from this status to Run will spend longer time than Standby
L	H	0	X		
L	H	1	0	Standby	This IC can move from this status to Run quickly. This IC can accept control data and operate clock and regulators, and consume more current than Battery Saving status.
L	H	1	1	Run	This IC can operate TX and RX. This IC current consumption and status transition time depend on the behaviors.

X: Don't care

In SPI Mode, MODE 1 pin is unrelated to the status control of TC32306FTG. Moving to Battery Saving Status by AutoOff function, registers"h'0A[D7] ENB, h'0A[D6] ACT" keep the value "1".

Table 6-7 IC Status in EEPROM Mode

MODE2 Pin	h'0A[D7]ENB	h'0A[D6]ACT	Status	Description
H	0	X	Battery Saving	The lowest current consumption status. TC32306FTG only can accept control data (register settings), and stop any other functions. The transition from this status to Run will spend longer time than Standby
H	1	0	Standby	This IC can move from this status to Run quickly. This IC can accept control data and operate clock and regulators, and consume more current than Battery Saving status.
H	1	1	Run	This IC can operate TX and RX. This IC current consumption and status transition time depend on the behaviors.

X: Don't care

In EEPROM Mode, MODE1 pin "H" leads EEPROM User Test Mode. This pin setting causes to stop the control from EEPROM. (TC32306FTG is slave.) In EEPROM Mode and EEPROM User Test Mode, ENB pin sets EEPROM address of configuration data and is unrelated to the status control of TC32306FTG. Moving to Battery Saving Status by AutoOff function, registers"h'0A[D7] ENB, h'0A[D6] ACT" keep the value "1".

6.3.3 Output Drive Settings

Select output drive setting at DATA_IO pin / MISO pin / DET_TMONI1 pin / DET_TMONI2 pin by setting registers"h'0D[D3]DATA_IO_D, h'0D[D2]MISO_D, h'0D[D1]TMONI_D". The settings become valid when reset is released (RESET = "H").

Table 6-8 Output Drive Settings

h'0D[D3]DATA_IO_D	DATA_IO pin drive setting
h'0D[D2]MISO_D	MISO pin drive setting
h'0D[D1]TMONI_D	DET_TMONI1, DET_TMONI2 pin drive setting
0	Low drive setting
1	High drive setting

X: Don't care

6.3.4 Antenna Switch Control

It is a function to control external antenna switch. Set registers"h'0A[D3]TX_SW, h'0A[D2]RX_SW", and TC32306FTG outputs control signals from TX_SW / RX_SW pin. The controls become valid at Run

and Standby Status. These pins cannot be available in EEPROM Mode and EEPROM User Test Mode as using for input pins.

Table 6-9 Antenna Switch Control Settings

MODE2 Pin	RESET Pin	Status	h'0A[D3]TX_SW h'0A[D2]RX_SW	TX_SW Pin RX_SW Pin
L	H	Buttery Saving	X	L
L	H	Run / Standby	0	L
L	H	Run / Standby	1	H
H	X	X	X	Input pin

X: Don't care

Notice: These pins condition "L" is pulled down through a resistor, and those pin conditions cause to stop driving external circuits.

6.3.5 Monitoring Control

Set registers"h'14[D6:D4], h'14[D2:D0]" and TC32306FTG outputs monitoring signals from DET_TMONI1 pin / DET_TMONI2 pin. The controls become valid at Run or Standby Status.

Table 6-10 Monitoring Signals

Status	h'14[D6] MONI1_SEL2 h'14[D2] MONI2_SEL2	h'14[D5] MONI1_SEL1 h'14[D1] MONI2_SEL1	h'14[D4] MONI1_SEL0 h'14[D0] MONI2_SEL0	DET_TMONI1 Pin Output Signal DET_TMON2 Pin Output Signal
Battery Saving	X	X	X	Low level output
Run / Standby	0	0	0	Low level output
Run / Standby	0	0	1	DET_out
Run / Standby	0	1	0	Preamble_DET_out
Run / Standby	0	1	1	RSSI_DET_out
Run / Standby	1	0	0	NDET_out
Run / Standby	1	0	1	Status_MONI
Run / Standby	1	1	0	Un_DET_out
Run / Standby	1	1	1	PLL_LD

X: Don't care

(1) DET_out Signal
TC32306FTG outputs the result of overall "Detection" judgment depending on RSSI detection , Noise detection and/or Preamble detection.
L : NOT determine "Signal Detection"
H : Determine "Signal Detection"

Set register:h'10[D2]DET_out_cnt_en="1", TC32306FTG holds DET_out output level "H" after first "Signal Detection".

Table 6-11 DET_out Signal Settings

h'10[D2] DET_out_cnt_en	DET_out Signal
0	Sequential updating
1	Hold output level "H" after first "Signal Detection"

Notice: To release DET_out signal output holding, move to Battery Saving / Standby Status.

(2) Preamble_DET_out Signal
TC32306FTG outputs the result of "Signal Detection" by Preamble Detector.
L : NOT determine "Signal Detection"
H : Determine "Signal Detection"

(3) RSSI_DET_out Signal
TC32306FTG outputs the result of "Singnal Detection" by RSSI Detector.
L : NOT determine "Signal Detection"
H : Determine "Signal Detection"

(4) NDET_out Signal
TC32306FTG outputs the result of "Signal Detection" by Noise Detector.
L : NOT determine "Signal Detection"
H : Determine "Signal Detection"

(5) Status_MONI Signal
TC32306FTG outputs its status.
L level: Battery Saving
H level: Standby / Run

(6) Un_DET_out Signal
TC32306FTG outputs the result of overall "No Signal Detection" judgment depending on RSSI detection , Noise detection and Preamble detection.
L : NOT determine "No Signal Detection"
H : Determine "No Signal Detection"

(7) PLL_LD Signal
TC32306FTG outputs the result of PLL lock detection.
L : No PLL lock detection
H : PLL lock detection.

Table 6-12 Logic of DET_out, Un_DET_out Signal

Detection			
RSSI Detection Signal	Noise Detection Signal	Preamble Detection Signal	DET_out Signal
*	*	H	H
*	*	L	L
*	H	OFF	H
H	L/OFF	OFF	H
L/OFF	L/OFF	OFF	L

H: "Signal Detection" is determined.
L: TC32306FTG can not determine "Signal Detection".
OFF: Stopping signal detection
*: Don't Care

No Detection			
RSSI Detection Signal	Noise Detection Signal	Preamble Detection Signal	Un_DET_out Signal
*	*	H	H
H	H	L/OFF	H
L	H	L/OFF	L
OFF	H	L/OFF	H
*	L	L/OFF	L
H	OFF	L/OFF	H
L	OFF	L/OFF	L
OFF	OFF	L/OFF	L

H: "No Signal Detection" is determined.
L: TC32306FTG can not determine "No Signal Detection".
OFF: Stopping signal detection
*: Don't Care

6.4 Local Oscillator

6.4.1 Local Oscillation Abstracts

Table 6-13 Local Oscillation Abstracts

Item	Function
Reference Clock Frequency	30.32MHz (Fixed)
PLL	Fractional - N PLL
VCO Frequency	1732 - 1896MHz
Divider	1/6, 1/4, 1/2 (Setting three stages)
Local Frequency	315, 434, 868 / 915 MHz

6.4.2 Reference Clock

Prepare 30.32MHz reference clock for TC32306FTG. To use crystal oscillator, connect it between XIN pin and XOUT pin with load capacitors. This IC is designed and considered to connect a crystal oscillator with the load capacitance of 6pF.

To use an external signal generator, for example TCXO, connect it to XIN Pin via a coupling capacitor. Also Open XOUT Pin and keep input signal level range from 0.5 V to 1.5 V (Peak to peak). Don't supply reference clock signal to external circuit from XOUT pin.

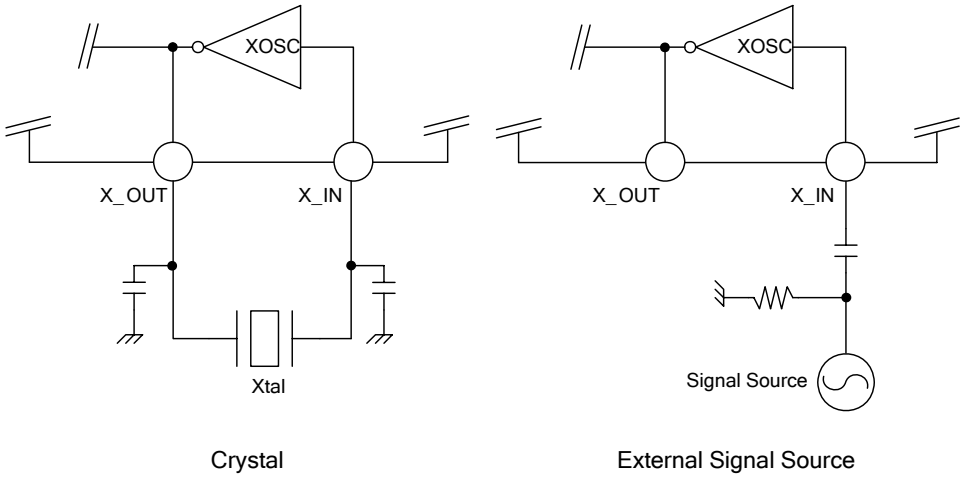


Fig 6-6 Case of Reference Clock Circuit

6.4.3 Local Oscillation

Local oscillator block is composed by the fractional-N PLL, VCO and frequency divider. Select the division ratio for expected frequency band. Set register:h'0A[D1:D0] and select the division ratio.

Table 6-14 RF Frequency & Division Ratio

h'0A[D1] BAND1	h'0A[D0] BAND0	RF Frequency Band	Division Ratio
0	0	315MHz	6
0	1	434MHz	4
1	X	868 / 915MHz	2

X: Don't care

Set the integer counter and fractional counter of registers"h'0B[D7:D0], h'0C[D7:D0]" to set Local frequency. When PLL is locked to the expected frequency, PLL_LD signal turns to be "H". To output PLL_LD signal from DET_TMONI1 pin and/or DET_TMONI2 pin, set registers"h'14[D6:D4], [D2:D0]".

(1) Local Oscillation Setting for RX

Set this Local Oscillator frequency at "Lowe Local".

”Receiving Local Frequency” = (”RF Recieving Frequency”–”IF Frequency”)×”Division Ratio”

Example 1
RF Frequency: 314.94MHz, IF Frequency: 280kHz, Division Ratio: 6 (Select 315MHz band)
”Receiving Local Frequency” = (314.94MHz - 0.28MHz)×6 = 1887.96MHz
Example 2
RF Frequency: 314.94MHz, IF Frequency: 230kHz, Division Ratio: 6 (Select 315MHz band)
”Receiving Local Frequency” = (314.94MHz - 0.23MHz)×6 = 1888.26MHz

(2) Local Oscillation Setting for TX

Set this Local Oscillator frequency equal as RF frequency to transmit.

”Transmitting Local Frequency” = ”RF Transmitting Frequency”×”Division Ratio”

Example
RF Frequency: 314.94MHz, Division Ratio: 6 (Select 315MHz band)
”Transmitting Local Frequency” = 314.94MHz×6 =1889.64MHz

6.5 RF Receiver

For RF-Receiving, set register:h'0A[D5] = "0".

6.5.1 RF-Receiving Abstract

Table 6-15 Receiving Function Abstracts

Item	Function	
RF-Receiving Frequency Band	315, 434, 868 / 915 MHz	
IF Frequency	IF = 230kHz, setting of IF Filter Bandwidth: wide = 320kHz(typ.) IF = 280kHz, setting of IF Filter Bandwidth: middle = 270kHz(typ.) Single conversion system (Using Image Cancel Mixer)	
Demodulation	FSK / ASK	
	FSK Demodulation	ASK Demodulation
IF Detection	Delay Detection, Pulse Count Detection	Envelope Detection
Signal Detection	RSSI Detection, Noise Detection, Preamble Detection	RSSI Detection, Preamble Detection
Additional Function	NIR (Near Interference Rejection) Filter	-
Bit Rate Filter Cutoff Frequency	0.436kHz -19.78kHz (12 steps)	

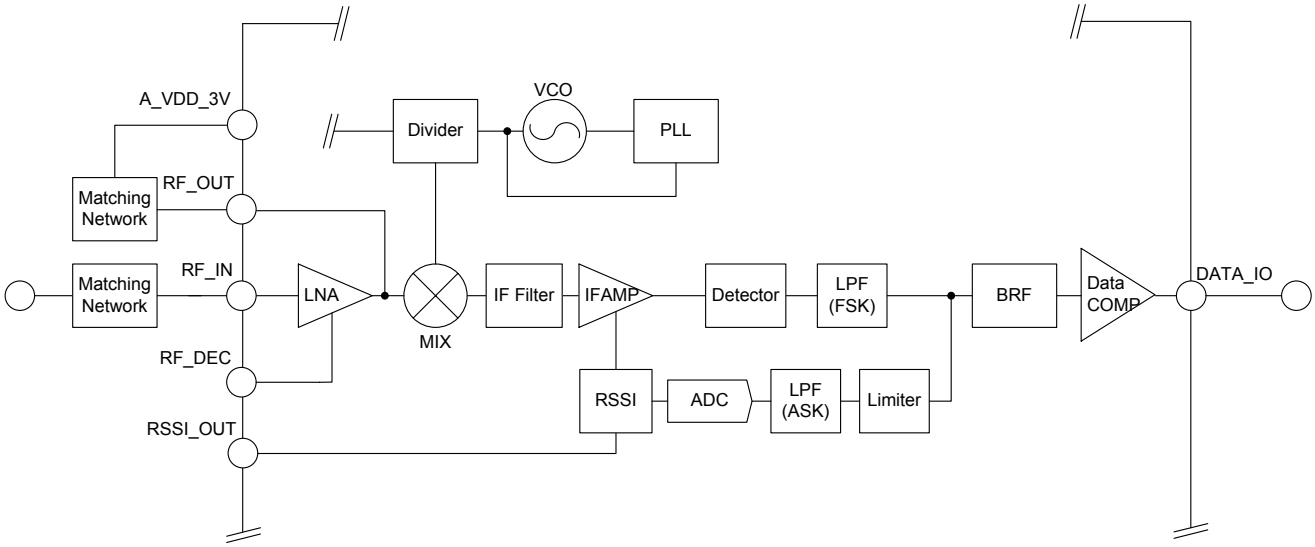


Fig 6-7 Receiver Block Diagram

6.5.2 Receiving Frequency Band

TC32306FTG is available following frequency bands, 315, 434, and 868/915 MHz.

6.5.3 Receiver Gain

Adjust overall gain of receiver block by matching network. The gain of LNA is controlled by the value of register: h'0E[D7:D6].

Table 6-16 LNA Gain Control

h'0E[D7] Lna_gain1	h'0E[D6] Lna_gain0	LNA Relative Gain (Reference value)
0	0	0 (Initial)
0	1	+0.8dB
1	0	+1.7dB
1	1	+2.5dB

Above are reference values at 315 MHz.

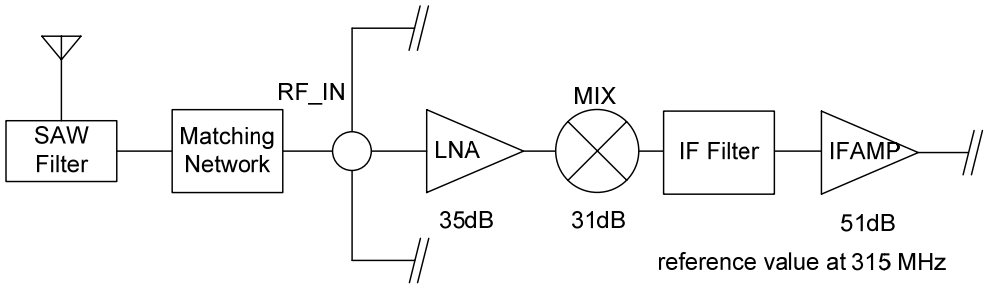


Fig 6-8 Receiver Gain Distribution

RF_IN pin is input of LNA. Input a RF signal via a suitable matching network. RF_OUT pin is output of LNA and open drain configuration. Supply voltage via a matching network. See the Evaluation Circuit for both input and output matching network. About RF_DEC pin, connect a capacitor (1000 pF (typ.)) and resister (100 Ω (typ.)), such as Fig 6-9 Typical LNA Network.

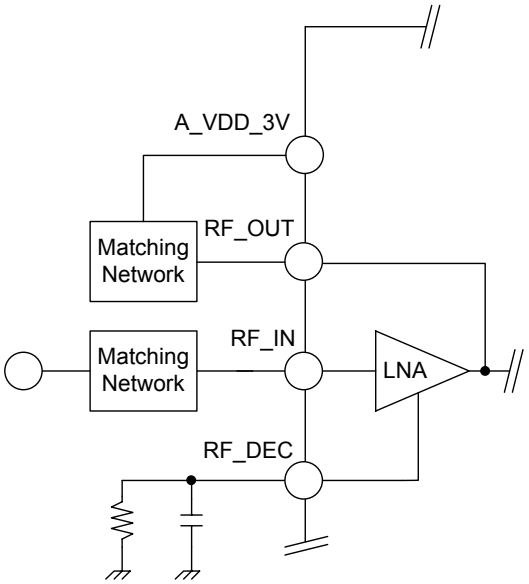


Fig 6-9 Typical LNA Network

6.5.4 IF Frequency

TC32306FTG has the single conversion system. The output of LNA is downconverted to IF frequency by Image Cancel Mixer. Select internal IF filter bandwidth (Middle: 280 kHz / Wide: 230 kHz) to consider that characteristics by the value of register:h'0E[D5].

Table 6-17 IF Frequency and Internal IF Filter Bandwidth

h'0E[D5] IFBW	IF Frequency (Selected)	Internal IF Filter Bandwidth (Selected)
0	230kHz	320 kHz (typ.)
1	280kHz	270 kHz (typ.)

6.5.5 Demodulation

Select a type of demodulation (ASK or FSK) by the value of register:h'0A[D4]. Depending upon a type of demodulation, IF filter output signal has different path, RF detection and additional functions.

Table 6-18 Demodulations

h'0A[D5]RX_TX	h'0A[D4]FSK_ASK	Status
0	0	FSK (RX)
0	1	ASK (RX)
1	XX	TX

XX: About TX, see Table 6-30.

6.5.6 FSK Demodulation

To select FSK, set register:h'0A[D4] to "0"(FSK).

(1) NIR (Near Interference Rejection) Filter

Select the filter Enable/Disable by the value of register:h'10[D1]. This filter reduces a interfere signal near +300 kHz offset frequency. This filter is a notch type and the peak attenuation is about 20 dB. The notch frequency is selectable by the value of register:h'1B[D2:D1].

Table 6-19 Settings of NIR Filter

h'10[D1]NIR_Fil_en	h'1B[D2]NIR_Frqth1	h'1B[D1]NIR_Frqth0	Filter Enable/Disable & Notch Frequency
0	X	X	Disable : -
1	0	0	Enable : 631 kHz
1	0	1	Enable : 659 kHz
1	1	0	Enable : 689 kHz
1	1	1	Enable : 712 kHz

X: Don't care

To use NIR filter (h'10[D1]NIR_Fil_en = "1"), Set following registers(h'0D[D0], h'0F[D0], h'12[D1:D0], h'13[D0], h'1A[D0], h'1B[D0], h'1C[D2:D0]) to those recommended value. (The values are not equal to initial values, so must change them.)

Table 6-20 Settings of NIR Filter (Recommended Values)

h'10[D1]NIR_Fil_en	Register Value			
0	No need to set			
1	h'0F[D0]NIR_L2	1	h'0D[D0]NIR_H2	0
	h'1C[D1]NIR_L1	1	h'13[D0]NIR_H1	0
	h'1C[D0]NIR_L0	0	h'1A[D0]NIR_H0	0
	h'1B[D0]NIR_2L1	1	h'12[D1]NIR_2H1	0
	h'1C[D2]NIR_2L0	0	h'12[D0]NIR_2H0	0

(2) IF Detector

Select a type of IF Detections (Delay Detection / Pulse Count Detection) by the value of register:h'10[D0]. Select either detector suitable to the application. Both Delay Detection and Pulse Count Detection can convert input signal frequency (0-500 kHz) to voltage output. In Pulse Count Detection, over 500 kHz input signal frequency is converted to the voltage output equal to 500 kHz. In Delay Detection, the characteristic of S curve is mirror inverted at 500 kHz signal input. Select the High Frequency Detector by the value of register:h'0F[D4] in Delay Detection, over 500 kHz input signal frequency is converted to the voltage output equal to 500 kHz.

Table 6-21 Settings of IF Detector / High Frequency Detector

h'10[D0]Sel_Det	h'0F[D4]Hdet_en	Status
0	0	Delay Detection: High Frequency Detector Disable
0	1	Delay Detection: High Frequency Detector Enable
1	X	Pulse Count Detection

X: Don't care

Notice:

- IF filter characteristics affects the maximum available signal frequency of High Frequency Detector.

- High Frequency Detector Auto Off

After DET_out Signal is H level in Signal Detection function, High Frequency Detector will be automatically turned off by the setting of register: h'1A[D1] = "1". That may reduce the influence on RF receiver sensitivity. When both Delay Detection and High Frequency Detector are enabled (h'10[D0]Sel_Det = "0" and h'0F[D4]Hdet_en = "1"), this function is valid. To use this function again after Auto Off, set status to Battery Saving / Standby or digital block being disabled. This setting will be valid immediately after the data input to register:h'1A.

(3) LPF for FSK

The cutoff frequency of LPF for FSK is about 20 kHz.

(4) Signal Detections

In FSK, TC32306FTG is available 3 types of Signal Detections, RSSI Detection / Noise Detection / Preamble Detection. These Signal Detections have various sensitivity and accuracy, so select Signal Detection suitable to the application. Each Signal Detection sets their Enable/Disable, detection interval, threshold level of detection and number times for judgment by register settings. These Signal Detections show signal situations as "Signal Detection" or "No Signal Detection" and these outputs depend on number of continuous times to be set in advance, which is above or below the threshold level.

Notice:
"Signal Detection" and "No Signal Detection" depend on TC32306FTG internal judgment. Those don't guarantee actual signal situations. It may be possible to be neither "Signal Detection" nor "No Signal Detection".

Table 6-22 Signal Detections in FSK

Item	RSSI Detection	Noise Detections	Preamble Detections
Method	Monitoring integrated signal level at IF AMP.	Monitoring noise level near 34 kHz in FSK demodulation signal.	Monitoring preamble signal at Data COMP. output (Data pattern:010101...), .
Signal Detection Enable / Disable	h'0F[D7]Drssi_en 0:Disable / 1:Enable	h'0F[D5]Ndet_en 0:Disable / 1:Enable	h'0F[D6]Preamble_en 0:Disable / 1:Enable
Detection Interval	h'1A[D7:D6]Ntime1..0 0.338 - 2.7ms (4steps) Cannot set RSSI detection and Noise detection independently.		h'1A[D2]Pre_DetTrig 0: signal period 1: signal bit
Detection Threshold Level	h'16[D7:D0]DRSSI_Th7..0 8bit(256steps)	h'19[D7:D2]Ndet_Th5..0 6bit(64steps)	Preamble detection Interval (512steps) h'18[D7]Pre_Time8/h'17[D7:D0]Pre_Time7..0 Preamble detection error margin(128steps) h'18[D6:D0]Err_Margin6..0
Detection Number of Times for judgment	h'1A[D5]DRSSI_judg 0: single detection 1: twice detection in succession	h'19[D1]Ndet_Judg 0: a single detection 1: twice detection in succession	h'1A[D4:D3]Pre_DetCount1..0 3-6 period / 6-12bit(4steps)
Signal Detection	above threshold. (RSSI_DET_out signal = "H")	below threshold. (NDET_out signal = "H")	Continuously within the error margin. (Preamble_DET_out signal = "H")
No Signal Detection	Below threshold level.	Above threshold level.	Continuously without the error margin.

- Each results of Signal Detection (RSSI_DET_out signal / NDET_out signal / Preamble_DET_out signal) can be monitored in User Test. Each results of "No Signal Detection" cannot be monitored directly.
- About each setting in detail see "Register Overview & Description".

TC32306FTG outputs DET_OUT signal (Judgment of "Signal Detection") and Un_DET_out signal (Judgment of "No Signal Detection") to DET_TMONI1 pin and DET_TMONI2 pin, as the result of 3 overall signal detection judgment.

A) Additional Note of noise addition for high frequency signal

Noise Detection monitors noise level near 34 kHz in FSK demodulation signal. Therefore, both "Signal Detection" and "No Signal Detection" in Noise Detection function may be false because of the noise reduction caused by high frequency signal. To avoid this, TC32306FTG has an additional function to improve detection accuracy.
This function improves detection accuracy to add a constant value to detected noise level when input signal is high frequency. Set register:h'19[D0]Add_Hdet_en = "1" and this is valid. This function operates independently following register settings, Noise Detection (h'0F[D5]]Ndet_en), IF Detection (h'10[D0]Sel_Det) and High Frequency Detector (h'0F[D4]Hdet_en).

Table 6-23 Settings of Noise Addition for High Frequency Signal

h'0F[D5] Ndet_en	h'19[D0] Add_Hdet_en	Function Status
0	0	Both Noise Detection and Noise Addtion for High Frequency Signal are not valid.
0	1	Noise Addtion for High Frequency Signal is valid. Noise Detection is not valid. "No Signal Detection" is operated, but "Signal Detection" is not operated.
1	0	Noise Detection is valid. Noise Addtion for High Frequency Signal is not valid.
1	1	Both Noise Detection and Noise Addtion for High Frequency Signal are valid.

Notice:

- In the settings of register: Ndet_en (f'0F[D5] = "0") and register: Add_Hdet_en (h'19[D0] = "1"), when High Frequency Signal is occupied in the half of RSSI / Noise detection interval set by register:[D7:D6]Ntime1..0, the register of Noise Signal Level Monitor (h'23[D7:D0]DNDET7..0) outputs "d'40". When High Frequency Signal is occupied in the full of RSSI / Noise detection interval, the register of Noise Signal Level Monitor (h'23[D7:D0]DNDET7..0) outputs "d'81".
- Noise Addition for High Frequency Signal can be valid in Pulse Count Detection and Delay Detection.
- Noise Addition for High Frequency Signal can be valid even if High Frequency Detector is not valid in Delay Detection.

B) Additional Note of Preamble Detection

The function of Preamble Detection checks signal by counting the number of clocks between the rising edges, or between the falling edge and the rising edge of output signal from Data COMP circuit. If the number of clocks is counted within the set value +/- error margin (h'18[D6:D0]), this signal is recognized as Preamble signal. The clock frequency is twice by the internal clock using in Bit Rate Filter. About internal clock frequency, see Table 6-25.

Notice:

- When the function of Preamble Detection checks signal by counting the number of clocks between the rising edges (h'1A[D2] = "0"), the number of count is as same as the setting value of register: Pre_Time8..0.
- When the function of Preamble Detection checks signal by counting the number of clocks between the rising edge and the falling edge (h'1A[D2] = "1"), the number of count is half of the setting value of register: Pre_Time8..0. If the value of register: Pre_Time8..0 is odd, half of this setting value is rounded down to the integer.
- Both signal counting the number of clocks between the rising edges (h'1A[D2] = "0") and between the rising edge and falling edge (h'1A[D2] = "1"), error margin is as same as the setting value of register: Err_Margin6..0.

Way of setting:

- Setting value: Pre_Time8..0(h'18[D7],h'17[D7:D0])
- Error margin: Err_Margin6..0(h'18[D6:D0])
- The number of clocks: Pre_Time8..0 = (2 x fbc)/fp
- fp: preamble signal cycle frequency
- fbc: internal clock frequency, fixed by Bit Rate Filter setting (h'0E[D4:D1]BRF_Bit3..0) See table 6-25.
- Error margin is as same as the setting value of register: Err_Margin6..0.

- Calculation example

fp = 600Hz

fbc = 23.69kHz (Set the cutoff frequency of Bit Rate Filter as 619Hz)

Pre_Time8..0 = (2 x 23.69) / 0.6 = 78.9 → 79(h'18[D7], h'17[D7:D0] = b'001001111)

If the number of clocks is within "79±Err_Margin6..0". RF receiving signal will be recognized as Preamble signal.

6.5.7 ASK Demodulation

To select ASK, set register:h'0A[D4] to "1"(ASK).

(1) RSSI
Detect the level of IF signal.

(2) AD converter (ADC)
Digitize the level of IF signal detected by RSSI.

(3) LFP (ASK)
The cutoff frequency of LPF (fc) is about 40 kHz.

(4) Limiter (This is only valid to use the function of Data Comparator Quick Charge 2.)
This is only valid to use the function of Data Comparator Quick Charge 2 in the subsequent Data Comparator circuit. RSSI signal voltage through LPF is kept over the internal setting value in Limiter circuit. Limit level is calculated with the peak voltage in the sequential. The peak voltage is detected in Peak Hold Circuit in the subsequent of Bit Rate Filter.

- Peak Hold Circuit
Peak Hold Circuit outputs peak voltage to track its input (Bit Rate Filter output) with time constant that is fast at the rising of the input signal and that is slow at the falling of the input signal. The time constants are tp' / fbc at charging and tr / fbc at discharging.
* fbc: internal clock frequency set by Bit Rate Filter, register:h'0E [D4:D1]BRF_Bit3..0
* tp': inverse number of 1/tp + 1/tr
* tp: peak hold voltage charge coefficient, register:h'1C [D4:D3] Peak_Charge1..0
* tr: peak hold voltage discharge coefficient, register:h'1C [D7:D5] Peak_Ref2..0
When TC32306FTG starts to Run status, Peak Hold Circuit output voltage will reach 90% of the peak voltage during "tp' / fbc x 2.30[s]".

Table 6-24 Setting of Peak Hold Circuit

Input Signal of Peak Hold Circuit	Status	Register to set time constant
During the signal rising	Viph – voph ≥ 0	h'1C[D4:D3]Peak_Charge1..0 h'1C[D7:D5]Peak_Ref2..0
During the signal falling	Viph – ph < 0	h'1C[D7:D5]Peak_Ref2..0

Viph: Input voltage of Peak Hold Circuit
Voph: Output voltage of Peak Hold Circuit

Notice:
- Must not set the value of tp (set by register:h'1C [D4:D3] Peak_Charge1..0) smaller than the value of Quick Charge Coefficient (set by register:h'1B[D7:D6]Charge2_Ref1..0).
- Set the value of tp (set by register:h'1C [D4:D3] Peak_Charge1..0) much smaller than the value of tr (set by register:h'1C[D7:D5]Peak_Ref2..0).
- The peak hold level can be monitored at the register:h'1F[D7:D0]PEAK7..0.
- Limiter will be bypassed when Data Comparator Quick Charge 2 is not used.

(5) Signal Detection
In ASK, TC32306FTG is available 2 types of detections, RSSI Detection / Preamble Detection. Those detections are as same as that in FSK. Noise Detection cannot be available in ASK.

6.5.8 Bit Rate Filter

The cutoff frequency of Bit Rate Filter can be available in 12 steps between 0.436 kHz and 19.78 kHz by the setting of register:h'0E[D4:D1]. Select and set suitable cutoff frequency regarding demodulated signal data rate. There are different characteristic of LPF in ASK or FSK. Set the cutoff frequency with considering them.
The cutoff frequency is only for Bit Rate Filter. Set it to consider the influence of LPF (FSK: fc = 20kHz, ASK: fc = 40 kHz) of the previous circuit.

Table 6-25 Settings of Bit Rate Filter and Cutoff Frequency including LPF

h'0E[D4] BRF_Bit3	h'0E[D3] BRF_Bit2	h'0E[D2] BRF_Bit1	h'0E[D1] BRF_Bit0	Cutoff Frequency (fc)	Cutoff Frequency including the previous LPF		Internal Clock (fbc)
					FSK	ASK	
0	0	0	0	19.8 kHz	14.1 kHz	17.8 kHz	758 kHz
0	0	0	1	14.0 kHz	11.5 kHz	13.2 kHz	758 kHz
0	0	1	0	9.90 kHz	8.91 kHz	9.62 kHz	379 kHz
0	0	1	1	6.98 kHz	6.60 kHz	6.88 kHz	379 kHz
0	1	0	0	4.95 kHz	4.81 kHz	4.91 kHz	189.5 kHz
0	1	0	1	3.49 kHz	3.44 kHz	3.47 kHz	189.5 kHz
0	1	1	0	2.48 kHz	2.46 kHz	2.47 kHz	94.75 kHz
0	1	1	1	1.74 kHz	1.74 kHz	1.74 kHz	94.75 kHz
1	0	0	0	1.24 kHz	1.24 kHz	1.24 kHz	47.38 kHz
1	0	0	1	0.872 kHz	0.872 kHz	0.872 kHz	47.38 kHz
1	0	1	0	0.619 kHz	0.619 kHz	0.619 kHz	23.69 kHz
1	0	1	1	0.436 kHz	0.436 kHz	0.436 kHz	23.69 kHz
1	1	0	0	19.8 kHz	14.1 kHz	17.8 kHz	758 kHz
1	1	0	1	14.0 kHz	11.5 kHz	13.2 kHz	758 kHz
1	1	1	0	19.8 kHz	14.1 kHz	17.8 kHz	758 kHz
1	1	1	1	14.0 kHz	11.5 kHz	13.2 kHz	758 kHz

Notice:
The cutoff frequency and the Internal Clock of Bit Rate Filter are derived from 30.32MHz Reference Clock Frequency.

6.5.9 Data Comparator

Data Comparator shapes the waveform of the demodulated output signal of Bit Rate Filter, and outputs the result signal to DATA_IO pin. That demodulated signal is inverted from modulated signal.

(1) Reference Voltage

The reference voltage of Data Comparator (vref) is determined by the value tracking input voltage of Data Comparator (vi) with slow time constant. The time constant is nr / fbc, and nr is set by register:h'1B[D5:D3]Cmp_Ref2..0. Set it suitable with considering the signal data rate or coding.

Time constant = nr / fbc

* fbc: internal clock frequency set by Bit Rate Filter, register:h'0E [D4:D1]BRF_Bit3..0

The duty of Data Comparator output will be worse, due to the large fluctuation of vref caused by setting of unsuitable time constant or number of consecutive data with the same sign. Then suitable time constant can be simply calculated by the following equation.

In the equation, vdiff[%] is fluctuation of vref and t is a maximum number of consecutive data of the same sign minus 1.

- Way of Setting

Time constant = nr / fbc = t / -ln(1 – vdiff / 100)

- Calculation Example
Data Rate = 600 Hz
fbc = 23.69 kHz (Set the cutoff frequency of Bit Rate Filter as 619 Hz.)
fluctuation of vref = 10%
The number of consecutive data with the same sign: 4
t = (4-1) / (2 x 600) = 0.0025s
nr/fbc = 0.0025 / (-ln(1-10/100)) = 0.0237
nr = 0.0237 x 23690 = 561.45
Suitable setting value of register: h'1B [D5:D3] is b'100(nr=512). This value is the nearest of 561.45.

The average of vref can be monitored from register: h'21[D7:D0]Ref_bias7..0 and the fluctuation of vref can be monitored from register:h'20[D7:D0]Ref_diff7..0. Also vref can be monitored from DET_TMONI3 or 4 pin. Because the time constant set by Data Comparator Reference Voltage Charge Coefficient (h'1B[D5:D3]Cmp_Ref2..0) is slower than the signal data rate, the rising time of the signal will be taken long. Data Comparator output voltage will reach 90% of vref during "nr / fbc x 2.30". To shorten rising time of the signal, use the function of Data Comparator Quick Charge 1 or 2.

(2) Data Comparator Quick Charge 1 (During a certain period)

The function is able to shorten the start period of TC32306FTG because time constant of vref will change to 1/16 or 1/4 only during that period. During start period, the output signal duty will be worse than that during normal condition, but Data Comparator output is obtained faster than the condition without the function. After finishing the certain period, the output signal duty will be improved because the time constant becomes nr / fbc (Normal condition).

Table 6-26 Quick Charge 1

	Functional Period of Quick Charge 1		Normal
	The Fastest	Faster	
Time Constant	(nr / fbc) x 1/16	(nr / fbc) x 1/4	nr / fbc
Validity Period	(nr / 4) / fbc	(nr / 2) / fbc	—

The time constant is switched as the Fastest → Faster → Normal.

(3) Data Comparator Quick Charge 2 (Tracking to depend on the voltage difference)

When the difference between the reference voltage of Data Comparator (vref) and the input voltage of it is larger than preset voltage threshold level (vth), the vref will track the vi as following time constant.

When the difference between vref and vi is large such as in the start period, Data Comparator output is obtained faster than the condition with Quick Charge 1.

Time constant = nr' / fbc

Data Comparator output voltage will reach 90% of vref during "nr / fbc x 2.30[s]".

*nr' : inverse number of (1/nr + 1/nc)

*nr : Data Comparator Reference Voltage Charge Coefficient
(Set by register:h'1B[D5:D3]Cmp_Ref2..0.)

*nc : Quick Charge Coefficient (Set by register:h'1B[D7:D6]Charge2_Ref1..0.)

Table 6-27 Quick Charge 2

	Value of |vi – vref|	Time Constant
Functional Period of Quick Charge 2	|vi – vref| ≥ vth	nr' / fbc
Normal	|vi – vref| < vth	nr / fbc

The threshold level (vi – vref) is set according to FSK deviation. When the threshold level is same or smaller than that deviation, receiver sensitivity will be worse because of signal noises around the level of receiver sensitivity. When the threshold level is larger than that deviation, the rising time of signal

will be taken longer. Check signals in User Test to set the threshold level as suitable. The threshold level is set by register:h'11[D7:D0]Charge2_Th7..0.

- Calculation Example of the threshold level
The case to set register:h'11 [D7:D0]Charge2_Th7..0 = 61 (b'00111101)
61 / 1.53 = 39.9 → equivalent ±39.9kHz
1.53 is a constant.

(4) DATA_IO pin control

DATA_IO pin outputs the demodulated signal. DATA_IO pin output can be controlled by the result of Signal Detection by setting register: h'0F[D3].

Table 6-28 Data_IO Pin Control

h'0A[D5] RX_TX	h'0F[D3] Dataout_cnt_en	DET_out Signal	Pin Behavior
0	0	X	Output demodulated signal
0	1	L → H	Output demodulated signal
1	X	X	Input pin for TX

X: Don't care

Notice:

- The register: h'0F[D3]Dataout_cnt_en is valid in RX.
- When the register: h'0F[D3] = "1", TC32306FTG will output demodulated signal from the first rising edge of DET_out signal. Till the first rising edge of DET_out signal, this IC outputs "L".
- When the register:h'0F[D3] = "1" and DET_out signal changes from "L" to "H", this IC outputs demodulated signal in spite of the condition of DET_out signal till this IC will be Battery Saving or Standby mode.
- When the register:h'0F[D3] = "1" and non use of Signal Detections, this IC doesn't output demodulated signal. (Fixed "L" output.)

6.6 RF Transmitter

For RF-Transmitting, set register:h'0A[D5] = "1".

6.6.1 RF-Transmitting Abstract

Table 6-29 RF-Transmitting Function Abstracts

Item	Function
Modulation	FSK / ASK
Deviation (FSK)	Unmodulated - +/-105 kHz (315MHz Band) Unmodulated - +/-157.5 kHz (434MHz Band) Unmodulated - +/-315kHz (868 / 915MHz Band) * 64 steps in each frequency band. (Including unmodulated)
RF-Transmitting Frequency Band	315, 434, 868 / 915 MHz
Output Level	Coarse: 4 steps Fine: 16 steps

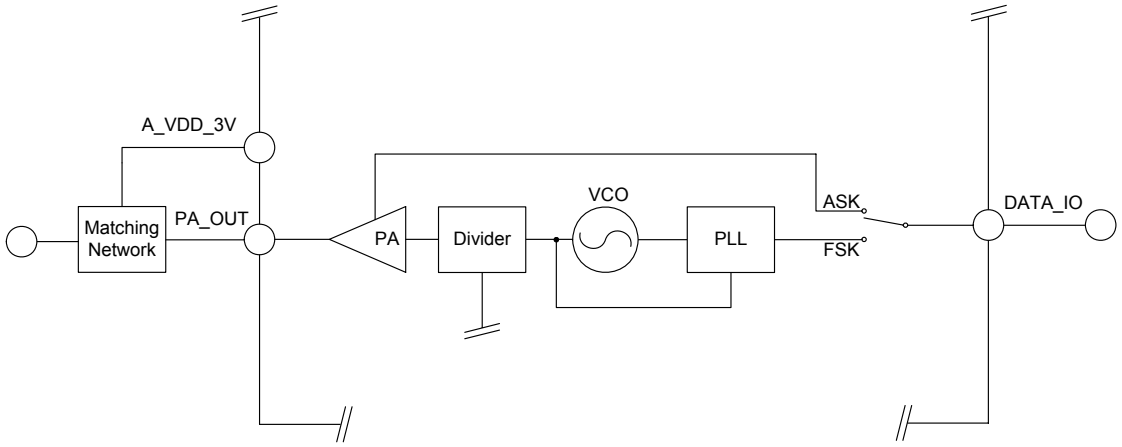


Fig 6-10 Transmitter Block Diagram

6.6.2 RF Signal Modulation

TC32306FTG is available 2 modulation, FSK and ASK to be set by register:h'0A[D4].

Table 6-30 RF Signal Modulation

h'0A[D5]RX_TX	h'0A[D4]FSK_ASK	Modulation
0	XX	RX
1	0	FSK (TX)
1	1	ASK (TX)

XX: About RX, see Table 6-18

6.6.3 FSK Modulation

To select FSK, set register:h'0A[D4] to "0"(FSK). TC32306FTG operates FSK modulation at PLL block with DATA_IO pin input signal. In FSK setting, the deviation is set by the register:h'12[D7:D2]Dev5..0. Available frequency deviation steps are different at each RF frequency band.

Table 6-31 Deviation Setting (FSK)

h'12[D7] Dev5	h'12[D6] Dev4	h'12[D5] Dev3	h'12[D4] Dev2	h'12[D3] Dev1	h'12[D2] Dev0	n	Deviation after divided (fdev)		
							315 MHz nd = 6	434 MHz nd = 4	868 / 915MHz nd = 2
0	0	0	0	0	0	0	Unmodulated	Unmodulated	Unmodulated
0	0	0	0	0	1	1	+/-1.67 kHz	+/-2.5 kHz	+/-5 kHz
0	0	0	0	1	0	2	+/-3.33 kHz	+/-5 kHz	+/-10 kHz
0	0	0	0	1	1	3	+/-5 kHz	+/-7.5 kHz	+/-15 kHz
....							….	….	….
0	0	1	1	0	0	12	+/-20 kHz	+/-30 kHz	+/-60 kHz
....							….	….	….
1	1	1	1	0	1	61	+/-101.67 kHz	+/-152.5 kHz	+/-305 kHz
1	1	1	1	1	0	62	+/-103.33 kHz	+/-155 kHz	+/-310 kHz
1	1	1	1	1	1	63	+/-105 kHz	+/-157.5 kHz	+/-315 kHz

Deviation after divided: fdev= (fd / nd)×n
fd: Frequency Resolution of VCO 10kHz (= fosc / 3032)　* fosc: Reference Clock Frequency (30.32MHz)
nd: Division Ratio (nd = 6 for 315 MHz Band, nd=4 for 434 MHz Band, nd = 2 for 868 / 915 MHz Band)
n: the value set by register:h'12 [D7:D2]Dev5..0. 0-63 (Converted to decimal.)

6.6.4 ASK Modulation

To select ASK, set register:h'0A[D4] to "1"(ASK). TC32306FTG operates ASK modulation by setting ON and OFF to RF-Transmitting Power Amplifier (PA) with DATA_IO pin input signal. If PA is enabled (See Table 6-33.), PA output is shown as table 6-32.

Table 6-32 PA Output and Input Logic (ASK)

DATA_IO Input Logic	PA Output
0	OFF
1	ON

6.6.5 TX Output

PA outputs modulated signal to an antenna.

(1) RF-Transmitting Power Amplifier (PA)

PA output (PA_OUT pin) is an open drain configuration. Connect a voltage supply (A_VDD_3V pin) via a matching circuit. PA is operated by the combination of register:h'0A[D5]RX_TX, register:h'13[D1]PA_en and internal lock detect signal (LD signal). LD signal is an internal signal only for PA, and it will keep high level after the first rising edge of PLL_LD signal which is monitored from DET_TMONI1/2 pin.

Table 6-33 Behavior of PA

h'0A[D5] RX_TX	h'13[D1] PA_en	Internal LD Signal	PA behavior
0	X	X	Disable
1	X	L	Disable
1	0	X	Disable
1	1	H	Enable

X: Don't care

Internal LD Signal is only use for PA, and the signal keeps "H" after the first rising edge of PLL_LD Signal. Above function is only available in TX and Internal LD Signal can not be monitored. To release the signal holding state, set one of the follows.

- Set TC32306FTG in the status of Battery Saving or Standby.
- Change from TX to RX.
- Change TX modulation. (ASK ↔ FSK)
- Change RF frequency. (In the change in the value of register "h'0B" and/or "h'0C")
- Change the value of register:h'12[D7:D2] for TX deviation. (This is only valid in FSK setting (h'0A[D4]FSK_ASK = "0"))

Notice:

- PA will continue to operate even though PLL_LD signal will be "L" because Internal LD signal still keeps to be "H".
- In PA operation, keep its load condition suitable, and that load condition must not be open or short.
- Only use for RX, keep PA_OUT pin to be open, and this IC must not be set to TX.
- Don't change RF-Transmitting Frequency Band (register: h'0A[D1:D0]) alone during TX. It may cause of unexpected radiation because the keeping of Internal LD signal level is not released.

(2) Output level

The output level is controlled 2 types of step (Coarse, Fine) independently by register.

Table 6-34 Example of PA Output Level (Coarse)

h'13[D3] TX_gain1	h'13[D2] TX_gain0	Output Level Variation Width (Reference value)
0	0	-10.1dB
0	1	-5.3dB
1	0	-2.0dB
1	1	0dB (Initial)

Above are reference values at 315 MHz Band.

Table 6-35 Example of PA Output Level (Fine)

h'13[D7] TX_subgain3	h'13[D6] TX_subgain2	h'13[D5] TX_subgain1	h'13[D4] TX_subgain0	Level Settings
0	0	0	0	Minimum
…..				…..
1	1	1	1	Maximum (Initial)

The reference level of each PA output settings are indicated in Fig 6-11. The output level steps are different from frequency band or TX_gain settings.

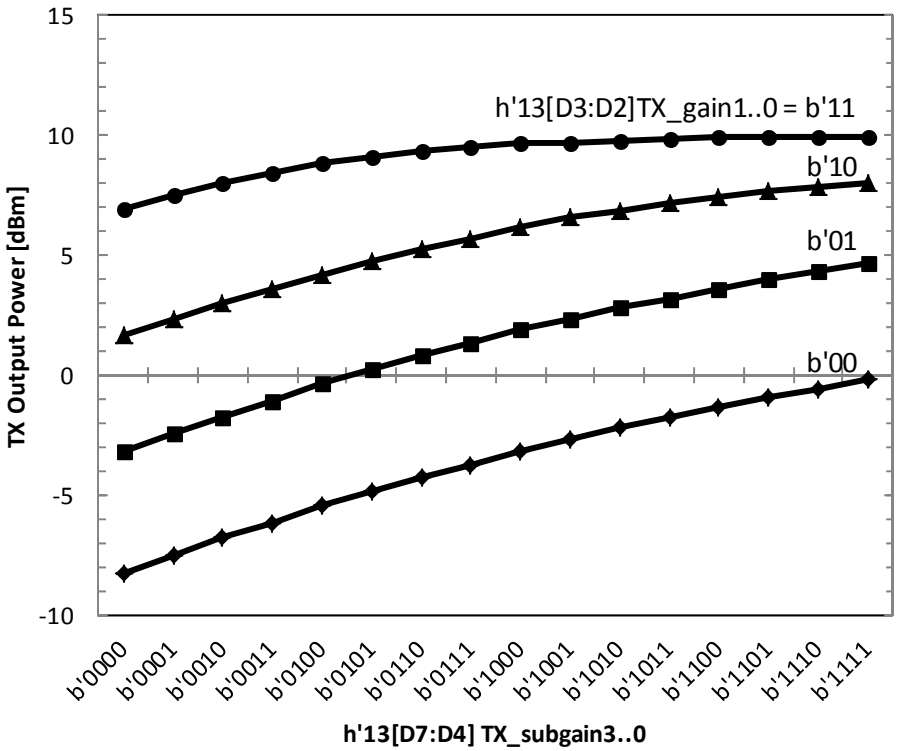


Fig 6-11 Output Level Settings (Reference Value)

6.7 Control System and Mode

6.7.1 Control System and Mode Abstract

Table 6-36 Control System and Mode Abstracts

Item	Mode / Function / pins
Way of Control	external pins, serial data control
External Pin	RESET pin, ENB pin
Control Method	SPI (Single Read/Write, Burst Read/Write), EEPROM
Control Mode	Normal / User Test

6.7.2 SPI Mode

MCU and TC32306FTG are connected by SPI lines and MCU controls this IC.

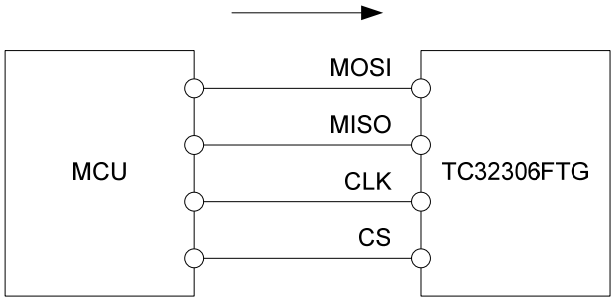


Fig 6-12 Conceptual Connection of SPI Control

In SPI Mode, TC32306FTG is available Single Read/Write and Burst Read/Write. These are selected from SPI instruction data.

Table 6-37 Single Read/Write and Burst Read/Write

Function	Explanation
Single Read/Write	To read and write only specified address register data. It is available for accessing to single or non-continuous address registers.
Burst Read/Write	To read and write in order from the specified address register data. It is available for accessing to continuous address registers. To specify the start address only causes to shorten the read/write time.

6.7.3 SPI Control Data Format

SPI control data format of TC32306FTG is constructed by instruction (8 bit), address (8 bit) and data (8 bit).

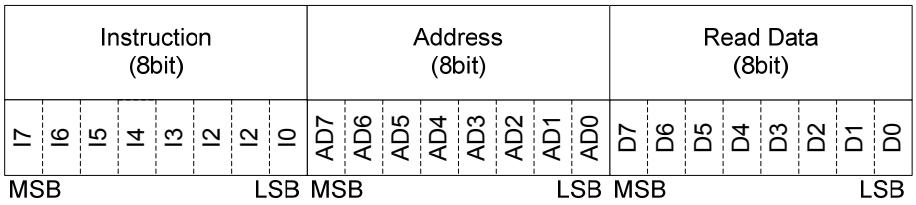


Fig 6-13 SPI Control Data Format

In SPI Mode, Single / Burst, Write / Read and Confirmation of written data are set by instruction data. Enter each SPI control data sequentially from most significant bit (MSB).

Table 6-38 Type of SPI Instructions and Settings

SPI Control		I7	I6	I5	I4	I3	I2	I1	I0
Single Read/Write	Write	0	0	0	0	X	1	1	0
	Read	0	0	0	0	X	1	1	1
Burst Read/Write	Write	0	0	0	0	X	0	1	0
	Read	0	0	0	0	X	0	1	1
	Confirmation of written data	0	0	0	0	X	1	0	1
Stop SPI Function		Except above data							

* x: 0 or 1

* Stop SPI Function: After entering SPI instruction data, subsequent data input will be invalid. To enable the input data again, enter SPI instruction data correctly after CS pin is set to be "H" once.

6.7.4 SPI Single Read/Write

(1) Write

Set the single Read/Write (Write) data pattern to the instruction area. Set to register address to the next 8 bit, then register data to after next 8 bit. To write other address registers' data continuously, repeat above routine. After input of 24 bit data (Instruction, address and data), the register value is updated. The register data from MOSI pin is written when CS pin is "L" and CLK signal is at the rising edge.

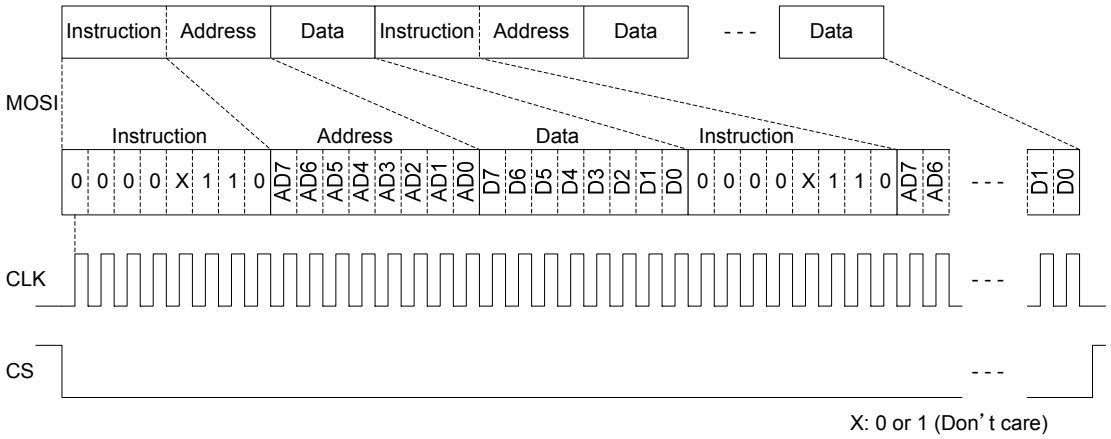


Fig 6-14 Write Format (SPI Single Read/Write)

(2) Read

Set the single Read/Write (Read) data pattern to the instruction area. Set to register address to the next 8 bit to read that data. After input the address, MISO pin outputs 8 bit data from the specified register. After output that 8 bit data, repeat above routine to read other address data continuously. During data read from MISO pin, MOSI pin does not accept input data. MISO pin outputs the register data when CS pin is "L" and CLK signal is at the falling edge.

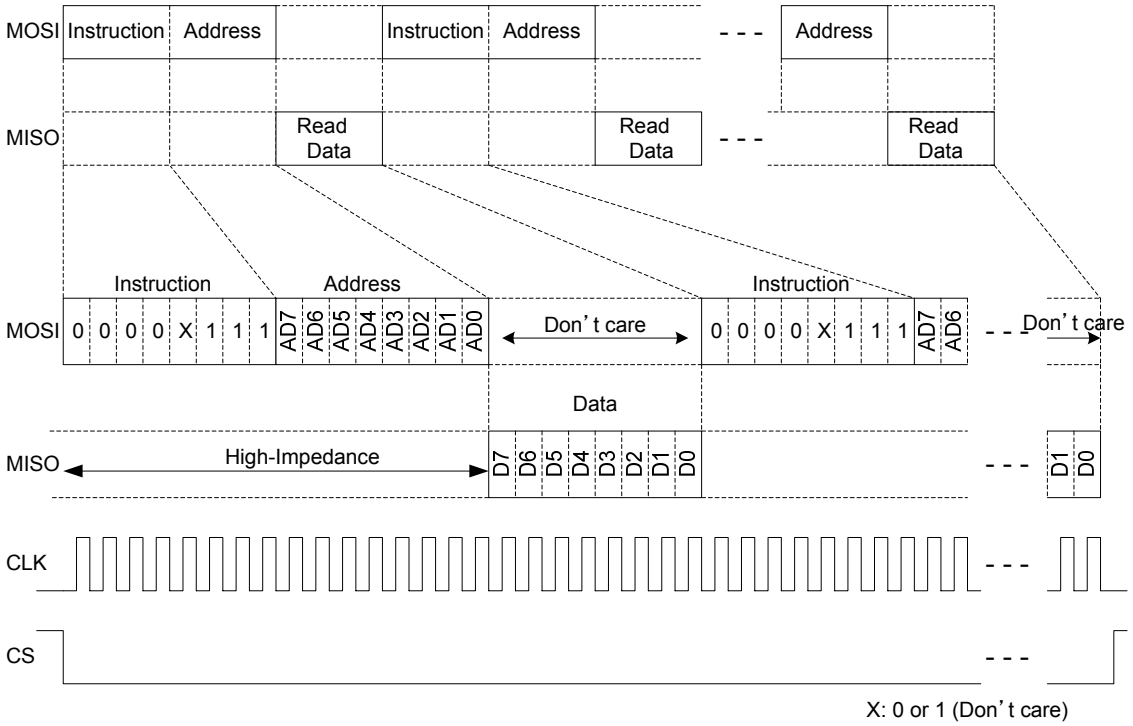


Fig 6-15 Read Format (SPI Single Read/Write)

6.7.5 SPI Burst Read/Write

(1) Write

This function continuously writes data to the order from the specified address. Set the burst Read/Write (Write) data pattern to the instruction area. Set to start register address to the next 8 bit, then register data to after next 8 bit. After that, repeat sequentially to set only 8 bit register data to the order. After every input of 8 bit data, the register value is updated. The register data from MOSI pin is written when CS pin is "L" and CLK signal is at the rising edge. Not to write unnecessary data to the following address, set CS pin to be "H" as soon as possible after writing all of the data.

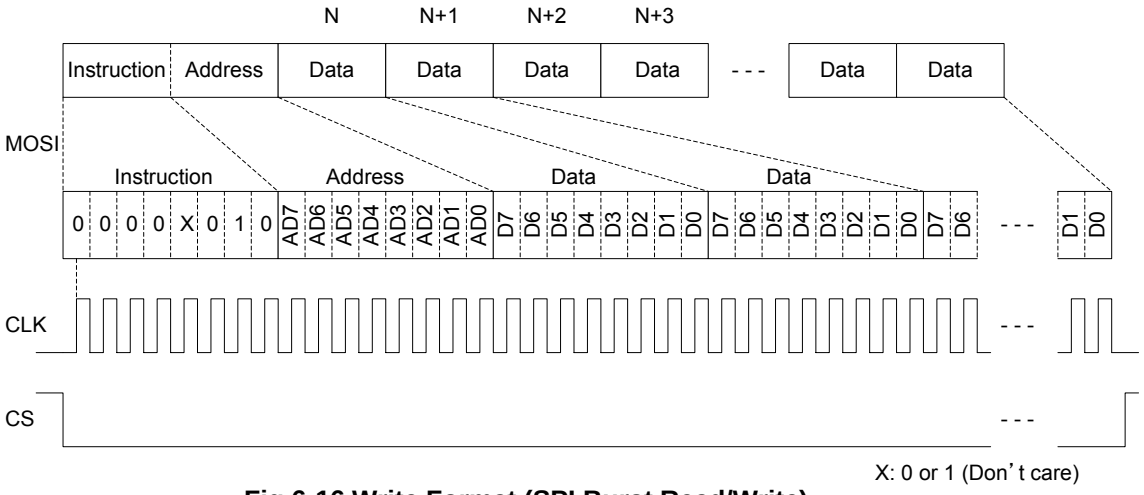


Fig 6-16 Write Format (SPI Burst Read/Write)

Notice: To change the instruction or start register address, once set CS pin to be "H" in the burst Read/Write.

(2) Read

This function continuously reads data to the order from the specified address. Set the burst Read/Write (Read) data pattern to the instruction area. Set to start register address to the next 8 bit to read that data. After input the address, MISO pin outputs 8 bit data from the specified register. To stop or finish reading data, set CS pin to be "H".

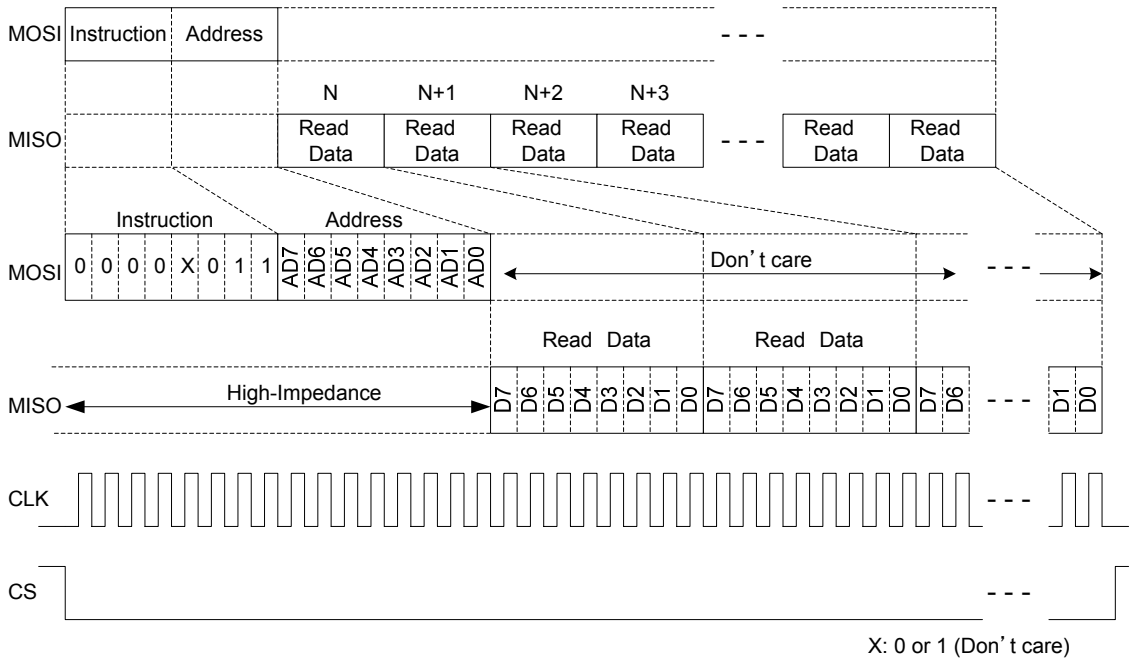


Fig 6-17 Read Format (SPI Burst Read/Write)

Notice:

- After reading data reaches the last register address (h'FF), TC32306FTG continues to output data from the beginning address (h'00).
- During outputting register value from MISO pin, MOSI pin does not accept input data.
- To change the instruction or start register address, once set CS pin to be "H" in the Burst Read/Write.

(3) Confirmation of written data

This function continuously writes data to the order from the specified address and confirms the written data.

Notice:

- This function is not intended to read the data inside the register. Use Single/Burst Read mode to confirm the data inside the register.

Set the Burst Read/Write (Confirmation of written data) data pattern to the register instruction area. Set same as the Burst Read/Write (Write) and input. The input data is output from MISO pin with 8 bit delay after the address area. The data writing is valid till the rising edge of CS signal, and the data reading is finished at the rising edge of CS signal.

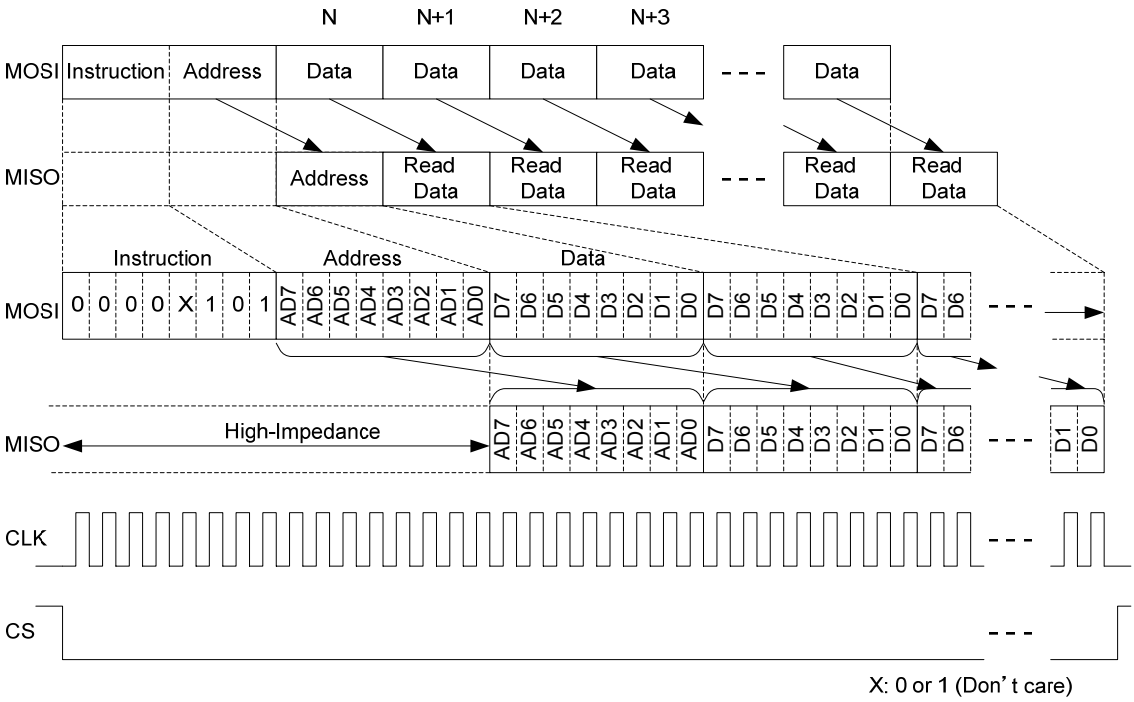


Fig 6-18 Confirmation of Written Data Format (SPI Burst Read Write)
(The number of write data is same as that of read data.)

6.7.6 SPI Mode Signal Timings

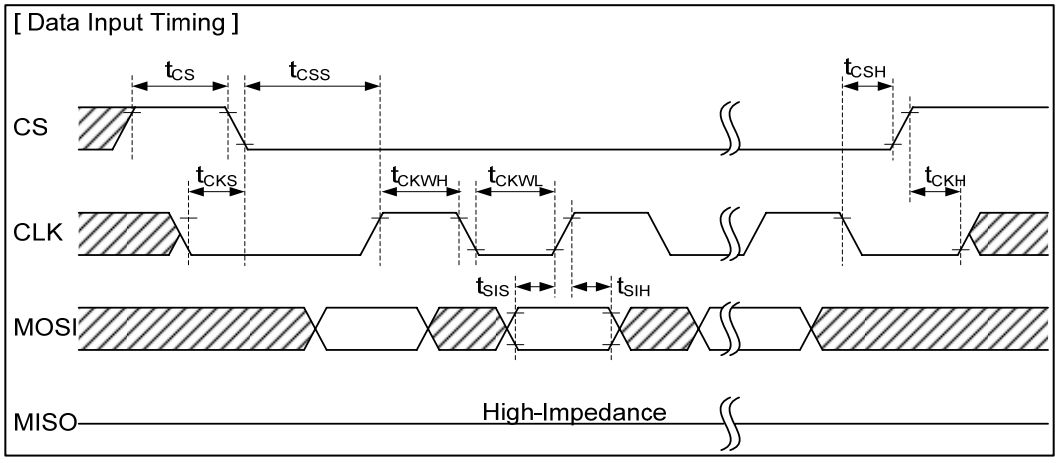


Fig 6-19 Example of SPI Write Timing

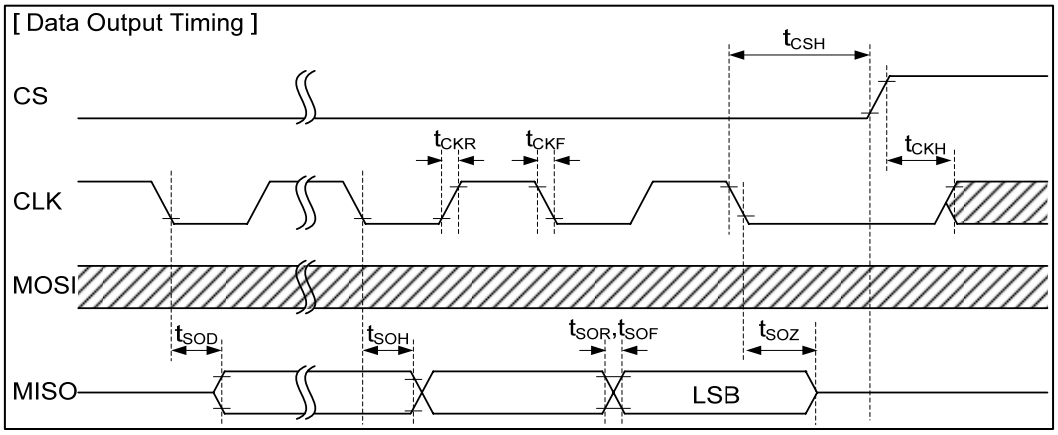


Fig 6-20 Example of SPI Read Timing (Single Read/Write)

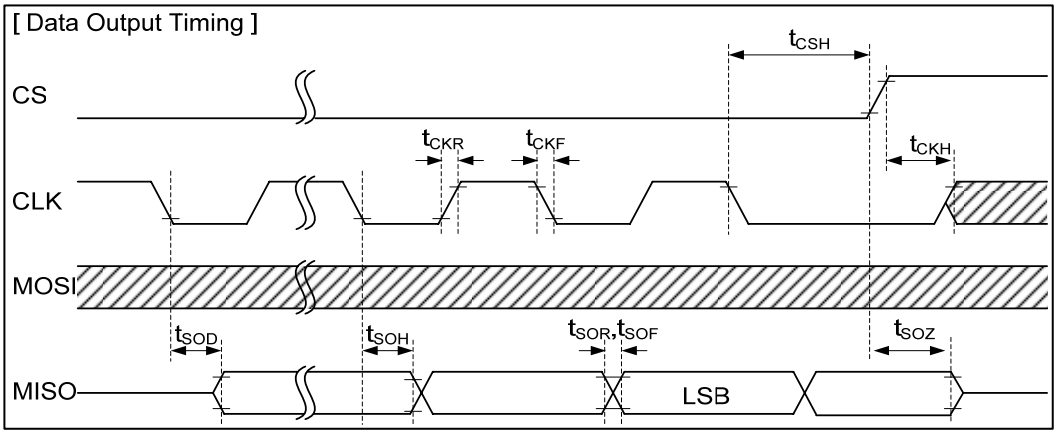


Fig 6-21 Example of SPI Read Timing (Burst Read/Write)

The timing chart for explaining the operation of features and may have been simplified.

Table 6-39 SPI Mode Timing

Item	Code	Min	Typ	Max	Unit
CLK Frequency	f_{ck}	-	-	3.0	MHz
CLK ”H” Time	t_{CKWH}	100	-	-	ns
CLK ”L” Time	t_{CKWL}	100	-	-	ns
CLK Setup Time	t_{CKS}	40	-	-	ns
CLK Hold Time	t_{CKH}	40	-	-	ns
CLK Rising Time	t_{CKR}	-	-	10	ns
CLK Falling Time	t_{CKF}	-	-	10	ns
CS “H” Time	t_{CS}	40	-	-	ns
CS Setup Time	t_{CSS}	30	-	-	ns
CS Hold Time	t_{CSH}	100	-	-	ns
MOSI Setup Time	t_{SIS}	30	-	-	ns
MOSI Hold Time	t_{SIH}	30	-	-	ns
MISO Delay Time *	t_{SOD}	-	-	100	ns
MISO Hold Time *	t_{SOH}	-	-	100	ns
MISO Disable Time *	t_{SOZ}	-	-	30	ns
MISO Rising Time *	t_{SOR}	-	-	50	ns
MISO Falling Time *	t_{SO}	-	-	50	ns

* Time values of MISO are derived at the load capacitance of 10pF.

6.7.7 EEPROM Mode

EEPROM and MCU, connect via TC32306FTG. This IC is controlled by the register data of EEPROM. Select up to 8 configuration data that are made as registers' modules from “h'0A” to “h'1C”, depending on the size of EEPROM. In this mode, use of pins and external connections are different from those of SPI Mode. For example, TX_SW / RX_SW / ENB pin are used to select configuration data of EEPROM. Must not set MODE2 pin to “L” (= for SPI Mode) at the circuit connection for EEPROM Mode.

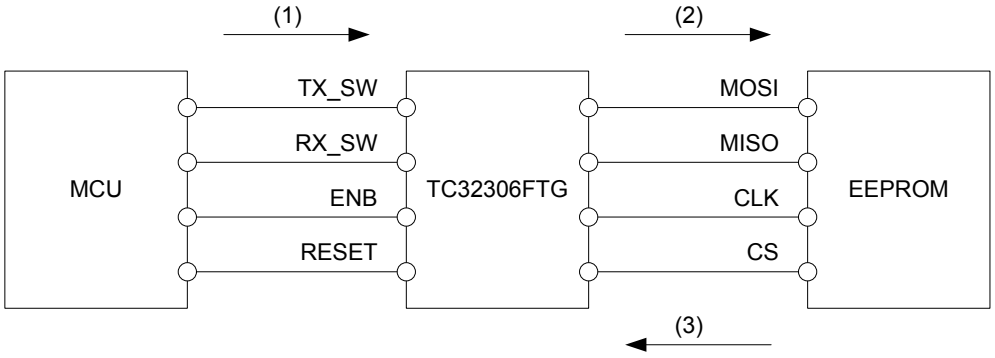


Fig 6-22 Conceptual Connection MCU, EEPROM and TC32306FTG

- In advance, write registers’ values to each configuration data area of EEPROM.
- MCU commands this IC for selecting configuration data area of EEPROM. (1)
- This IC read a configuration data from EEPROM by SPI lines at the rising edge of RESET pin signal. (2)
- This IC is operated depending on EEPROM data. (3)

- Majority logic

In EEPROM Mode, the majority logic is adopted to reduce the probability of unexpected operation due to data corruption of EEPROM. Each configuration data prepares 3 set of data area in EEPROM, and the register of This IC read them. Then the data values are decided by a majority vote of each bit. In advance, three same data are written for each configuration to the specified address of EEPROM. The relation between EEPROM address and the register address of this IC are shown in Table 6-40.

6.7.8 EEPROM Control Data Format

In EEPROM Mode, TC32306FTG operates Burst Read for the EEPROM. The configuration data is selected by the combination of TX_SW pin, RX_SW pin and ENB pin.

Notice:
- The memory size of 1 k, 2 k and 4 k bit are available for EEPROM. The configuration data of 2,4 and 8 are available respectively.
- Select EEPROM adapted for Burst Read.
- The serial clock (= CLK pin output signal) to read EEPROM data generated by the inner oscillator of TC32306FTG is frequency of about 2 MHz. Select EEPROM adapted for that frequency.

(1) Set the configuration data to read by TX_SW pin, RX_SW pin and ENB pin from MCU. Then set RESET pin is "H". (= The reset is released.) The configuration data change is available all the time, however the operation is valid at the time of change of RESET pin from "L" to "H".
(2) TC32306FTG operates Burst Read to the first set data area of EEPROM through SPI lines. Burst Read operates from the start address till the end address of the configuration data sequentially. After the reading, this IC starts to run as the configuration of first set data area.
(3) This IC operates Burst Read to the second and third set data area continuously, then the register setting is fixed by majority logic.
(4) This IC runs depending on the register:h'0A[D7]ACT.

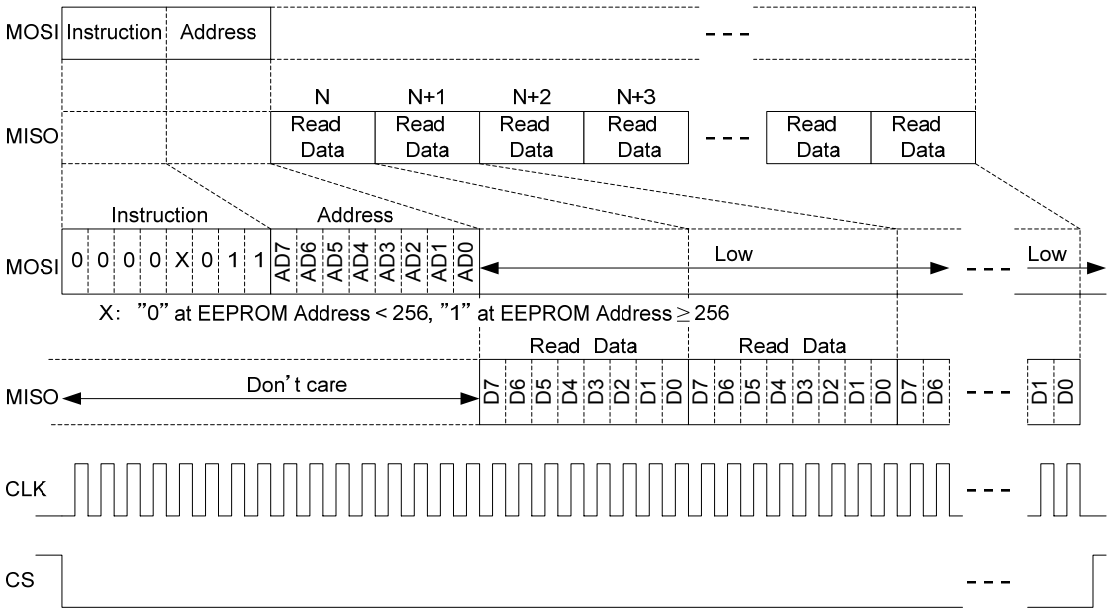


Fig 6-23 Read Format from EEPROM (EEPROM Mode)

Table 6-40 Relation between EEPROM and TC32306FTG Register Address

Config.	Pin Name			Read Order	EEPROM Address									EEPROM Size		
	RX_SW	TX_SW	ENB													
Config. 1	0	0	0	1st	0	1	2	3	…	15	16	17	18	1k-bit(128words)	2k-bit(256words)	4k-bit(512words)
				2nd	20	21	21	23	…	35	36	37	38			
				3rd	40	41	42	43	…	55	56	57	58			
Config. 2	0	0	1	1st	64	65	66	67	…	79	80	81	82			
				2nd	84	85	86	87	…	99	100	101	102			
				3rd	104	105	106	107	…	119	120	121	122			
Config. 3	0	1	0	1st	128	129	130	131	…	143	144	145	146			
				2nd	148	149	150	151	…	163	164	165	166			
				3rd	168	169	170	171	…	183	184	185	186			
Config. 4	0	1	1	1st	192	193	194	195	…	207	208	209	210			
				2nd	212	213	214	215	…	227	228	229	230			
				3rd	232	233	234	235	…	247	248	249	250			
Config. 1	1	0	0	1st	256	257	258	259	…	271	272	273	274			
				2nd	276	277	278	279	…	291	292	293	294			
				3rd	296	297	298	299	…	311	312	313	314			
Config. 5	1	0	1	1st	320	321	322	323	…	335	336	337	338			
				2nd	340	341	342	343	…	355	356	357	358			
				3rd	360	361	362	363	…	375	376	377	378			
Config. 6	1	1	0	1st	384	385	386	387	…	399	400	401	402			
				2nd	404	405	406	407	…	419	420	421	422			
				3rd	424	425	426	427	…	439	440	441	442			
Config. 7	1	1	1	1st	448	449	450	451	…	463	464	465	466			
				2nd	468	469	470	471	…	483	484	485	486			
				3rd	488	489	490	491	…	503	504	505	506			
TC32306FTG Register Address					h'0A	h'0B	h'0C	h'0D	…	h'19	h'1A	h'1B	h'1C			

6.7.9 EEPROM Mode Signal Timings

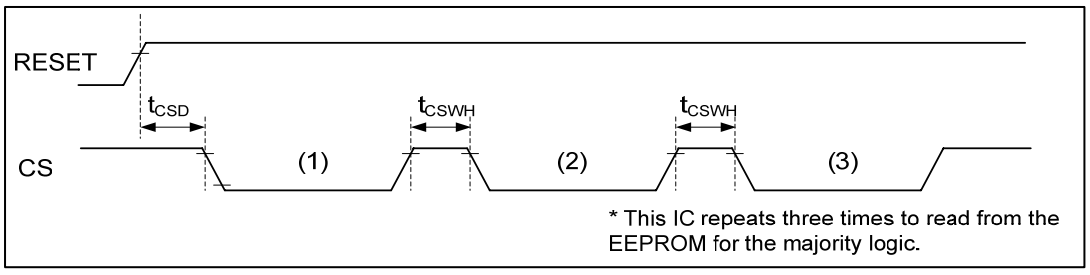


Fig 6-24 Example of EEPROM Control Timing

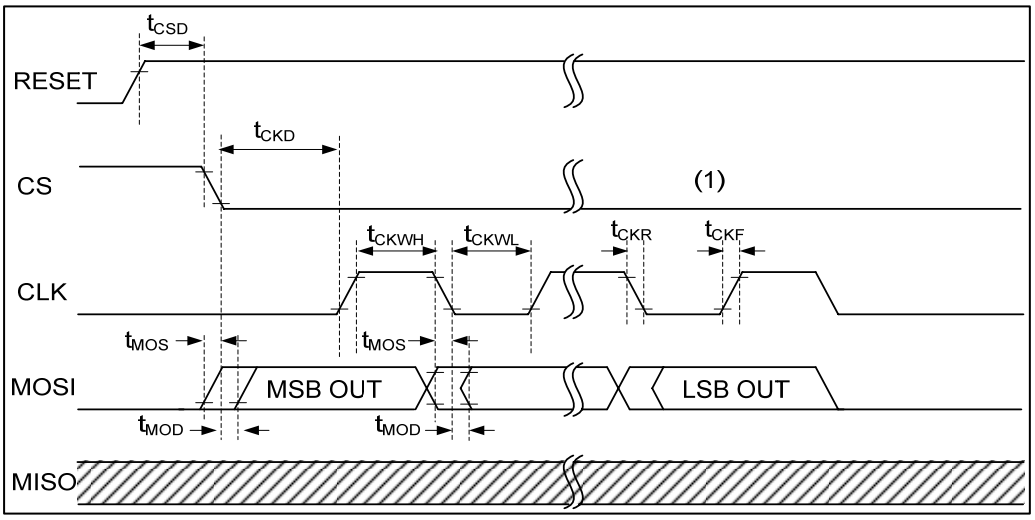


Fig 6-25 Example of EEPROM Output Timing

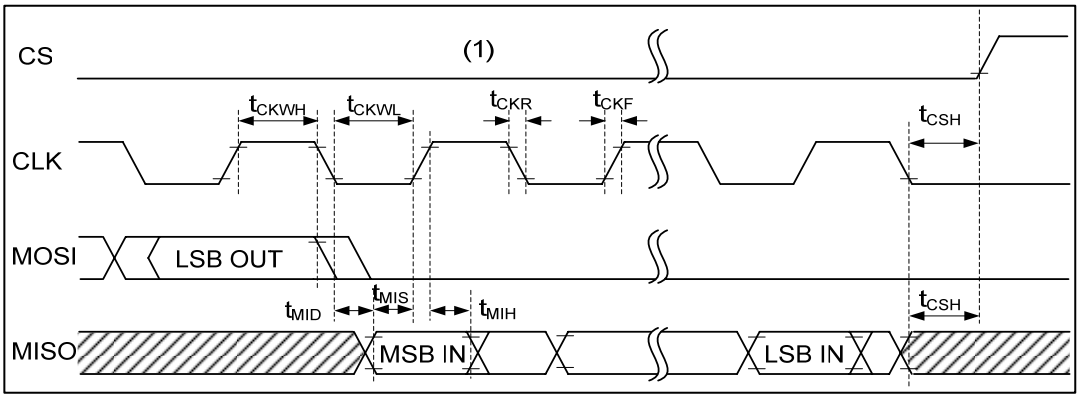


Fig 6-26 Example of EEPROM Input Timing

The timing chart for explaining the operation of features and may have been simplified.

Table 6-41 EEPROM Mode Timing (COM_VDD = 3.0 - 5.5V)

Item	Code	Min	Typ	Max	Unit
CLK Frequency *	f_{ck}	1.0	2.0	3.0	MHz
CLK ”H” Time *	t_{CKWH}	125	-	-	ns
CLK ”L” Time *	t_{CKWL}	125	-	-	ns
CLK Rising Time *	t_{CKR}	-	-	50	ns
CLK Falling Time *	t_{CKF}	-	-	50	ns
CLK Delay Time *	t_{CKD}	150	-	-	ns
CS Delay Time *	t_{CSD}	400	-	-	ns
CS “H” Time *	t_{CSWH}	500	-	-	ns
CS Hold Time *	t_{CSH}	100	-	-	ns
MOSI Preceding Time *	t_{MOS}	-	-	50	ns
MOSI Delay Time *	t_{MOD}	-	-	50	ns
MISO Delay Time	t_{MID}	-	-	90	ns
MISO Setup Time	t_{MIS}	-	-	10	ns
MISO Hold Time	t_{MIH}	-	-	100	ns

* Time values of CLK, MISO and MOSI are derived at the load capacitance of 10pF.

Table 6-42 EEPROM Mode Timing (COM_VDD = 2.5 - 3.0V)

Item	Code	Min	Typ	Max	Unit
CLK Frequency *	f_{ck}	1.0	2.0	3.0	MHz
CLK ”H” Time *	t_{CKWH}	150	-	-	ns
CLK ”L” Time *	t_{CKWL}	150	-	-	ns
CLK Rising Time *	t_{CKR}	-	-	50	ns
CLK Falling Time *	t_{CKF}	-	-	50	ns
CLK Delay Time *	t_{CKD}	150	-	-	ns
CS Delay Time *	t_{CSD}	400	-	-	ns
CS “H” Time *	t_{CSWH}	500	-	-	ns
CS Hold Time *	t_{CSH}	100	-	-	ns
MOSI Preceding Time *	t_{MOS}	-	-	50	ns
MOSI Delay Time *	t_{MOD}	-	-	50	ns
MISO Delay Time	t_{MID}	-	-	120	ns
MISO Setup Time	t_{MIS}	-	-	10	ns
MISO Hold Time	t_{MIH}	-	-	100	ns

* Time values of CLK, MISO and MOSI are derived at the load capacitance of 10pF.

6.8 User Test

This is a mode to monitor inner digital signal for design, development, manufacturing or shipping inspection. Set MODE1 pin to be “H” and/or the register: USER_TEST bit is “1” then TC32306FTG moves to User Test. In User Test, various inner signals for the adjustment are converted to analog and are output from DET_TMONI3 pin or DET_TMONI4 pin by the setting of register. The setting register of SPI Mode is different from that of EEPROM Mode.

Table 6-43 Inner Signal Monitor (DET_TMONI3 Pin)

Status	h'10[D3] USER_TEST / MODE1Pin	h'15[D6] MONI3_SEL2	h'15[D5] MONI3_SEL1	h'15[D4] MONI3_SEL0	Signal
Battery Saving	X	X	X	X	"Z"
Run / Standby	0 and L	X	X	X	"L" Output
Run / Standby	1 or H	0	0	0	BRF_out
Run / Standby	1 or H	0	0	1	BRF_in
Run / Standby	1 or H	0	1	0	Data_compREF
Run / Standby	1 or H	0	1	1	DRSSI_out
Run / Standby	1 or H	1	0	0	Noise _out
Run / Standby	1 or H	1	0	1	Peak_out
Run / Standby	1 or H	1	1	0	"L" Output
Run / Standby	1 or H	1	1	1	"L" Output

X: Don't care

Table 6-44 Inner Signal Monitor (DET_TMONI4 Pin)

Status	h'10[D3] USER_TEST / MODE1 Pin	h'15[D6] MONI3_SEL2	h'15[D5] MONI3_SEL1	h'15[D4] MONI3_SEL0	Signal
Battery Saving	X	X	X	X	"Z"
Run / Standby	0 and L	X	X	X	"L" Output
Run / Standby	1 or H	0	0	0	Data_compREF
Run / Standby	1 or H	0	0	1	BRF_in
Run / Standby	1 or H	0	1	0	BRF_out
Run / Standby	1 or H	0	1	1	DRSSI_out
Run / Standby	1 or H	1	0	0	Noise _out
Run / Standby	1 or H	1	0	1	Peak_out
Run / Standby	1 or H	1	1	0	"L" Output
Run / Standby	1 or H	1	1	1	"L" Output

X: Don't care

Table 6-45 Internal Signals Available in User Test

Signal	Explanation of Signal
BRF_out	Output of Bit Rate Filter
BRF_in	Input of Bit Rate Filter (FSK / ASK Demodulation LPF Output)
Data_compREF	Output of Data Comparator Reference Voltage
DRSSI_out	RSSI Output (Digital RSSI Output Converted to Analog)
Noise _out	Noise Detection Voltage Output of Noise Detector
Peak_out	Peak Hold Voltage Output of Peak Hold Circuit

Notice:

- Set User Test only for development or estimation, not for actual use (consumer products). Sensitivity of this IC may be worse by the radiation from monitor pins.

(1) Register settings in SPI Mode

In SPI Mode, set them as same as normal use.

(2) Register settings in EEPROM Mode

In EEPROM Mode, the register can be set them through SPI lines connecting EEPROM. Usually, in EEPROM Mode, TC32306FTG as a master reads the register data in EEPROM through SPI lines. But in User Test, this IC as a slave accepts input from SPI lines. In the case, SPI control settings and the instructions in SPI format changes. (The MBS "I7" in the instruction changes from 0 to 1.)

Table 6-46 Type of EEPROM Instructions in User Test and Settings

EEPROM Control		I7	I6	I5	I4	I3	I2	I1	I0
Single Read/Write	Write	1	0	0	0	x	1	1	0
	Read	1	0	0	0	x	1	1	1
Burst Read/Write	Write	1	0	0	0	x	0	1	0
	Read	1	0	0	0	x	0	1	1
	Confirmation of written data	1	0	0	0	x	1	0	1
SPI Function Stop		Except above data							

* x: 0 or 1

* SPI Function Stop: After writing SPI instruction data, subsequent data input will be disabled. Again, to enable the input data, enter SPI instruction data correctly after CS pin is set to be "H" once.

Notice:

- In User Test, don't select that TC32306FTG and EEPROM are both signal output side at SPI lines to set their registers.
- Take care of avoiding chattering to enter User Test by MODE1 pin.

6.9 Status Transition

The Status Transition is carried out after the register value is written. The status after the transition depends on the register settings. Each status can be moved as following figure by the register settings.

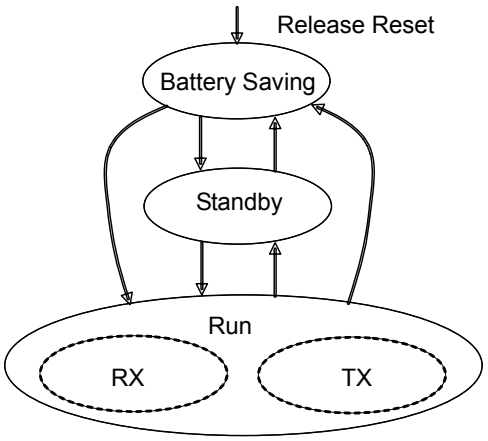


Fig 6-27 Status and Status Transition

Table 6-47 Status Control in SPI Mode

External Pin	Register Settings		Operations of Function Blocks			Status
ENB Pin (Only in SPI Mode)	h'0A[D7] ENB	h'0A[D6] ACT	SPI	Reference Clock / Internal Regulator	Others	
L	X	X	ON	OFF	OFF	Battery Saving
H	0	X	ON	OFF	OFF	
H	1	0	ON	ON	OFF	Standby
H	1	1	ON	ON	ON	Run

X: Don't care

6.9.1 Power On → Battery Saving → Run

TC32306FTG will enter the setup sequence after Power On, releasing reset and register settings. In the setup sequence, this IC starts to setup and operate internal function blocks simultaneously.

- Delay Setting

The setup sequence will start after about 105.5 µs (Initial value) from the output level of Reference Clock Oscillator is over a certain level. Delay is selected by the register setting. Set it with considering Reference Clock oscillation stabilization time. The start timing of Delay is whichever later that output level of Reference Clock oscillator will be over a certain level or that TC32306FTG status will move to Run by the register settings.

Table 6-48 Delay Time Setting of the Setup Sequence Start

h'0D[D7] Delay_en	h'0D[D6] Delay2	h'0D[D5] Delay1	h'0D[D4] Delay0	Delay time until the setup sequence starts.
0	X	X	X	105.5µs
1	0	0	0	105.5µs
1	0	0	1	211.1µs
1	0	1	0	316.5µs
1	0	1	1	527.5µs
1	1	0	0	949.5µs
1	Except Above			105.5µs

X: Don't care

Notice:

- Delay is derived from 30.32MHz Reference Clock Frequency.
- In SPI Mode, the initial register setting is h'0D[D7]Delay_en = "0". Delay is always about 105.5 µs.
- In SPI Mode, to enter the setup sequence with setting Delay time, move TC32306FTG status from Battery Saving/Standby to Run after the register setting.
- If the register of Delay time is set in Run status, the value of Delay time is valid at the next status moving form Battery Saving/Standby to Run.
- In EEPROM Mode (Except User Test), this IC enters the setup sequence with the setting Delay time because this IC status definitely moves from Standby to Run after the register setting..

- Example of Boot Sequence 1: RX (in SPI Mode)

The following Fig 6-28 shows status transition from Battery Saving/Standby to RX-Run.

1. Power On, then reset is released after the voltage supply becomes stable.
2. Set registers if necessary with Standby (ENB pin = "H", register:h'0A[D7]ENB = "1", register:h'0A[D7]ACT = "0"). Then internal regulators and Reference Clock Oscillator start to operate.
3. After the output of internal regulators become stable, set register:h'0A and move to Run. (ENB pin = "H", register:h'0A[D7]ENB = "1", register:h'0A[D7]ACT = "1")
4. The setup sequence and operation of internal function blocks will start after setting Delay time from the output level of Reference Clock Oscillator is over a certain level.

5. Signal Detections (RSSI & Noise Detection) with operating cycle (Initial value: 1.35 ms) set by register will start after the internal setup (about 0.22 ms) is finished.
6. Start timing of the demodulation output (from DATA_IO pin) is varied with Bit Rate Filter setting, data rate or other register settings. Preamble Detection output starts after the demodulation output is obtained.

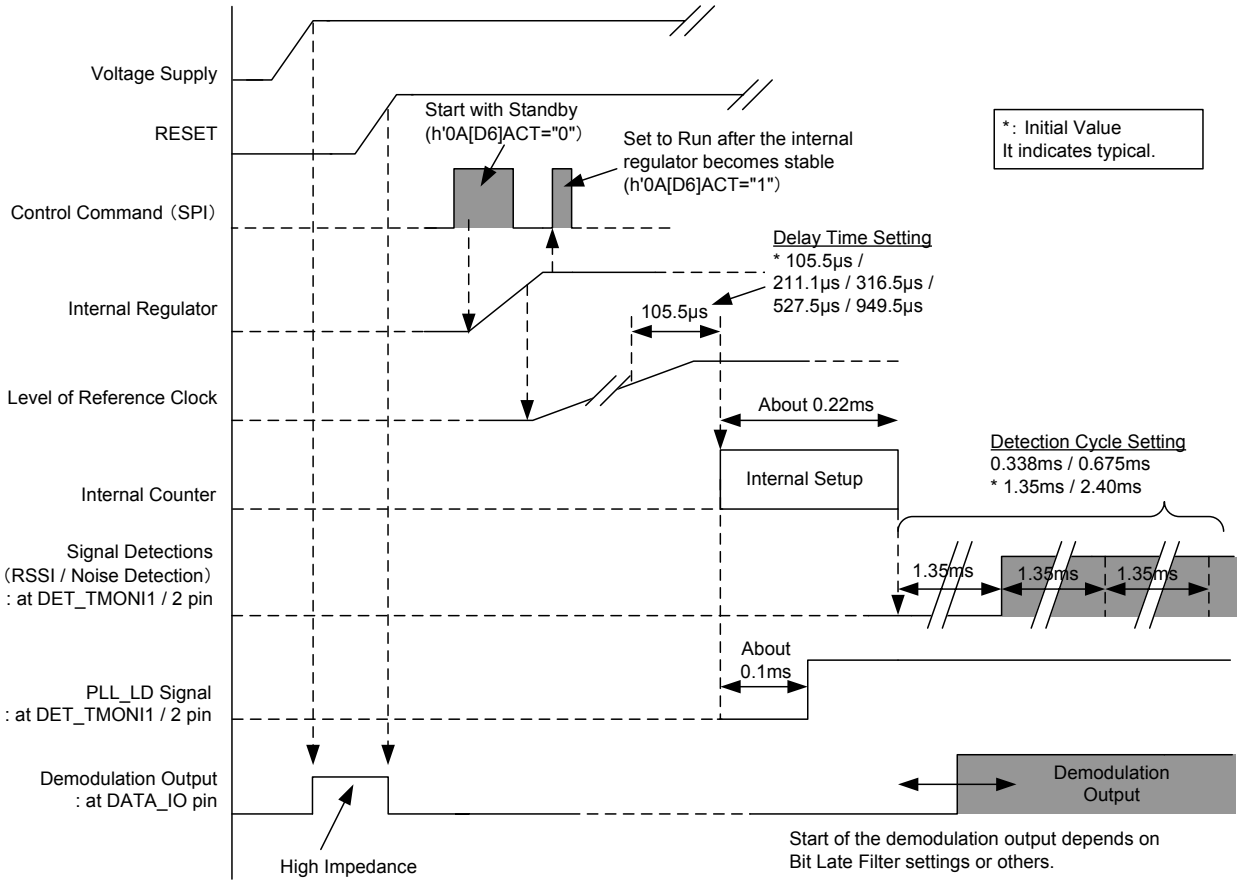


Fig 6-28 Example of Boot Sequence Timing Chart (SPI Mode / RX)

* The example of timing chart may be omitted or simplified for explanatory purposes.

Notice:

- It is recommended that TC32306FTG starts with Standby and set registers then move to Run so that all the register settings are valid at the first boot sequence.
- It is possible to move to Run without going through Standby. However in that case, DATA_IO pin / DET_TMONI1 pin / DET_TMONI2 pin may be undefined output until reaching the stable output of internal regulator. Capture this IC outputs by the external MCU after the internal regulator has been stable.
- When this IC will move to Run without going through Standby and the clock frequency of SPI will be slow, register settings during the internal setup should be avoided. It may cause unexpected operation. Not to be avoided, this IC operation starts with Standby and set registers then moves to Run.

- Example of Boot Sequence 2: TX (in SPI Mode)

The following Fig 6-29 shows status transition from Battery Saving/Standby to TX-Run.

1. Power On, and reset is released after the voltage supply becomes stable.
2. Set registers if necessary with Standby (ENB pin = “H”, register:h’0A[D7]ENB = ”1”, register:h’0A[D7]ACT = ”0”). Then internal regulators and Reference Clock Oscillator start to operate.
3. After the output of internal regulators become stable, set register:h’0A and move to Run. (ENB pin = “H”, register:h’0A[D7]ENB = ”1”, register:h’0A[D7]ACT = ”1”)
4. The setup sequence and operation of internal function blocks will start after setting Delay time

from the output level of Reference Clock Oscillator is over a certain level.

5. PLL Block will start after the internal setup (about 0.05 ms). After locking the expected frequency is detected, PLL_LD signal and Internal LD signal will be from "L" to "H". PLL lock-up time is approximately 0.05 ms after internal setup is finished. About Internal LD signal, see section 6.6.5.
6. Input the signal for modulation to DATA_IO pin. The RF modulated Signal will be transmitted from PA after PLL_LD signal turns to be "H" immediately, because initial value of register:h'13[D1]PA_en is "1". It is also possible to set the register:h'13[D1]PA_en = "0" at the first register setting.

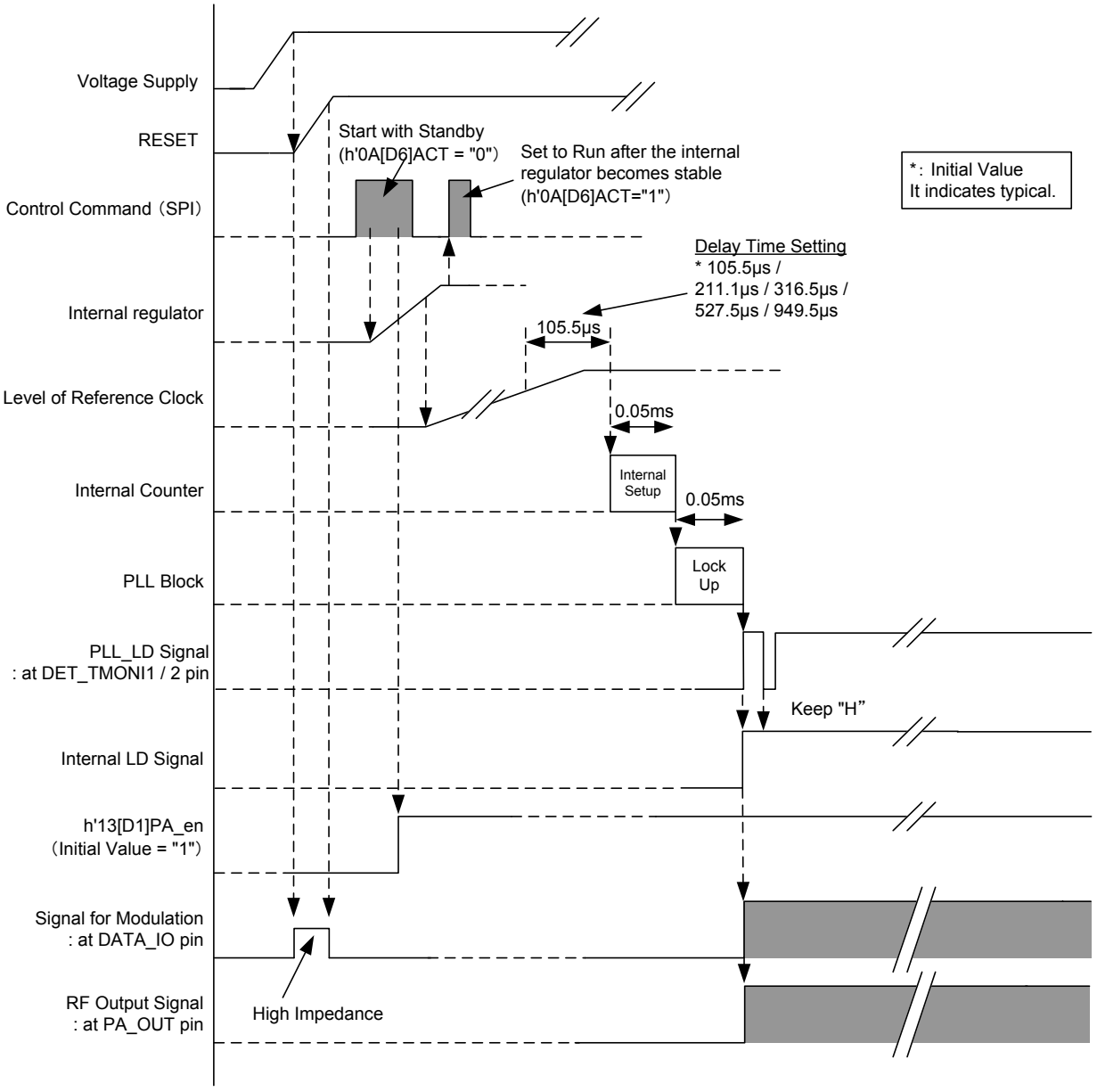


Fig 6-29 Example of Boot Sequence Timing Chart (SPI Mode / TX)

* The example of timing chart may be omitted or simplified for explanatory purposes.

Notice:

- It is recommended that TC32306FTG starts with Standby and set registers then move to Run so that all the register settings are valid at the first boot sequence.
- It is possible to move to Run without going through Standby. However in that case, DATA_IO pin / DET_TMONI1 pin / DET_TMONI2 pin may be undefined output until reaching the stable output of internal regulator. Capture this IC outputs by the external MCU after the internal regulator has been stable.
- PLL_LD signal is not undefined internally during undefined output with DAT_TMONI1/2 pin

moving to Run without going through Standby. PA is not enabled during this period.

- When this IC will move to Run without going through Standby and the clock frequency of SPI will be slow, register settings during the internal setup should be avoided. It may cause unexpected operation. Not to be avoided, this IC operation starts with Standby and set registers then moves to Run.

- Example of Boot Sequence 3: RX (in EEPROM Mode)

The following Fig 6-30 shows boot sequence of RX in EEPROM Mode in Fig 6-30.

1. Power On, and reset is released after the voltage supply becomes stable.
2. Start to read the register of first set data area of EEPROM sequentially. (It is indicated by the combination of TX_SW pin, RX_SW pin and ENB pin.)
3. Start to operate with Standby despite of the value of the register:h'0A[D7]ACT. Internal regulators and Reference Clock Oscillator start to operate.
4. Read the second and third set data area continuously then the register setting is fixed.
5. Continue to operate depending on the setting of the register:h'0A[D7]ACT.
6. The setup sequence and operation of internal function blocks will start after setting Delay time from the output level of Reference Clock Oscillator is over a certain level.
7. Signal Detections (RSSI & Noise Detection) with operating cycle (Initial value: 1.35 ms) set by register will start after the internal setup (about 0.22 ms) is finished.
8. Start timing of the demodulation output (from DATA_IO pin) is varied with Bit Rate Filter setting, data rate or other register settings. Preamble Detection output starts after the demodulation output is obtained.

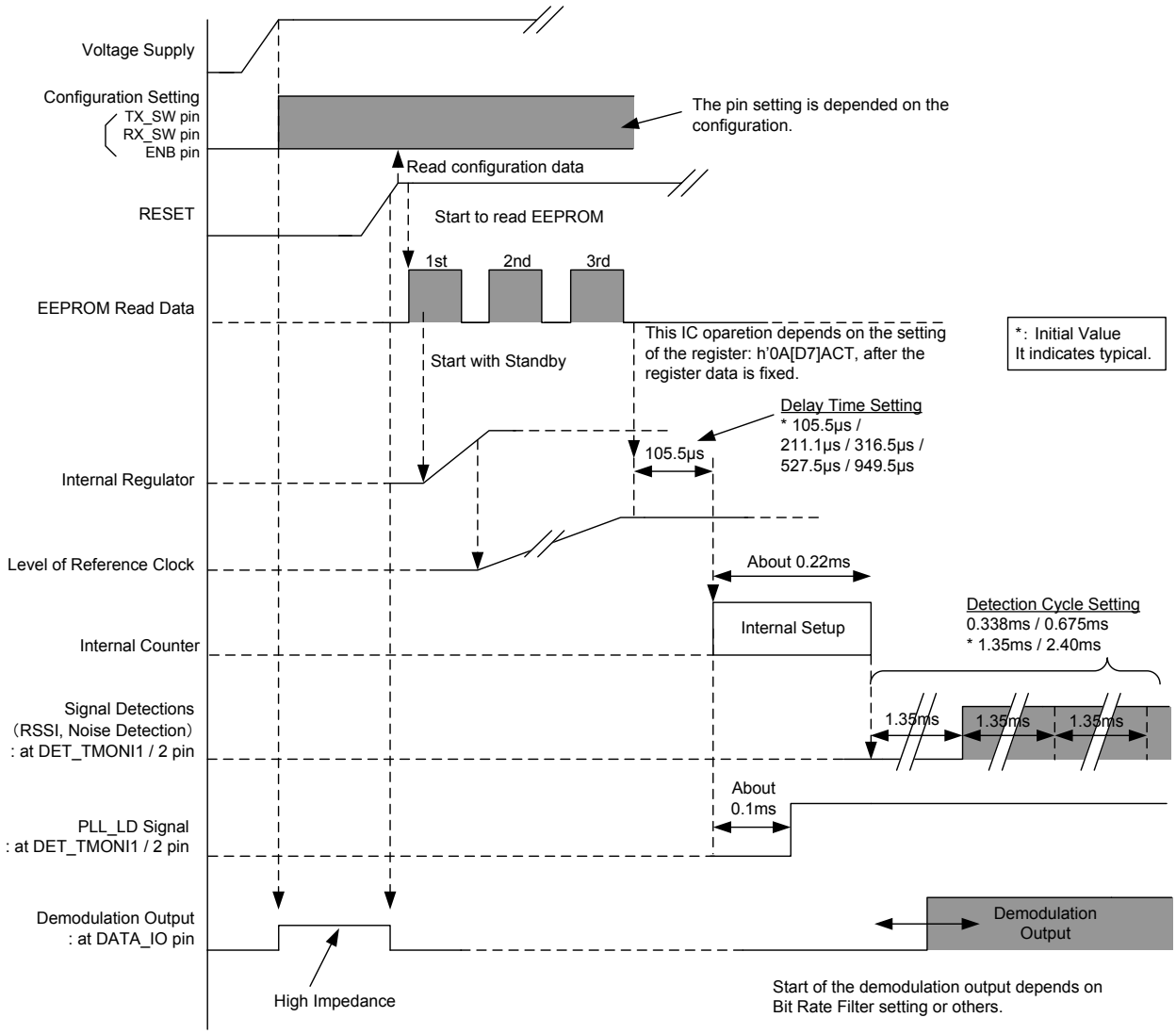


Fig 6-30 Example of Boot Sequence Timing Chart (EEPROM Mode / RX)

* The example of timing chart may be omitted or simplified for explanatory purposes.

Notice:

- In EEPROM Mode, internal regulator with suitable external capacitor value becomes stable till moving to Run. DAT_TMONI1/2 pin have no undefined period.
- Input the configuration data during the stable voltage supply.

6.9.2 Transition in Rum Status (RX → TX → RX)

Transition of RX/TX each other in Run Status by setting the register: h'0A[D5]RX_TX.

Example: RX → TX → RX (SPI Mode)

The example of the transition "RX → TX → RX" in SPI Mode is shown as Fig 6-31.

1. At the end of RX, set the register: h'0A[D5]RX_TX = "1" then TC32306FTG changes to TX.
2. After finishing all register settings, CS pin becomes "H", then this IC will start the setup sequence, PLL lock-up and the operation set by registers.
3. At the end of TX, set the register: h'0A[D5]RX_TX = "0" then change to RX. After finishing all register settings, CS pin becomes "H", then this IC will start the setup sequence, PLL lock-up and the operation set by registers.

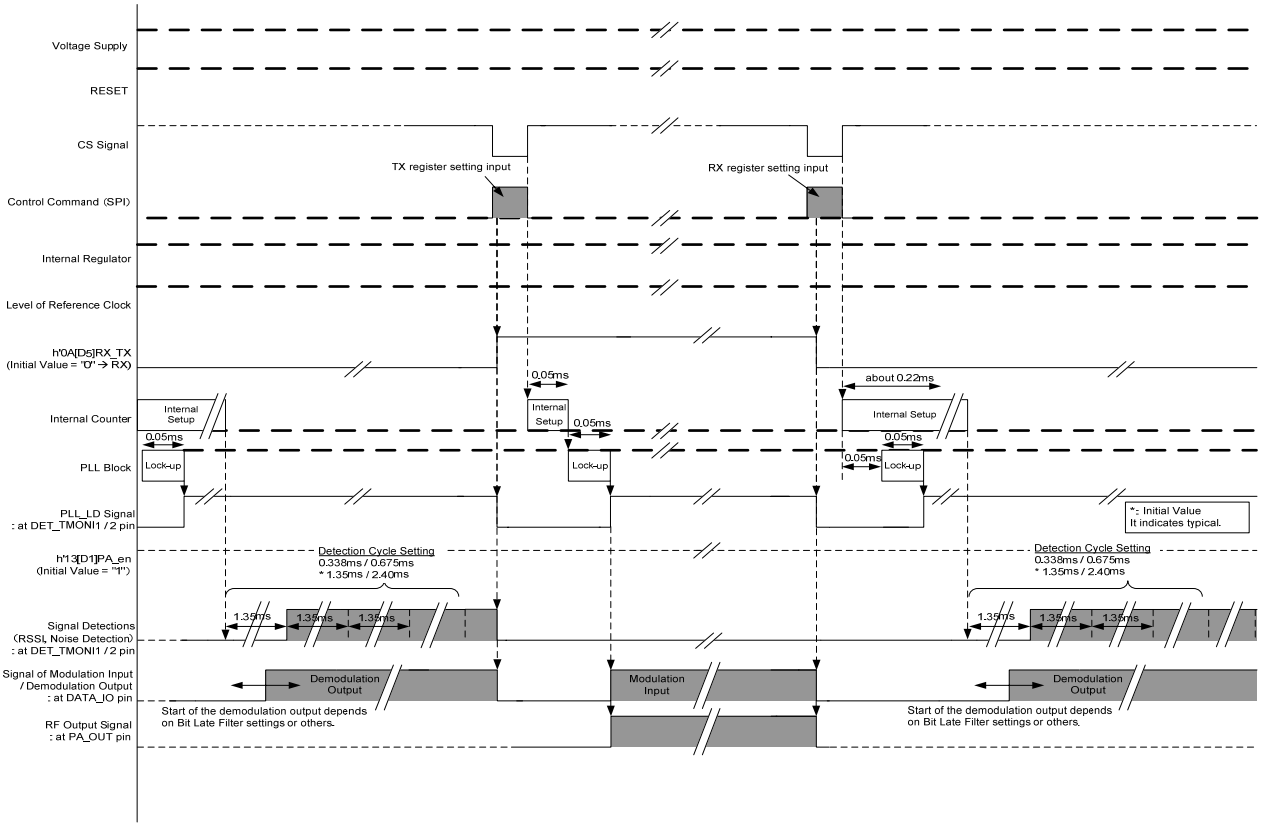


Fig 6-31 Example of Timing Chart (RX → TX → RX in SPI Mode)

Notice:

- In transition between TX and RX through Battery Saving Status, it takes time to start the next operation because of the oscillation of XOSC to stop one moment.

6.9.3 Run → Battery Saving

TC32306FTG will move to Battery Saving by the setting of registers (h'0A[D7]ENB, h'0A[D7]ACT), ENB pin or RESET pin. In RX, it is possible to move to Battery Saving by the use of AutoOff function.

Notice:

- In TX, to move to Battery Saving under disabled PA is recommended. It may reduce unexpected signal transmission caused by the OFF timing gaps of each function blocks.

6.9.4 AutoOff Function

It is the function to move from Run (RX) to Battery Saving automatically without the register setting. AutoOff functions are the type A and B. These are valid when Signal Detections are enabled.

Notice:

- When to move to Battery Saving by AutoOff function, the value of registers (h'0A[D7]ENB, h'0A[D7]ACT) will not change. Output and check Status_MONI signal at DET_TMONI1 pin and/or DET_TMONI2 pin to confirm the transition to Battery Saving by this function.
- About the pins behavior at the transition to Battery Saving by AutoOff, see Table 5-2.

Table 6-49 AutoOff Function Settings and Status

h'10[D5] AutoOffA_en	h'10[D4] AutoOffB_en	AutoOff Type A	AutoOff Type B	Status
0	0	OFF	OFF	—
0	1	OFF	ON	Move to Battery Saving if the determination of "Signal Detection"(Det_out signal = "H") is not indicated within the timer period set by register:h'1D[D7:D0].
1	0	ON	OFF	Move to Battery Saving if the determination of "No Signal Detection" is indicated (Un_Det_out signal = "H").
1	1	ON	ON	Move to Battery Saving whichever earlier AutoOff Type A or Type B.

(1) AutoOff Type A (AutoOff by Signal Detections)

TC32306FTG will move from Run to Battery Saving if the determination of "No Signal Detection" is indicated (Un_Det_out signal = "H"). It is valid to set register:h'10[D5]AutoOffA_en = "1".

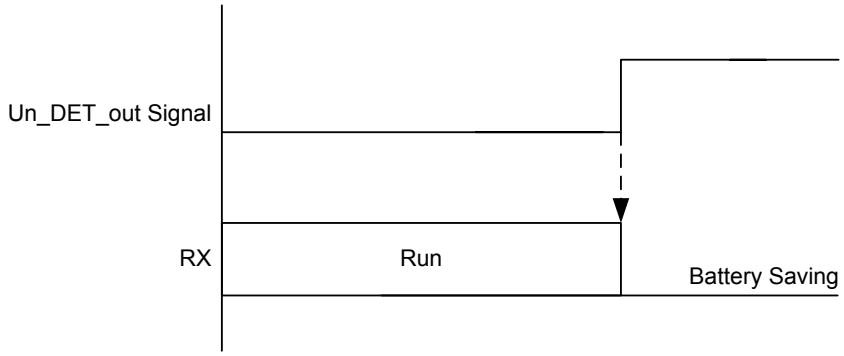


Fig 6-32 AutoOff Type A

* The example of timing chart may be omitted or simplified for explanatory purposes.

- Continuing RX in AutoOff Type A

When AutoOff Type A is valid, TC32306FTG will keep to be RX despite of the condition of Un_DET_out signal and DET_out signal, once after DET_out signal turns to be "H" before Un_DET_out signal turns to be "H". To release from the continuing RX, need to set new register and/or change RESET/ENB pin.

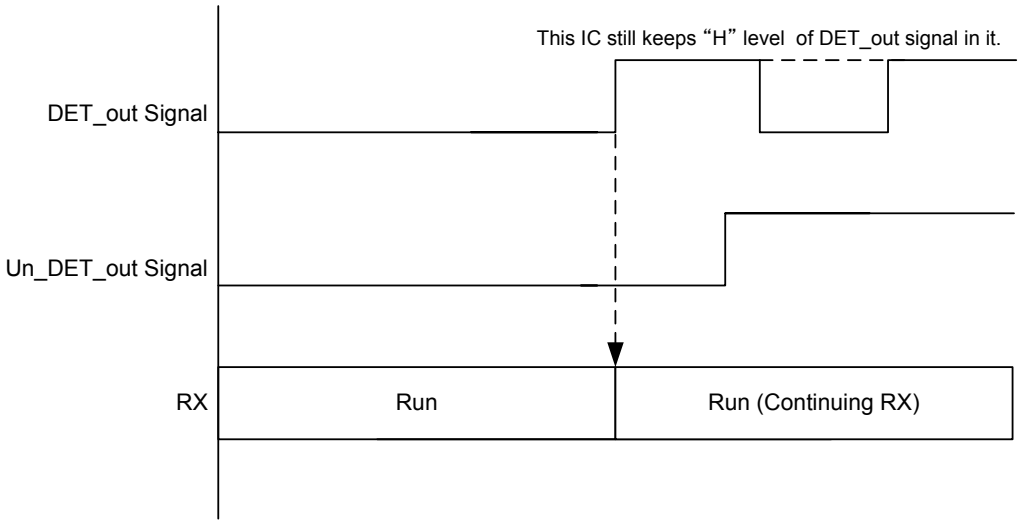


Fig 6-33 AutoOff Type A (Continuing RX)

* The example of timing chart may be omitted or simplified for explanatory purposes.

Notice:

- The function of AutoOff Type A is valid immediately after the register:h'10 is finished to write.
- To use AutoOff Type A again from Battery Saving which status caused by the operation of AutoOff Type A, set TC32306FTG status to Battery Saving or Standby by setting new registers and/or change RESET/ENB pin..
- To use AutoOff Type A again in the continuing RX, set this IC status to Battery Saving or Standby by setting new registers and/or change RESET/ENB pin.

(2) AutoOff Type B (AutoOff by Timer Setting)

TC32306FTG will move from Run to Battery Saving if the determination of "Signal Detection" (Det_out signal = "H") is not indicated within the timer period set by register. It is valid to set register:h'10[D4]AutoOffB_en = "1". The duration of Run (RX timer period) is set by the register:h'1D[D7:D0]Ontime7..0.

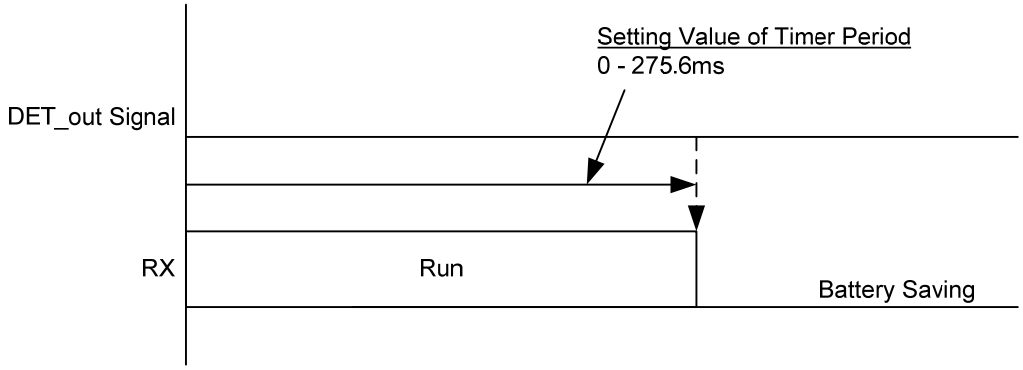


Fig 6-34 AutoOff Type B

* The example of timing chart may be omitted or simplified for explanatory purposes.

- Continuing AutoOff Type B

When AutoOff Type B is valid, TC32306FTG will stop the timer countdown and continue to be RX if DET_out signal turns to be "H" before the end of timer period set by register. After that, this IC keeps to be RX despite of the condition of DET_out signal. To move from continuing RX to Battery Saving, need to set new registers and/or change RESET/ENB pin.

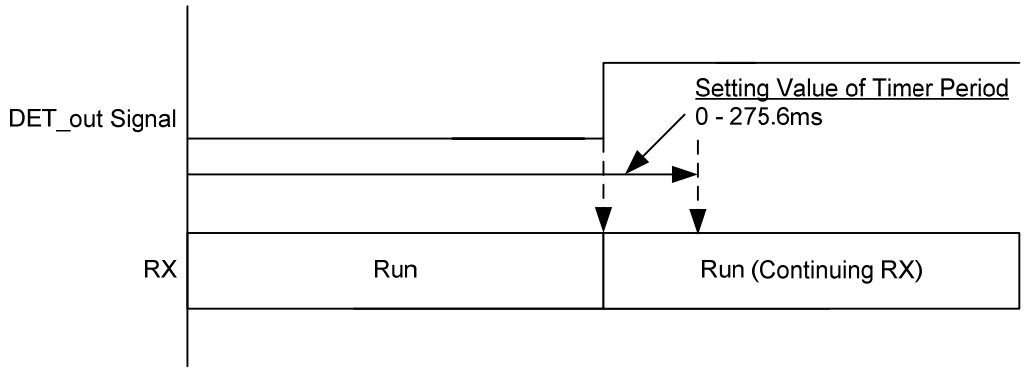


Fig 6-35 AutoOff Type B (Continuing RX)

* The example of timing chart may be omitted or simplified for explanatory purposes.

Notice:

- The timer period setting is derived from 30.32MHz Reference Clock Frequency.
- The timer period setting is valid after TC32306FTG moves from Battery Saving or Standby to Run.
- The timer countdown will start after about 0.06 ms from the start of internal setup, when this IC moves from Battery Saving or Standby to Run. The timer countdown will start immediately to finish register writing, if the setting of register:h'10 is valid in Run status.
- If the timer period is set to 0 ms, this IC will move to Battery Saving after the starting of timer countdown before RX.
- Renewal AutoOff Type B setting is invalid during the continuing RX, because the timer is not reset. This IC needs to move to Battery Saving or Standby to be reset and valid the timer function.
- In EEPROM Mode, the setting of the timer period is only 275.6 ms and cannot be set other value.

6.9.5 Change Settings during Run

The registers in Table 6-50 must have finished writing data before internal setup will start. When to change register settings after the internal setup has finished, do them in Battery Saving or Standby. About the internal setup, see section 6.9.1.

Table 6-50 Changing Register Prohibited during Run

Register	Location
Ndet_judg	h'19[D1]
Ntime1..0	h'1A [D7:D6]
DRSSI_judg	h'1A[D5]

The registers in Table 6-51 are valid by the transition from Battery Saving or Standby to Run. In SPI Mode, to be valid the register settings at the starting of TC32306FTG operation, set the registers during the status of Battery Saving or Standby then move to the status of Run.

Table 6-51 Register to be Valid by the Transition to Run

Register	Location
Delay2..0	h'0D[D6:D4]
Ontime7..0	h'1D[D7:D0]

6.10 Register Overview & Description

Available register's addresses in SPI Mode are "h'09-h'23", and these in EEPROM Mode are "h'0A-h'1C".

Table 6-52 Available Register Addresses

Code	Address AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	Type	Name	In EEPROM Mode
h'09	0	0	0	0	1	0	0	1	R / W	Software Reset	—
h'0A	0	0	0	0	1	0	1	0	R / W	General Settings	○
h'0B	0	0	0	0	1	0	1	1	R / W	Local Frequency Settings 1	○
h'0C	0	0	0	0	1	1	0	0	R / W	Local Frequency Settings 2	○
h'0D	0	0	0	0	1	1	0	1	R / W	Delay & Drive Settings	○
h'0E	0	0	0	0	1	1	1	0	R / W	RX LNA, IF Filter, BRF Settings	○
h'0F	0	0	0	0	1	1	1	1	R / W	RX Function Settings 1	○
h'10	0	0	0	1	0	0	0	0	R / W	RX Function Settings 2	○
h'11	0	0	0	1	0	0	0	1	R / W	Charge2 Threshold Setting	○
h'12	0	0	0	1	0	0	1	0	R / W	TX Deviation Setting	○
h'13	0	0	0	1	0	0	1	1	R / W	TX PA Settings	○
h'14	0	0	0	1	0	1	0	0	R / W	Monitor Settings1	○
h'15	0	0	0	1	0	1	0	1	R / W	Monitor Settings2	○
h'16	0	0	0	1	0	1	1	0	R / W	RSSI Threshold Setting	○
h'17	0	0	0	1	0	1	1	1	R / W	Preamble Detector Setting 1	○
h'18	0	0	0	1	1	0	0	0	R / W	Preamble Detector Settings 2	○
h'19	0	0	0	1	1	0	0	1	R / W	Noise Detector Threshold Setting	○
h'1A	0	0	0	1	1	0	1	0	R / W	Signal Detector Settings	○
h'1B	0	0	0	1	1	0	1	1	R / W	Comparator Settings	○
h'1C	0	0	0	1	1	1	0	0	R / W	Peak Hold Settings	○
h'1D	0	0	0	1	1	1	0	1	R / W	AutoOff Type B Setting	—
h'1E	0	0	0	1	1	1	1	0	R	Signal Detect and Lock Detect Monitors	—
h'1F	0	0	0	1	1	1	1	1	R	Peak Hold Level Monitor	—
h'20	0	0	1	0	0	0	0	0	R	Data Comparator Monitor 1	—
h'21	0	0	1	0	0	0	0	1	R	Data Comparator Monitor 2	—
h'22	0	0	1	0	0	0	1	0	R	RSSI Level Monitor	—
h'23	0	0	1	0	0	0	1	1	R	Noise Signal Level Monitor	—

Notice:

- "○": accessible register's addresses in EEPROM Mode
- R / W: Read and Write Register
- R: Read only Register

Table 6-53 View of Register Settings (Reset & Status Control)

Register Settings					Address
Software Reset					h'09[D7:D0]
	Reset	—			—
	Reset is Released	Output Current Drive Setting			h'0D[D3:D1]
		Status Control 1			h'0A[D7]
			Buttery Saving	—	—
			Run / Standby	Status Control 2	h'0A[D6]
				Standby	—
				Run	→ See next table

Notice)

- "h'09" shows register's byte is "09" by hexadecimal, and [D7:D0] shows bit number are from the 7th- to the 0.

Table 6-54 View of Register Settings (In Run Status)

Register Settings						Address
Antenna Switch Control						h'0A[D3:D2]
Monitors						h'14[D6:D4], h'14[D2:D0]
	Except DET_out Signal	—				—
	DET_out Signal	DET_out Signal Output Control				h'10[D2]
User Test						h'10[D3]
	Normal	—				—
	User Test	Monitor Signal Output				h'15[D6:D4], h'15[D2:D0]
Delay Setting Enable / Disable						h'0D[D7]
	Disable	—				—
	Enable	Delay Time				h'0D[D6:D4]
RF Frequency Band						h'0A[D1:D0]
Local Frequency						h'0B[D7:D0], h'0C[D7:D0]
RX & TX						h'0A[D5]
	RX	LNA Gain				h'0E[D7:D6]
		IF Filter Bandwidth				h'0E[D5]
		Demodulation				→ See next table
		Bit Rate Filter Cutoff Frequency				h'0E[D4:D1]
		Data Comparator Reference Voltage Charge Coefficient				h'1B[D5:D3]
		Data Comparator Quick Charge 1 Enable / Disable				h'10[D7]
		Data Comparator Quick Charge 2 Enable / Disable				h'10[D6]
			Disable	—		—
			Enable	Quick Charge Coefficient		h'1B[D7:D6]
				Quick Charge 2 Threshold Level		h'11[D7:D0]
		DATA_IO Control				h'0F[D3]
		AutoOff Type A Enable / Disable				h'10[D5]
		AutoOff Type B Enable / Disable				h'10[D4]
			Disable	—		—
			Enable	Duration		h'1D[D7:D0]
	TX	PA Control				h'13[D1]
			Disable	—		—
			Enable	Modulation		h'0A[D4]
					FSK Deviation	h'12[D7:D2]
					ASK —	—
				Output Level (Coarse)		h'13[D3:D2]
				Output Level (Fine)		h'13[D7:D4]

Table 6-55 View of Register Settings (Detections Overall)

Register Settings					Address
Demodulation（FSK / ASK）					h'0A[D4]
FSK	NIR (Near Interference Rejection) Filter Enable / Disable				h'10[D1]
		Disable	—		—
		Enable	NIR Filter Frequency Control		h'1B[D2:D1]
			NIR Parameters(Recommended)		h'0D[D0], h'0F[D0], h'12[D1:D0], h'13[D0], h'1A[D0], h'1B[D0], h'1C[D2:D0]
	IF Detection				h'10[D0]
		Delay Detection	High Frequency Detector Enable / Disable		h'0F[D4]
			Disable	—	—
			Enable	High Frequency Detector AutoOff	h'1A[D1]
		Pulse Count Detection			—
	Noise Detection Enable / Disable				h'0F[D5]
		Disable	Noise Addition by High Frequency Detector		h'19[D0]
		Enable	Threshold Level of Detection		h'19[D7:D2]
			Number of Times for Judgment		h'19[D1]
			Detection Interval		h'1A[D7:D6]
			Noise Addition by High Frequency Detector		h'19[D0]
	RSSI Detection Enable / Disable				h'0F[D7]
		Disable	—		—
		Enable	Threshold Level of Detection		h'16[D7:D0]
			Number of Times for Judgment		h'1A[D5]
			Detection Interval		h'1A[D7:D6]
	Preamble Detection Enable / Disable				h'0F[D6]
		Disable	—		—
		Enable	Preamble Signal Cycle		h'17[D7:D0], h'18[D7]
			Error Margin		h'18[D6:D0]
			Number of Times for Judgment		h'1A[D4:D3]
			Detection Trigger		h'1A[D2]
ASK	Data Comparator Quick Charge 2 Enable / Disable				h'10[D6]
		Disable	—		—
		Enable	Limiter (Peak Hold Voltage Discharge Coefficient)		h'1C[D7:D5]
			Limiter (Peak Hold Voltage Charge Coefficient)		h'1C[D4:D3]
	RSSI Detection Enable / Disable				h'0F[D7]
		Disable	—		—
		Enable	Threshold Level of Detection		h'16[D7:D0]
			Number of Times for Judgment		h'1A[D5]
			Detection Interval		h'1A[D7:D6]
	Preamble Detection Enable / Disable				h'0F[D6]
		Disable	—		—
		Enable	Threshold Level of Detection		h'17[D7:D0], h'18[D7]
			Number of Times for Judgment		h'18[D6:D0]
			Detection Interval		h'1A[D4:D3]
			Detection Trigger		h'1A[D2]

6.10.1 h'09 Software Reset

Table 6-56 Register (h'09)

	D7	D6	D5	D4	D3	D2	D1	D0
Name	RESET7	RESET6	RESET5	RESET4	RESET3	RESET2	RESET1	RESET0
Initial	0	0	0	0	0	0	0	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Set register:[D7:D0] = b'01010101 : Initialize Register
- Others: Not Initialize

After entering register:[D0] data, TC32306FTG becomes Reset status, and then the reset is released whichever faster the rising edge of next SPI-Clock signal or the rising edge of next SPI-CS signal. Set this IC to SPI Read, this IC outputs register's data "b'00000000". Set this IC to SPI Confirmation Write, then this IC outputs registers' data written just before.

6.10.2 h'0A General Settings

Table 6-57 Register (h'0A)

	D7	D6	D5	D4	D3	D2	D1	D0
Name	ENB	ACT	RX_TX	FSK_ASK	TX_SW	RX_SW	BAND1	BAND0
Initial	0	1	0	0	0	0	0	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[D7]ENB [Status Control 1]

The combinations of this register and register:[D6] result as the right table.

In SPI Mode, ENB pin = "H" leads these settings are valid and ENB pin = "L" leads TC32306FTG is Battery Saving Status.

[D6]ACT [Status Control 2]

The combinations of this register and register:[D7] result as the right table.

In SPI Mode, ENB pin = "H" leads these settings are valid and ENB pin = "L" leads TC32306FTG is Battery Saving Status.

[D7]ENB	[D6]ACT	Status
0	X	Battery Saving
1	0	Standby
1	1	Run

X: Don't care

[D5]RX_TX [RX / TX]

0: Receiving // 1: Transmitting

[D4]FSK_ASK [Modulation & Demodulation]

0: FSK / 1: ASK

[D3]TX_SW [Antenna Switch Control (TX)]

0: TX_SW pin = "L" / 1: TX_SW pin = "H"

In SPI Mode, this register result as the right table.

In EEPROM Mode, these settings are invalid.

[D2]RX_SW [Antenna Switch Control (RX)]

0: RX_SW pin = "L" / 1: RX_SW pin = "H"

In SPI Mode, this register result as the right table.

In EEPROM Mode, these settings are invalid.

[D3]TX_SW [D2]RX_SW	Status	TX_SW Pin RX_SW Pin
X	Except Run / Standby	L
0	Run / Standby	L
1	Run / Standby	H

X: Don't care

L: Pull Down

[D1:D0]BAND1..0 [RF Frequency Band]

[D1:D0] = b'00: 315 MHz

[D1:D0] = b'01: 434 MHz

[D1:D0] = b'10: 868 / 915 MHz

[D1:D0] = b'11: 868 / 915 MHz

6.10.3 h'0B Local Frequency Settings 1

Table 6-58 Register (h'0B)

	D7	D6	D5	D4	D3	D2	D1	D0
Name	NC3	NC2	NC1	NC0	FC11	FC10	FC9	FC8
Initial	1	0	0	1	0	0	1	1
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[D7:D4]NC3..0 [Local Frequency : Integer Counter]
$NC = 2^3 \times NC3 + 2^2 \times NC2 + 2^1 \times NC1 + 2^0 \times NC0$
Initial Value: NC = 9

h'0C [D7:D0]FC7..0 & h'0B [D3:D0]FC11..8 [Local Frequency : Fractional Counter]
$FC = -2^{11} \times FC11 + 2^{10} \times FC10 + 2^9 \times FC9 + 2^8 \times FC8 + 2^7 \times FC7 + 2^6 \times FC6 + 2^5 \times FC5 + 2^4 \times FC4 + 2^3 \times FC3 + 2^2 \times FC2 + 2^1 \times FC1 + 2^0 \times FC0$
Initial Value: FC = 1016 (Two's complement format)
Must set the FC value between -1516 to +1515.

Example)
VCO frequency "fvco" is set as follows.
fvco = (NC+53) x fosc + FC x fstep
fvco: VCO Frequency
fosc: Reference Clock Frequency (30.32MHz)
fstep: Frequency Step (= fosc / 3032)

<Case of setting fvco = 1890MHz>
fvco = 1890MHz / fosc = 30.32MHz / fstep = 10kHz (= 3032 / 30.32MHz)
NC = fvco / fosc – 53 = 1890MHz / 30.32MHz – 53 = 9.335 → C = 9 (This number is rounded to an integer.)

FC = fvco / fosc – (NC+53)) x fosc / fstep
= (1890MHz / 30.32MHz – (9+53)) x 30.32MHz / 10kHz = 1016

NC = 9 → NC = "b'1001" (Binary)
FC = 1016 → FC = "b'001111111000" (Two's complement format)

Notice: The change of "fosc" results the change of "fvco" in the same NC and FC.

6.10.4 h'0C Local Frequency Settings 2

Table 6-59 Register (h'0C)

	D7	D6	D5	D4	D3	D2	D1	D0
Name	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0
Initial	1	1	1	1	1	0	0	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[D7:D0]FC7..0 [Local Frequency : Fractional Counter]
See register h'0B section.

6.10.5 h'0D Delay & Drive Functions

Table 6-60 Register (h'0D)

	D7	D6	D5	D4	D3	D2	D1	D0
Name	Delay_en	Delay2	Delay1	Delay0	DATA_IO_D	MISO_D	TMONI_D	NIR_H2
Initial	0	0	0	0	0	0	0	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[D7]Delay_en [Delay Setting]

0: Disable fixed as 105.5us

1: Enable set by [D6:D4]Delay_2..0

[D6:D4]delay_2..0 [Delay Time]

TC32306FTG status changes from Battery Saving / Standby to Run, then this IC starts operation with this delay time when the register:[D7]Delay_en value is "1".

[D6:D4] = b'000: Delay Time = 105.5us

[D6:D4] = b'001: Delay Time = 211.1us

[D6:D4] = b'010: Delay Time = 316.5us

[D6:D4] = b'011: Delay Time = 527.5us

[D6:D4] = b'100: Delay Time = 949.5us

Other: Delay Time = 105.5us

Notice:

To start TC32306FTG with this delay time, changing the status from Battery Saving / Standby to Run after setting this register. If this register is set during Run, this register setting will be valid after the next transition from Battery Saving / Standby to Run.

[D3]DATA_IO_D [DATA_IO Output Drive Setting]

0: Low / 1:High

[D2]MISO_D [MISO Output Drive Setting]

0: Low / 1:High

[D1]TMONI_D [DET_TMONI1 / DET_TMONI2 Output Drive Setting]

0: Low / 1:High

[D0] NIR_H2

Notice: When to use NIR filter (h'10[D1]NIR_Fil_en = "1"), Set this register "0". (Recommended Value)

6.10.6 h'0E RX LNA, IF Filter, BRF Settings

Table 6-61 Register (h'0E)

	D7	D6	D5	D4	D3	D2	D1	D0
Name	Lna_gain1	Lna_gain0	IFBW	BRF_Bit3	BRF_Bit2	BRF_Bit1	BRF_Bit0	—
Initial	0	0	0	1	0	0	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[D7:D6]Lna_gain1..0 [LNA Gain]

LNA gain depends on RF frequency band.

[D7:D6] = b'00: LNA Gain = Minimum Setting

[D7:D6] = b'11: LNA Gain = Maximum Setting

[D5]IFBW [IF Filter Bandwidth]

[D5]IFBW	IF Filter Bandwidth	IF Frequency
0	320kHz	230kHz
1	270kHz	280kHz

Change IF Frequency depends on IF Filter Bandwidth.

[D4:D1]BRF_Bit3..0 [Bit Rate Filter Cutoff Frequency]
For details, see Table 6-25.

[D0] Unused bit.
Set to “0”.

6.10.7 h’0F RX Function Settings 1

Table 6-62 Register (h’0F)

	D7	D6	D5	D4	D3	D2	D1	D0
Name	Drssi_en	Preamble_ en	Ndet_en	Hdet_en	Dataout_ cnt_en	Digital_en	Det_reset_n	NIR_L2
Initial	0	0	0	0	0	1	1	1
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[D7]Drssi_en [RSSI Detection]
0: Disable / 1: Enable

[D6]Preamble_en [Preamble Detection]
0: Disable / 1: Enable

[D5]Ndet_en [Noise Detection]
0: Disable / 1: Enable

[D4] Hdet_en [High Frequency Detector]
In Delay Detection (h'10[D0]Sel_Det = "0"), this register setting is valid.
0: Disable / 1: Enable

[D3]Dataout_cnt_en [DATA_IO Control]
0: Disable / 1: Enable

[D2]Digital_en [Digital Block Control]
Digital Block (Detctor, LPF(ASK), LPF(FSK), BRF, Data COMP) Control
0: Disable / 1: Enable

[D1]Det_reset_n [Detection Reset (RSSI Detection / Noise Detection / Preamble Detection)]
0: Detection Reset (Auto resume)
1: Reset is released

Notice:
These detections are reset after writing all the registers in this address.
The function is resumed automatically at the rising edge of CS signal after setting this register.
TC32306FTG always outputs previous input value of the register whichever the auto resume or not,
(If this register is written to "0", the register outputs "0", after that auto resume.)

[D0] NIR_L2
When to use NIR filter (h'10[D1]NIR_Fil_en = "1"), Set this register "1". (Recommended Value)

6.10.8 h'10 RX Function Settings 2

Table 6-63 Register (h'10)

	D7	D6	D5	D4	D3	D2	D1	D0
Name	Charge1_en	Charge2_en	AutoOffA_ en	AutoOffB_ en	USER_ TEST	DET_out_ cnt_en	NIR_Fil_en	Sel_Det
Initial	0	1	0	0	0	1	0	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[D7]Charge1_en [Data Comparator Quick Charge 1]
0: Disable / 1: Enable

[D6]Charge2_en [Data Comparator Quick Charge 2]
0: Disable / 1: Enable

[D5]AutoOffA_en [AutoOff Type A]
0: Disable / 1: Enable

[D4] AutoOffB_en [AutoOff Type B]
0: Disable / 1: Enable

[D3]USER_TEST [User Test]
0: Disable / 1: Enable (Internal monitor signals output from DET_TMONI3 / DET_TMONI4 Pin.)

[D2]Det_out_cnt_en [DET_out Signal Output Control]
0: Disable / 1: Enable

[D1]NIR_Fil_en [NIR (Near Interference Rejection) Filter Control]
When to use FSK Demodulation (h'0A[D4]FSK_ASK = "0"), this setting is valid.
0: Disable / 1: Enable

[D0] Sel_Det [IF Detection Select]
When to use FSK Demodulation (h'0A[D4]FSK_ASK = "0"), this setting is valid.
0: Delay Detection / 1: Pulse Count Detection

6.10.9 h'11 Charge2 Threshold Setting

Table 6-64 Register (h'11)

	D7	D6	D5	D4	D3	D2	D1	D0
Name	Charge2_ Th7	Charge2_ Th6	Charge2_ Th5	Charge2_ Th4	Charge2_ Th3	Charge2_ Th2	Charge2_ Th1	Charge2_ Th0
Initial	0	0	1	1	1	1	0	1
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[D7:D0]Charge2_Th7..0 [Quick Charge 2 Threshold Level]

When to set Data Comparator Quick Charge 2 (h'10[D6]Charge2_en = "1") and FSK Demodulation (h'0A[D4]FSK_ASK = "0"), this setting is valid.

In ASK Demodulation (h'0A[D4]FSK_ASK = "1"), input to this register is invalid, because the threshold level is automatically set.

- Setting Range

[D7:D0] = 0 - 255 (b'00000000 – b'11111111)

Initial Value: 61 (b'00111101)

For details, see section 6.5.9.

Notice: In ASK Demodulation (h'0A[D4]FSK_ASK = "1"), the value of that threshold level for automatically setting can not be read.

6.10.10 h'12 TX Deviation Setting

Table 6-65 Register (h'12)

	D7	D6	D5	D4	D3	D2	D1	D0
Name	Dev5	Dev4	Dev3	Dev2	Dev1	Dev0	NIR_2H1	NIR_2H0
Initial	0	0	1	1	0	0	0	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[D7:D2]Dev5..0 [Deviation]

This deviation depends on the setting of RF frequency band.

- Setting Range

[D7:D2] = 0 – 63 (b'000000 – 111111)

Initial Value: 12 (b'001100)

- Deviation Setting Range at 30.32MHz Reference Clock Frequency.

315 MHz : Unmodulated, from +/-1.67kHz to +/-105kHz

434 MHz : Unmodulated, from +/-2.5kHz to +/-157.5kHz

868 / 915 MHz : Unmodulated, from +/-5kHz to +/-315kHz

Notice: When to set this register value to "0", RF output signal is unmodulated.

Example)

Deviation: +/-dev = fd × n / nd

fd: Frequency Resolution of VCO 10kHz (= fosc / 3032) * fosc: Reference Clock Frequency (30.32MHz)

nd: Division Ratio (nd = 6 at 315MHz Band, nd = 4 at 434MHz Band nd = 2 at 868 / 915MHz Band)

n: value of register:[D7:D2]Dev5..0 (Converted to decimal)

Notice:

In ASK, this register setting is invalid.

The change of "fosc" results the change of deviation.

[D1] NIR_2H1

When to use NIR filter (h'10[D1]NIR_Fil_en = "1"), Set this register "0". (Recommended Value)

[D0] NIR_2H0

When to use NIR filter (h'10[D1]NIR_Fil_en = "1"), Set this register "0". (Recommended Value)

6.10.11h'13 TX PA Settings

Table 6-66 Register (h'13)

	D7	D6	D5	D4	D3	D2	D1	D0
Name	TX _ subgain3	TX _ subgain2	TX _ subgain1	TX _ subgain1	TX_gain1	TX_gain0	PA_en	NIR_H1
Initial	1	1	1	1	1	1	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[D7:D4] TX_subgain3..0 [Output Level (Fine)]

The output level depends on RF frequency band.

[D7:D4] = b'0000: Minimum

[D7:D4] = b'1111: Maximum

[D3:D2] TX_gain1..0 [Output Level (Coarse)]

The output level depends on RF frequency band.

[D3:D2] = b'00: Minimum

[D3:D2] = b'11: Maximum

[D1]PA_en [PA Enable / Disable]

The combination register:h'0A[D5]RX_TX and Internal LD Signal (The result of PLL lock detection: see below) results the operation of PA in the below table.

h'0A[D5] RX_TX	[D1]PA_en	Internal LD Signal	PA Function
0	X	X	Disable
1	X	L	Disable
1	0	X	Disable
1	1	H	Enable

X: Don't care

Internal LD Signal is only use for PA, and the signal keeps "H" after the first rising edge of PLL_LD Signal. Above function is only available in TX and the Internal LD Signal can not be monitored. To release the signal holding state, set one of the follows.

- Set TC32306FTG in the status of Battery Saving or Standby.
- Change from TX to RX.
- Change TX modulation. (ASK ↔ FSK)
- Change RF frequency. (In the change in the value of register "h'0B" and/or "h'0C")
- Change the value of register:h'12[D7:D2] for TX deviation. (This is only valid in FSK setting (h'0A[D4]FSK_ASK = "0"))

[D0] NIR_H1

When to use NIR filter (h'10[D1]NIR_Fil_en = "1"), Set this register "0". (Recommended Value)

6.10.12 h'14 Monitor Settings1

Table 6-67 Register (h'14)

	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved	MONI1_ SEL2	MONI1_ SEL1	MONI1_ SEL0	Reserved	MONI2_ SEL2	MONI2_ SEL1	MONI2_ SEL0
Initial	0	0	0	0	0	0	0	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[D7] Reserved.
Set the value "0".

[D6:D4] MONI1_SEL2..0 [DET_TMONI1 Pin Output]

[D6] MONI1_SEL2	[D5] MONI1_SEL1	[D4] MONI1_SEL0	Signal Name	Description
0	0	0	—	Low level output
0	0	1	DET_out	The result of "Signal Detection"
0	1	0	Preamble_DET_ out	The result of Preamble detection
0	1	1	RSSI_DET_out	The result of RSSI detection
1	0	0	NDET_out	The result of Noise detection
1	0	1	Status_MONI	TC32306FTG status (Standby, Run) / Battery Saving
1	1	0	Un_DET_out	The result of "No Signal Detection"
1	1	1	PLL_LD	The result of PLL lock detection

[D3] Reserved.
Set the value "0".

[D2:D0]MONI2_SEL2..0 [DET_TMONI2 Pin Output]

[D2] MONI2_SEL2	[D1] MONI2_SEL1	[D0] MONI2_SEL0	Signal Name	Description
0	0	0	—	Low level output
0	0	1	DET_out	The result of "Signal Detection"
0	1	0	Preamble_DET_ out	The result of Preamble detection
0	1	1	RSSI_DET_out	The result of RSSI detection
1	0	0	NDET_out	The result of Noise detection
1	0	1	Status_MONI	TC32306FTG status (Standby, Run) / Battery Saving
1	1	0	Un_DET_out	The result of "No Signal Detection"
1	1	1	PLL_LD	The result of PLL lock detection

6.10.13 h'15 Monitor Settings2

Table 6-68 Register (h'15)

	D7	D6	D5	D4	D3	D2	D1	D0
Name	—	MONI3_ SEL2	MONI3_ SEL1	MONI3_ SEL0	—	MONI4_ SEL2	MONI4_ SEL1	MONI4_ SEL0
Initial	0	0	0	0	0	0	0	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[D7] Unused bit.
Set the value "0".

[D6:D4]MONI3_SEL2..0 [DET_TMONI3 Pin Output]
When to select User Test (h'10[D3]USER_TEST = "1" and/or MODE1 pin = "H"), these settings are valid.

[D6] MONI3_SEL2	[D5] MONI3_SEL1	[D4] MONI3_SEL0	Signal Name	Description
0	0	0	BRF_out	Bit Rate Filter output signal
0	0	1	BRF_in	Bit Rate Filter input signal
0	1	0	Data_compREF	Data Comparator Reference voltage
0	1	1	DRSSI_out	RSSI output voltage (After the digital to analog conversion)
1	0	0	Noise _out	Noise detection output voltage
1	0	1	Peak_out	Peak hold voltage of Peak Hold Circuit
1	1	0	—	Low level output
1	1	1	—	Low level output

[D3] Unused bit.
Set the value "0".

[D2:D0]MONI4_SEL2..0 [DET_TMONI4 Pin Output]
When to select User Test (h'10[D3]USER_TEST = "0" and/or MODE1 pin = "H"), these settings are valid.

[D2] MONI4_SEL2	[D1] MONI4_SEL1	[D0] MONI4_SEL0	Signal Name	Description
0	0	0	Data_compREF	Data Comparator Reference voltage
0	0	1	BRF_in	Bit Rate Filter input signal
0	1	0	BRF_out	Bit Rate Filter output signal
0	1	1	DRSSI_out	RSSI output voltage (After the digital to analog conversion)
1	0	0	Noise _out	Noise detection output voltage
1	0	1	Peak_out	Peak hold voltage of Peak Hold Circuit
1	1	0	—	Low level output
1	1	1	—	Low level output

6.10.14 h'16 RSSI Threshold Setting

Table 6-69 Register (h'16)

	D7	D6	D5	D4	D3	D2	D1	D0
Name	DRSSI_Th7	DRSSI_Th6	DRSSI_Th5	DRSSI_Th4	DRSSI_Th3	DRSSI_Th2	DRSSI_Th1	DRSSI_Th0
Initial	0	0	0	0	0	0	0	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[D7:D0]DRSSI_Th7..0 [RSSI Threshold Level of Detection]

- Setting Range
[D7:D0] = 0 – 255 (b'00000000 – b'11111111)
Initial Value: 0

To set RSSI threshold level of detection, refer the value of "h'22[D7:D0] RSSI Level Monitor".

6.10.15 h'17 Preamble Detector Setting 1

Table 6-70 Register (h'17)

	D7	D6	D5	D4	D3	D2	D1	D0
Name	Pre_Time7	Pre_Time6	Pre_Time5	Pre_Time4	Pre_Time3	Pre_Time2	Pre_Time1	Pre_Time0
Initial	1	0	0	1	1	1	1	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

h'18[D7] & h'17[D7:D0]Pre_Time8..0 [Preamble Signal Cycle]
When to set Preamble detection (h'0F[D6]Preamble_en = "1"), this setting is valid.

- Setting Range
h'18[D8] & h'17[D7:D0] = 0 – 511 (b'000000000 - b'111111111)
Initial Value: 158(b'010011110)

See section 6.5.6 about the Function of Preamble detection.

Notice: The cutoff frequency of Bit Rate Filter is derived from 30.32MHz Reference Clock Frequency.

6.10.16 h'18 Preamble Detector Settings 2

Table 6-71 Register (h'18)

	D7	D6	D5	D4	D3	D2	D1	D0
Name	Pre_Time8	Err_Margin6	Err_Margin5	Err_Margin4	Err_Margin3	Err_Margin2	Err_Margin1	Err_Margin0
Initial	0	0	0	0	0	1	0	1
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[D7]Pre_Time8 [Preamble Signal Cycle]
See register h'17.

[D6:D0]Err_Margin6..0 [Error Margin]
When to set Preamble detection (h'0F[D6]Preamble_en = "1"), this setting is valid.

- Setting Range
[D6:D0] = 0 – 127 (b'0000000 – b'1111111)
Initial Value: 5 (b'0000101)

See section 6.5.6 about the Function of Preamble Detection.

Notice: The cutoff frequency of Bit Rate Filter is derived from 30.32MHz Reference Clock Frequency.

6.10.17 h'19 Noise Detector Threshold Setting

Table 6-72 Register (h'19)

	D7	D6	D5	D4	D3	D2	D1	D0
Name	Ndet_Th5	Ndet_Th4	Ndet_Th3	Ndet_Th2	Ndet_Th1	Ndet_Th0	Ndet_Judg	Add_Hdet_en
Initial	0	0	0	0	0	0	0	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[D7:D2] Ndet_Th5..0 [Noise Detector Threshold Level of Detection]
When to set FSK Demodulation (h'0A[D4]FSK_ASK = "0") and Noise Detection (h'0F[D5] Ndet_en = "1"), this setting is valid.

- Setting Range
[D7:D2] = 0 – 63 (b'000000 – b'111111)
Initial Value: 0

To set Noise Detector threshold level, refer the value of "h'23[D7:D0] Noise Signal Level Monitor".

[D1] Ndet_Judg [Noise Detection Number of Times for Judgment]
0: Judged by a single detection. / 1: Judged by twice detections in succession.

Notice:
To be valid the setting of this register setting, finish writing the value to this register before the internal setup will start. When the internal setup has finished and TC32306FTG is Run status, move this IC status to Battery Saving / Standby and change this register value.

[D0] Add_Hdet_en [Noise Addition by High Frequency Detector]
0: Disable / 1: Enable

6.10.18 h'1A Signal Detector Settings

Table 6-73 Register (h'1A)

	D7	D6	D5	D4	D3	D2	D1	D0
Name	Ntime1	Ntime0	DRSSI_judg	Pre_ DetCount1	Pre_ DetCount0	Pre_DetTrig	Auto_Hdet_ Off	NIR_H0
Initial	1	0	0	1	0	0	0	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[D7:D6]Ntime1..0 [Detection Interval]

Set the interval Noise Detection and RSSI Detection.

[D7]Ntime1	[D6]Ntime0	n	Judgment Interval (tdet)
0	0	1	0.338ms
0	1	2	0.675ms
1	0	4	1.35 ms
1	1	8	2.70ms

tdet: Detection Interval, fosc: Reference Clock Frequency (30.32MHz)

n: Coefficient determined by the setting of "[D7:D6]Ntime1..0"

tdet = n×1/((fosc / 256) / 40) sec

Notice:

This tdet value in above table is derived from 30.32MHz Reference Clock Frequency.

To be valid the setting of this register setting, finish writing the value to this register before the internal setup will start. When the internal setup has finished and TC32306FTG is Run status, move this IC status to Battery Saving / Standby and change this register value.

[D5]DRSSI_judg [RSSI Detection Number of Times for Judgement]

0: judged by a single detection / 1: Judged by twice detection in succession

Notice:

To be valid the setting of this register setting, finish writing the value to this register before the internal setup will start. When the internal setup has finished and TC32306FTG is Run status, move this IC status to Battery Saving / Standby and change this register value.

[D4:D3]Pre_DetCount1..0 [Preamble Detection Number of Times for Judgment]

- Judged "Detection" by continuous detection within the error margin.
- Judged "No Detection" by continuous detection outside the error margin.

[D2]Pre_DetTrig [Preamble Detection Trigger]

0: Judged by period (Checked at the rising edge of the signal)

1: Judged by bit (Checked both rising and falling edge of the signal)

[D4] Pre_DetCount1	[D3] Pre_DetCount0	[D2] Pre_DetTrig	Judgment Criteria
0	0	0	3 Period
0	0	1	6 Bit
0	1	0	4 Period
0	1	1	8 Bit
1	0	0	5 Period (Initial)
1	0	1	10 Bit
1	1	0	6 Period
1	1	1	12 Bit

[D1] Auto_Hdet_Off [High Frequency Detector AutoOff]

When to set High Frequency Detection (h'0F[D4] Hdet_en = "1"), this setting is valid.

0: Disable / 1: Enable

[D0] NIR_H0

When to use NIR filter (h'10[D1]NIR_Fil_en = "1"), Set this register "0". (Recommended Value)

6.10.19 h'1B Data Comparator Settings

Table 6-74 Register (h'1B)

	D7	D6	D5	D4	D3	D2	D1	D0
Name	Charge2_ Ref1	Charge2_ Ref0	Cmp_Ref2	Cmp_Ref1	Cmp_Ref0	NIR_Frqth1	NIR_Frqth0	NIR_2L1
Initial	0	1	1	0	0	0	0	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[D7:D6]Charge2_Ref1..0 [Data Comparator Quick Charge Coefficient]

When to set Data Comparator Quick Charge 2 (h'10[D6]Charge2_en = "1"), this setting is valid. Set the tracking time constant τ of the data comparator reference voltage (vref). This is valid only if an absolute value of the difference between vref and vi (Data comparator input voltage) will be greater than the threshold level set by register:h'11[D7:D0]Charge2_Th7..0".

tracking time constant τ: τ = nc' / fbc

nc': Inverse of "(1/nr)+(1/nc)"

nc: Setting value of this register:Charge2_Ref1..0 (Refer to the table below.)

nr: Setting value of this register:[D5:D3]Cmp_Ref2..0

fbc: Internal clock signal frequency depends on Bit Rate Filter register:h'0E [D4:D1]BRF_Bit3..0

[D7]Charge2_Ref1	[D6]Charge2_Ref0	1/nc	nc
0	0	1/4	4
0	1	1/8	8
1	0	1/16	16
1	1	1/32	32

See section 6.5.9 about Data Comparator Quick Charge 2.

Notice: The cutoff frequency of Bit Rate Filter is derived from 30.32MHz Reference Clock Frequency.

[D5:D3]Cmp_Ref2..0 [Data Comparator reference Level]

Set the tracking time constant τ under the following conditions.

1. No use of Data Comparator Quick Charge 1 & 2

2. Certain time has spent after starting Data Comparator Quick Charge 1.

3. An absolute value of the difference between vref and vi (Data comparator input voltage) will be less than the threshold level set by register:h'11[D7:D0]Charge2_Th7..0.

tracking time constant τ: τ = nr / fbc

nr: Setting value of this register:[D5:D3]Cmp_Ref2..0 (Refer to the table below.)

fbc: Internal clock signal frequency depends on Bit Rate Filter register:h'0E [D4:D1]BRF_Bit3..0

[D5]Cmp_Ref2	[D4]Cmp_Ref1	[D3]Cmp_Ref0	1/nr	nr
0	0	0	1/128	128
0	0	1	1/256+1/512	170. 7
0	1	0	1/256	256
0	1	1	1/512+1/1024	341.3
1	0	0	1/512	512
1	0	1	1/1024+1/2048	682. 7
1	1	0	1/1024	1024
1	1	1	1/2048+1/4096	1365.3

See section 6.5.9 about Data Comparator Reference Voltage.

Notice: The cutoff frequency of Bit Rate Filter is derived from 30.32MHz Reference Clock Frequency.

[D2:D1] NIR_Frqth1..0 [NIR Filter Frequency Control]

[D1:D0] = b'00: 631 kHz (Recommended Value)

[D1:D0] = b'01: 659 kHz

[D1:D0] = b'10: 689 kHz

[D1:D0] = b'11: 712 kHz

[D0] NIR_2L1

When to use NIR filter (h'10[D1]NIR_Fil_en = "1"), Set this register "1". (Recommended Value)

* The value is not equal to initial value, so must change the value to use NIR filter.

6.10.20 h'1C Peak Hold Settings

Table 6-75 Register (h'1C)

	D7	D6	D5	D4	D3	D2	D1	D0
Name	Peak_Ref2	Peak_Ref1	Peak_Ref0	Peak_ Charge1	Peak_ Charge0	NIR_2L0	NIR_L1	NIR_L0
Initial	1	0	0	0	1	0	0	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[D7:D5] Peak_Ref2..0 [Limiter (Peak Hold Voltage Discharge Coefficient)]

When to set ASK Demodulation (h'0A[D4]FSK_ASK = "1") and Data Comparator Quick Charge 2 (h'10[D6]Charge2_en = "1"), this setting is valid. Set the discharge time constant of Peak Hold circuit.

Discharge time constant τ: τ = tr / fbc

tr: Setting value of this register:Peak_Ref2..0 (Refer to the table below.)

fbc: Internal clock signal frequency depends on Bit Rate Filter register:h'0E [D4:D1]BRF_Bit3..0

[D7]Peak_Ref2	[D6]Peak_Ref1	[D5]Peak_Ref0	1/tr	tr
0	0	0	1/64	64
0	0	1	1/128+1/256	85.3
0	1	0	1/128	128
0	1	1	1/256+1/512	170.7
1	0	0	1/256	256
1	0	1	1/512+1/1024	341.3
1	1	0	1/512	512
1	1	1	1/1024+1/2048	682.7

See section 6.5.7 about Peak Hold circuit.

Notice: The cutoff frequency of Bit Rate Filter is derived from 30.32MHz Reference Clock Frequency.

[D4:D3] Peak_Charge1..0 [Limiter (Peak Hold Voltage Charge Coefficient)]

When to set ASK Demodulation (h'0A[D4]FSK_ASK = "1") and Data Comparator Quick Charge 2 (h'10[D6]Charge2_en = "1"), this setting is valid. Set the charging time constant peak tracking of Peak Hold circuit.

Charge time constant peak tracking τ: τ = tp' / fbc

tp': Inverse of "(1/tp)+(1/tr)"

tp: Setting value of this register:Peak_Charge1..0 (Refer to the table below.)

tr: Setting value of this register:Peak_Ref2..0

fbc: Internal clock signal frequency depends on Bit Rate Filter register:h'0E [D4:D1]BRF_Bit3..0

[D4]Peak_ Charge1	[D3]Peak_ Charge0	1/tp	tp
0	0	1/8	8
0	1	1/16	16
1	0	1/32	32
1	1	1/64	64

See section 6.5.7 about Peak Hold circuit.

Notice: The cutoff frequency of Bit Rate Filter is derived from 30.32MHz Reference Clock Frequency.

[D2]NIR_2L0

When to use NIR filter (h'10[D1]NIR_Fil_en = "1"), Set this register "0". (Recommended Value)

[D1] NIR_L1

When to use NIR filter (h'10[D1]NIR_Fil_en = "1"), Set this register "1". (Recommended Value)

* The value is not equal to initial value, so must change the value to use NIR filter.

[D0]NIR_L0

When to use NIR filter (h'10[D1]NIR_Fil_en = "1"), Set this register "0". (Recommended Value)

6.10.21 h'1D AutoOff Type B Setting

Table 6-76 Register (h'1D)

	D7	D6	D5	D4	D3	D2	D1	D0
Name	Ontime7	Ontime6	Ontime5	Ontime4	Ontime3	Ontime2	Ontime1	Ontime0
Initial	0	0	0	0	0	0	0	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[D7:D0]Ontime7..0 [Duration]

When to set AutoOff Type B (h'10[D4]AutoOffB_en = "1"), this setting is valid.

Set value of timer period till the function of AutoOff Type B starts to operate. TC32306FTG will move to Battery Saving after the value of timer period is passed, if this IC will not find "Signal Detection" after the boot sequence.

- Setting Range

[D7:D0] = 0 – 255 (b'00000000 – b'11111111)

Initial Value: 0 (b'00000000)

Maximum: 275.6ms(b'00000000)

Minimum: 0ms(b'00000001)

* The Maximum & Minimum value of timer periods depend on 30.32MHz Reference Clock Frequency.

- Way of setting

n: Setting value of register:[D7:D0]Ontime7..0

Setting value of timer period: toff = 2^{15}/fosc×(n-1) (except n = 0)

Setting value of timer period: toff = 2^{15}/fosc×255 (n = 0)

fosc: Reference Clock Frequency (30.32MHz)

Notice:

To be valid the setting of timer period, move TC32306FTG status from Battery Saving / Standby to Run after the register setting. The setting of timer period will be valid after the next moving from Battery Saving / Standby to Run, if the register setting will be described after the moving to Run. In EEPROM Mode, this register cannot be changed from the initial value.

6.10.22 h'1E Signal Detect and Lock Detect Monitors

Table 6-77 Register (h'1E)

	D7	D6	D5	D4	D3	D2	D1	D0
Name	Lock_DET	DRSSI_DET	Noise_DET	Pre_DET	—	—	—	—
Type	R	R	R	R	R	R	R	R

[D7]Lock_DET [Lock Detect Signal Monitor]

The status of PLL lock.

0: Unlocked

1: Locked

[D6]DRSSI_DET [RSSI Detection]

0: During the detection / Disable

1: Detected (RSSI_DET_out Signal = "H")

[D5]Noise_DET [Noise Detection]
0: During the detection / Disable
1: Detected (NDET_out Signal = ”H”)

[D4]Pre_DET [Preamble Detection]
0: During the detection / Disable
1: Detected (Preamble_DET_out Signal = ”H”)

[D3:D0] Unused bit.
This output is always “0”.

6.10.23 h’1F Peak Hold Level Monitor

Table 6-78 Register (h’1F)

	D7	D6	D5	D4	D3	D2	D1	D0
Name	PEAK7	PEAK6	PEAK5	PEAK4	PEAK3	PEAK2	PEAK1	PEAK0
Type	R	R	R	R	R	R	R	R

[D7:D0]PEAK7..0 [Peak Hold Level Monitor]
The output is 8 bit Peak Hold values of Peak Hold circuit. In FSK, the output this register is the value “b’00000000”.

Notice:
In ASK, the register outputs the values of the Peak Hold Circuit without the function of Data Comparator Quick Charge 2.

6.10.24 h’20 Data Comparator Monitor 1

Table 6-79 Register (h’20)

	D7	D6	D5	D4	D3	D2	D1	D0
Name	Ref_diff7	Ref_diff6	Ref_diff5	Ref_diff4	Ref_diff3	Ref_diff2	Ref_diff1	Ref_diff0
Type	R	R	R	R	R	R	R	R

[D7:D0]Ref_diff7..0 [Data Comparator Reference Level Drift Monitor 1]
The output is 8 bit reference level drift of Data Comparator circuit. It is available to monitor for the adjustment for the register setting of that circuit. The output of 1 LSB will be equivalent to the drift of (1/1.53) kHz. The output this register is the value "b'11111111" when the drift increase than 165.75kHz. When the Digital Block circuits are disabled, the output of this register is the value "b'00000000".

6.10.25 h’21 Data Comparator Monitor 2

Table 6-80 Register (h’21)

	D7	D6	D5	D4	D3	D2	D1	D0
Name	Ref_bias7	Ref_bias6	Ref_bias5	Ref_bias4	Ref_bias3	Ref_bias2	Ref_bias1	Ref_bias0
Type	R	R	R	R	R	R	R	R

[D7:D0]Ref_bias7..0 [Data Comparator Average Reference Level Monitor]
The output is 8 bit average reference of the Data Comparator circuit. 1 LSB will be equivalent to the average of (1/1.53) kHz × 4 at the setting of FSK. When the Digital Block circuits are disabled, the output of this register is the value "b'00000000".

6.10.26 h'22 RSSI Level Monitor

Table 6-81 Register (h'22)

	D7	D6	D5	D4	D3	D2	D1	D0
Name	DRSSI7	DRSSI6	DRSSI5	DRSSI4	DRSSI3	DRSSI2	DRSSI1	DRSSI0
Type	R	R	R	R	R	R	R	R

[D7:D0]DRSSI7..0 [Digital RSSI Level Monitor]

The output is 8 bit Digital RSSI level. When Digital RSSI circuit is disabled, the output of this register is the value "b'00000000".

6.10.27 h'23 Noise Signal Level Monitor

Table 6-82 Register (h'23)

	D7	D6	D5	D4	D3	D2	D1	D0
Name	DNDET7	DNDET6	DNDET5	DNDET4	DNDET3	DNDET2	DNDET1	DNDET0
Type	R	R	R	R	R	R	R	R

[D7:D0]DNDET7..0 [Noise Detection Level Monitor]

The output is 8 bit Noise Detection level. When Noise Detection circuit is disabled, the output of this register is the value "b'00000000".

7. Absolute Maximum Ratings

Table 7-1 Absolute Maximum Ratings

(The temperature for unspecified temperature ranges is Ta = 25°C; voltage is ground referenced.)

Characteristics	Symbol / Pin Name	Rating	Unit
Power supply voltage 1	COM_VDD, A_VDD_5V	Min. -0.2 / Max. +6.0	V
Power supply voltage 2	A_VDD_3V	Min. -0.2 / Max. +3.6	V
Voltage difference between pins 1	COM_VDD - A_VDD_3V	Min. -0.2 / Max. +6.0	V
Voltage difference between pins 2	A_VDD_5V - A_VDD_3V	Min. -0.2 / Max. +6.0	V
Voltage difference between pins 3	COM_VDD - A_VDD_5V	Min. -0.2 / Max. +0.2	V
Input voltage (I/O pin)	DATA_IO, CS, CLK, MOSI, MISO	Min. -0.2 / Max. COM_VDD+0.2 or 6.0 (Whichever is lower.)	V
Input pin voltage 1	ENB, 3V/5V	Min. -0.2 / Max. COM_VDD+0.2 or 6.0 (Whichever is lower.)	V
Input pin voltage 2	RESET, TEST, MODE1, MODE2	Min. -0.2 / Mx. +6.0	V
Input pin voltage 3	RX_SW, TX_SW	Min. -0.2 / Max. A_VDD_5V+0.2 or 6.0 (Whichever is lower.)	V
Signal pin voltage	RF_OUT, PA_OUT	Min. -0.2 / Max. +3.6	V
Maximum input power	RF_IN	Max. 10	dBm
Power dissipation	PD	Max. 1.0	W
Storage temperature range	Tstg	Min. -55 / Max. +125	°C

The absolute maximum rating is a technical specification that must never be exceeded, even for an instant. Stresses above absolute maximum rating conditions listed here may cause permanent damage to TC32306FTG and the application system including this IC. Do not operate at conditions which exceed this technical specification.

8. Operating Range

Table 8-1 Operating Range

(The temperature for unspecified temperature ranges is Ta = 25°C; voltage is ground referenced.)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Temperature range	Topr	—	—	-40	25	110	°C
Supply voltage range (For 5V Use, in SPI Mode)	$V_{DD\ (5V)}$	—	—	2.4	5.0	5.5	V
Supply voltage range (For 3V Use, in SPI Mode)	$V_{DD\ (3V)}$	—	—	2.0	3.0	3.3	V
Supply voltage range (For 5V Use, in EEPROM Mode)	$V_{DDE2P\ (5V)}$	—	—	2.5	5.0	5.5	V
Supply voltage range (For 3V Use, in EEPROM Mode)	$V_{DDE2P\ (3V)}$	—	—	2.5	3.0	3.3	V
RF frequency range at 315MHz	$f_{RF\ (315)}$	—	IF = 230kHz/ Wide band XOSC: 30.32MHz	310	314.94	316	MHz
RF frequency range at 434MHz	$f_{RF\ (434)}$	—	IF = 230kHz/ Wide band XOSC: 30.32MHz	433	433.92	435	MHz
RF frequency range at 868MHz	$f_{RF\ (868)}$	—	IF = 230kHz/ Wide band XOSC: 30.32MHz	868	868	870	MHz
RF frequency range at 915MHz	$f_{RF\ (915)}$	—	IF = 230kHz/ Wide band XOSC: 30.32MHz	902	915	928	MHz
X_IN Signal input level	V_{X_IN}	—	Peak to peak value	0.5	—	1.5	V

The operating range indicates the conditions under which basic functional operation is possible even when there are fluctuations in the electrical characteristics of a device.

9. Electrical Data

(Unless otherwise specified, Ta=25°C, V_{DD}=5.0V (For 5V use), fin(RF)=314.94MHz, fin(X_IN)=30.32MHz, Vin(X_IN)=1.5Vp-p, deviation=+/-40kHz, fmod=600Hz, FSK modulation, ENB=High, f(IF)=230kHz(Wide band), Set register:h'0A[D7]="1", Set other registers initial)

Table 9-1 General Characteristics

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Current consumption, RF-receiving, no signal, FSK 1	$I_{DDfm\ (RX)1}$	11-2	314.94MHz	7.2	9.7	12.2	mA
Current consumption, RF-receiving, no signal, FSK 2	$I_{DDfm\ (RX)2}$	11-2	433.92MHz	6.9	9.2	11.5	mA
Current consumption , RF-receiving, no signal, FSK 3	$I_{DDfm\ (RX)3}$	11-2	915MHz	8.1	10.8	13.5	mA
Current consumption , RF-receiving, no signal, ASK 1	$I_{DDam\ (RX)1}$	11-2	314.94MHz	7.4	9.9	12.4	mA
Current consumption , RF-receiving, no signal, ASK 2	$I_{DDam\ (RX)2}$	11-2	433.92MHz	7.1	9.5	11.9	mA
Current consumption , RF-receiving, no signal, ASK 3	$I_{DDam\ (RX)3}$	11-2	868MHz, 915MHz	8.3	11.1	13.9	mA
Current consumption , RF-transmitting 1	$I_{DD\ (TX)1}$	11-2	314.94MHz, TX, Set maximum output, Unmodulated	9.0	12.0	15.0	mA
Current consumption , RF-transmitting, PA off	$I_{DD\ (TX)PAOFF}$	11-2	314.94MHz, TX, PA off, Unmodulated	3.6	4.8	6.0	mA
Current consumption, in Battery Saving	$I_{DD\ (BS)}$	11-2	—	—	0	5	μA

Table 9-2 Pin Characteristics

Characteristics	Symbol	Test Circuit	Test Condition			Min	Typ.	Max	Unit
Input low voltage 1	V_{IL1}	—	ENB, RESET, 3V/5V, MODE2, DATA_IO, MISO, MOSI, CLK, CS			-0.2	0	COM_VDD × 0.2	V
Leakage current 1 (Low voltage input)	I_{IL1}	—				—	—	5	μA
Input high voltage 1	V_{IH1}	—				COM_VDD × 0.8	COM_VDD	COM_VDD +0.2	V
Leakage current 1 (High voltage input)	I_{IH1}	—				—	—	5	μA
Input low voltage 2	V_{IL2}	—	TX_SW, RX_SW			-0.2	0	A_VDD_5V × 0.2	V
Leakage current 2 (Low voltage input)	I_{IL2}	—				—	—	5	μA
Input high voltage 2	V_{IH2}	—				A_VDD_5V × 0.8	A_VDD_5V	A_VDD_5V +0.2	V
Leakage current 2 (High voltage input)	I_{IH2}	—				—	—	5	μA
Output resistance	R_{OH1}	—	DATA_IO, DET_TMONI1, DET_TMONI2	Low Drive		7.5	10	12.5	kΩ
Output low voltage 1	V_{OL1}	—		High Drive	I_{OL} = 0.5mA	—	—	0.4	V
Output high voltage 1	V_{OH1}	—			I_{OH} = -0.5mA	4.6	—	—	V
Output low voltage 2	V_{OL2}	—	MISO	Low Drive	I_{OL} = 0.5mA	—	—	0.4	V
Output high voltage 2	V_{OH2}	—			I_{OH} = -0.5mA	4.6	—	—	V
Output low voltage 3	V_{OL3}	—		High Drive	I_{OL} = 1.0mA	—	—	0.4	V
Output high voltage 3	V_{OH3}	—			I_{OH} = -1.0mA	4.6	—	—	V
Output low voltage 4	V_{OL4}	—	CLK, CS, MOSI		I_{OL} = 1.0mA	—	—	0.4	V
Output high voltage 4	V_{OH4}	—			I_{OH} = -1.0mA	4.6	—	—	V
Output high voltage 5	V_{OH5}	—	RX_SW, TX_SW		I_{OH} = -2.0mA	4.2	—	—	V

Table 9-3 RF-Receiving Characteristics

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
LNA gain	$G_{v\ (LNA)}$	11-4	50 Ω termination	-11	-8	-5	dB
IF filter lower cutoff frequency 1	IF_{L1}	—	fo-3dB point IF = 230kHz / Wide band	—	70	90	kHz
IF filter higher cutoff frequency 1	IF_{H1}	—	fo-3dB point IF = 230kHz / Wide band	370	390	—	kHz
IF filter lower cutoff frequency 2	IF_{L2}	—	fo-3dB point IF = 280kHz / Middle band	—	140	160	kHz
IF filter higher cutoff frequency 2	IF_{H2}	—	fo-3dB point IF = 280kHz / Middle band	390	410	—	kHz
RSSI output voltage 1	V_{RSSI1}	11-5	$V_{IN\ (MIX)}$ = -80dBm, Unmodulated	0.30	0.55	0.80	V
RSSI output voltage 2	V_{RSSI2}	11-5	$V_{IN\ (MIX)}$ = -60dBm, Unmodulated	0.85	1.25	1.60	V
RSSI output voltage 3	V_{RSSI3}	11-5	$V_{IN\ (MIX)}$ = -30dBm, Unmodulated	1.85	2.35	2.80	V
RSSI output resistance	R_{RSSI}	11-3	—	37.5	50	62.5	kΩ
Duty ratio	DR_{fm}	11-5	$V_{IN\ (MIX)}$ = -60dBm, DATA_IO pin output, Data pattern : 010101···	45	50	55	%

(Unless otherwise specified, Ta=25°C, V_{DD}=5.0V (For 5V use), fin(RF)=314.94MHz, fin(X_IN)=30.32MHz, Vin(X_IN)=1.5Vp-p, FSK modulation, ENB=High, RF transmitting, Unmodulated, Set register·h'0A[D7]="1", Set other registers initial)

Table 9-4 RF-Transmitting Characteristics

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output level (315MHz) 1	$P_{TX\ (315)1}$	11-6	FSK, 314.94MHz,Unmodulated, Via a matching circuit, Set maximum output, ASK, 314.94MHz, Peak power, Via a matching circuit, Set maximum output,	8	10	12	dBm

10. Reference Characteristics Data

This item contains reference values and does not contain any guaranteed values.

(Unless otherwise specified, Ta = 25°C, VDD = 5.0V (For 5V use), fin(RF) = 314.94MHz, fin(X_IN) = 30.32MHz, Vin(X_IN) = 1.5Vp-p, deviation = +/-40kHz, fmod = 600Hz, FSK modulation, ENB = High, f(IF) = 230kHz(Wide band), Set register:h'0A[D7] = "1", Set other registers initial)

Table 10-1 Reference General Characteristics Data

Characteristics	Symbol	Test Circuit	Test Condition	Typ.	Unit
Regulator output voltage 1	A_REG30	—	For 5V use	3.0	V
Regulator output voltage 2	A_REG15	—	—	1.5	V
Regulator output voltage 3	D_REG	—	—	1.5	V
Regulator output voltage 4	PLL_REG	—	—	1.5	V

Table 10-2 Reference RF-Receiving Characteristics Data

Characteristics	Symbol	Test Circuit	Test Condition	Typ.	Unit
Receiver sensitivity 12dB SINAD1	12dB SINAD1	—	314.94/ 433.92MHz, IF = 280kHz / Middle band, FSK, Deviation = +/-40kHz	-117	dBm
Receiver sensitivity 12dB SINAD2	12dB SINAD2	—	314.94/ 433.92MHz, IF = 230kHz / Wide band, FSK, Deviation = +/-40kHz	-116	dBm
Receiver sensitivity 12dB SINAD3	12dB SINAD3	—	915MHz, IF = 280kHz / Middle band, FSK, Deviation = +/-40kHz, except for the harmonics of reference clock	-116	dBm
Receiver sensitivity 12dB SINAD4	12dB SINAD4	—	915MHz, IF = 230kHz / Wide band, FSK, Deviation = +/-40kHz, except for the harmonics of reference clock	-115	dBm
Receiver sensitivity 12dB SINAD5	12dB SINAD5	—	314.94 MHz, IF = 230kHz / Wide band, ASK, 90% depth, square wave input	-121	dBm
LNA voltage gain (315 / 434 MHz)	$G_{v\ (LNA)H}$	—	314.94 / 433.92MHz, via a matching circuit	35	dB
LNA voltage gain (868 / 915 MHz)	$G_{v\ (LNA)L}$	—	868 / 915MHz, via a matching network	26	dB
Mixer conversion gain 1	$G_{v\ (MIX)1}$	—	314.94 / 433.92MHz, 50 Ω termination	31	dB
Mixer conversion gain 2	$G_{v\ (MIX)2}$	—	868 / 915MHz, 50 Ω termination	35	dB
Mixer Intercept point (3rd order)	IIP3	—	Input referred value	-9	dBm
Mixer 1dB compression	IP1dB	—	Input referred value	-18	dBm
Image rejection ratio	IRR	—	—	35	dB
IF AMP gain	$G_{v\ (IF)}$	—	—	51	dB
IF filter attenuation	IFF_{ATT}	—	300kHz offset, IF = 280kHz / Middle band	25	dB

(Unless otherwise specified, Ta=25°C, V_{DD}=5.0V (For 5V use), fin(RF)=314.94MHz, fin(X_IN)=30.32MHz, Vin(X_IN)=1.5Vp-p, FSK modulation, ENB=High, RF transmitting, Unmodulated, Set register:h'0A[D7]="1", Set other registers initial)

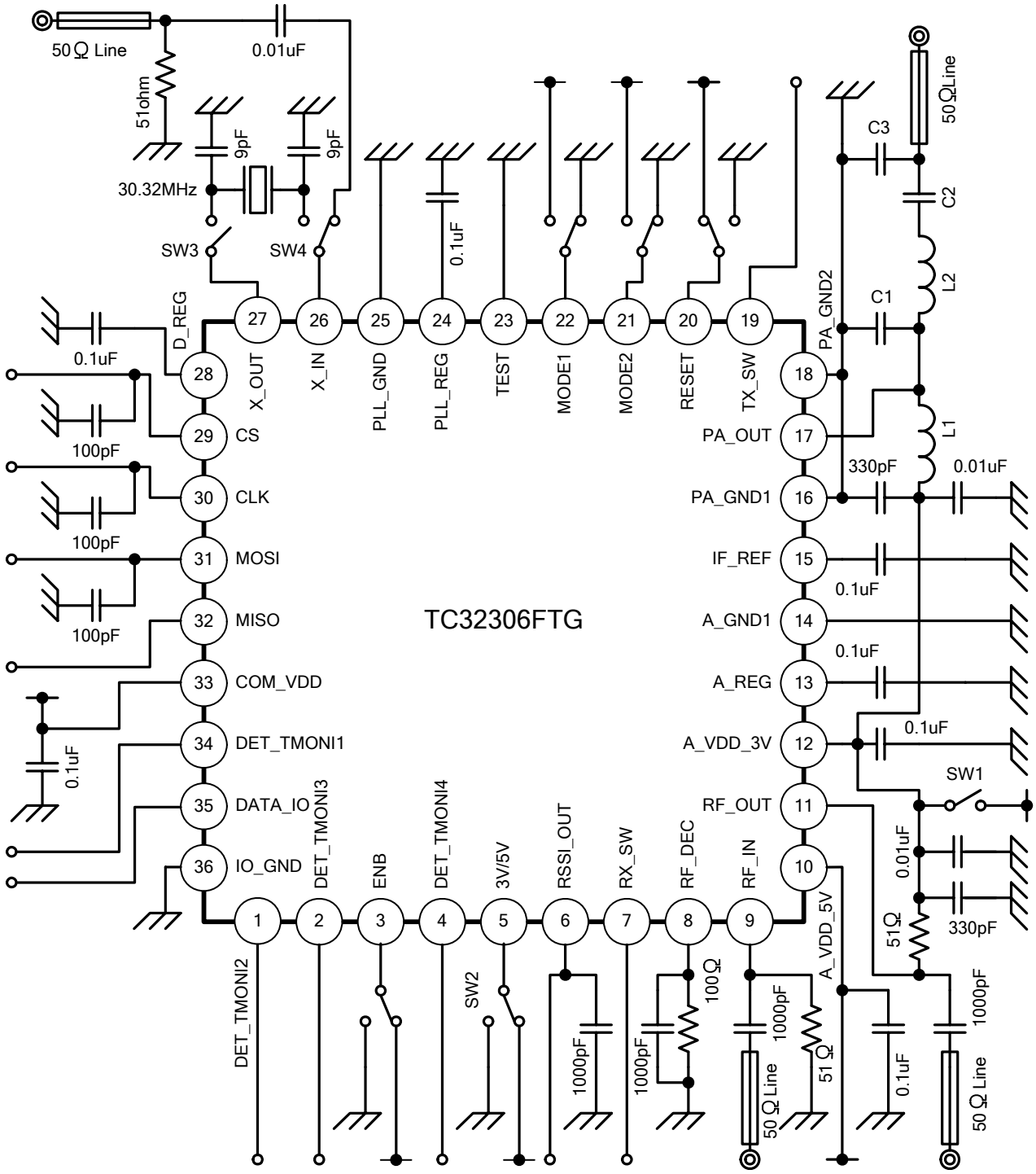
Table 10-3 Reference RF-Transmitting Characteristics Data

Characteristics	Symbol	Test Circuit	Test Condition	Typ.	Unit
Current consumption , RF-transmitting 2	$I_{DD\ (TX)2}$	—	Register:h'13 [D3:D2] = "10"	10.4	mA
Current consumption , RF-transmitting 3	$I_{DD\ (TX)3}$	—	Register:h'13 [D3:D2] = "01"	8.8	mA
Current consumption , RF-transmitting 4	$I_{DD\ (TX)4}$	—	Register:h'13 [D3:D2] = "00" (Minimum level)	7.3	mA
RF-transmitting power level (315MHz) 2	$P_{TX\ (315)2}$	—	Register:h'13 [D3:D2] = "10"	8	dBm
RF-transmitting power level (315MHz) 3	$P_{TX\ (315)3}$	—	Register:h'13 [D3:D2] = "01"	4.7	dBm
RF-transmitting power level (315MHz) 4	$P_{TX\ (315)4}$	—	Register:h'13 [D3:D2] = "00" (Minimum level)	0	dBm

Table 10-4 Reference PLL Characteristics Data

Characteristics	Symbol	Test Circuit	Test Condition	Typ.	Unit
Lockup time	T_{PLL}	—	—	50	μs
450kHz offset C/N (RF-transmitting)	C/N1	—	315 / 434MHz, Unmodulated	51	dBc/ 100kHz
1MHz offset C/N (RF-transmitting)	C/N2	—	915MHz, Unmodulated	60	dBc/ 300kHz

11. Typical Test Circuit

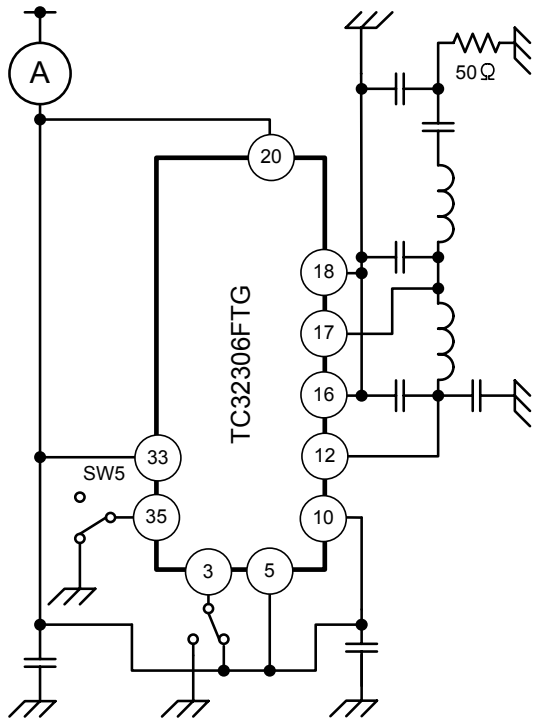


Test Characteristics: $V_{DD\ (5V)}$, $V_{DD\ (3V)}$, $f_{RF\ (315)}$, $f_{RF\ (434)}$, $f_{RF\ (868)}$, $f_{RF\ (915)}$

Notice:

Measure after the parts tuning that shows a part number. TC32306FTG supply voltage is selected by SW1 and SW2. SW3 and SW4 allow selecting the crystal oscillator and external signal.

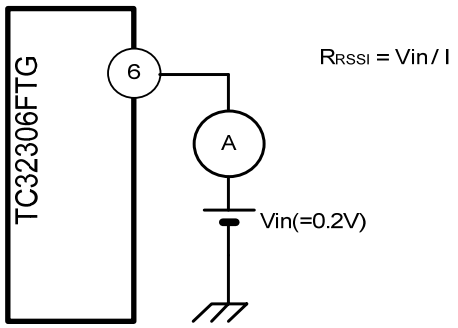
Fig 11-1 Typical Test Circuit



Test Characteristics: $I_{DDfm\ (RX)1}$, $I_{DDfm\ (RX)2}$, $I_{DDfm\ (RX)3}$, $I_{DDam\ (RX)1}$ $I_{DDam\ (RX)2}$, $I_{DDam\ (RX)3}$, $I_{DD\ (TX)1}$, $I_{DD\ (TX)PAOFF}$, $I_{DD\ (BS)}$

* For 5V mode, set 5 pin to high level.
In the measurement of RF-Receiving, set to be open 35 pin by operating SW5.
In the measurement of RF-Transmitting, set to be low level and set to unmodulated by register. In the measurement of RF-Transmitting without PA operation, set the register:h13[D1]PA_en = ”0”.
Also in the measurement of RF-Transmitting, set the output pin via a 50Ω termination as illustrated.
In the measurement of Battery Saving Status, set 3 pin to low level.

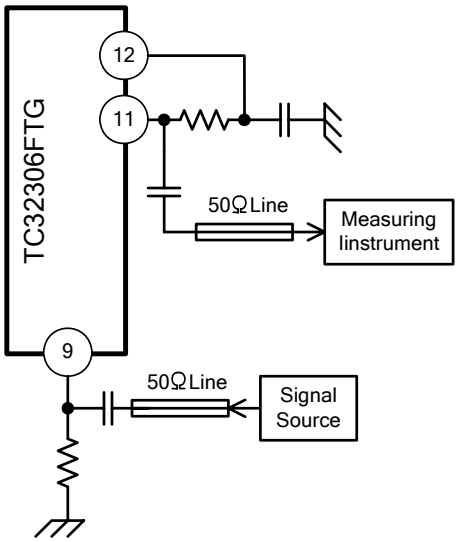
Fig 11-2 Test Circuit (Current Consumption)



Test Characteristics: R_{RSSI}

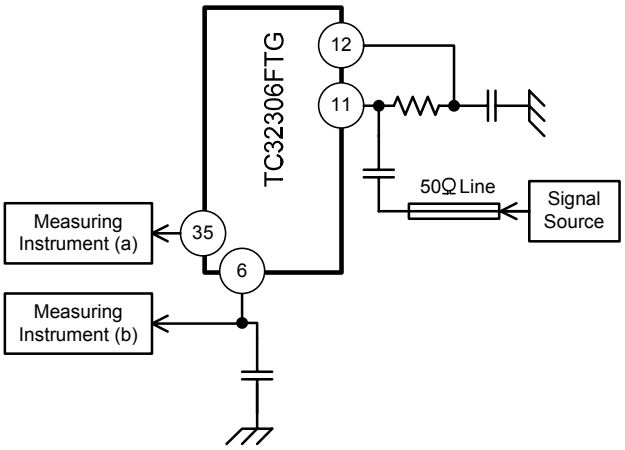
* It will be measured at no voltage supply to TC32306FTG, and applied lower voltage not to work internal protection diodes.

Fig 11-3 Test Circuit (RSSI_OUT Pin Output Resistance)



Test Characteristics: $G_{v\ (LNA)}$

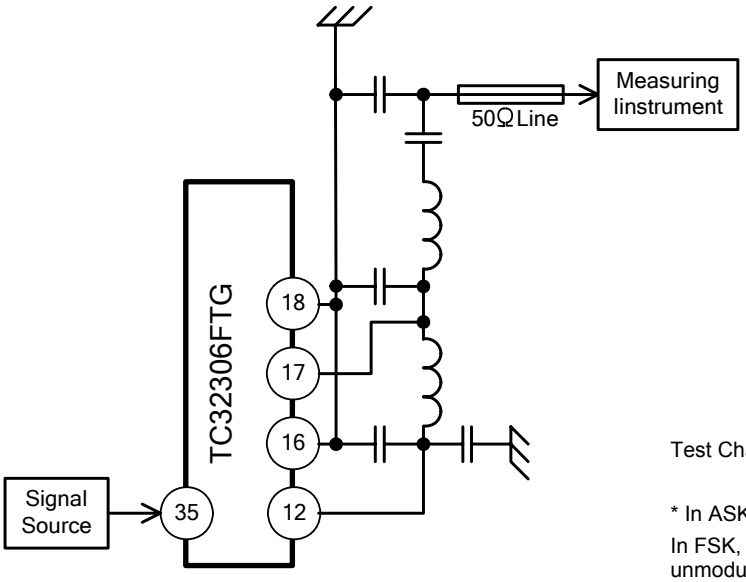
Fig 11-4 Test Circuit (LNA Gain)



Test Characteristics: $V_{RSSI1,}$ $V_{RSSI2,}$ $V_{RSSI3,}$ DR_{fm}

* Measure VRSSI1/VRSSI2/VRSSI3 by connecting (a).
Measure DRfm by connecting (b).

Fig 11-5 Test Circuit (RF-Receiving)



Test Characteristics: $P_{TX\ (315)1}$

* In ASK, measure by connecting the signal source to 35 pin.
In FSK, measure by setting 35 pin to low level. (Set to unmodulated by register)

Fig 11-6 Test Circuit (RF-Transmitting)

12. Application Circuits

Toshiba does not guarantee this application circuit example as a production design. Please evaluate carefully when developing the production design for your application.

12.1 Example of Evaluation Circuit

The following is an example of Toshiba's evaluation circuit.

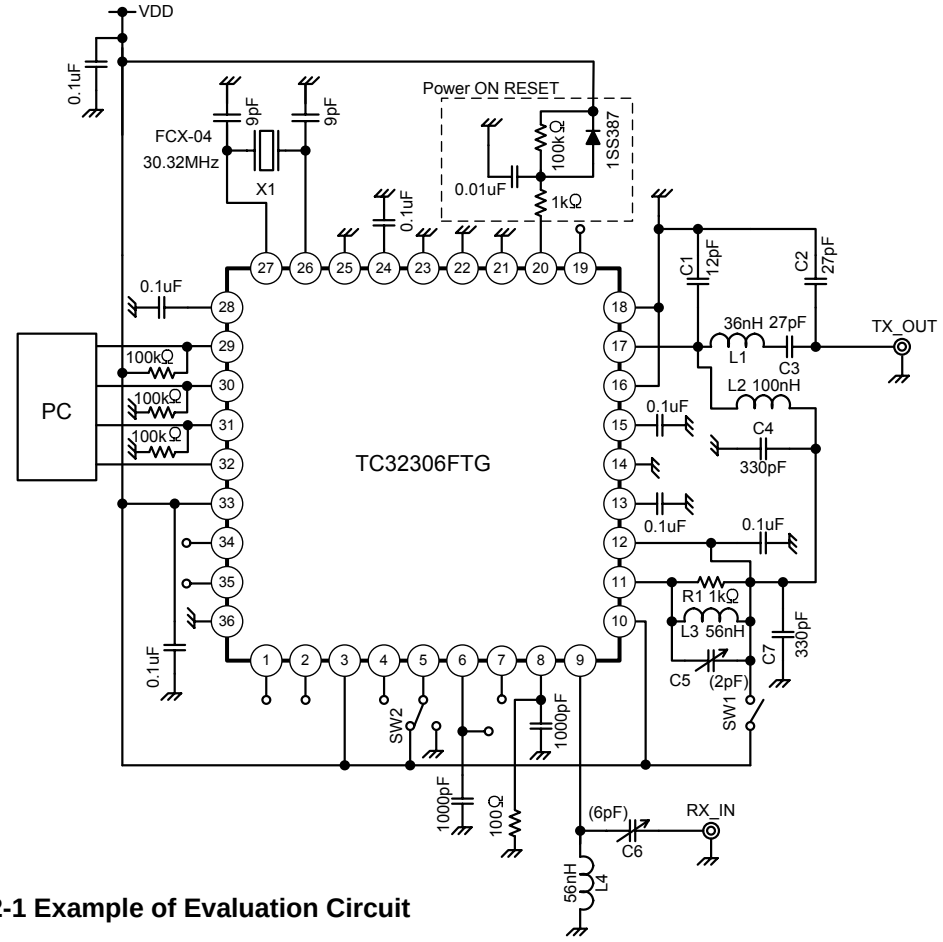


Fig 122-1 Example of Evaluation Circuit

- Above circuit is a 5V use. For 3V use, connect SW2 to low level, and be short circuit in SW1.
- Above circuit is a use for 315MHz and the circuit parts constants are suitable for that frequency. For other frequency use, see Table 12-1.
- Above circuit is SPI Mode and external PC controls to read or write SPI register of TC32306FTG,
- In above circuit, a control of an antenna switch is not use.
- The capacitor C5 and C6 is adjusted by a trimmer capacitor.

  Toshiba use capacitors shown in the following, Murata Manufacturing Company, Ltd.

  i. TZY2Z060A001 (6pF)

  ii.TZY2Z030A001 (3pF)

  iii. TZY2Z010A001 (1pF)
- The inductance L1-L4: LQF series, Murata Manufacturing Company, Ltd.
- X1: FCX-0430.320MHZ-J90842, RIVER ELETEC CORPORATION

Table 122-1 Example of Matching Constants

Frequency	315MHz	434MHz	915MHz
C1	12pF	10pF	4pF
C2	27pF	20pF	9pF
C3	27pF	18pF	6pF
C4	330pF	330pF	330pF
C5	ii *	ii *	iii *
C6	i *	i *	1pF
C7	330pF	330pF	330pF
L1	36nH	22nH	10nH
L2	100nH	100nH	43nH
L3	51nH	22nH	6.8nH
L4	56nH	33nH	9.1nH
R1	1kΩ	2kΩ	510Ω

*: usage trimmer capacitor

12.2 Example of Application Circuit 1

The following is an example of application circuit controlled by MCU.

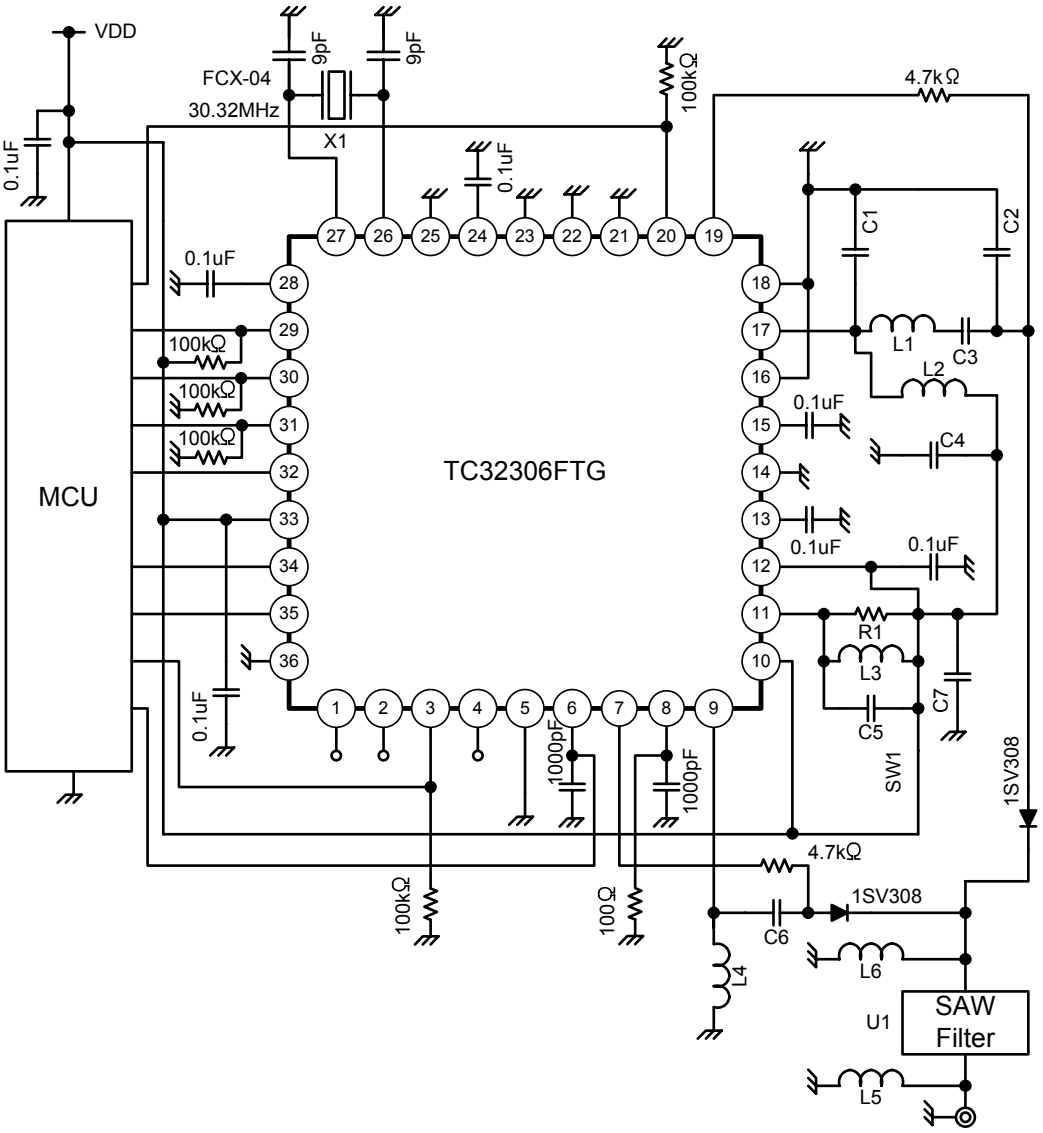


Fig 122-2 Example of Application Circuit 1

- Above circuit is SPI Mode and external MCU I/O is connected to SPI control pins of TC32306FTG,
- MCU also controls RESET pin and ENB pin.
- MCU accepts a signal from DET_TMONI1 pin as an interrupt signal.
- MCU monitors RSSI_OUT pin signal.
- The antenna is use for RX and TX, and this IC controls the antenna switch, 1SV308: Toshiba Corporation.

12.3 Example of Application Circuit 2

The following is an example of application circuit controlled by MCU and EEPROM.

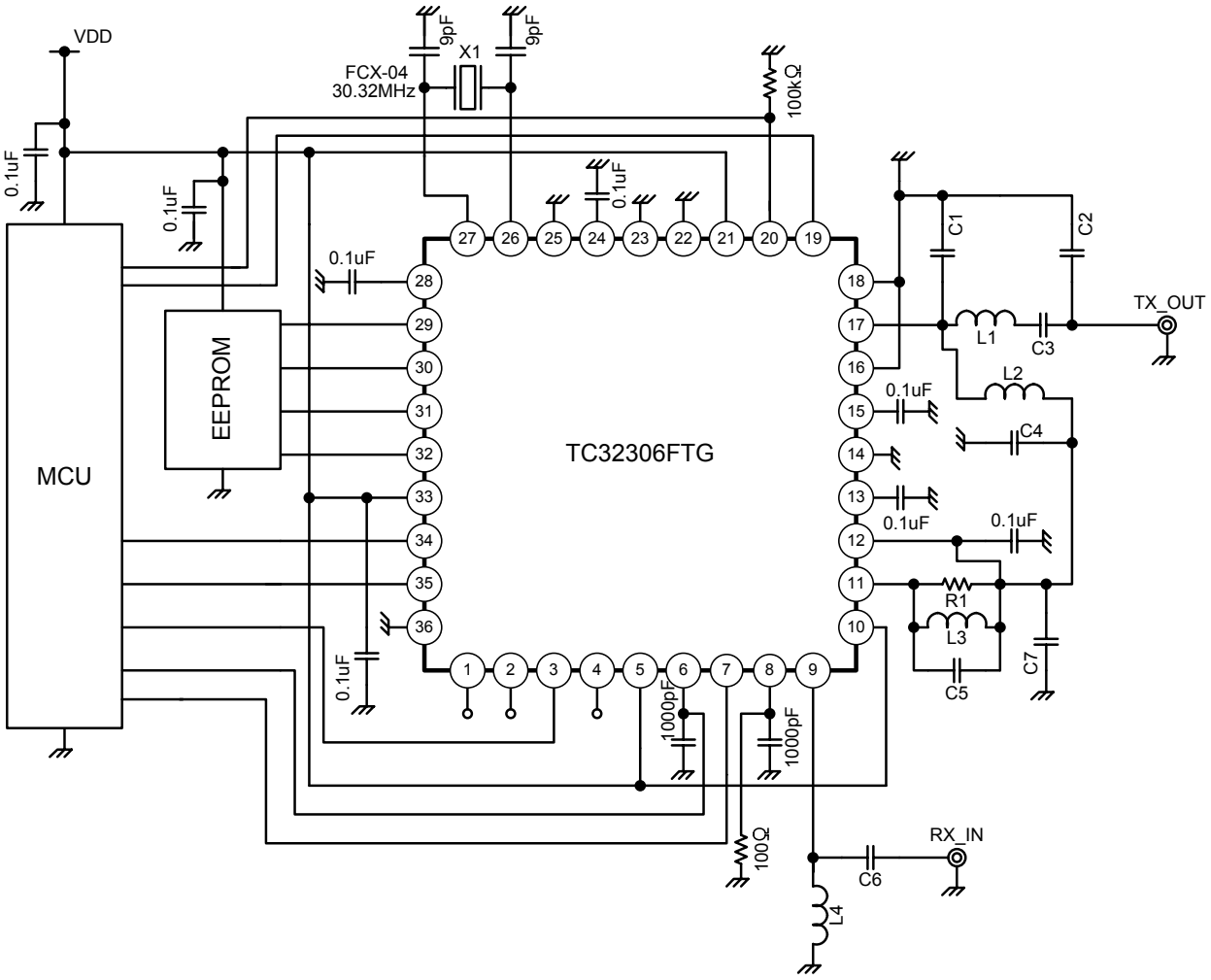


Fig 122-3 Example of Application Circuit 2

- Above circuit is EEPROM Mode and external EEPROM I/O is connected to SPI control pins of TC32306FTG,
- MCU controls RESET pin.
- The connection and H/L control from MCU to ENB pin, RX_SW pin and TX_SW pin decide a read data configuration from EEPROM.
- MCU accepts a signal from DET_TMONI1 pin as an interrupt signal.
- MCU monitors RSSI_OUT pin signal.
- In EEPROM Mode, this IC doesn't prepare antenna switch control.
- About EEPROM pin termination, see that manual.

12.4 Example of Application Circuit 3

The following is an example of application circuit only for receiving controlled by MCU and EEPROM.

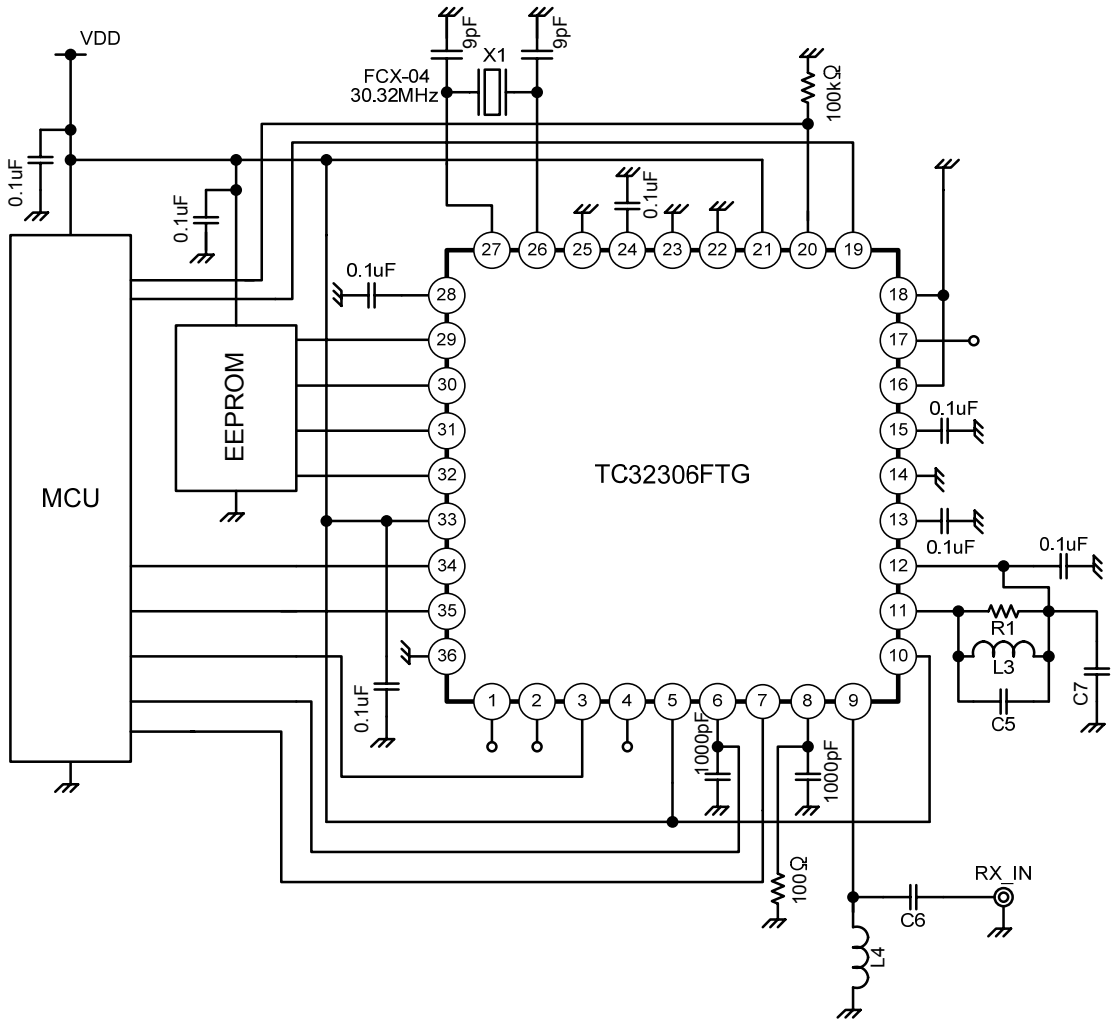
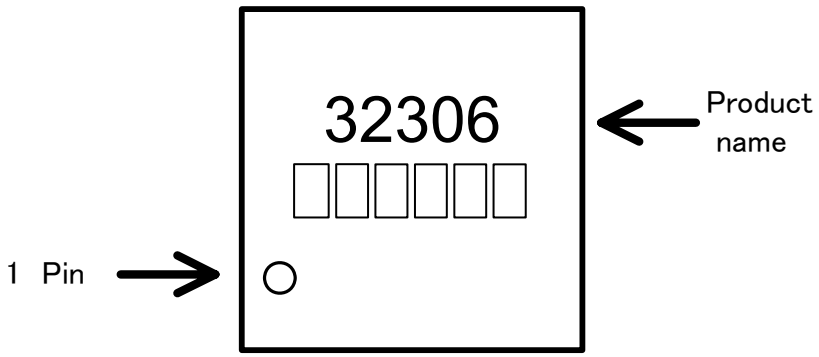


Fig 122-4 Example of Application Circuit 3

- Above circuit is the EEPROM Mode and external EEPROM I/O is connected to SPI control pins of TC32306FTG,
- PA_OUT pin is open.
- MCU controls RESET pin.
- The connection and H/L control from MCU to ENB pin, RX_SW pin and TX_SW pin decide a read data configuration from EEPROM.
- MCU accepts a signal from DET_TMONI1 pin as an interrupt signal.
- MCU monitors RSSI_OUT pin signal.
- In EEPROM Mode, this IC doesn't prepare antenna switch control.
- About EEPROM pin termination, see that manual.

13. Marking (Top View)



Lot Code

□□□□□□

1) 2) 3) 4)

1) The year of manufacture (1 last figure of the year)

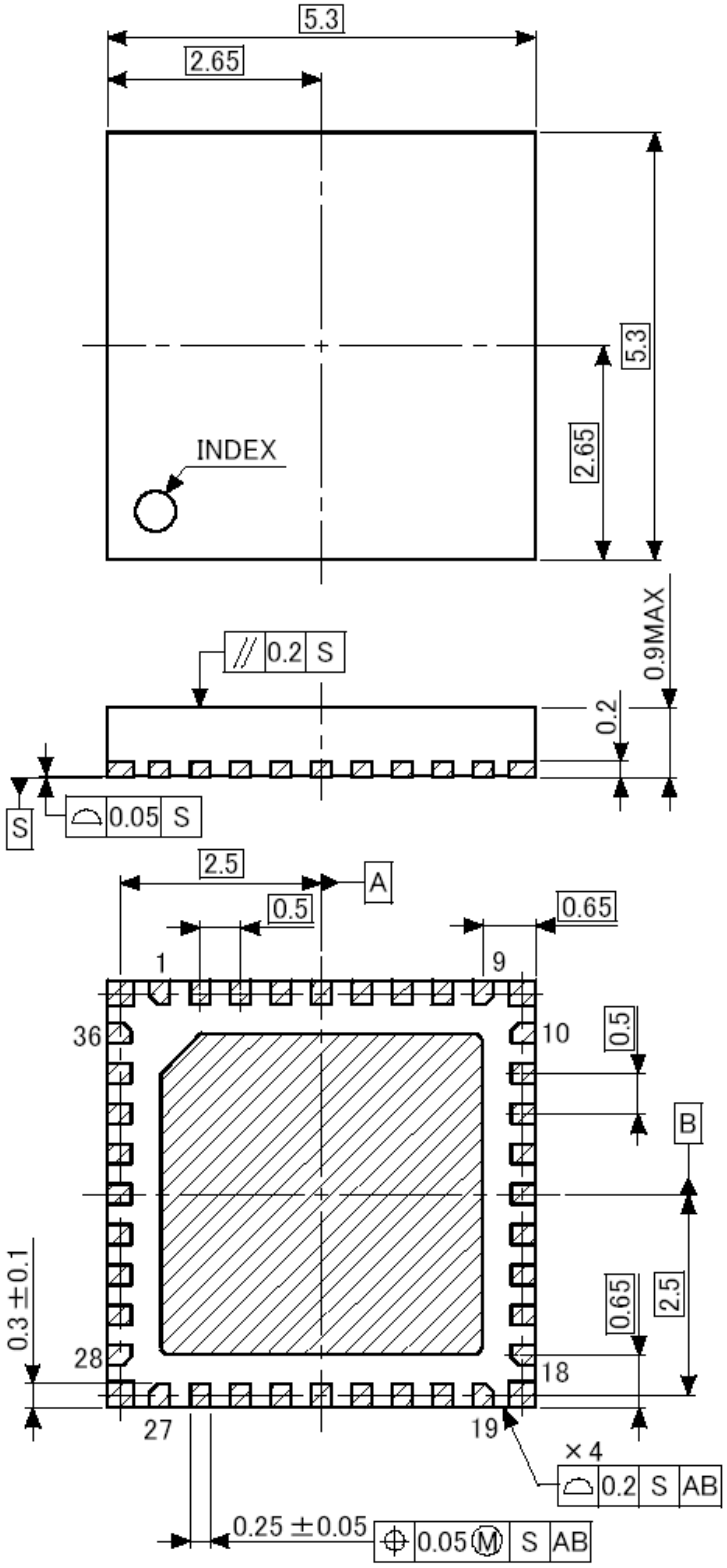
2) The week of manufacture (“01” as first week of the year, from 1 to 52 or 53)

3) Toshiba factory management code

4) Assembly code

14. Package Dimensions

QFN36-P-0606-0.50 "Unit : mm"



Weight: 0.08g (Typ.)

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