TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

262,144-WORD BY 16-BIT FULL CMOS STATIC RAM

Lead-Free

DESCRIPTION

The TC55NEM216ASGV is a 4,194,304-bit static random access memory (SRAM) organized as 262,144 words by 16 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 2.7 to 5.5 V power supply. Advanced circuit technology provides both high speed and low power at an operating current of 3 mA/MHz (typ) and a minimum cycle time of 55 ns. It is automatically placed in low-power mode at 1.8 μA standby current (typ) when chip enable ($\overline{CE}$) is asserted high or chip select (CS) is asserted low. There are three control inputs. $\overline{CE}$ is used to select the device and for data retention control, and output enable ($\overline{OE}$) provides fast memory access. Data byte control pin ($\overline{LB}$, $\overline{UB}$) provides lower and upper byte access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating extreme temperature range of –40° to 85°C, the TC55NEM216ASGV can be used in environments exhibiting extreme temperature conditions. The TC55NEM216ASGV is available in a plastic 44-pin thin-small-outline package (TSOP).

FEATURES

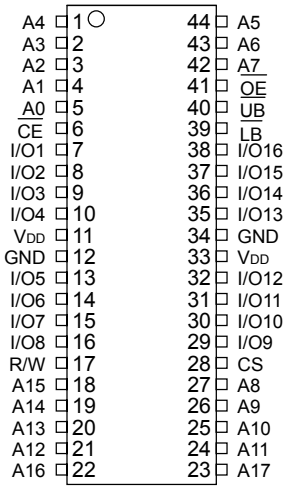
- Low-power dissipation
  Operating: 15 mW/MHz (typical)
- Single power supply voltage of 2.7 to 5.5 V
- Power down features using $\overline{CE}$
- Data retention supply voltage of 2.0 to 5.5 V
- Direct TTL compatibility for all inputs and outputs
- Wide operating temperature range of –40° to 85°C
- Standby Current (maximum): 20 μA
- Access Times (maximum):

	5 V ± 10%		2.7 V~5.5 V	
	55	70	55	70
Access Time	55 ns	70 ns	85 ns	100 ns
$\overline{CE}$ Access Time	55 ns	70 ns	85 ns	100 ns
$\overline{OE}$ Access Time	30 ns	35 ns	60 ns	70 ns

- Package:
  TSOP II44-P-400-0.80 (Weight:0.47 g typ)
- Lead-Free

PIN ASSIGNMENT (TOP VIEW)

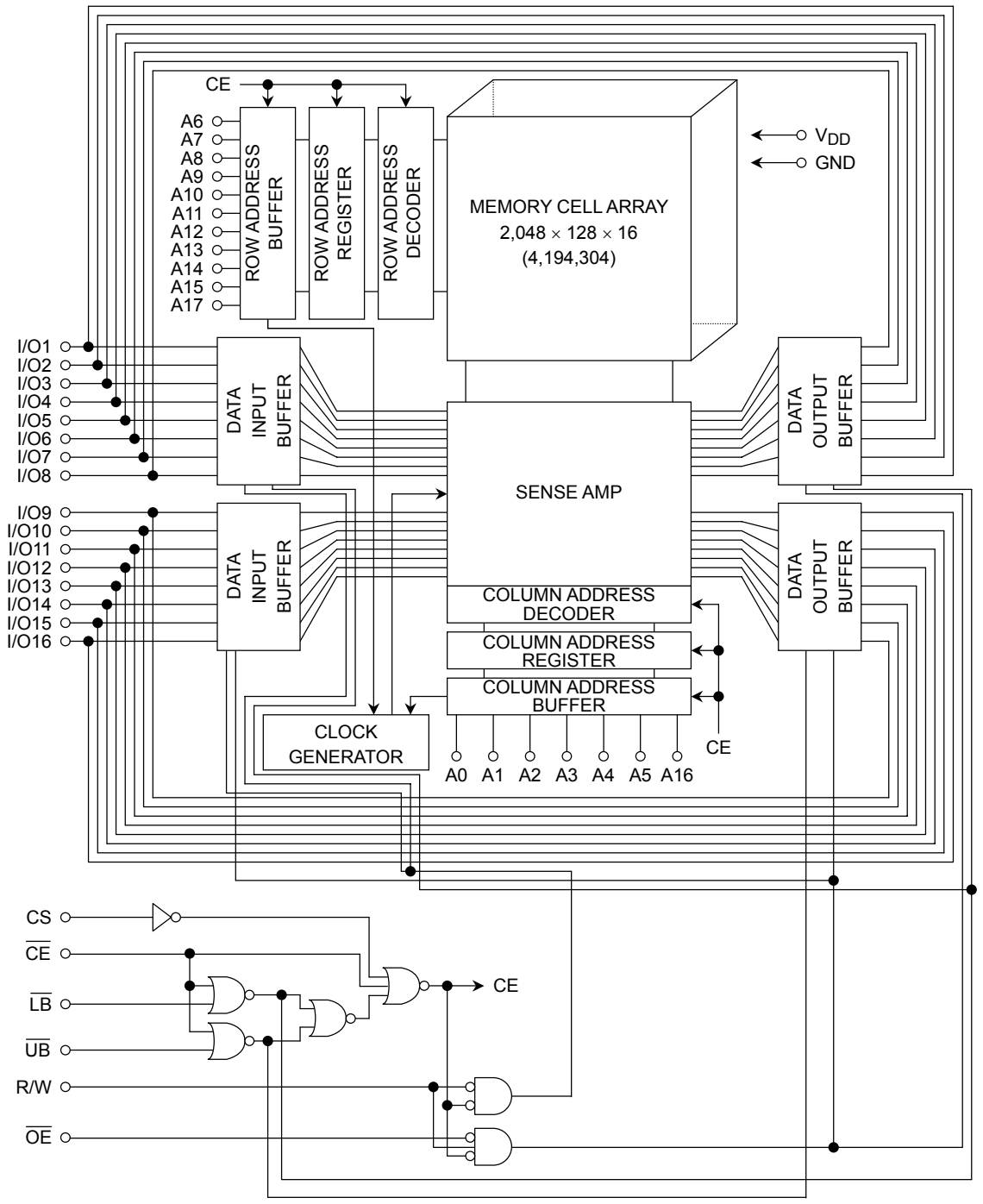
44 PIN TSOP



PIN NAMES

A0~A17	Address Inputs
$\overline{CE}$	Chip Enable
CS	Chip Select
R/W	Read/Write Control
$\overline{OE}$	Output Enable
$\overline{LB}$, $\overline{UB}$	Data Byte Control
I/O1~I/O16	Data Inputs/Outputs
V_{DD}	Power
GND	Ground
NC	No Connection

BLOCK DIAGRAM



OPERATING MODE

MODE	$\overline{CE}$	CS	$\overline{OE}$	R/W	$\overline{LB}$	$\overline{UB}$	I/O1~I/O8	I/O9~I/O16	POWER
Read	L	H	L	H	L	L	Output	Output	I_{DDO}
	L	H	L	H	H	L	High-Z	Output	I_{DDO}
	L	H	L	H	L	H	Output	High-Z	I_{DDO}
Write	L	H	*	L	L	L	Input	Input	I_{DDO}
	L	H	*	L	H	L	High-Z	Input	I_{DDO}
	L	H	*	L	L	H	Input	High-Z	I_{DDO}
Output Deselect	L	H	H	H	L	L	High-Z	High-Z	I_{DDO}
	L	H	H	H	H	L	High-Z	High-Z	I_{DDO}
	L	H	H	H	L	H	High-Z	High-Z	I_{DDO}
CS Standby	*	L	*	*	*	*	High-Z	High-Z	I_{DDS}
Standby	H	*	*	*	*	*	High-Z	High-Z	I_{DDS}
	*	*	*	*	H	H	High-Z	High-Z	I_{DDS}

* = don't care
H = logic high
L = logic low

MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{DD}	Power Supply Voltage	−0.3~7.0	V
V_{IN}	Input Voltage	−0.3*~7.0	V
$V_{I/O}$	Input/Output Voltage	−0.5~V_{DD} + 0.5	V
P_D	Power Dissipation	0.6	W
T_{solder}	Soldering Temperature (10s)	260	°C
T_{stg}	Storage Temperature	−55~150	°C
T_{opr}	Operating Temperature	−40~85	°C

*: −2.0 V when measured at a pulse width of 20ns

DC RECOMMENDED OPERATING CONDITIONS (Ta = −40° to 85°C)

SYMBOL	PARAMETER	5 V ± 10%			2.7 V~5.5 V			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	2.7	5.0	5.5	V
V_{IH}	Input High Voltage	2.4*1	—	V_{DD} + 0.3	V_{DD} − 0.2	—	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	−0.3*2	—	0.6	−0.3*2	—	0.2	V
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	2.0	—	5.5	V

*1: CS pin = V_{DD} × 0.7
*2: −2.0V when measured at a pulse width of 20 ns

DC CHARACTERISTICS (Ta = –40° to 85°C, V_{DD} = 5 V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V~V_{DD}			—	—	±1.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4 V			–1.0	—	—	mA
I_{OL}	Output Low Current	V_{OL} = 0.4 V			2.1	—	—	mA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or CS = V_{IL} or $\overline{LB}$ = $\overline{UB}$ = V_{IH} or R/W = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0 V~V_{DD}			—	—	±1.0	μA
I_{DDO1}	Operating Current	$\overline{CE}$ = V_{IL} and CS = V_{IH} and R/W = V_{IH}, $\overline{LB}$ = $\overline{UB}$ = V_{IL}, I_{OUT} = 0 mA, Other Input = V_{IH}/V_{IL}	t_{cycle}	MIN	—	—	35	mA
				1 μs	—	8	—	
I_{DDO2}		$\overline{CE}$ = 0.2 V and CS = V_{DD} – 0.2 V and R/W = V_{DD} – 0.2 V, $\overline{LB}$ = $\overline{UB}$ = 0.2 V, I_{OUT} = 0 mA, Other Input = V_{DD} – 0.2 V/0.2 V	t_{cycle}	MIN	—	—	30	mA
				1 μs	—	3	—	
I_{DDS1}	Standby Current	1) $\overline{CE}$ = V_{IH} 2) CS= V_{IL} 3) $\overline{LB}$ = $\overline{UB}$ = V_{IH}			—	—	3	mA
I_{DDS2}		1) $\overline{CE}$ = V_{DD} – 0.2 V 2) CS = 0.2 V 3) $\overline{LB}$ = $\overline{UB}$ = V_{DD} – 0.2 V, $\overline{CE}$ = 0.2 V, CS = V_{DD} – 0.2 V	Ta = 25°C		—	1.8	—	μA
			Ta = –40~40°C		—	—	3	
			Ta = –40~85°C		—	—	20	

DC CHARACTERISTICS (Ta = –40° to 85°C, V_{DD} = 3 V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V~V_{DD}			—	—	±1.0	μA
I_{OH}	Output High Current	V_{OH} = V_{DD} – 0.2 V			–0.1	—	—	mA
I_{OL}	Output Low Current	V_{OL} = 0.2 V			0.1	—	—	mA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or CS = V_{IL} or $\overline{LB}$ = $\overline{UB}$ = V_{IH} or R/W = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0 V~V_{DD}			—	—	±1.0	μA
I_{DDO2}	Operating Current	$\overline{CE}$ = 0.2 V and CS = V_{DD} – 0.2 V and R/W = V_{DD} – 0.2 V, $\overline{LB}$ = $\overline{UB}$ = 0.2 V, I_{OUT} = 0 mA, Other Input = V_{DD} – 0.2 V/0.2 V	t_{cycle}	MIN	—	—	30	mA
				1 μs	—	3	—	
I_{DDS2}	Standby Current	1) $\overline{CE}$ = V_{DD} – 0.2 V 2) CS = 0.2 V 3) $\overline{LB}$ = $\overline{UB}$ = V_{DD} – 0.2 V, $\overline{CE}$ = 0.2 V, CS = V_{DD} – 0.2 V	Ta = 25°C		—	1.6	—	μA
			Ta = –40~40°C		—	—	3	
			Ta = –40~85°C		—	—	20	

CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS AND OPERATING CONDITIONS

(Ta = –40° to 85°C, V_{DD} = 5 V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC55NEM216ASGV				UNIT
		55		70		
		MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	55	—	70	—	ns
t_{ACC}	Address Access Time	—	55	—	70	
t_{CO}	Chip Enable Access Time	—	55	—	70	
t_{OE}	Output Enable Access Time	—	30	—	35	
t_{BA}	Data Byte Control Access Time	—	55	—	70	
t_{COE}	Chip Enable Low to Output Active	5	—	5	—	
t_{OEE}	Output Enable Low to Output Active	0	—	0	—	
t_{BE}	Data Byte Control Low to Output Active	5	—	5	—	
t_{OD}	Chip Enable High to Output High-Z	—	25	—	30	
t_{ODO}	Output Enable High to Output High-Z	—	25	—	30	
t_{BD}	Data Byte Control High to Output High-Z	—	25	—	30	
t_{OH}	Output Data Hold Time	10	—	10	—	

WRITE CYCLE

SYMBOL	PARAMETER	TC55NEM216ASGV				UNIT
		55		70		
		MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	55	—	70	—	ns
t_{WP}	Write Pulse Width	40	—	50	—	
t_{CW}	Chip Enable to End of Write	45	—	55	—	
t_{BW}	Data Byte Control to End of Write	45	—	55	—	
t_{AS}	Address Setup Time	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	
t_{ODW}	R/W Low to Output High-Z	—	25	—	30	
t_{OEW}	R/W High to Output Active	0	—	0	—	
t_{DS}	Data Setup Time	25	—	30	—	
t_{DH}	Data Hold Time	0	—	0	—	

Note: t_{OD}, t_{ODO}, t_{BD} and t_{ODW} are specified in time when an output becomes high impedance, and are not judged depending on an output voltage level.

AC TEST CONDITIONS

PARAMETER	TEST CONDITION
Input pulse level	0.4 V, 2.6 V
t_R, t_F	5 ns
Timing measurements	1.5 V
Reference level	1.5 V
Output load	30 pF + 1 TTL Gate (55) 100 pF + 1 TTL Gate (70)

AC CHARACTERISTICS AND OPERATING CONDITIONS

(Ta = –40° to 85°C, V_{DD} = 2.7 to 5.5 V)

READ CYCLE

SYMBOL	PARAMETER	TC55NEM216ASGV				UNIT
		55		70		
		MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	85	—	100	—	ns
t_{ACC}	Address Access Time	—	85	—	100	
t_{CO}	Chip Enable Access Time	—	85	—	100	
t_{OE}	Output Enable Access Time	—	60	—	70	
t_{BA}	Data Byte Control Access Time	—	85	—	100	
t_{COE}	Chip Enable Low to Output Active	5	—	5	—	
t_{OEE}	Output Enable Low to Output Active	0	—	0	—	
t_{BE}	Data Byte Control Low to Output Active	5	—	5	—	
t_{OD}	Chip Enable High to Output High-Z	—	35	—	40	
t_{ODO}	Output Enable High to Output High-Z	—	35	—	40	
t_{BD}	Data Byte Control High to Output High-Z	—	35	—	40	
t_{OH}	Output Data Hold Time	10	—	10	—	

WRITE CYCLE

SYMBOL	PARAMETER	TC55NEM216ASGV				UNIT
		55		70		
		MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	85	—	100	—	ns
t_{WP}	Write Pulse Width	55	—	60	—	
t_{CW}	Chip Enable to End of Write	60	—	70	—	
t_{BW}	Data Byte Control to End of Write	60	—	70	—	
t_{AS}	Address Setup Time	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	
t_{ODW}	R/W Low to Output High-Z	—	35	—	40	
t_{OEW}	R/W High to Output Active	0	—	0	—	
t_{DS}	Data Setup Time	35	—	40	—	
t_{DH}	Data Hold Time	0	—	0	—	

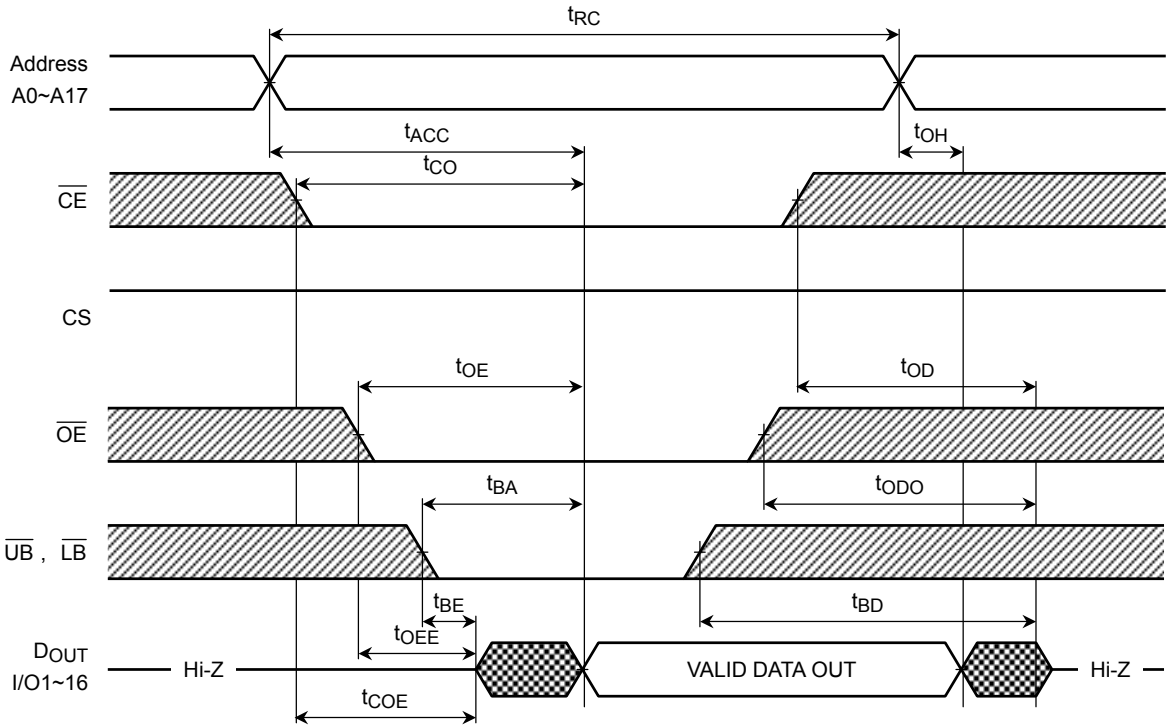
Note: t_{OD}, t_{ODO}, t_{BD} and t_{ODW} are specified in time when an output becomes high impedance, and are not judged depending on an output voltage level.

AC TEST CONDITIONS

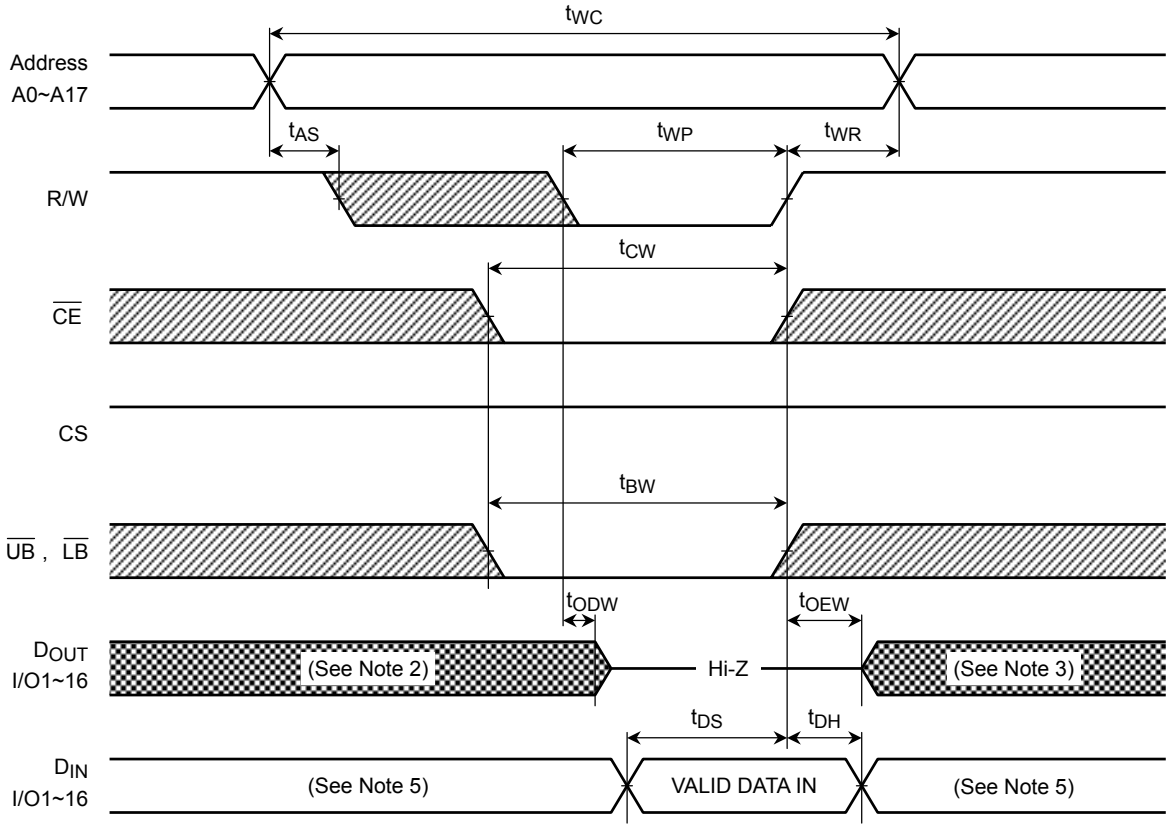
PARAMETER	TEST CONDITION
Input pulse level	0.2 V, V_{DD} – 0.2 V
t_R, t_F	5 ns
Timing measurements	1.5 V
Reference level	1.5 V
Output load	30 pF (Include Jig) (55) 100 pF (Include Jig) (70)

TIMING DIAGRAMS

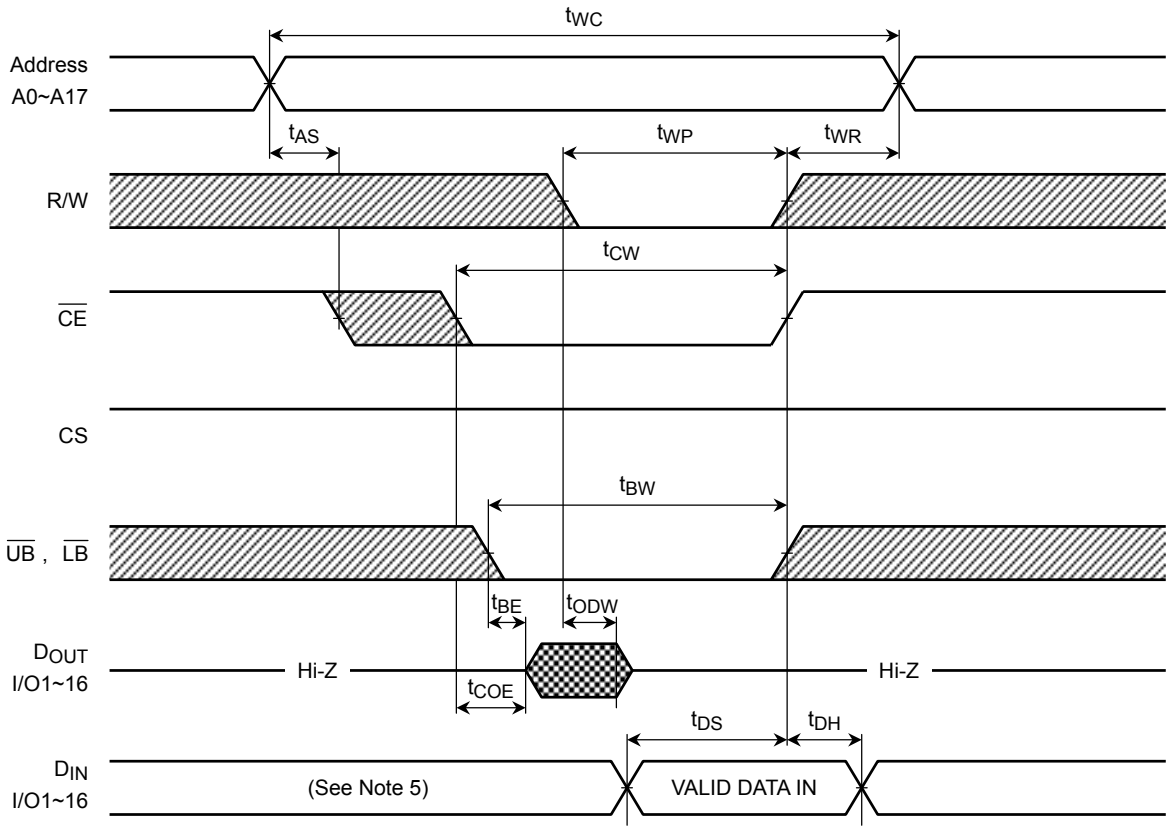
READ CYCLE (See Note 1)



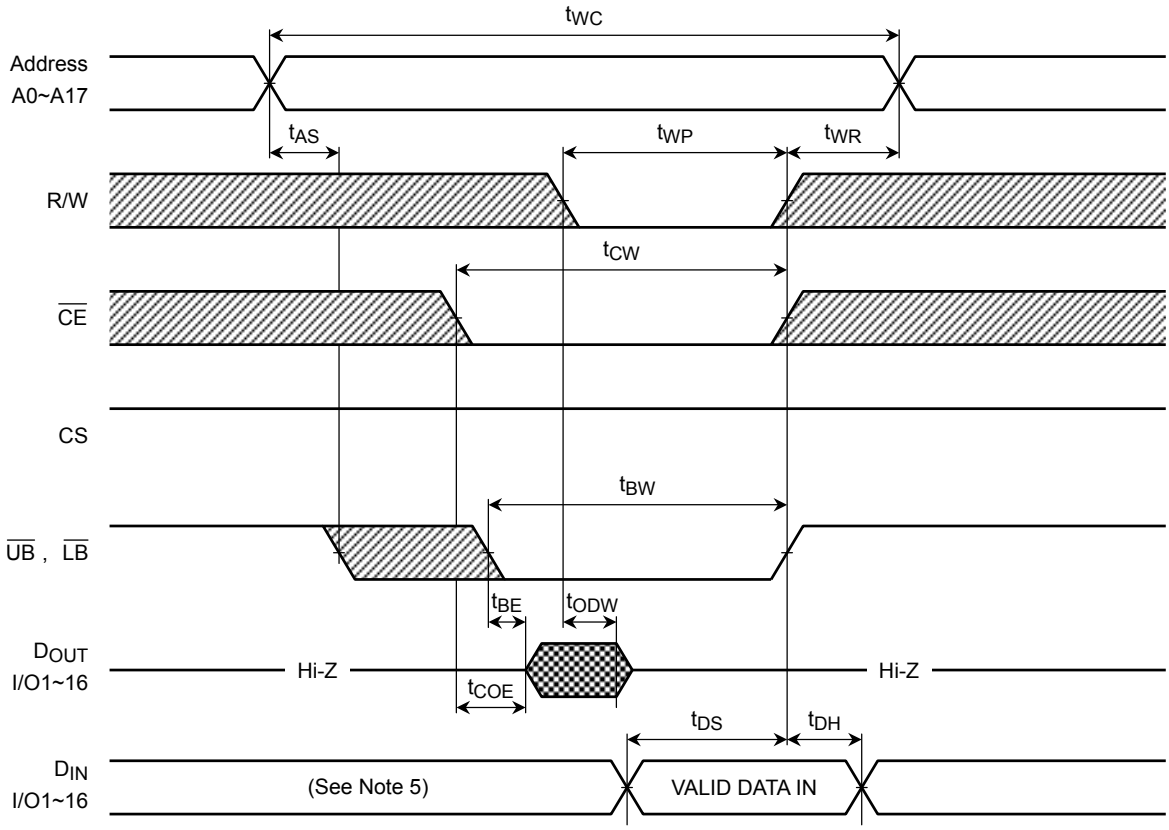
WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)



WRITE CYCLE 2 ($\overline{CE}$ CONTROLLED) (See Note 4)



WRITE CYCLE 3 ($\overline{UB}$, $\overline{LB}$ CONTROLLED) (See Note 4)



Note:

(1) R/W remains HIGH for the read cycle.

(2) If $\overline{CE}$ (or $\overline{UB}$ or $\overline{LB}$) goes LOW(or CS goes HIGH) coincident with or after R/W goes LOW, the outputs will remain at high impedance.

(3) If $\overline{CE}$ (or $\overline{UB}$ or $\overline{LB}$) goes HIGH(or CS goes LOW) coincident with or before R/W goes HIGH, the outputs will remain at high impedance.

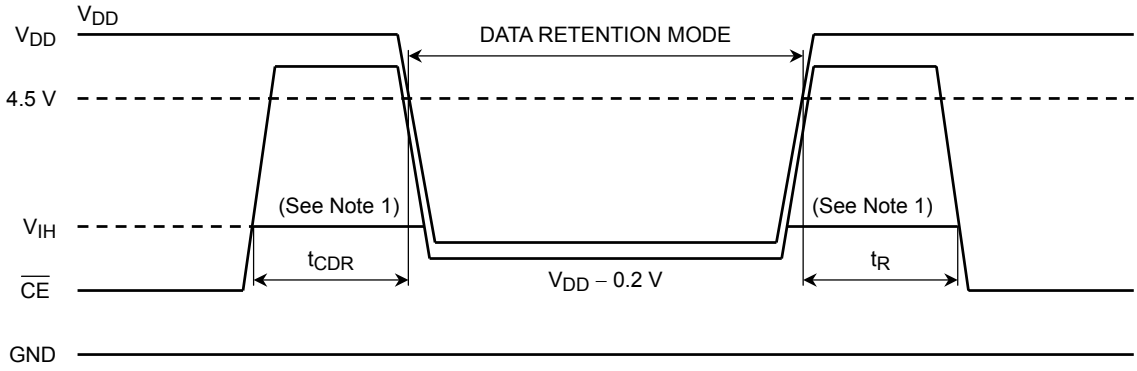
(4) If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.

(5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

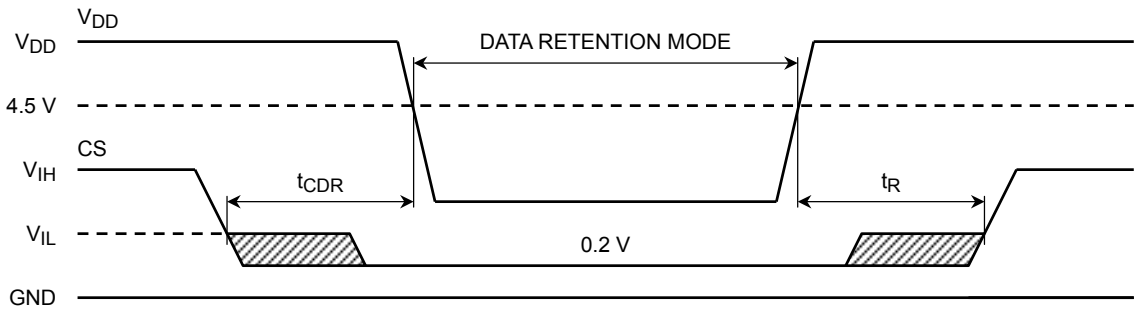
DATA RETENTION CHARACTERISTICS (Ta = –40° to 85°C)

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	—	5.5	V
I_{DDS2}	Standby Current	Ta = –40~40°C	—	—	3	μA
		Ta = –40~85°C	—	—	20	
t_{CDR}	Chip Deselect to Data Retention Mode Time		0	—	—	ns
t_R	Recovery Time		5	—	—	ms

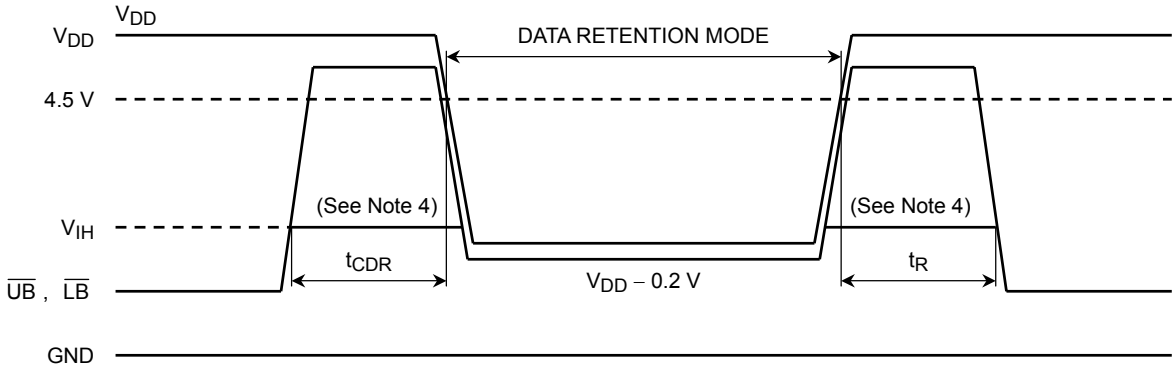
$\overline{CE}$ CONTROLLED DATA RETENTION MODE



CS CONTROLLED DATA RETENTION MODE (See Note 2)



$\overline{UB}$, $\overline{LB}$ CONTROLLED DATA RETENTION MODE (See Note 3)



Note:

(1) In $\overline{CE}$ controlled data retention mode, minimum standby current mode is entered when CS ≤ 0.2 V or CS ≥ V_{DD} – 0.2 V.

(2) When $\overline{CE}$ is operating at the V_{IH}(min.) level(2.4 V), the operating current is given by I_{DDS1} during the transition of V_{DD} from 4.5 to 2.6 V.

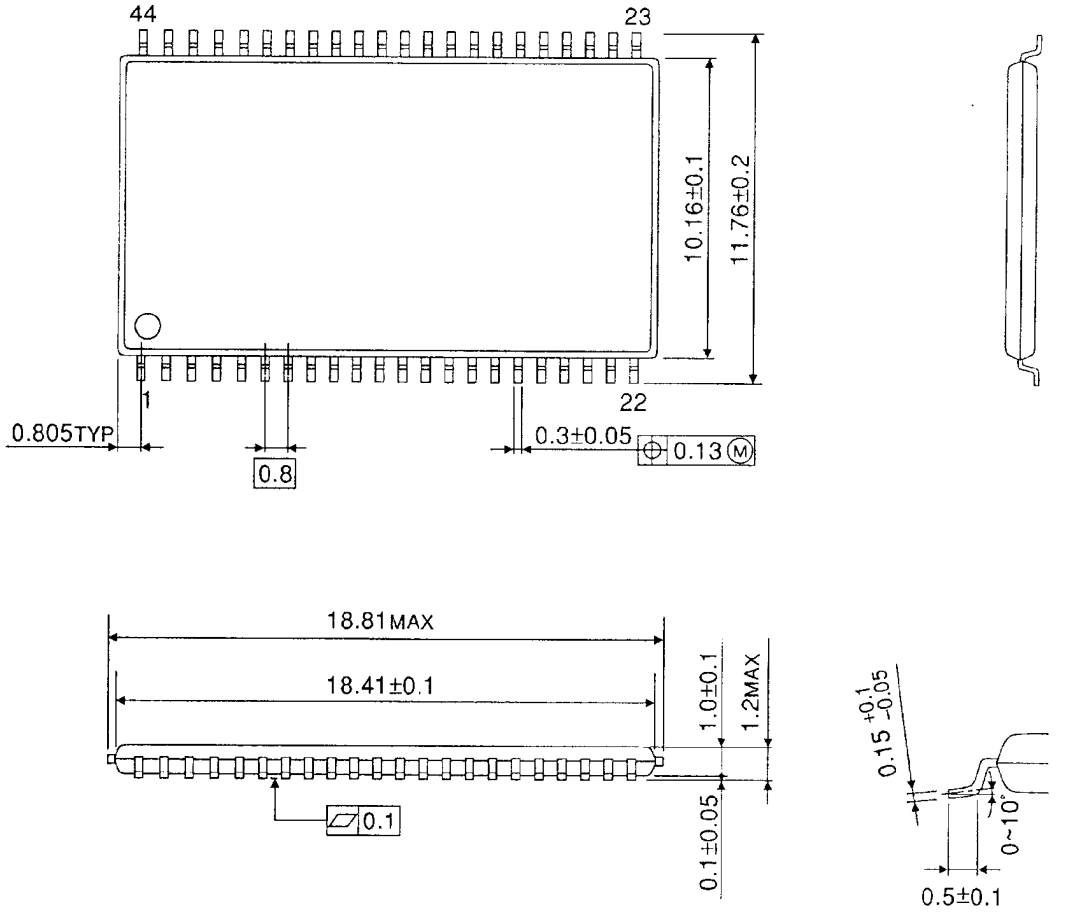
(3) In CS controlled data retention mode, minimum standby current mode is entered when CS ≤ 0.2 V.

(4) In $\overline{UB}$ (or $\overline{LB}$) controlled data retention mode, minimum standby current mode is entered when $\overline{CE}$, CS ≤ 0.2 V or $\overline{CE}$, CS ≥ V_{DD} – 0.2 V.

(5) When $\overline{UB}$ (or $\overline{LB}$) is operating at the V_{IH}(min.) level(2.4 V), the operating current is given by I_{DDS1} during the transition of V_{DD} from 4.5 to 2.6 V.

PACKAGE DIMENSIONS

TSOP II 44-P-400-0.80 Unit : mm



Weight:0.47 g (typ)

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