

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

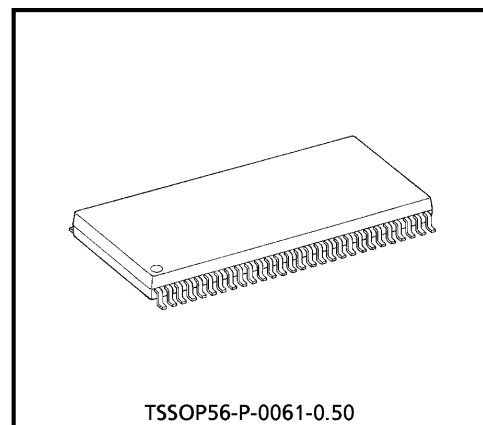
**TC74VCX162841FT****LOW-VOLTAGE 20-BIT D-TYPE LATCH  
WITH 3.6 V TOLERANT INPUTS AND OUTPUTS**

The TC74VCX162841FT is a high performance CMOS 20-bit D-TYPE LATCH. Designed for use in 1.8, 2.5 or 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. It is also designed with over voltage tolerant inputs and outputs up to 3.6 V.

The TC74VCX162841FT can be used as two 10-bit latches or one 20-bit latch. The 20 latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs. While the latch-enable (1LE or 2LE) input is high, the Q outputs of the corresponding 10-bit latch follow the D inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

When the  $\overline{OE}$  input is high, the outputs are in a high impedance state. This device is designed to be used with 3-state memory address drivers, etc.

The 26- $\Omega$  series resistor helps reducing output overshoot and undershoot without external resistor. All inputs are equipped with protection circuits against static discharge.



Weight : 0.25 g (Typ.)

**FEATURES**

- 26- $\Omega$  Series Resistors on Outputs.
- Low Voltage Operation :  $V_{CC} = 1.8 \sim 3.6$  V
- High Speed Operation :  $t_{pd} = 3.9$  ns (max) at  $V_{CC} = 3.0 \sim 3.6$  V  
                                   :  $t_{pd} = 4.8$  ns (max) at  $V_{CC} = 2.3 \sim 2.7$  V  
                                   :  $t_{pd} = 9.6$  ns (max) at  $V_{CC} = 1.8$  V
- 3.6 V Tolerant inputs and outputs.
- Output Current :  $I_{OH} / I_{OL} = \pm 12$  mA (min) at  $V_{CC} = 3.0$  V  
                           :  $I_{OH} / I_{OL} = \pm 8$  mA (min) at  $V_{CC} = 2.3$  V  
                           :  $I_{OH} / I_{OL} = \pm 4$  mA (min) at  $V_{CC} = 1.8$  V
- Latch-up Performance :  $\pm 300$  mA
- ESD Performance : Human Body Model  $> \pm 2000$  V  
                           : Machine Model  $> \pm 200$  V
- Package : TSSOP  
                           (Thin Shrink Small Outline Package)
- Power Down Protection is provided on all inputs and outputs.
- Supports live insertion / withdrawal (Note 1)

(Note 1) : To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

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For information or to contact us:

Market Maker Systems Canada

Phone: 1-514-333-1245

Fax: 1-514-333-1489

Email: [sales@searchdatasheets.com](mailto:sales@searchdatasheets.com)

