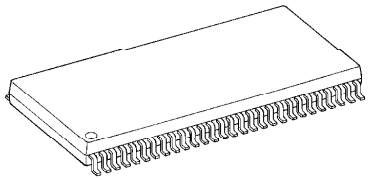
ADVANCE INFORMATION

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VCX16543FT

LOW-VOLTAGE 16-BIT REGISTERED TRANSCEIVER WITH 3.6V TOLERANT INPUTS AND OUTPUTS

The TC74VCX16543FT is a high performance CMOS 16-bit REGISTERED TRANSCEIVER. Designed for use in 1.8, 2.5 or 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.
It is also designed with over voltage tolerant inputs and outputs up to 3.6V.
The TC74VCX16543FT can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.
The A-to-B enable ($\overline{CEAB}$) input must be low in order to enter data from A or to output data from B. If $\overline{CEAB}$ is low and $\overline{LEAB}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.
When the $\overline{OE}$ input is high, the outputs are in a high impedance state. This device is designed to be used with 3-state memory address drivers, etc.
All inputs are equipped with protection circuits against static discharge.



TSSOP56-P-0061-0.50

Weight : 0.25g (Typ.)

PRELIMINARY

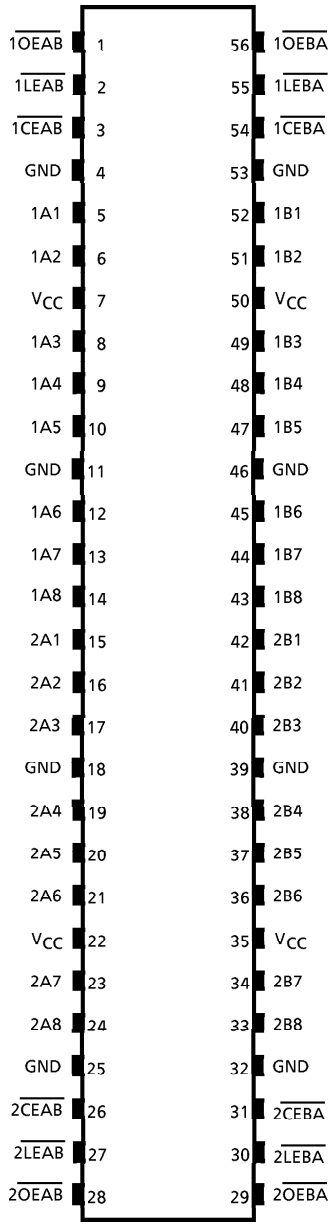
FEATURES

- Low Voltage Operation : V_{CC} = 1.8~3.6V
- High Speed Operation : t_{pd} = TBD (max.) at V_{CC} = 3.0~3.6V
  : t_{pd} = TBD (max.) at V_{CC} = 2.3~2.7V
  : t_{pd} = TBD (max.) at V_{CC} = 1.8V
- 3.6V Tolerant inputs and outputs.
- Output Current : I_{OH} / I_{OL} = ±24mA (min.) at V_{CC} = 3.0V
  : I_{OH} / I_{OL} = ±12mA (min.) at V_{CC} = 2.3V
  : I_{OH} / I_{OL} = ±6mA (min.) at V_{CC} = 1.8V
- Latch-up Performance : ±300mA
- ESD Performance : Human Body Model > ±2000V
  : Machine Model > ±200V
- Package : TSSOP
  (Thin Shrink Small Outline Package)
- Power Down Protection is provided on all inputs and outputs.

Note 1) Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.
2) All floating (high impedance) bus terminal must have their input level fixed by means of pull up or pull down resistors.

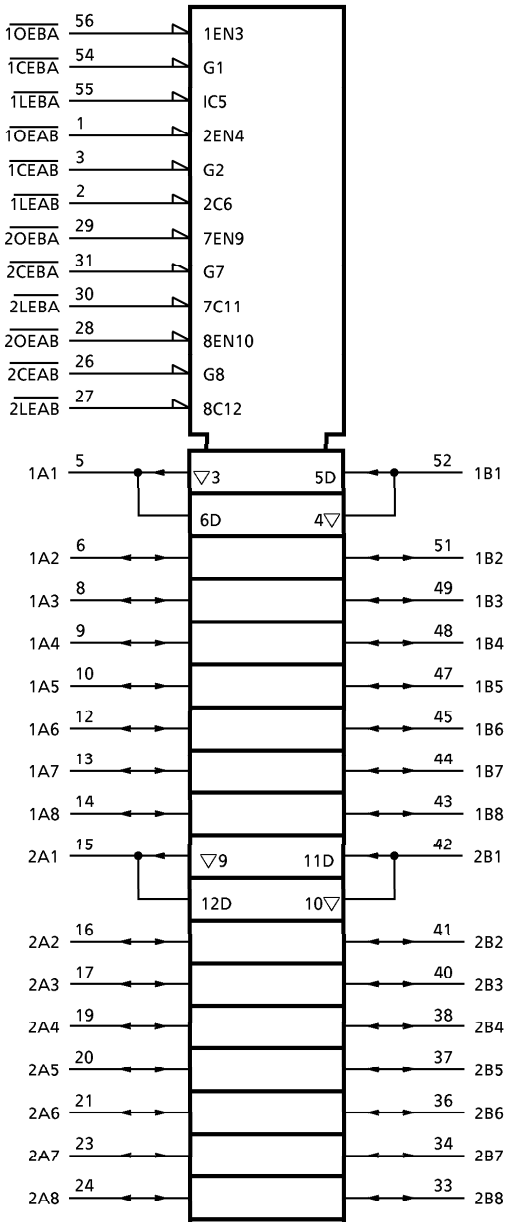
961001EBA2

PIN ASSIGNMENT



(TOP VIEW)

SYMBOL



PRELIMINARY

961001EBA2'

FUNCTION TABLE* (each 8-bit latch)

INPUTS				OUTPUTS
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A	B
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0**
L	L	L	L	L
L	L	L	H	H

* A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.

** Output level before the indicated steady-state input conditions were established.

PRELIMINARY

SYSTEM DIAGRAM