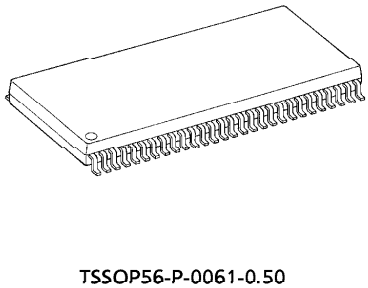
ADVANCE INFORMATION

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VCX16646FT

LOW VOLTAGE 16-BIT BUS TRANSCEIVER / REGISTER WITH 3.6V TOLERANT INPUTS AND OUTPUTS

The TC74VCX16646FT is a high performance CMOS 16-bit BUS TRANSCEIVER / REGISTER. Designed for use in 1.8, 2.5 or 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.
It is also designed with over voltage tolerant inputs and outputs up to 3.6V.
This device is bus transceiver with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the internal registers.
All inputs are equipped with protection circuits against static discharge.



TSSOP56-P-0061-0.50

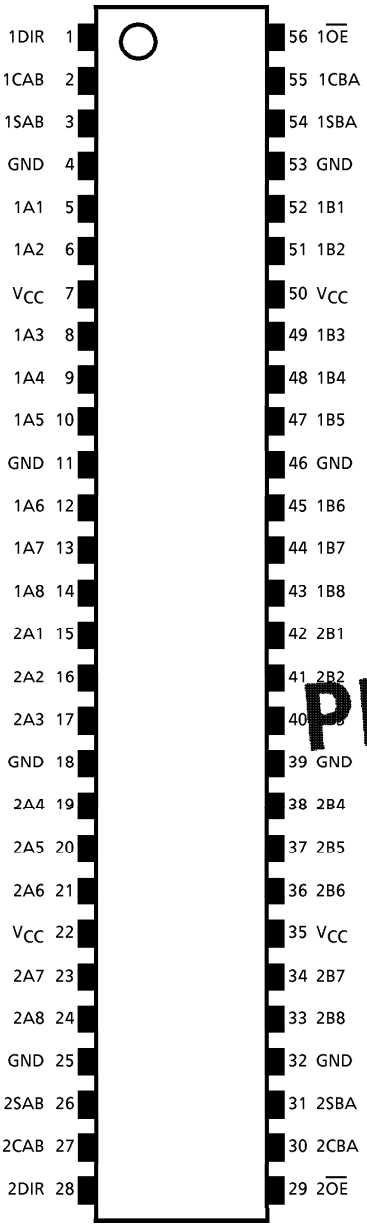
Weight : 0.25g (Typ.)

FEATURES

- Low Voltage Operation : V_{CC} = 1.8~3.6V
- High Speed Operation : tpd = TBD (max.) at V_{CC} = 3.0~3.6V
  : t_{pd} = TBD (max.) at V_{CC} = 2.3~2.7V
  : tpd = TBD (max.) at V_{CC} = 1.8V
- 3.6V Tolerant inputs and outputs.
- Output Current : I_{OH} / I_{OL} = ± 24mA (min.) at V_{CC} = 3.0V
  : I_{OH} / I_{OL} = ± 18mA (min.) at V_{CC} = 2.3V
  : I_{OH} / I_{OL} = ± 6mA (min.) at V_{CC} = 1.8V
- Latch-up Performance : ± 300mA
- ESD Performance : Human Body Model > ± 2000V
  : Machine Model > ± 200V
- Package : TSSOP (Thin Shrink Small Outline Package)
- Bidirectional interface between 2.5V and 3.3V signals.
- Power Down Protection is provided on all inputs and outputs

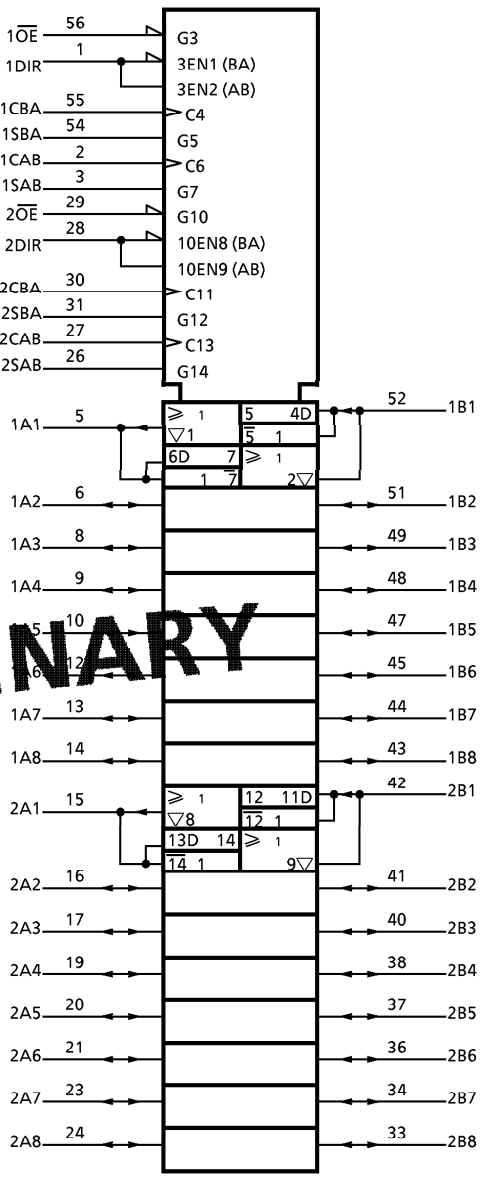
Note 1) Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.
2) All floating (high impedance) bus terminal must have their input level fixed by means of pull up or pull down resistors.

PIN ASSIGNMENT



(TOP VIEW)

SYMBOL



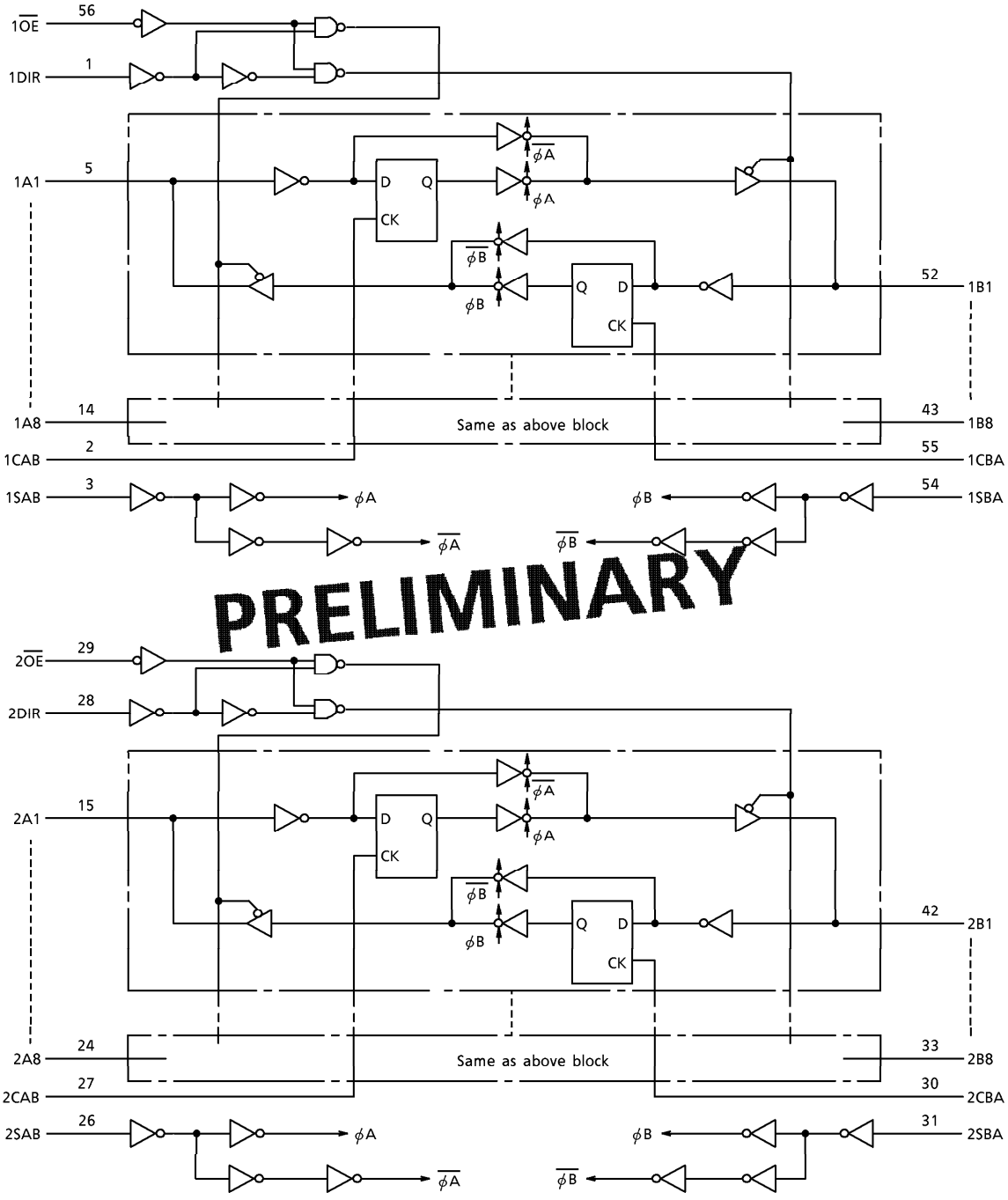
TRUTH TABLE

CONTROL INPUTS						BUS		FUNCTION
$\overline{OE}$	DIR	CAB	CBA	SAB	SBA	A	B	
H	X	X*	X*	X	X	INPUT	INPUT	The output functions of A and B Busses are disabled.
						Z	Z	
		↓	↓	X	X	X	X	Both A and B Busses are used as inputs to the internal flip-flops. Data on the Bus will be stored on the rising edge of the Clock.
L	H	X*	X*	L	X	INPUT	OUTPUT	The data on the A bus are displayed on the B bus.
						L	L	
						H	H	
		↓	X*	L	X	L	L	The data on the A bus are displayed on the B Bus, and are stored into the A storage flip-flops on the rising edge of CAB.
						H	H	
		X*	X*	H	X	X	Qn	The data in the A storage flop-flops are displayed on the B Bus.
		↓	X*	H	X	L	L	The data on the A Bus are stored into the A storage flip-flops on the rising edge of CAB, and the stored data propagate directly onto the B Bus.
						H	H	
L	L	X*	X*	X	X	OUTPUT	INPUT	The data on the B Bus are displayed on the A bus.
						L	L	
						H	H	
		X*	↓	X	L	L	L	The data on the B Bus are displayed on the A Bus, and are stored into the B storage flip-flops on the rising edge of CBA.
						H	H	
		X*	X*	X	H	Qn	X	The data in the B storage flip-flops are displayed on the A Bus.
		X*	↓	X	H	L	L	The data on the B Bus are stored into the B storage flip-flops on the rising edge of CBA, and the stored data propagate directly onto the A Bus.
						H	H	

X : Don't care
Z : High Impedance
Qn : The data stored into the internal flip-flops by most recent low to high transition of the clock inputs.

* The clocks are not internally with either $\overline{OE}$ or DIR. Thefore, data on the A and / or B Busses may be clocked into the storage flip-flops at any time.

SYSTEM DIAGRAM



PRELIMINARY