CMOS 8-Bit Microcontroller

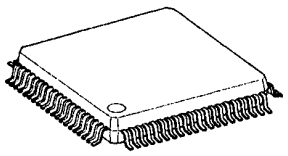
TMP86CP24F

The TMP86CP24 is the high-speed, high-performance and low-power consumption 8-bit microcomputer, including ROM, RAM, LCD driver, multi-function timer/counter, serial interface (UART, HSIO), a 10-bit AD converter and two clock generators on chip.

Product No.	ROM	RAM	Package	Flash MCU	Emulation Chip
TMP86CP24F	48 K × 8 bits	2 K × 8 bits	P-LQFP80-1212-0.50A	TMP86FP24F	TMP86C948XB

Feautures

P-LQFP80-1212-0.50A



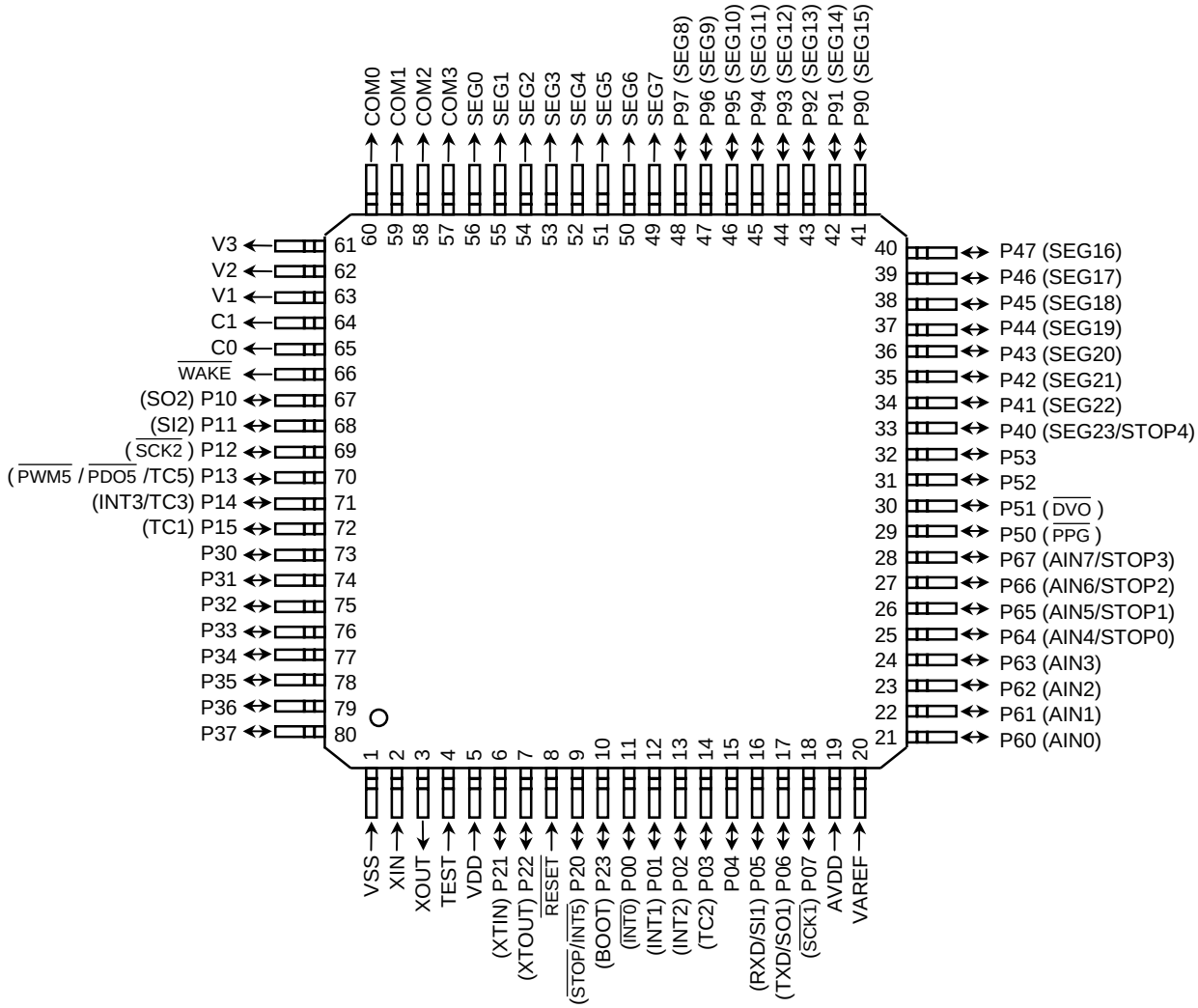
TMP86CP24

- 8-bit single chip microcomputer TLCS-870/C series
- Instruction execution time: 0.25 μs (at 16 MHz)
  122 μs (at 32.768 kHz)
- 132 types and 731 basic instructions
- 19 interrupt sources (External: 5, Internal: 14)
- Input/output ports (54 pins)
  (Out of which 16 pins are also used as SEG pins)
- 16-bit timer counter: 2 ch
  - Timer, event counter, pulse width measurement, external trigger timer, window, PPG output modes
- 8-bit timer counter: 2 ch
  - Timer, event counter, PWM output, programmable divider output, capture modes
- Time base timer
- Divider output function
- Watchdog timer
  - Interrupt source/internal reset generate (Programmable)

- Serial interface
  - UART/SIO: 1ch
  - SIO: 1ch
- ROM corrective function
  - Four register bank
  - 1 byte or 2 bytes replace mode
  - Address replace mode
- 10-bit successive approximation type AD converter
  - Analog input: 8 ch
- Five key-on wakeup pins
- LCD driver/controller
  - Built-in voltage booster for LCD driver
  - With display memory (12 bytes)
  - LCD direct drive capability (Max 24 seg × 4 com)
  - 1/4, 1/3, 1/2 duties or static drive are programmably selectable
- Dual clock operation
  - Single/dual clock mode
- Nine power saving operating modes
  - STOP mode: Oscillation stops. Battery/capacitor backup. Port output hold/high impedance.
  - SLOW1, 2 mode: Low power consumption operation using low-frequency clock (32.768 kHz).
  - IDLE0 mode: CPU stops, and peripherals operate using high-frequency clock of time-base-timer. Release by falling edge of TBTCR<TBTCK> setting.
  - IDLE1 mode: CPU stops, and peripherals operate using high-frequency clock. Release by interrupts.
  - IDLE2 mode: CPU stops, and peripherals operate using high and low frequency clock. Release by interrupts.
  - SLEEP0 mode: CPU stops, and peripherals operate using low-frequency clock of time-base-timer. Release by falling edge of TBTCR<TBTCK> setting.
  - SLEEP1 mode: CPU stops, and peripherals operate using low-frequency clock. Release by interrupts.
  - SLEEP2 mode: CPU stops, and peripherals operate using high and low frequency clock. Release by interrupts.
- Wide operating voltage: 1.8 to 3.6V at 8 MHz/32.768 kHz
  2.7 to 3.6V at 16 MHz/32.768 kHz

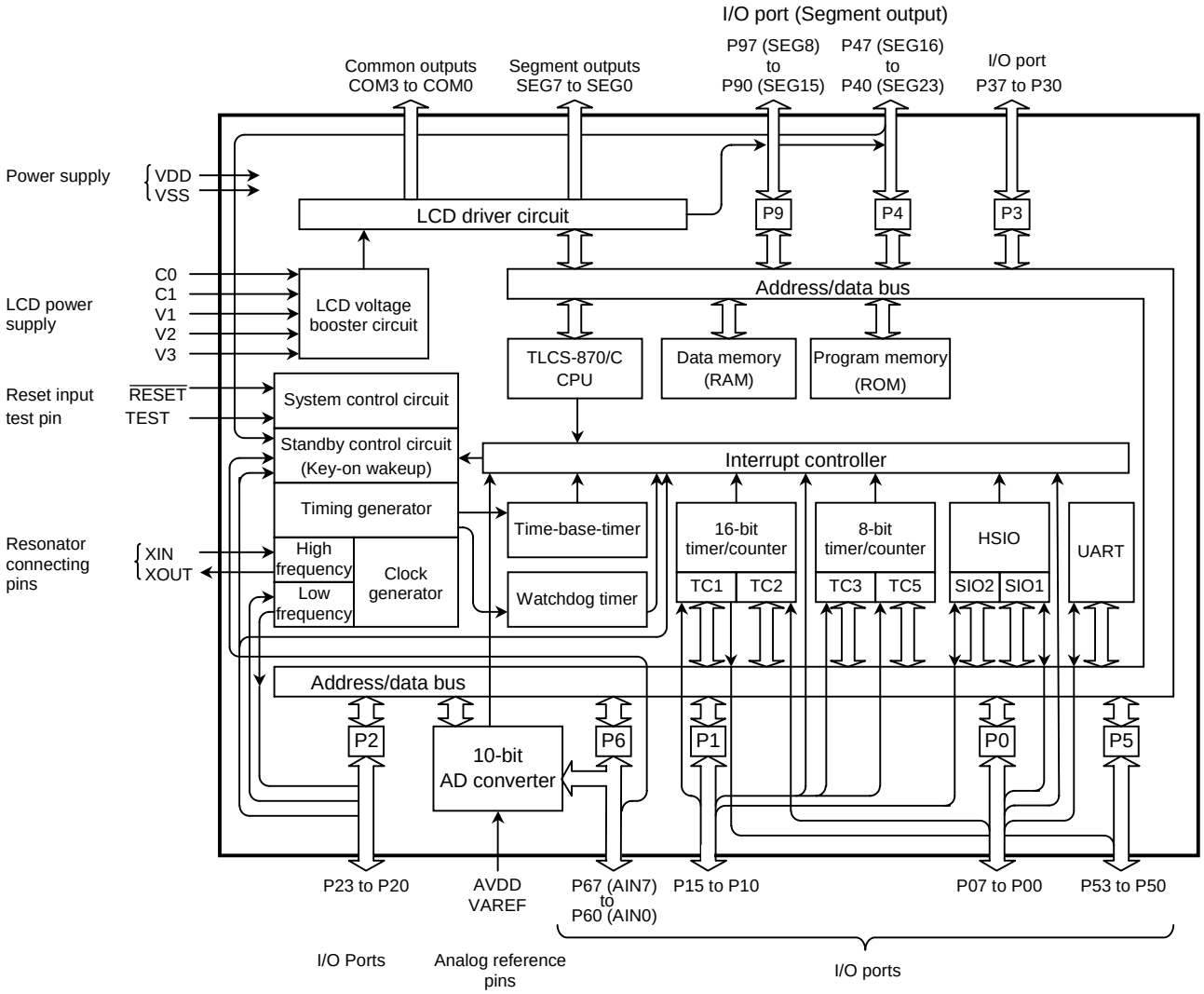
Pin Assignments (Top view)

P-LQFP80-1212-0.50A



Note: BOOT function of P23 is included in only TMP86FP24F.

Block Diagram



Pin Functions (1/2)

Pin Name	Input/Output	Functions	
P07 ($\overline{SCK1}$)	I/O (I/O)	8-bit input/output port with latch. When used as a serial interface output or UART output, respective output latch (P0DR) should be set to “1”. When used as an input port, an serial interface input, UART input, timer counter input or an external interrupt input, respective output control (P0OUTCR) should be cleared to “0” after setting P0DR to “1”.	Serial clock input/output 1
P06 (TXD, SO1)	I/O (Output)		UART data output, serial data output 1
P05 (RXD, SI1)	I/O (Input)		UART data input, serial data input 1
P04	I/O		
P03 (TC2)	I/O (Input)		Timer counter 2 input
P02 (INT2)	I/O (Input)		External interrupt 2 input
P01 (INT1)	I/O (Input)		External interrupt 1 input
P00 ($\overline{INT0}$)	I/O (Input)		External interrupt 0 input
P15 (TC1)	I/O (Input)	6-bit input/output port with latch. When used as a timer/counter output or serial interface output, respective output latch (P1DR) should be set to “1”. When used as an input port, a timer counter input, an external interrupt input or serial interface input, respective output control (P1OUTCR) should be cleared to “0” after setting P1DR to “1”.	Timer counter 1 input
P14 (TC3, INT3)	I/O (Input)		Timer counter 3 input, External interrupt 3 input
P13 ($\overline{PWM5}$, $\overline{PDO5}$, TC5)	I/O (I/O)		PWM5 output, PDO5 output, Timer/counter 5 input
P12 ($\overline{SCK2}$)	I/O (I/O)		Serial clock input/output 2
P11 (SI2)	I/O (Input)		Serial data input 2
P10 (SO2)	I/O (Output)		Serial data output 2
P23	I/O	4-bit input/output port with latch. When used as an input port or an external interrupt input, respective output control (P2OUTCR) should be cleared to “0” after setting output latch (P2DR) to “1”.	
P22 (XTOUT)	I/O (Output)		Resonator connecting pins (32.768 kHz) For inputting external clock, XTIN is used and XTOUT is opened.
P21 (XTIN)	I/O (Input)		
P20 ($\overline{INT5}$, $\overline{STOP}$)	I/O (Input)		External interrupt input 5 or STOP mode release signal input
P37 to P30	I/O	8-bit input/output port with latch (N-ch high current output). When used as an input port, respective output control (P3OUTCR) should be cleared to “0” after setting output latch (P3DR) to “1”.	
P47 (SEG16) to P41 (SEG22)	I/O (Output)	7-bit input/output port with latch. When used as an input port, respective output latch (P4DR) should be set to “1” after LCD output control (P4LCR) is cleared to “0”.	LCD segment output
P40 (SEG23, STOP4)	I/O (I/O)	1-bit input/output port with latch. When used as an input port, the output latch (P4DR) should be set to “1” after the LCD output control (P4LCR) is cleared to “0”. When used as a LCD output, the P4LCR should be set to “1” after the STOPCR<STOP4EN> should be cleared to “0”. When used as a key-on wakeup input, the STOPCR<STOP4EN> should be set to “1”.	LCD segment output STOP mode release input
P53	I/O	4-bit input/output port with latch (N-ch high current output). When used as an input port, respective output control (P5OUTCR) should be cleared to “0” after setting output latch (P5DR) to “1”. When used as a PPG output or divider output, respective P5DR should be set to “1”.	
P52	I/O		
P51 ($\overline{DVO}$)	I/O (Output)		Divider output
P50 ($\overline{PPG}$)	I/O (Output)		PPG output

Pin Functions (1/2)

Pin Name	Input/Output	Functions		
P67 (AIN7, STOP3)	I/O (Input)	8-bit programmable input/output port (Tri-state). Each bit of this port can be individually configured as an input or an output under software control. When used as an input port, respective input/output control (P6CR1) should be cleared to "0" after setting input control (P6CR2) to "1". When used as an analog input or key-on wakeup input, respective P6CR1 should be cleared to "0" after clearing P6CR2 to "0". When used as a key-on wakeup input, STOPCR<STOPiEN> should be set to "1". (i = 0 to 3)	STOP 3 input	AD converter analog inputs
P66 (AIN6, STOP2)	I/O (Input)		STOP 2 input	
P65 (AIN5, STOP1)	I/O (Input)		STOP 1 input	
P64 (AIN4, STOP0)	I/O (Input)		STOP 0 input	
P63 (AIN3)	I/O (Input)			
P62 (AIN2)	I/O (Input)			
P61 (AIN1)	I/O (Input)			
P60 (AIN0)	I/O (Input)			
P97 (SEG8) to P90 (SEG15)	I/O (Output)	8-bit input/output port with latch. When used as an input port, respective output latch (P9DR) should be set to "1" after LCD output control (P9LCR) is cleared to "0".	LCD segment output	
SEG7 to SEG0	Output	LCD segment outputs		
COM3 to COM0		LCD common outputs		
V3 to V1	LCD voltage booster pin	LCD voltage booster pin. Capacitors are required between C0 and C1 pin and V1/V2/V3 pin and GND.		
C1 to C0				
$\overline{\text{WAKE}}$	Output	STOP mode monitor output. During CPU operation (including IDLE0/1/2, SLEEP0/1/2, warm-up period), it becomes "L" level state. In RESET and STOP mode, it becomes the high-impedance state.		
XIN, XOUT	Input output	Resonator connecting pins for high-frequency clock. For inputting external clock, XIN is used and XOUT is opened.		
$\overline{\text{RESET}}$	Input	Reset signal input		
TEST	Input	Test pin for out-going test. Be fixed to low.		
VDD, VSS	Power supply	Power supply for operation		
VAREF		Analog reference voltage for AD conversion		
AVDD		AD circuit power supply		

Operational Description

1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, and an interrupt controller.

This section provides a description of the CPU core, the program memory, the data memory, the external memory interface, and the reset circuit.

1.1 Memory Address Map

The TMP86CP24 memory consists of 4 blocks: ROM, RAM, DBR (Data buffer register) and SFR (Special function register). They are all mapped in 64-Kbyte address space. Figure 1.1.1 shows the TMP86CP24 memory address map. The general-purpose registers are not assigned to the RAM address space.

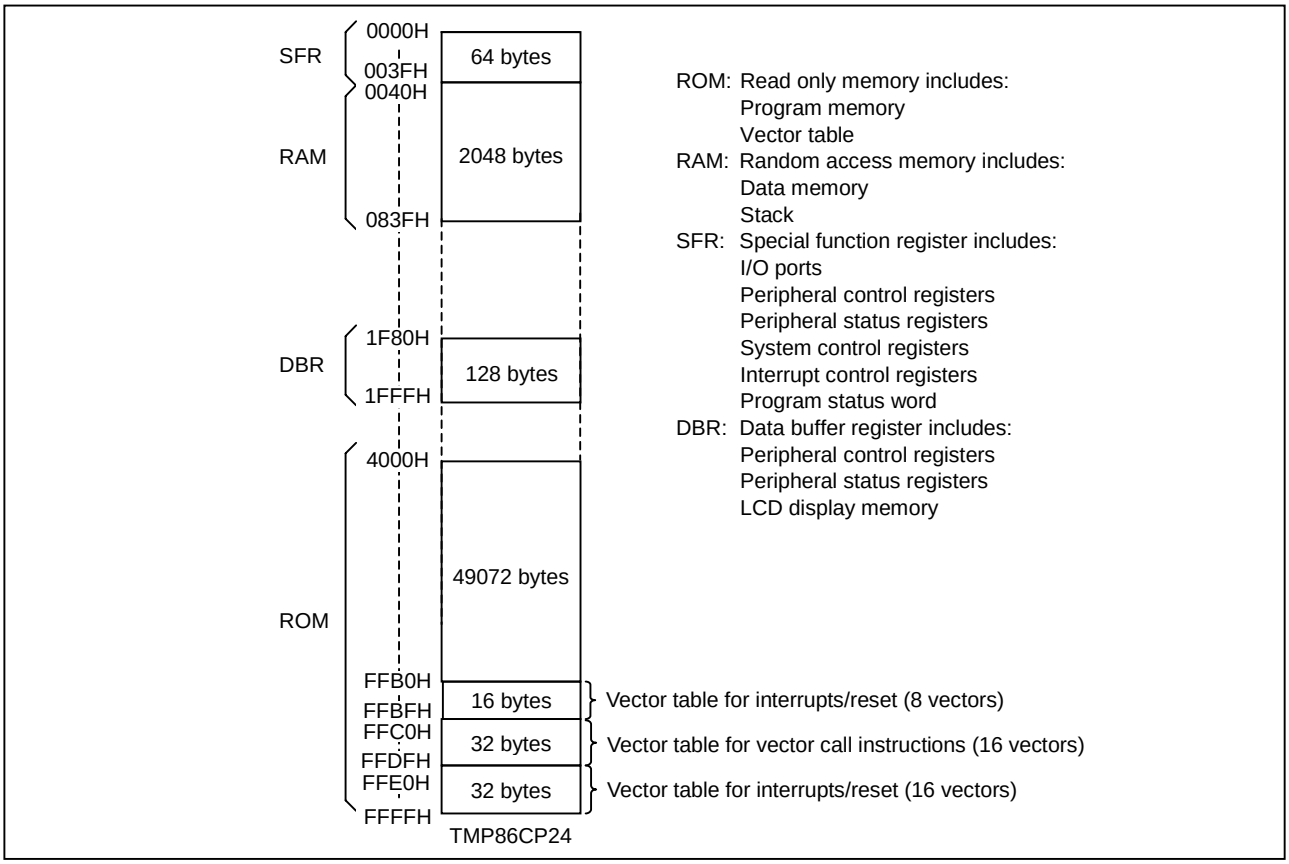


Figure 1.1.1 Memory Address Maps

1.2 Program Memory (ROM)

The TMP86CP24 has a 48 K × 8 bits (Address 4000H to FFFFH) of program memory (Mask programmed ROM).

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Pins	Rating	Unit
Supply voltage	V_{DD}		−0.3 to 4.0	V
Input voltage	V_{IN}		−0.3 to V_{DD} + 0.3	
Output voltage	V_{OUT1}	Except V3 pin	−0.3 to V_{DD} + 0.3	
	V_{OUT2}	V3 pin	-0.3 to 4.0	
Output current (Per 1 pin)	I_{OUT1}	P0, P1, P20, P23, P3, P5, P6 ports	−2	mA
	I_{OUT2}	P0, P1, P2, P4, P6, P9, $\overline{\text{WAKE}}$ ports	2	
	I_{OUT3}	P3, P5 Ports	10	
Output current (Total)	ΣI_{OUT1}	P0, P1, P20, P23, P3, P5, P6 ports	−80	
	ΣI_{OUT2}	P0, P1, P2, P4, P6, P9, $\overline{\text{WAKE}}$ ports	80	
	ΣI_{OUT3}	P3, P5 ports	30	
Power dissipation [Topr = 85°C]	PD		350	mW
Soldering temperature (time)	Tsld		260 (10 s)	°C
Storage temperature	Tstg		−55 to 125	
Operating temperature	Topr		−40 to 85	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Condition (V_{SS} = 0 V, Topr = −40 to 85°C)

Parameter	Symbol	Pins	Condition		Min	Max	Unit
Supply voltage	V_{DD}		fc = 16 MHz	NORMAL1, 2 mode	2.7	3.6	V
				IDLE0, 1, 2 mode			
			fc = 8 MHz (In case of connecting the resonator)	NORMAL1, 2 mode	1.8		
				IDLE0, 1, 2 mode			
			fc = 4.2 MHz (In case of external clock input)	NORMAL1, 2 mode			
				IDLE0, 1, 2 mode			
			fs = 32.768 kHz	SLOW1, 2 mode	1.8		
				SLEEP0, 1, 2 mode			
				STOP mode			
Input high level	V_{IH1}	Except hysteresis input	$V_{DD} \geq 2.7$ V		$V_{DD} \times 0.70$	V_{DD}	
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 2.7$ V		$V_{DD} \times 0.80$		
Input low level	V_{IL1}	Except hysteresis input	$V_{DD} \geq 2.7$ V		0	$V_{DD} \times 0.30$	
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 2.7$ V			$V_{DD} \times 0.20$	
Clock frequency (In case of connecting the resonator)	fc	XIN, XOUT	V_{DD} = 1.8 to 3.6 V		1.0	8.0	MHz
			V_{DD} = 2.7 to 3.6 V			16.0	
	fs	XTIN, XTOUT	V_{DD} = 1.8 to 3.6 V		30.0	34.0	kHz
Clock frequency (In case of external clock input)	fc	XIN, XOUT	V_{DD} = 1.8 to 3.6 V		1.0	4.2	MHz
			V_{DD} = 2.7 to 3.6 V			16.0	
	fs	XTIN, XTOUT	V_{DD} = 1.8 to 3.6 V		30.0	34.0	kHz
LCD reference voltage	V1		Booster circuit is enable ($V3 \geq V_{DD}$)		0.8	1.2	V
	V2				1.6	2.4	
Capacity for LCD booster circuit	C_{LCD}		LCD booster circuit is enable ($V3 \geq V_{DD}$)		0.1	0.47	μF

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (Supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

DC Characteristics (V_{SS} = 0 V, Topr = −40 to 85°C)

Parameter	Symbol	Pins	Condition	Min	Typ.	Max	Unit
Hysteresis voltage	V_{HS}	Hysteresis input	V_{DD} = 3.3 V	–	0.4	–	V
Input current	I_{IN1}	TEST	V_{DD} = 3.6 V, V_{IN} = 0 V	–	–	−5	μA
	I_{IN2}	Sink open drain, Tri-state	V_{DD} = 3.6 V, V_{IN} = 3.6 V/0 V	–	–	±5	
	I_{IN4}	$\overline{RESET}$	V_{DD} = 3.6 V, V_{IN} = 3.6 V	–	–	+5	
Input resistor	R_{IN1}	TEST pull down	V_{DD} = 3.6 V, V_{IN} = 3.6 V	–	70	–	kΩ
	R_{IN2}	$\overline{RESET}$ pull up P21,P22 ports	V_{DD} = 3.6 V, V_{IN} = 0 V	100	220	450	
	R_{IN3}	Programmable pull down (P4, P9 Ports)		–	T.B.D.	–	
High frequency feedback resistor	R_{FB}	XOUT	V_{DD} = 3.6 V	–	3	–	MΩ
Low frequency feedback resistor	R_{FBT}	XTOUT	V_{DD} = 3.6 V	–	20	–	
Output leakage current	I_{LO}	Sink open drain, Tri-state	V_{DD} = 3.6 V V_{OUT} = 3.4V / 0.2 V	–	–	±10	μA
Output high voltage	V_{OH}	CMOS, Tri-state	V_{DD} = 3.6 V, I_{OH} = −0.6 mA	3.2	–	–	V
Output low voltage	V_{OL}	Except XOUT,P3 and P5 ports	V_{DD} = 3.6 V, I_{OL} = 0.9 mA	–	–	0.4	
Output low current	I_{OL}	P3, P5 ports	V_{DD} = 3.6 V, V_{OL} = 1.0 V	–	6	–	mA
LCD output voltage (LCD booster is enable)	$V_{2\text{-}3OUT}$	V2 pin	$V3 \geq V_{DD}$ Reference supply pin: V1 SEG/COM pin: No load	–	V1 × 2	–	V
		V3 pin		–	V1 × 3	–	
	$V_{1\text{-}3OUT}$	V1 pin	$V3 \geq V_{DD}$ Reference supply pin: V2 SEG/COM pin: No load	–	V2 × 1/2	–	
		V3 pin		–	V2 × 3/2	–	
LCD output current capacity (LCD booster is enable)	I_{LCDV3}	V3 pin	V_{DD} = 3 V, fc = 16 MHz, C_{LCD} = 0.1 μF, Reference supply pin: V1 = 1 V, <VFSEL> = 00	–	T.B.D.	–	mV/μA
			<VFSEL> = 01	–	T.B.D.	–	
			<VFSEL> = 10	–	T.B.D.	–	
			<VFSEL> = 11	–	T.B.D.	–	
			V_{DD} = 3 V, fc = 16 MHz, C_{LCD} = 0.1 μF, Reference supply pin: V2 = 2V, <VFSEL> = 00	–	T.B.D.	–	
			<VFSEL> = 01	–	T.B.D.	–	
			<VFSEL> = 10	–	T.B.D.	–	
			<VFSEL> = 11	–	T.B.D.	–	
Supply current in NORMAL 1, 2 mode	I_{DD}		V_{DD} = 3.6 V V_{IN} = 3.4 V/0.2 V fc = 16 MHz fs = 32.768 kHz	–	T.B.D.	T.B.D.	mA
Supply current in IDLE 0, 1, 2 mode				–	T.B.D.	T.B.D.	
Supply current in SLOW 1 mode			V_{DD} = 3 V V_{IN} = 2.8 V/0.2 V fs = 32.768 kHz	–	T.B.D.	T.B.D.	μA
Supply current in SLEEP 1 mode				–	T.B.D.	T.B.D.	
Supply current in SLEEP 0 mode				–	T.B.D.	T.B.D.	
Supply current in STOP mode			V_{DD} = 3.6 V V_{IN} = 3.4 V/0.2 V	–	T.B.D.	T.B.D.	

Note 1: Typical values show those at Topr = 25°C, V_{DD} = 3.3 V

Note 2: Input current (I_{IN1}, I_{IN2}): The current through pull-up or pull-down resistor is not included.

Note 3: I_{DD} does not include I_{REF} current.

Note 4: The supply currents of SLOW 2 and SLEEP 2 modes are equivalent to IDLE 0, 1, 2.

Note 5: Current capacity indicates the drop in pin V3 output voltage per 1 μA. Select an appropriate booster frequency setting in LCDCR<VFSEL> according to LCD panel. To maintain stable operation, the current capacity for the reference pin must be more than ten times that of the output current capacity.

AD Conversion Characteristics (V_{SS} = 0.0 V, 2.7 V ≤ V_{DD} ≤ 3.6 V, Topr = −40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog reference voltage	V_{AREF}		A_{VDD} − 1.0	−	A_{VDD}	V
Power supply voltage of analog control circuit	A_{VDD}		V_{DD}			
Analog reference voltage range (Note 4)	ΔV_{AREF}		2.5	−	−	
Analog input voltage	V_{AIN}		V_{SS}	−	V_{AREF}	
Power supply current of analog reference voltage	I_{REF}	V_{DD} = A_{VDD} = V_{AREF} = 3.6 V V_{SS} = 0.0 V	−	T.B.D.	T.B.D.	mA
Non linearity error		V_{DD} = A_{VDD} = 2.7 V V_{SS} = 0.0 V V_{AREF} = 2.7 V	−	−	±2	LSB
Zero point error			−	−	±2	
Full scale error			−	−	±2	
Total error			−	−	±2	

(V_{SS} = 0.0 V, 2.0 V ≤ V_{DD} < 2.7 V, Topr = −40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog reference voltage	V_{AREF}		A_{VDD} − 0.6	−	A_{VDD}	V
Power supply voltage of analog control circuit	A_{VDD}		V_{DD}			
Analog reference voltage range (Note 4)	ΔV_{AREF}		2.0	−	−	
Analog input voltage	V_{AIN}		V_{SS}	−	V_{AREF}	
Power supply current of analog reference voltage	I_{REF}	V_{DD} = A_{VDD} = V_{AREF} = 2.0V V_{SS} = 0.0 V	−	T.B.D.	T.B.D.	mA
Non linearity error		V_{DD} = A_{VDD} = 2.0 V V_{SS} = 0.0 V V_{AREF} = 2.0 V	−	−	±4	LSB
Zero point error			−	−	±4	
Full scale error			−	−	±4	
Total error			−	−	±4	

(V_{SS} = 0.0 V, 1.8 V ≤ V_{DD} < 2.0 V, Topr = −10 to 85°C) (Note 5)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog reference voltage	V_{AREF}		A_{VDD} − 0.1	−	A_{VDD}	V
Power supply voltage of analog control circuit	A_{VDD}		V_{DD}			
Analog reference voltage range (Note 4)	ΔV_{AREF}		1.8	−	−	
Analog input voltage	V_{AIN}		V_{SS}	−	V_{AREF}	
Power supply current of analog reference voltage	I_{REF}	V_{DD} = A_{VDD} = V_{AREF} = 1.8V V_{SS} = 0.0 V	−	T.B.D.	T.B.D.	mA
Non linearity error		V_{DD} = A_{VDD} = 1.8 V V_{SS} = 0.0 V V_{AREF} = 1.8 V	−	−	±4	LSB
Zero point error			−	−	±4	
Full scale error			−	−	±4	
Total error			−	−	±4	

Note 1: The total error includes all errors except a quantization error, and is defined as a maximum deviation from the ideal conversion line.

Note 2: Conversion time is different in recommended value by power supply voltage.
About conversion time, please refer to 2.12.2 “Register configuration”.

Note 3: Please use input voltage to AIN input Pin in limit of V_{AREF} − V_{SS}.
When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.

Note 4: Analog reference voltage range: ΔV_{AREF} = V_{AREF} − V_{SS}

Note 5: When AD is used with V_{DD} < 2.0 V, the guaranteed temperature range varies with the operating voltage.

Note 6: When AD converter is not used, fix the AVDD pin on the VDD level.

AC Characteristics (V_{SS} = 0 V, V_{DD} = 2.7 to 3.6 V, Topr = –40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine cycle time	tcy	NORMAL1, 2 mode	0.25	–	4	μs
		IDLE1, 2 mode				
		SLOW1, 2 mode	117.6	–	133.3	
		SLEEP1, 2 mode				
High level clock pulse width	twcH	For external clock operation (XIN input) fc = 16 MHz	–	31.25	–	ns
Low level clock pulse width	twcL					
High level clock pulse width	twcH	For external clock operation (XTIN input) fs = 32.768 kHz	–	15.26	–	μs
Low level clock pulse width	twcL					

(V_{SS} = 0 V, V_{DD} = 1.8 to 3.6 V, Topr = –40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine cycle time	tcy	NORMAL1, 2 mode	0.5	–	4	μs
		IDLE1, 2 mode				
		SLOW1, 2 mode	117.6	–	133.3	
		SLEEP1, 2 mode				
High level clock pulse width	twcH	For external clock operation (XIN input) fc = 4.2 MHz	–	119.04	–	ns
Low level clock pulse width	twcL					
High level clock pulse width	twcH	For external clock operation (XTIN input) fs = 32.768 kHz	–	15.26	–	μs
Low level clock pulse width	twcL					

Recommended Oscillating Conditions

Note 1: An electrical shield by metal shield plate on the surface of IC package is recommended in order to protect the device from the high electric field stress applied from CRT (Cathodic ray tube) for continuous reliable operation.

Note 2: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL:
http://www.murata.co.jp/search/index.html