2.95-V to 6-V Input, 6-A Output, 2-MHz, Synchronous Step-Down Switcher With Integrated FETs

Check for Samples: TPS54618-Q1

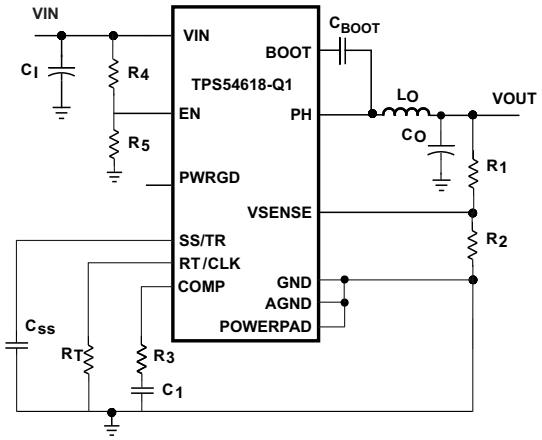
FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C4B
- Two 12-mΩ (Typical) MOSFETs for High Efficiency at 6-A Loads
- 300-kHz to 2-MHz Switching Frequency
- 0.8-V ±1% Voltage Reference Overtemperature (–40°C to 150°C)
- Synchronizes to External Clock
- Adjustable Slow Start and Sequencing
- UV and OV Power-Good Output
- Thermally Enhanced 3-mm × 3-mm 16-pin QFN

APPLICATIONS

- Low-Voltage, High-Density Power Systems
- Point-of-Load Regulation for High-Performance DSPs, FPGAs, ASICs and Microprocessors
- Broadband, Networking, and Optical Communications Infrastructure

SIMPLIFIED SCHEMATIC



DESCRIPTION

The TPS54618RTE-Q1 SWIFT™ integrated circuit is a full-featured 6-V, 6-A, synchronous step-down current-mode converter with two integrated MOSFETs.

The TPS54618RTE-Q1 enables small designs by integrating the MOSFETs, implementing current-mode control to reduce external component count, reducing inductor size by enabling up to 2-MHz switching frequency, and minimizing the IC footprint with a small 3-mm × 3-mm thermally enhanced QFN package.

The TPS54618RTE-Q1 provides accurate regulation for a variety of loads with an accurate ±1% voltage reference (VREF) overtemperature.

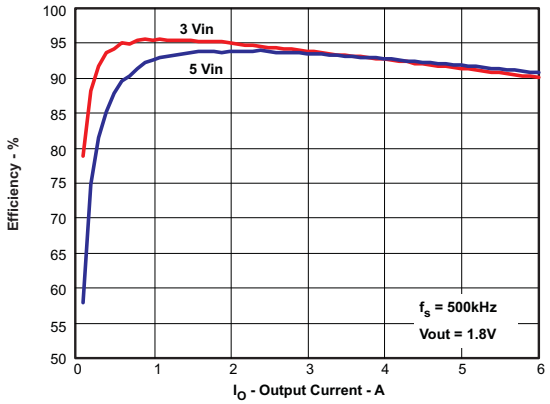
The integrated 12-mΩ MOSFETs and 515-µA typical supply current maximize efficiency. Using the enable pin reduces the shutdown supply current to 5.5 µA when the device enters shutdown mode.

The undervoltage lockout internal setting is 2.6 V, but can be increased by programming the threshold with a resistor network on the enable pin. The slow-start pin controls the output-voltage start-up ramp. An open-drain power-good signal indicates when the output is within 93% to 107% of its nominal voltage.

Frequency foldback and thermal shutdown protect the device during an overcurrent condition.

The SwitcherPro™ software tool, available at www.ti.com/switcherpro, supports the TPS54618RTE-Q1.

For more SWIFT™ integrated-circuit documentation, see the TI Web site at www.ti.com/swift.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DEVICE INFORMATION(1)(2)

T_A	P/N	PACKAGE	TOP-SIDE MARKING
–40ºC to 125ºC	TPS54618QRTERQ1	QFN, 3x3	618Q1

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS(1)

		VALUE	UNIT
Input voltage	VIN	–0.3 to 7	V
	EN	–0.3 to 3.3	
	BOOT	PH + 7	
	VSENSE	–0.3 to 3	
	COMP	–0.3 to 3	
	PWRGD	–0.3 to 7	
	SS/TR	–0.3 to 3	
	RT/CLK	–0.3 to 3.3	
Output voltage	BOOT-PH	7	V
	PH	–0.6 to 7	
	PH, 10-ns transient	–2 to 10	
Source current	EN	100	µA
	RT/CLK	100	
Sink current	COMP	100	µA
	PWRGD	10	mA
	SS/TR	100	µA
Electrostatic discharge (ESD) ratings	Human-body model, (HBM) AEC-Q100 Classification Level H2	2	kV
	Charged-device model, (CDM) AEC-Q100 Classification Level C4B	750	V
Temperature	T_J	–40 to 150	°C
	T_{stg}	–65 to 150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS54618-Q1 RTE 16 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance(2)	45.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	43.1	°C/W
θ_{JB}	Junction-to-board thermal resistance(4)	18.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter(5)	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter(6)	18.5	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	4.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

T_A = –40°C to 125°C, VIN = 2.95 to 6 V (unless otherwise noted)

DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)					
Operating input voltage		2.95		6	V
Internal undervoltage lockout threshold	VIN UVLO STOP		2.28	2.5	V
	VIN UVLO START		2.45	2.6	
Shutdown supply current	EN = 0 V, 25°C, 2.95 V ≤ VIN ≤ 6 V		5.5	15	µA
Quiescent current - I_q	VSENSE = 0.9 V, VIN = 5 V, 25°C, RT = 400 kΩ		515	650	µA
ENABLE AND UVLO (EN PIN)					
Enable threshold	Rising		1.25		V
	Falling		1.18		
Input current	Enable threshold + 50 mV		–3.5		µA
	Enable threshold – 50 mV		–1.9		
VOLTAGE REFERENCE (VSENSE PIN)					
Voltage reference	2.95 V ≤ VIN ≤ 6 V, –40°C <T_J < 150°C	0.791	0.799	0.807	V
MOSFET					
High-side switch resistance	BOOT-PH = 5 V		12	25	mΩ
	BOOT-PH = 2.95 V		16	33	
Low-side switch resistance	VIN = 5 V		13	25	mΩ
	VIN = 2.95 V		17	33	
ERROR AMPLIFIER					
Input current			2		nA
Error amplifier transconductance (gm)	–2 µA < $I_{(COMP)}$ < 2 µA, $V_{(COMP)}$ = 1 V		245		µmhos
Error amplifier transconductance (gm) during slow start	–2 µA < $I_{(COMP)}$ < 2 µA, $V_{(COMP)}$ = 1 V, VSENSE = 0.4 V		79		µmhos
Error amplifier source or sink	$V_{(COMP)}$ = 1 V, 100-mV overdrive		±20		µA
COMP to Iswitch gm			25		A/V

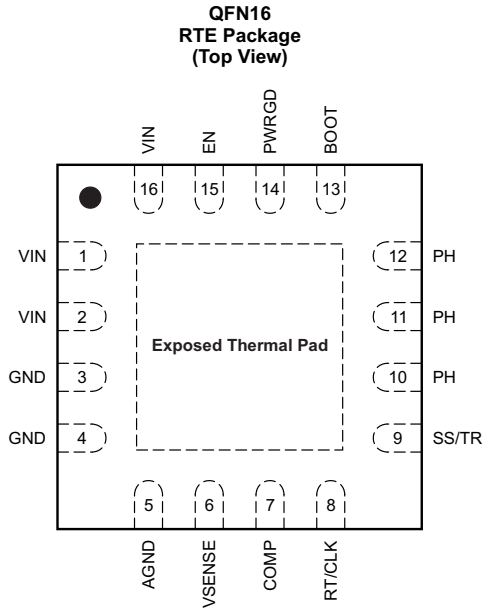
ELECTRICAL CHARACTERISTICS (continued)

T_A = –40°C to 125°C, VIN = 2.95 to 6 V (unless otherwise noted)

DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT					
Current-limit threshold	VIN = 6 V, 25°C < T_J < 150°C	7.46	10.6	15.3	A
	VIN = 2.95 V, 25°C < T_J < 150°C	7.68	10.2	13.5	
THERMAL SHUTDOWN					
Thermal Shutdown			168		°C
Hysteresis			20		°C
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)					
Switching-frequency range using RT mode		200		2000	kHz
Switching frequency	RT = 400 kΩ	400	500	600	kHz
Switching-frequency range using CLK mode		300		2000	kHz
Minimum CLK pulse duration		75			ns
RT/CLK voltage	$R_{(RT/CLK)}$ = 400 kΩ		0.5		V
RT/CLK high threshold			1.6	2.5	V
RT/CLK low threshold		0.4	0.6		V
RT/CLK falling edge to PH rising edge delay	Measure at 500 kHz with RT resistor in series		90		ns
PLL lock-in time	Measure at 500 kHz		42		µs
PH (PH PIN)					
Minimum on-time	Measured at 50% points on PH, I_{OUT} = 3 A		75		ns
	Measured at 50% points on PH, VIN = 6 V, I_{OUT} = 0 A		120		
Minimum off-time	Prior to skipping off-pulses, BOOT-PH = 2.95 V, I_{OUT} = 3 A		60		ns
Rise time	VIN = 6 V, 6 A		2.25		V/ns
Fall time			2		
BOOT (BOOT PIN)					
BOOT charge resistance	VIN = 5 V		16		Ω
BOOT-PH UVLO	VIN = 2.95 V		2.1		V
SLOW-START AND TRACKING (SS/TR PIN)					
Charge current	$V_{(SS/TR)}$ = 0.4 V		2		µA
SS/TR to VSENSE matching	$V_{(SS/TR)}$ = 0.4 V		54		mV
SS/TR to reference crossover	98% normal		1.1		V
SS/TR discharge voltage (overload)	VSENSE = 0 V		61		mV
SS/TR discharge current (overload)	VSENSE = 0 V, $V_{(SS/TR)}$ = 0.4 V		350		µA
SS discharge current (UVLO, EN, thermal fault)	VIN = 5 V, V(SS) = 0.5 V		1.9		mA
POWER GOOD (PWRGD PIN)					
VSENSE threshold	VSENSE falling (fault)		91		% Vre
	VSENSE rising (good)		93		
	VSENSE rising (fault)		109		
	VSENSE falling (good)		107		
Hysteresis	VSENSE falling		2		% Vref
Output high leakage	VSENSE = VREF, $V_{(PWRGD)}$ = 5.5 V		7		nA
On-resistance			56	100	Ω
Output low	$I_{(PWRGD)}$ = 3 mA		0.2	0.3	V
Minimum VIN for valid output	$V_{(PWRGD)}$ < 0.5 V at 100 µA		0.65	1.5	V

DEVICE INFORMATION

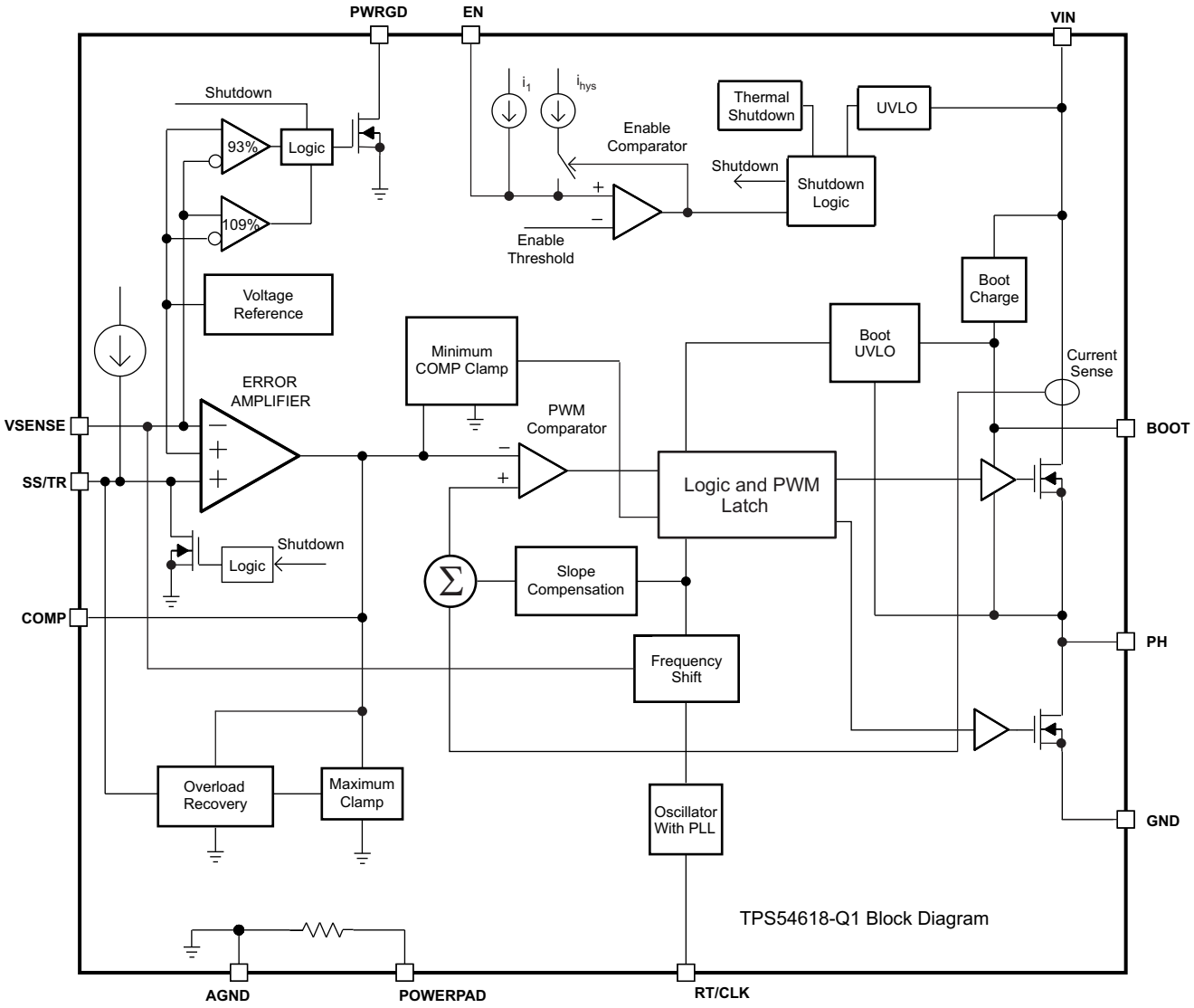
PIN CONFIGURATION



PIN FUNCTIONS

PIN		DESCRIPTION
NAME	NO.	
AGND	5	Connect analog ground electrically to GND close to the device.
BOOT	13	The device requires a bootstrap capacitor between BOOT and PH. A voltage on this capacitor below the minimum required by the BOOT UVLO forces the output to switch off until the capacitor recharges.
COMP	7	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation components to this pin.
EN	15	Enable pin, internal pullup current source. Pull below 1.2 V to disable. Float to enable. Use of two additional resistors can set the on-and-off threshold (adjust UVLO).
GND	3, 4	Directly connect this power-ground pin electrically to the thermal pad under the IC.
PH	10, 11, 12	The source of the internal high-side power MOSFET, and drain of the internal low-side (synchronous) rectifier MOSFET.
PWRGD	14	An open-drain output; asserts low if output voltage is low due to thermal shutdown, overcurrent, over or undervoltage, or EN shutdown.
RT/CLK	8	Resistor timing or external clock input pin
SS/TR	9	Slow-start and tracking. An external capacitor connected to this pin sets the output-voltage rise time. Another use of this pin can be for tracking.
VIN	1, 2, 16	Input supply voltage, 2.95 V to 6 V.
VSENSE	6	Inverting node of the transconductance (gm) error amplifier
Thermal pad		Connect the GND pin to the exposed thermal pad for proper operation. Connect this thermal pad to any internal PCB ground plane using multiple vias for good thermal performance.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS CURVES

HIGH-SIDE AND LOW-SIDE $r_{DS(on)}$ versus TEMPERATURE

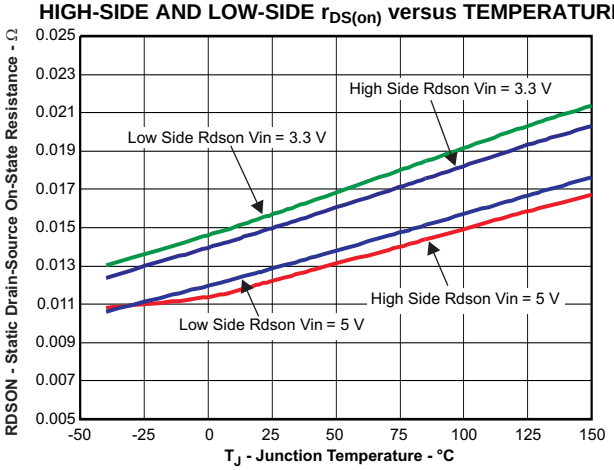


Figure 1.

FREQUENCY versus TEMPERATURE

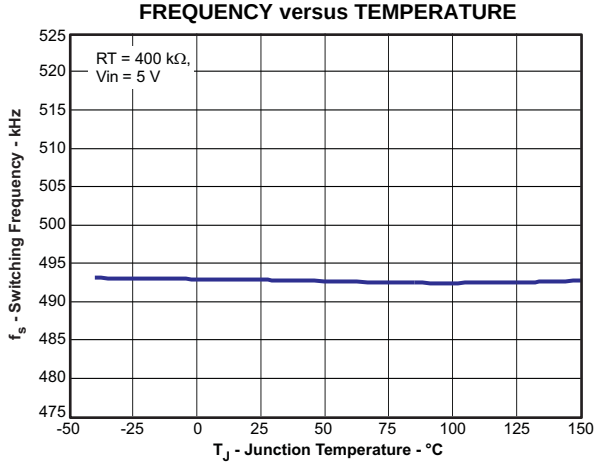


Figure 2.

HIGH-SIDE CURRENT LIMIT versus TEMPERATURE

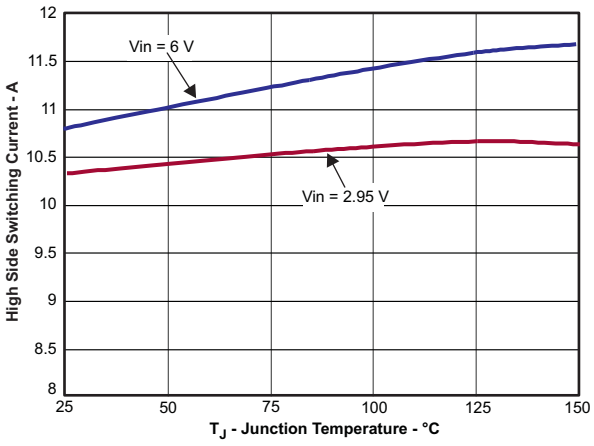


Figure 3.

VOLTAGE REFERENCE versus TEMPERATURE

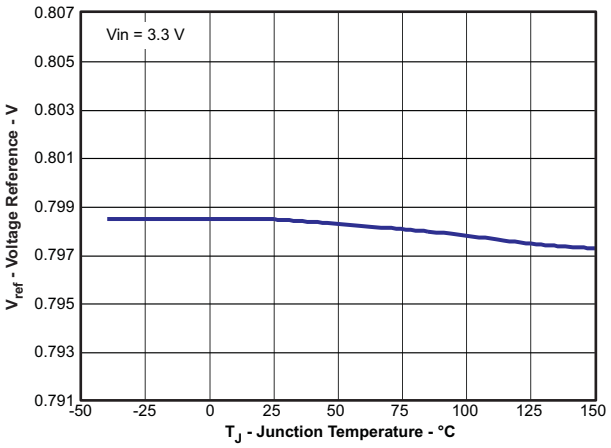


Figure 4.

SWITCHING FREQUENCY versus RT RESISTANCE LOW-FREQUENCY RANGE

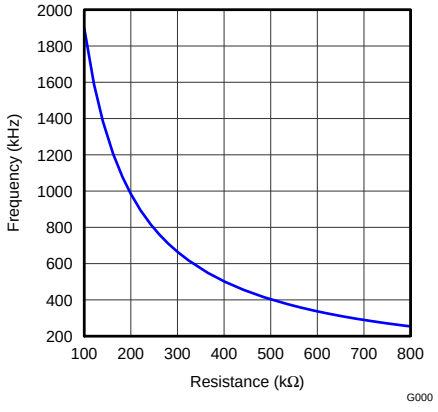


Figure 5.

SWITCHING FREQUENCY versus VSENSE

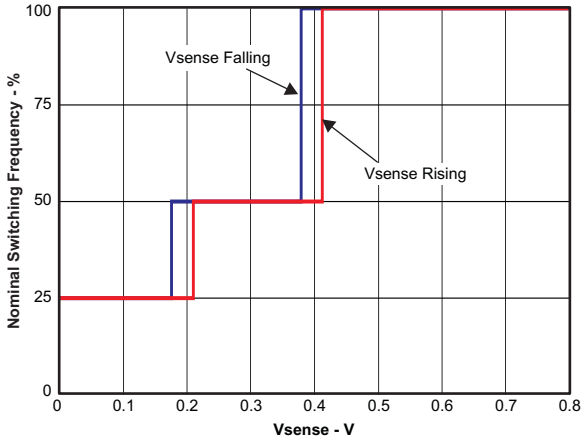


Figure 6.

TYPICAL CHARACTERISTICS CURVES (continued)

TRANSCONDUCTANCE versus TEMPERATURE

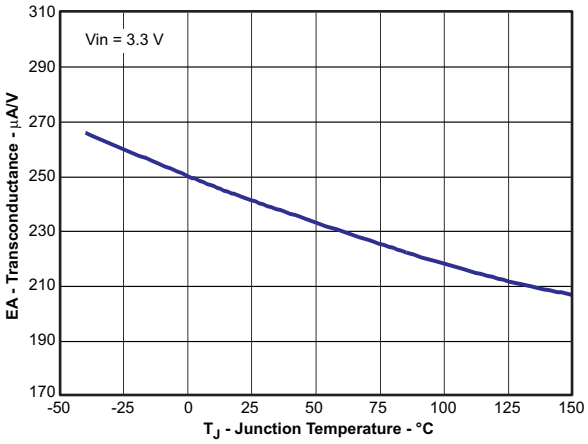


Figure 7.

TRANSCONDUCTANCE (SLOW START) versus JUNCTION TEMPERATURE

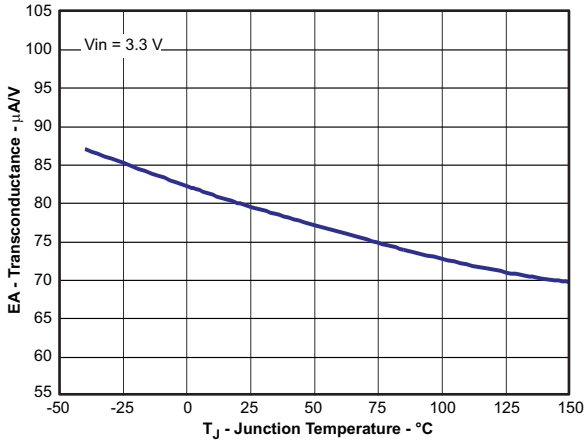


Figure 8.

EN PIN VOLTAGE versus TEMPERATURE

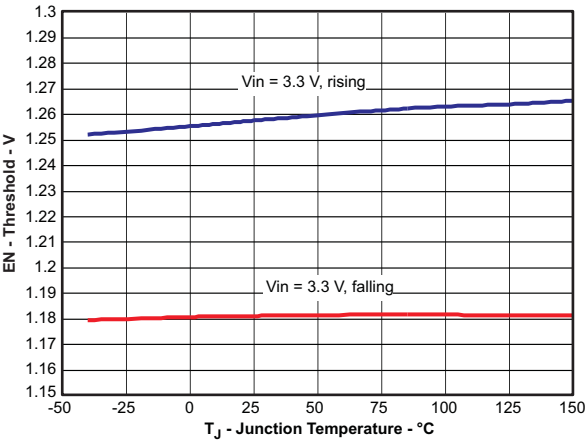


Figure 9.

EN PIN CURRENT versus TEMPERATURE

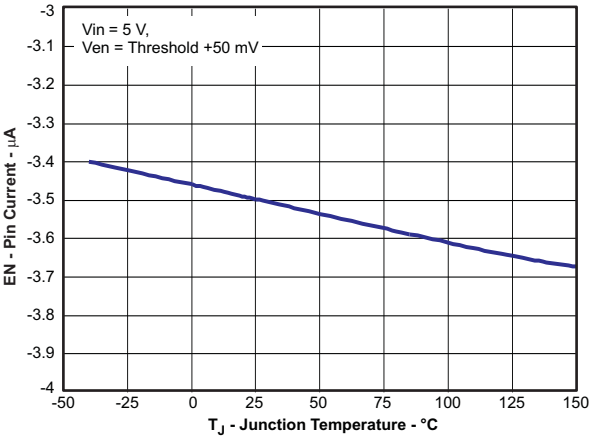


Figure 10.

EN PIN CURRENT versus TEMPERATURE

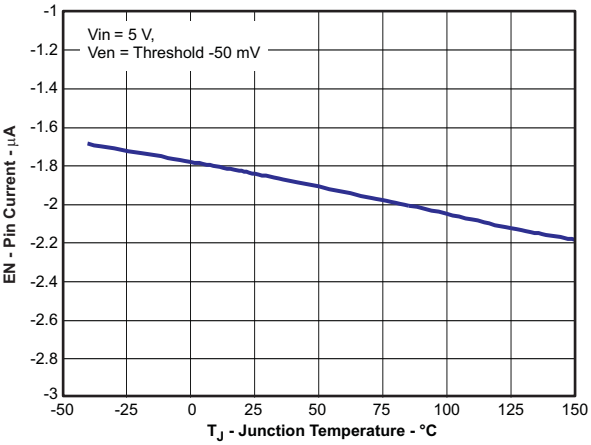


Figure 11.

CHARGE CURRENT versus TEMPERATURE

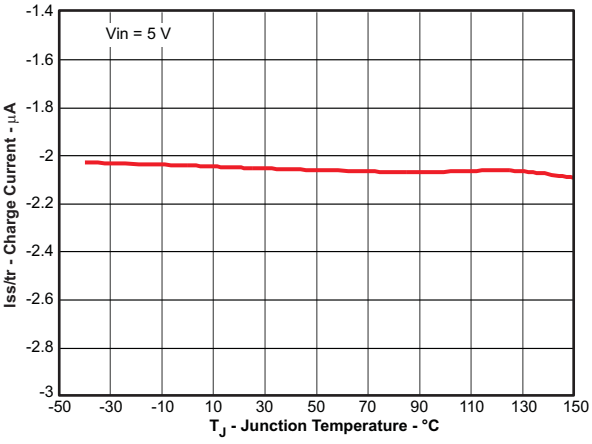


Figure 12.

TYPICAL CHARACTERISTICS CURVES (continued)

INPUT VOLTAGE versus TEMPERATURE

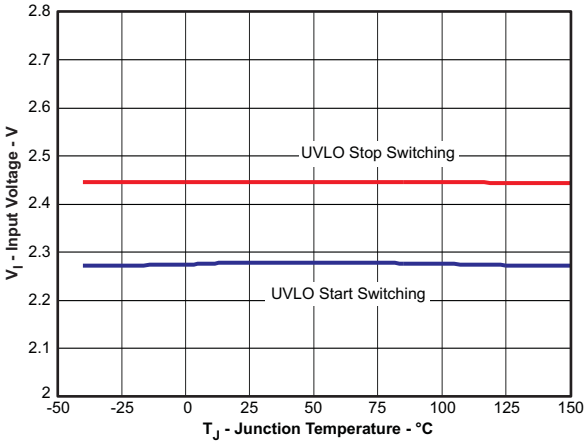


Figure 13.

SHUTDOWN SUPPLY CURRENT versus TEMPERATURE

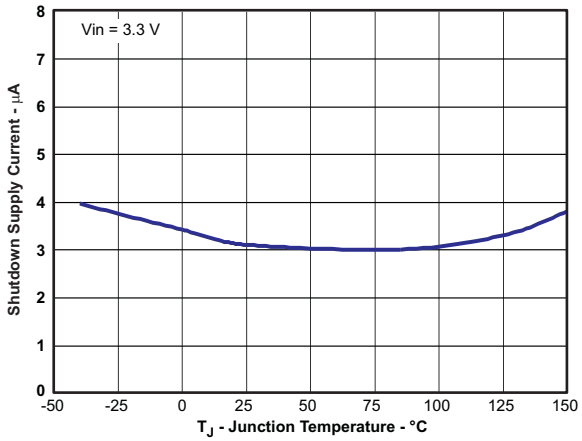


Figure 14.

SHUTDOWN SUPPLY CURRENT versus INPUT VOLTAGE

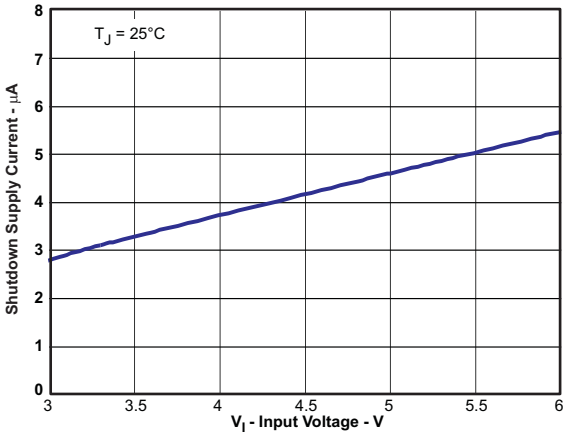


Figure 15.

VIN SUPPLY CURRENT versus JUNCTION TEMPERATURE

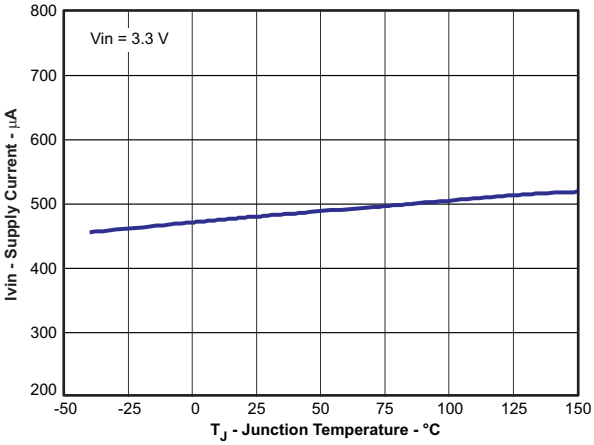


Figure 16.

VIN SUPPLY CURRENT versus INPUT VOLTAGE

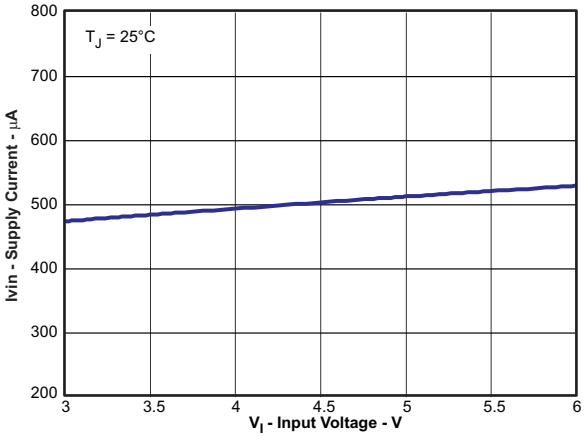


Figure 17.

PWRGD THRESHOLD versus TEMPERATURE

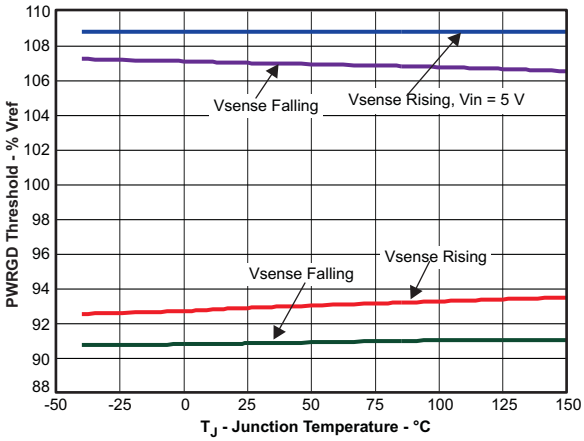


Figure 18.

TYPICAL CHARACTERISTICS CURVES (continued)

PWRGD ON-RESISTANCE versus TEMPERATURE

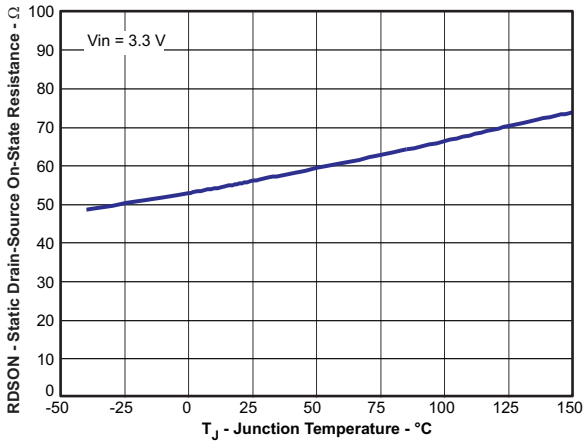


Figure 19.

SS/TR-TO-VSENSE OFFSET versus TEMPERATURE

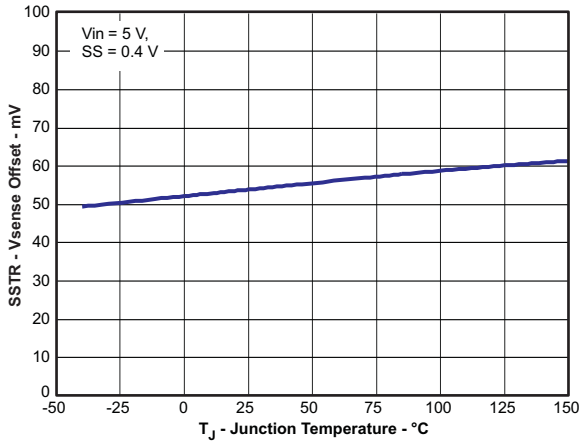


Figure 20.

EFFICIENCY versus LOAD CURRENT

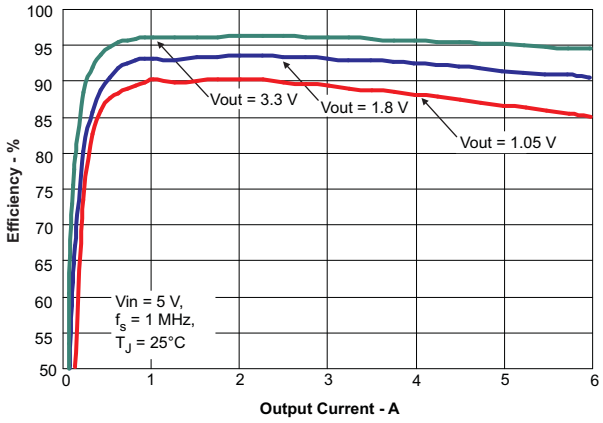


Figure 21.

EFFICIENCY versus LOAD CURRENT

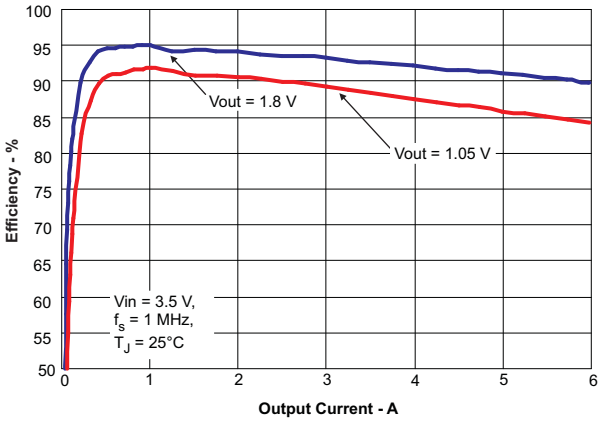


Figure 22.

EFFICIENCY versus LOAD CURRENT

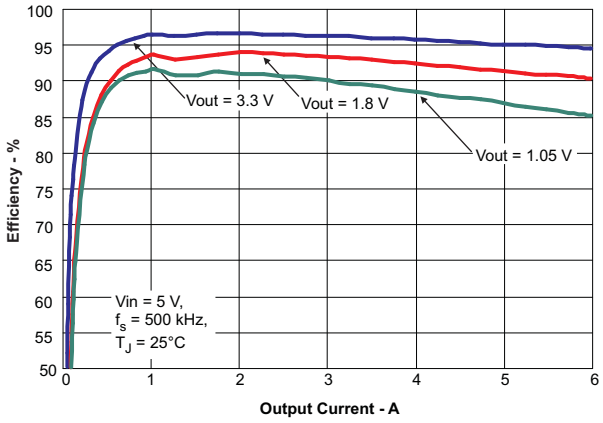


Figure 23.

EFFICIENCY versus LOAD CURRENT

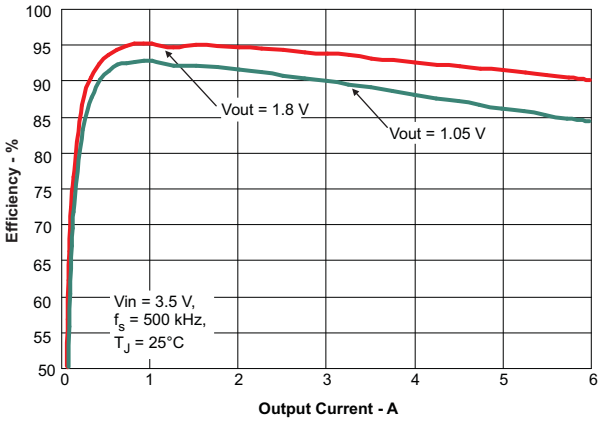


Figure 24.

OVERVIEW

The TPS54618RTE-Q1 is a 6-V, 6-A, synchronous step-down (buck) converter with two integrated n-channel MOSFETs. To improve performance during line and load transients, the device implements a constant-frequency, peak-current-mode control which reduces output capacitance and simplifies external frequency-compensation design. The wide switching-frequency range of 200 kHz to 2000 kHz allows for efficiency and size optimization when selecting the output-filter components. A resistor to ground on the RT/CLK pin adjusts the switching frequency. The device has an internal phase-lock loop (PLL) on the RT/CLK pin that synchronizes the power switch turnon to the falling edge of an external system clock.

The TPS54618RTE-Q1 has a typical default start-up voltage of 2.45 V. The EN pin has an internal pullup current source that is usable for adjusting the input voltage undervoltage lockout (UVLO) with two external resistors. In addition, the pullup current provides a default condition for the device to operate when the EN pin is floating. The total operating current for the TPS54618RTE-Q1 is typically 515 μA when not switching and under no load. When the device is disabled, the supply current is less than 5.5 μA.

The integrated 12-mΩ MOSFETs allow for high-efficiency power-supply designs with continuous output currents up to 6 amperes.

The TPS54618RTE-Q1 reduces the external component count by integrating the boot recharge diode. A capacitor between the BOOT and PH pins supplies the bias voltage for the integrated high-side MOSFET. A UVLO circuit monitors the boot capacitor voltage and turns off the high-side MOSFET when the voltage falls below a preset threshold. This BOOT circuit allows the TPS54618RTE-Q1 to operate approaching 100%. The device can step down the output voltage to as low as the 0.799-V reference.

The TPS54618RTE-Q1 has a power-good (PWRGD) comparator with 2% hysteresis.

The TPS54618RTE-Q1 minimizes excessive output overvoltage transients by taking advantage of the overvoltage power-good comparator. The regulated output voltage rising above 109% of the nominal voltage activates the overvoltage comparator, turning off the high-side MOSFET and masking it from turning back on until the output voltage is lower than 107%.

A use of the SS/TR (slow start/tracking) pin is to minimize inrush currents or provide power-supply sequencing during power up. Couple a small-value capacitor to the pin for slow start. Discharge of the SS/TR pin occurs before the output power up to ensure a repeatable restart after an overtemperature fault, UVLO fault, or disabled condition.

The use of a frequency fold-back circuit reduces the switching frequency during start-up and overcurrent fault conditions to help limit the inductor current.

DETAILED DESCRIPTION

FIXED FREQUENCY PWM CONTROL

The TPS54618RTE-Q1 uses an adjustable fixed-frequency, peak-current-mode control. External resistors on the VSENSE pin compare the output voltage to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turnon of the high-side power switch. The device compares the error-amplifier output to the high-side power-switch current. When the power-switch current reaches the COMP voltage level, the high-side power switch turns off and the low-side power switch turns on. The COMP pin voltage increases and decreases as the output current increases and decreases. The device implements a current limit by clamping the COMP pin voltage to a maximum level and also implements a minimum clamp for improved transient response performance.

SLOPE COMPENSATION AND OUTPUT CURRENT

The TPS54618RTE-Q1 adds a compensating ramp to the switch-current signal. This slope compensation prevents sub-harmonic oscillations as duty cycle increases. The available peak inductor current remains constant over the full duty-cycle range.

BOOTSTRAP VOLTAGE (BOOT) AND LOW-DROPOUT OPERATION

The TPS54618RTE-Q1 has an integrated boot regulator and requires a small ceramic capacitor between the BOOT and PH pins to provide the gate-drive voltage for the high-side MOSFET. The value of the ceramic capacitor should be 0.1 µF. TI recommends a ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher because of the stable characteristics over temperature and voltage.

To improve dropout, the TPS54618RTE-Q1 operates at 100% duty cycle as long as the BOOT to PH pin voltage is greater than 2.2 V. The high-side MOSFET turns off using a UVLO circuit, allowing for the low-side MOSFET to conduct when the voltage from BOOT to PH drops below 2.2 V. Because the supply current sourced from the BOOT pin is very low, the high-side MOSFET can remain on for more switching cycles than are required to refresh the capacitor. Thus, the effective duty cycle of the switching regulator is very high.

ERROR AMPLIFIER

The TPS54618RTE-Q1 has a transconductance amplifier. The error amplifier compares the VSENSE voltage to the lower of the SS/TR pin voltage or the internal 0.799-V voltage reference. The transconductance of the error amplifier is 245 µA/V during normal operation. When the voltage of VSENSE pin is below 0.799 V and the device is regulating using the SS/TR voltage, the gm is typically greater than 79 µA/V, but less than 245 µA/V. The placement of frequency-compensation components is between the COMP pin and ground.

VOLTAGE REFERENCE

The voltage-reference system produces a precise ±1% voltage reference over temperature by scaling the output of a temperature-stable band-gap circuit. The band-gap and scaling circuits produce 0.799 V at the non-inverting input of the error amplifier.

ADJUSTING THE OUTPUT VOLTAGE

A resistor divider from the output node to the VSENSE pin sets the output voltage. TI recommends using divider resistors with 1% tolerance or better. Start with 100 kΩ for the R1 resistor and use Equation 1 to calculate R2. To improve efficiency at very light loads, consider using larger-value resistors. If the values are too high, the regulator is more susceptible to noise and voltage errors from the VSENSE input current are noticeable.

$$R2 = R1 \times \left(\frac{0.799\ V}{V_O - 0.799\ V} \right) \quad (1)$$

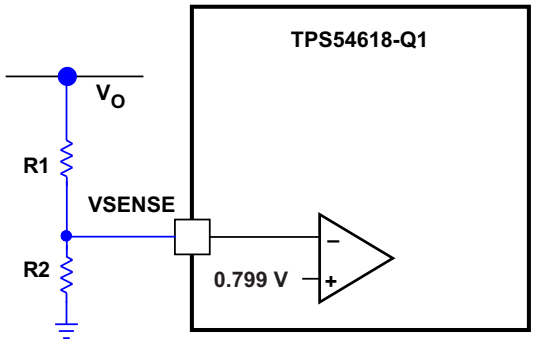


Figure 25. Voltage-Divider Circuit

ENABLE AND ADJUSTING UNDERVOLTAGE LOCKOUT

The VIN pin voltage falling below 2.28 Vdisables the TPS54618RTE-Q1. If an application requires a higher undervoltage lockout (UVLO), use the EN pin as shown in Figure 26 to adjust the input-voltage UVLO by using two external resistors. TI recommends using the EN resistors to set the UVLO falling threshold (V_{STOP}) above 2.6 V. Set the rising threshold (V_{START}) to provide enough hysteresis to allow for any input supply variations. The EN pin has an internal pullup current source that provides the default condition of the TPS54618RTE-Q1 operating when the EN pin floats. Once the EN pin voltage exceeds 1.25 V, an additional 1.6 µA of hysteresis is added. Pulling the EN pin below 1.18 V removes the 1.6 µA. This additional current facilitates input-voltage hysteresis.

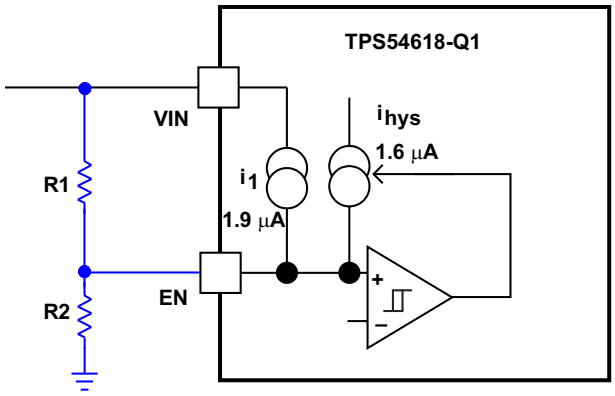


Figure 26. Adjustable Undervoltage Lockout

$$R1 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_p\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \quad (2)$$

$$R2 = \frac{R1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R1(I_p + I_h)} \quad (3)$$

where R1 and R2 are in ohms, I_h = 1.6 µA, I_p = 1.9 µA, $V_{ENRISING}$ = 1.25 V, $V_{ENFALLING}$ = 1.18 V

SLOW-START OR TRACKING PIN

The TPS54618RTE-Q1 regulates to the lower of the SS/TR pin and the internal reference voltage. A capacitor on the SS/TR pin to ground implements a slow-start time. The TPS54618RTE-Q1 has an internal pullup current source of 2 µA which charges the external slow-start capacitor. Equation 4 calculates the required slow-start capacitor value, where t_{SS} is the desired slow-start time in ms, I_{SS} is the internal slow-start charging current of 2 µA, and V_{REF} is the internal voltage reference of 0.799 V.

$$Css(nF) = \frac{Tss(mS) \times Iss(\mu A)}{Vref(V)} \quad (4)$$

During normal operation, the VIN going below UVLO, the pulling of the EN pin voltage below 1.2 V, or the occurrence of a thermal shutdown event stops the TPS54618RTE-Q1 from switching. On the VIN going above UVLO, the release or pulling high of the EN pin, or exit of a thermal shutdown, SS/TR discharges to below 40 mV before reinitiating a power-up sequence. The VSENSE voltage follows the SS/TR pin voltage with a 54-mV offset up to 85% of the internal voltage reference. When the SS/TR voltage is greater than 85% of the internal reference voltage, the offset increases as the effective system reference transitions from the SS/TR voltage to the internal voltage reference.

SEQUENCING

One can implement many of the common power-supply sequencing methods using the SS/TR, EN, and PWRGD pins. Implementation of the sequential method can be by using an open-drain or collector output of a power-on-reset pin of another device. Figure 27 shows the sequential method. Coupling of the power-good signal to the EN pin on the TPS54618RTE-Q1 enables the second power supply once the primary supply reaches regulation.

One can implement ratiometric start-up by connecting the SS/TR pins together. The regulator outputs ramp up and reach regulation at the same time. Double the current source in Equation 4 when calculating the slow-start time. Figure 29 illustrates the ratiometric method.

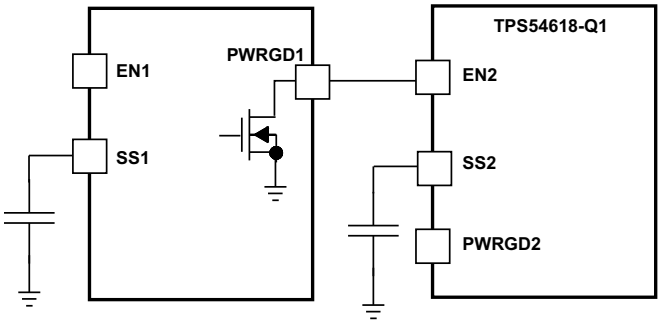


Figure 27. Sequential Start-Up Sequence

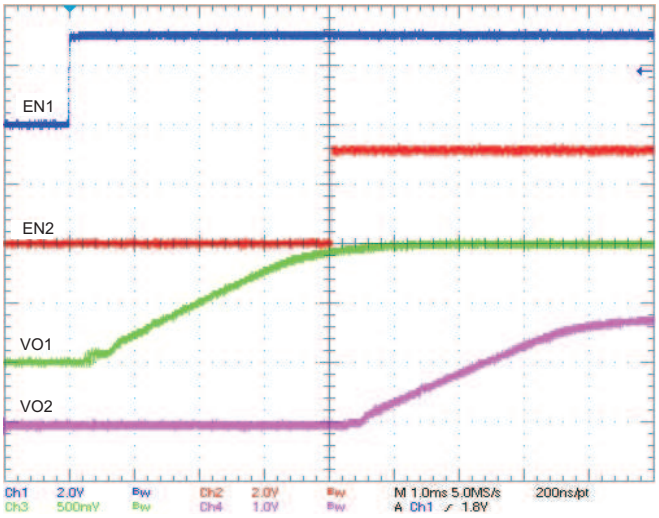


Figure 28. Sequential Startup using EN and PWRGD

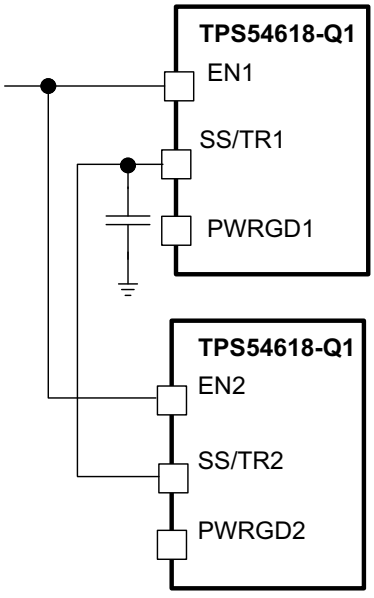


Figure 29. Schematic for Ratiometric Start-Up Sequence

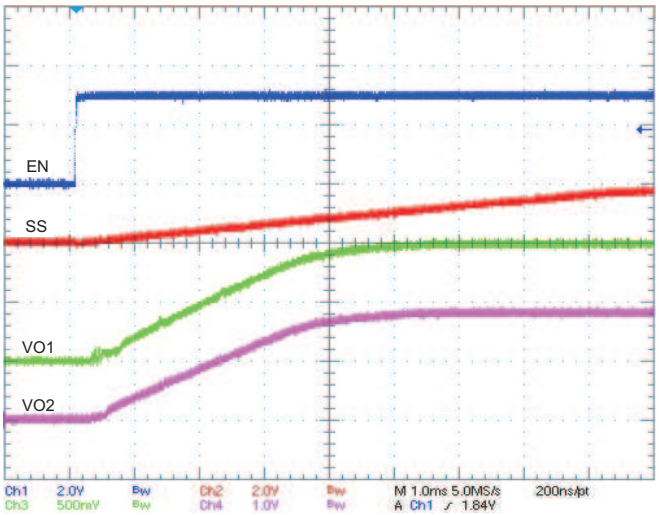


Figure 30. Ratiometric Startup

One can implement ratiometric and simultaneous power-supply sequencing by connecting the resistor network of R1 and R2 shown in Figure 31 to the output of the power supply to be tracked or to another voltage reference source. Using Equation 5 and Equation 6, calculate values of the tracking resistors to initiate the VOUT2 slightly before, after, or at the same time as VOUT1. Equation 7 is the voltage difference between VOUT1 and VOUT2. The ΔV variable is zero volts for simultaneous sequencing. Including $V_{SSOFFSET}$ and I_{SS} are included as variables in the equations minimizes the effect of the inherent SS/TR to VSENSE offset ($V_{SSOFFSET}$) in the slow-start circuit and the offset created by the pullup current source (I_{SS}) and tracking resistors. To design a ratiometric start-up in which the VOUT2 voltage is slightly greater than the VOUT1 voltage when VOUT2 reaches regulation, use a negative number in Equation 5 through Equation 7 for ΔV. Equation 7 results in a positive number for applications in which the VOUT2 is slightly lower than VOUT1 when VOUT2 regulation is achieved. The requirement for pulling the SS/TR pin below 40 mV before starting after an EN, UVLO, or thermal-shutdown fault necessitates careful selection of the tracking resistors to ensure the device restarts after a fault. Make sure the calculated R1 value from Equation 5 is greater than the value calculated in Equation 8 to ensure the device can recover from a fault. As the SS/TR voltage becomes more than 85% of the nominal reference voltage, the $V_{SSOFFSET}$ becomes larger as the slow-start circuits gradually hand off the regulation reference to the internal voltage reference. The SS/TR pin voltage must be greater than 1.1 V for a complete handoff to the internal voltage reference as shown in Figure 30.

$$R1 = \frac{Vout2 + \Delta V}{Vref} \times \frac{Vssoffset}{Iss} \tag{5}$$

$$R2 = \frac{Vref \times R1}{Vout2 + \Delta V - Vref} \tag{6}$$

$$\Delta V = Vout1 - Vout2 \tag{7}$$

$$R1 > 2930 \times Vout1 - 145 \times \Delta V \tag{8}$$

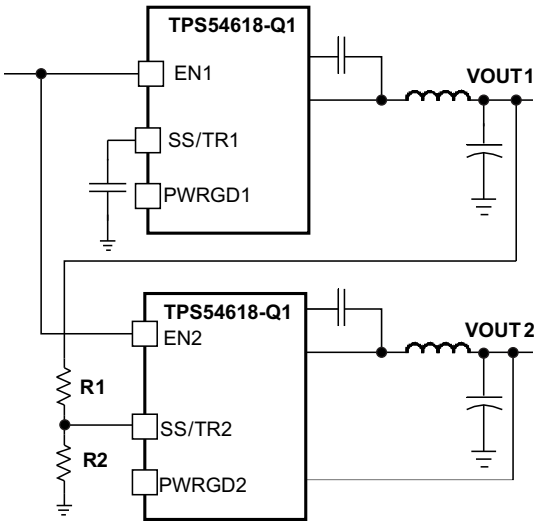


Figure 31. Ratiometric and Simultaneous Start-Up Sequence

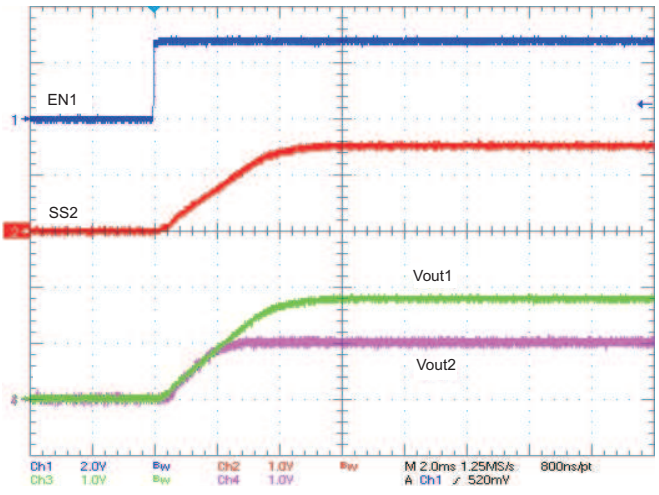


Figure 32. Ratiometric Start-Up Using Coupled SS/TR Pins

CONSTANT SWITCHING FREQUENCY and TIMING RESISTOR (RT/CLK Pin)

The switching frequency of the TPS54618RTE-Q1 is adjustable over a wide range from 300 kHz to 2000 kHz by placing a maximum of 700 kΩ and minimum of 85 kΩ, respectively, on the RT/CLK pin. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. RT/CLK is typically 0.5 V. To determine the timing resistance for a given switching frequency, use the curve in Figure 5 or Equation 9.

$$RT\left(k\Omega\right) = \frac{235892}{f_{SW}\left(kHz\right)^{1.027}} \tag{9}$$

$$f_{SW}\left(kHz\right) = \frac{171032}{RT\left(k\Omega\right)^{0.974}} \tag{10}$$

To reduce the solution size, one would typically set the switching frequency as high as possible, but consider tradeoffs of the efficiency, maximum input voltage, and minimum controllable on-time.

The minimum controllable on time is typically 75 ns at full-current load and 120 ns at no load, and limits the maximum operating input voltage or output voltage.

OVERCURRENT PROTECTION

The TPS54618RTE-Q1 implements a cycle-by-cycle current limit. During each switching cycle, there is a comparison of the high-side switch current to the voltage on the COMP pin. When the instantaneous switch current intersects the COMP voltage, the high-side switch turns off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP pin high, increasing the switch current. An internal clamp on the error amplifier output functions as a switch-current limit.

FREQUENCY SHIFT

To operate at high switching frequencies and provide protection during overcurrent conditions, the TPS54618RTE-Q1 implements a frequency shift. Without implementation of the frequency shift, during an overcurrent condition the low-side MOSFET may not be turn off long enough to reduce the current in the inductor, causing a current runaway. With frequency shift, during an overcurrent condition the switching frequency is reduced from 100%, then 50%, then 25%, as the voltage decreases from 0.799 to 0 volts on the VSENSE pin, to allow the low-side MOSFET to be off long enough to decrease the current in the inductor. During start-up, the switching frequency increases as the voltage on VSENSE increases from 0 to 0.799 volts. See Figure 6 for details.

REVERSE OVERCURRENT PROTECTION

The TPS54618RTE-Q1 implements low-side current protection by detecting the voltage across the low-side MOSFET. When the converter sinks current through its low-side FET, the control circuit turns off the low-side MOSFET if the reverse current is typically more than 4.5 A. By implementing this additional protection scheme, the converter is able to protect itself from excessive current during power cycling and start-up into pre-biased outputs.

SYNCHRONIZE USING THE RT/CLK PIN

A use of the RT/CLK pin is to synchronize the converter to an external system clock. See Figure 33. To implement the synchronization feature in a system, connect a square wave to the RT/CLK pin with an on-time of at least 75 ns. Pulling the pin above the PLL upper threshold initiates a mode change, and the pin becomes a synchronization input. The device disables the internal amplifier, and the pin is a high-impedance clock input to the internal PLL. Cessation of clocking edges re-enables the internal amplifier and the mode returns to the frequency set by the resistor. The square-wave amplitude at this pin must transition lower than 0.6 V and higher than 1.6 V, typically. The synchronization frequency range is 300 kHz to 2000 kHz. The rising edge of the PH synchronizes to the falling edge of the RT/CLK pin.

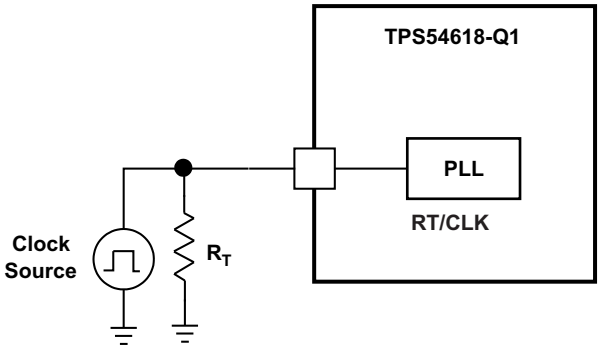


Figure 33. Synchronizing to a System Clock

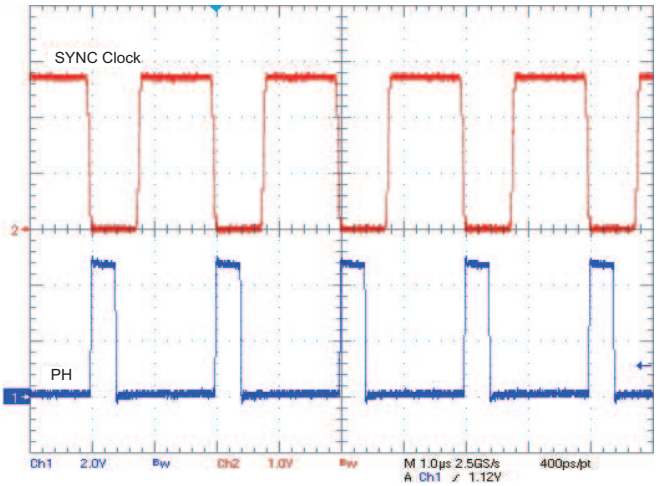


Figure 34. Plot of Synchronizing to System Clock

POWER GOOD (PWRGD PIN)

The PWRGD pin output is an open-drain MOSFET. The VSENSE voltage entering the fault condition by falling below 91% or rising above 109% of the nominal internal reference voltage pulls the output low. There is a 2% hysteresis on the threshold voltage, so when the VSENSE voltage rises to the good condition above 93% or falls below 107% of the internal voltage reference, the PWRGD output MOSFET turns off. TI recommends use of a pullup resistor between the values of 1 kΩ and 100 kΩ to a voltage source that is 6 V or less. PWRGD is in a valid state once the VIN input voltage is greater than 1.5 V.

OVERVOLTAGE TRANSIENT PROTECTION

The TPS54618RTE-Q1 incorporates an overvoltage-transient-protection (OVTP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients. The OVTP feature minimizes the output overshoot by implementing a circuit to compare the VSENSE pin voltage to the OVTP threshold, which is 109% of the internal voltage reference. The VSENSE pin voltage going greater than the OVTP threshold disables the high-side MOSFET, preventing current from flowing to the output and minimizing output overshoot. The VSENSE voltage dropping lower than the OVTP threshold allows the high-side MOSFET to turn on during the next clock cycle.

THERMAL SHUTDOWN

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 168°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. Once the die temperature decreases below 150°C, the device reinitiates the power-up sequence by discharging the SS pin to below 40 mV. The thermal shutdown hysteresis is 20°C.

SMALL-SIGNAL MODEL FOR LOOP RESPONSE

Figure 35 shows for the TPS54618RTE-Q1 control loop an equivalent model which one can modeled in a circuit-simulation program to check frequency response and dynamic load response. The error amplifier is a transconductance amplifier with a gm of 245 µA/V. One can model the error amplifier using an ideal voltage-controlled current source. Resistor R0 and capacitor C0 model the open-loop gain and frequency response of the amplifier. The 1-mV ac voltage source between nodes a and b effectively breaks the control loop for the frequency-response measurements. Plotting a / c shows the small-signal response of the frequency compensation. Plotting a / b shows the small-signal response of the overall loop. One can check the dynamic loop response by replacing the R_L with a current source with the appropriate load-step amplitude and step rate in a time-domain analysis.

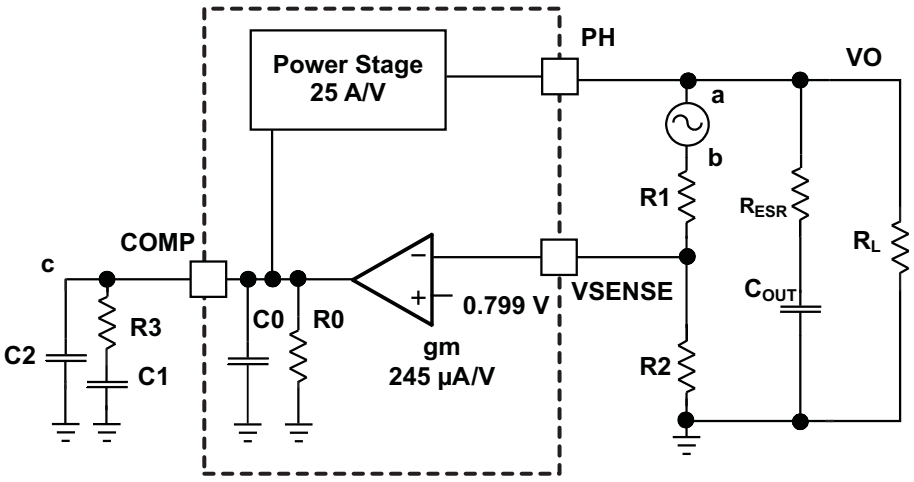


Figure 35. Small-Signal Model for Loop Response

SIMPLE SMALL-SIGNAL MODEL FOR PEAK CURRENT MODE CONTROL

Figure 35 is a simple small-signal model that one can use to understand how to design the frequency compensation. A voltage-controlled current source (duty cycle modulator) supplying current to the output capacitor and load resistor an approximate the TPS54618RTE-Q1 power stage. The control to output transfer function, shown in Equation 11, consists of a dc gain, one dominant pole, and one ESR zero. The quotient of the change in switch current and the change in COMP pin voltage (node c in Figure 35) is the power-stage transconductance. The gm for the TPS54618RTE-Q1 is 25 A/V. The low-frequency gain of the power-stage frequency response is the product of the transconductance and the load resistance, as shown in Equation 12. As the load current increases and decreases, the low-frequency gain decreases and increases, respectively. This variation with load may seem problematic at first glance, but the dominant pole moves with load current (see Equation 13). The combined effect is highlighted by the dashed line in the right half of Figure 36. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same for the varying load conditions, which makes it easier to design the frequency compensation.

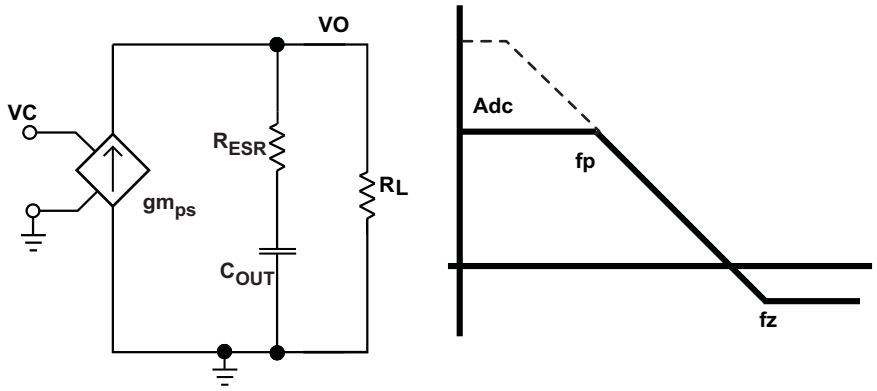


Figure 36. Simple Small-Signal Model and Frequency Response for Peak-Current-Mode Control

$$\frac{vo}{vc} = Adc \times \frac{\left(1+\frac{s}{2\pi \times fz}\right)}{\left(1+\frac{s}{2\pi \times fp}\right)} \quad (11)$$

$$Adc = gm_{ps} \times R_L \quad (12)$$

$$fp = \frac{1}{C_{OUT} \times R_L \times 2\pi} \quad (13)$$

$$fz = \frac{1}{C_{OUT} \times R_{ESR} \times 2\pi} \quad (14)$$

SMALL-SIGNAL MODEL FOR FREQUENCY COMPENSATION

The TPS54618RTE-Q1 uses a transconductance amplifier for the error amplifier and readily supports two of the commonly used frequency-compensation circuits. Figure 37 shows the compensation circuits. High-bandwidth power-supply designs using low-ESR output capacitors most likely implement Type 2 circuits. Type 2A adds one additional high-frequency pole to attenuate high-frequency noise.

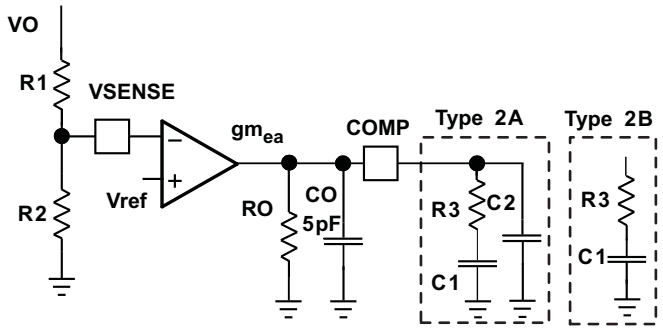


Figure 37. Types of Frequency Compensation

The design guidelines for TPS54618RTE-Q1 loop compensation are as follows:

1. Calculate the modulator pole, f_{pmod}, and the ESR zero, f_{z1}, using Equation 15 and Equation 16. The output capacitor (C_{OUT}) may require derating if the output voltage is a high percentage of the capacitor rating. Use the capacitor manufacturer information to derate the capacitor value. Use Equation 17 and Equation 18 to estimate a starting point for the crossover frequency, f_c. Equation 17 is the geometric mean of the modulator pole and the ESR zero, and Equation 18 is the mean of the modulator pole and the switching frequency. Use the lower value of Equation 17 or Equation 18 as the maximum crossover frequency.

$$fp\ mod = \frac{Ioutmax}{2\pi \times Vout \times Cout} \quad (15)$$

$$fz\ mod = \frac{1}{2\pi \times Resr \times Cout} \quad (16)$$

$$f_C = \sqrt{fp\ mod \times fz\ mod} \quad (17)$$

$$f_C = \sqrt{fp\ mod \times \frac{fsw}{2}} \quad (18)$$

2. Determine R3 by

$$R3 = \frac{2\pi \times fc \times Vo \times C_{OUT}}{gm_{ea} \times Vref \times gm_{ps}} \quad (19)$$

where is the gm_{ea} amplifier gain (245 µA/V) and gm_{ps} is the power stage gain (25 A/V).

3. Place a compensation zero at the dominant pole. $fp = \frac{1}{C_{OUT} \times R_L \times 2\pi}$
4. Determine C1 by:

$$C1 = \frac{R_L \times C_{OUT}}{R3} \quad (20)$$

5. C2 is optional. One can use C2 to cancel the zero from the ESR of C0.

$$C2 = \frac{Resr \times C_{OUT}}{R3} \quad (21)$$

APPLICATION INFORMATION

DESIGN GUIDE – STEP-BY-STEP DESIGN PROCEDURE

This example details the design of a high-frequency switching-regulator design using ceramic output capacitors. This design is available as the HPA606 evaluation module (EVM). One must know a few parameters in order to start the design process. Determination of these parameters is typically at the system level. For this example, we start with the following known parameters:

Output voltage	1.8 V
Transient response 1.5-A to 4.5-A load step	ΔV_{OUT} = 4%
Maximum Output Current	6 A
Input voltage	3 V to 6 V, 5-V nominal
Output-voltage ripple	< 30 mV p-p
Switching frequency (f_{sw})	1000 kHz

SELECTING THE SWITCHING FREQUENCY

The first step is to decide on a switching frequency for the regulator. Typically, one wants to choose the highest switching frequency possible, because this produces the smallest solution size. The high switching frequency allows for lower-valued inductors and smaller output capacitors, compared to a power supply that switches at a lower frequency. However, the highest switching frequency causes extra switching losses, which hurt the converter's performance. The converter is capable of running from 300 kHz to 2 MHz. Unless a small solution size is an ultimate goal, select a moderate switching frequency of 1 MHz to achieve both a small solution size and high-efficiency operation. Using Equation 9, the calculated value of R4 is 180 kΩ. Choose a standard 1% 182-kΩ value for the design.

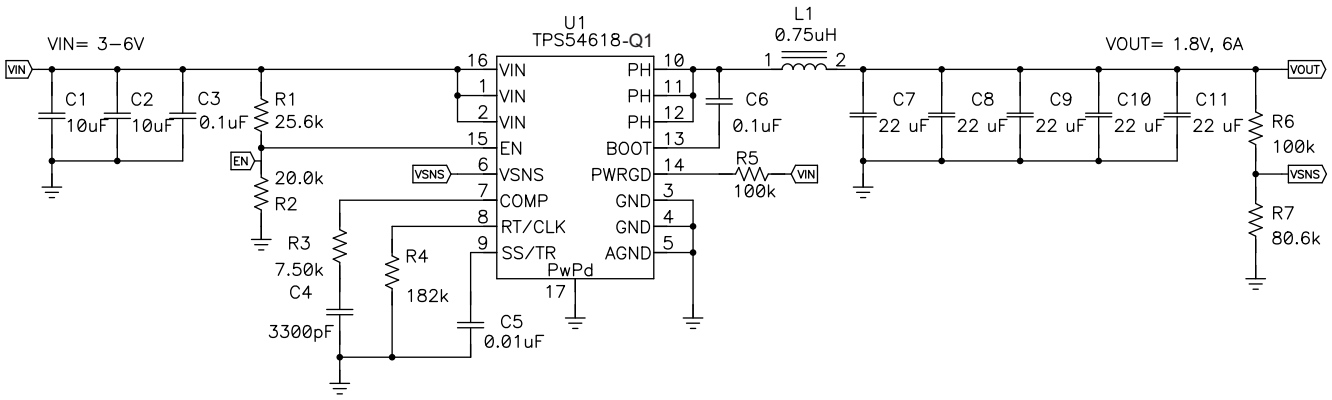


Figure 38. High Frequency, 1.8-V Output Power-Supply Design With Adjusted UVLO

OUTPUT-INDUCTOR SELECTION

The inductor selected works for the entire TPS54618RTE-Q1 input voltage range. To calculate the value of the output inductor, use Equation 22. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The output capacitor filters the inductor ripple current. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor, because the output capacitor must have a ripple-current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, K_{IND} is normally from 0.1 to 0.3 for the majority of applications.

For this design example, use K_{IND} = 0.3 and calculate the inductor value to be 0.7 µH. For this design, choose a nearest standard value: 0.75 µH. For the output filter inductor, it is important that the rms-current and saturation-current ratings not be exceeded. The rms and peak inductor current can be found from Equation 24 and Equation 25.

For this design, the rms inductor current is 6.01 A and the peak inductor current is 6.84 A. The chosen inductor is a Toko FDV0630-R75M. It has a saturation-current rating 0f 10 A and an rms-current rating of 8.9 A.

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults, or transient-load conditions, the inductor current can increase above the peak inductor current level calculated previously. In transient conditions, the inductor current can increase up to the switch-current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch-current limit rather than the peak inductor current.

$$L1 = \frac{Vinmax - Vout}{Io \times Kind} \times \frac{Vout}{Vinmax \times fsw} \quad (22)$$

$$Iripple = \frac{Vinmax - Vout}{L1} \times \frac{Vout}{Vinmax \times fsw} \quad (23)$$

$$ILrms = \sqrt{Io^2 + \frac{1}{12} \times \left(\frac{Vo \times (Vinmax - Vo)}{Vinmax \times L1 \times fsw}\right)^2} \quad (24)$$

$$ILpeak = Iout + \frac{Iripple}{2} \quad (25)$$

OUTPUT CAPACITOR

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The basis of the output capacitance selection must be the most-stringent of these three criteria.

The desired response to a large change in the load current is the first criterion. The output capacitor must supply the load with current when the regulator cannot. This situation would occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is temporarily not able to supply sufficient output current if there is a large, fast increase in the current needs of the load such as transitioning from no load to a full load. The regulator usually requires two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitor size must be able to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for two clock cycles while only allowing a tolerable amount of droop in the output voltage. Equation 26 shows the minimum output capacitance necessary to accomplish this.

For this example, the transient load response specification is a 3% change in Vout for a load step from 1.5 A (25% load) to 4.5 A (75% load). For this example, ΔIout = 4.5 – 1.5 = 3.0 A and ΔVout = 0.04 × 1.8 = 0.072 V. Using these numbers gives a minimum capacitance of 83 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

Equation 27 calculates the minimum output capacitance needed to meet the output-voltage ripple specification, where fsw is the switching frequency, Vripple is the maximum allowable output voltage ripple, and Iripple is the inductor ripple current. In this case, the maximum output-voltage ripple is 30 mV. Under this requirement, Equation 27 yields 7 uF.

$$Co > \frac{2 \times \Delta Iout}{fsw \times \Delta Vout} \quad (26)$$

$$Co > \frac{1}{8 \times fsw} \times \frac{1}{\frac{Voripple}{Iripple}} \quad (27)$$

where ΔIout is the change in output current, *f*sw is the regulators switching frequency, and ΔVout is the allowable change in the output voltage.

Equation 28 calculates the maximum ESR an output capacitor can have to meet the output-voltage ripple specification. Equation 28 indicates the ESR should be less than 18 mΩ. In this case, the ESR of the ceramic capacitor is much less than 18 mΩ.

Factoring in additional capacitance de-ratings for aging, temperature, and dc bias increases this minimum value. For this example, use five 22-µF 10-V X5R ceramic capacitors with 3 mΩ of ESR. The estimated capacitance after derating by a factor of 0.75 is 82.5 µF.

Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. One must select an output capacitor that can support the inductor ripple current. Some capacitor data sheets specify the rms (root mean square) value of the maximum ripple current. Use Equation 29 to calculate the rms ripple current that the output capacitor must support. For this application, Equation 29 yields 520 mA.

$$Resr < \frac{Voripple}{Iripple} \tag{28}$$

$$Icorms = \frac{Vout \times (Vinmax - Vout)}{\sqrt{12} \times Vinmax \times L1 \times fsw} \tag{29}$$

INPUT CAPACITOR

The TPS54618RTE-Q1 requires a high-quality ceramic, type X5R or X7R, input decoupling capacitor of at least 10 µF of effective capacitance, and in some applications, a bulk capacitance. The effective capacitance includes any dc bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple-current rating greater than the maximum input-current ripple of the TPS54618RTE-Q1. Calculate the input-current ripple using Equation 30.

The value of a ceramic capacitor varies significantly over temperature and the amount of dc bias applied to the capacitor. One can minimize the capacitance variations due to temperature by selecting a dielectric material that is stable over temperature. Designers usually select X5R and X7R ceramic dielectrics for power regulator capacitors because they have a high capacitance-to-volume ratio and are fairly stable over temperature. One must also select the output capacitor with the dc bias taken into account. The capacitance value of a capacitor decreases as the dc bias across a capacitor increases.

This example design requiresa ceramic capacitor with at least a 10-V voltage rating to support the maximum input voltage. The selection for this example is two 10-µF and one 0.1-µF 10-V capacitors in parallel. The input capacitance value determines the input ripple voltage of the regulator. Calculate the input-voltage ripple using Equation 31. Using the design example values, Ioutmax = 6 A, Cin = 20 µF, and Fsw = 1 MHz, yields an input voltage ripple of 149 mV and an rms input ripple current of 2.94 A.

$$Icirms = Iout \times \sqrt{\frac{Vout}{Vinmin} \times \frac{(Vinmin - Vout)}{Vinmin}} \tag{30}$$

$$\Delta Vin = \frac{Ioutmax \times 0.25}{Cin \times fsw} \tag{31}$$

SLOW-START CAPACITOR

The slow-start capacitor determines the minimum amount of time it takes for the output voltage to reach its nominal programmed value during power up. This is useful if a load requires a controlled voltage-slew rate. This is also useful if the output capacitance is very large and would require large amounts of current to charge the capacitor quickly to the output-voltage level. The large currents necessary to charge the capacitor may make the TPS54618RTE-Q1 reach the current limit, or excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output-voltage slew rate solves both of these problems.

One can calculate the slow-start capacitor value using Equation 32. For the example circuit, the slow-start time is not too critical because the output-capacitor value is 110 µF, which does not require much current to charge to 1.8 V. The example circuit has the slow-start time set to an arbitrary value of 4 ms, which requires a 10-nF capacitor. In TPS54618RTE-Q1, Iss is 2.2 µA and Vref is 0.799 V.

$$Css(nF) = \frac{Tss(ms) \times Iss(\mu A)}{Vref(V)} \quad (32)$$

BOOTSTRAP CAPACITOR SELECTION

Connect a 0.1-µF ceramic capacitor between the BOOT to PH pin for proper operation. TI recommends using a ceramic capacitor with X5R or better-grade dielectric. The capacitor should have a 10-V or higher voltage rating.

OUTPUT-VOLTAGE AND FEEDBACK RESISTOR SELECTION

For the example design, the R6 selection was 100 kΩ. Calculating with Equation 33, R7 is 80 kΩ. The nearest standard 1% resistor is 80.6 kΩ.

$$R7 = \frac{Vref}{Vo - Vref} R6 \quad (33)$$

Due to the internal design of the TPS54618RTE-Q1, there is a minimum output voltage limit for any given input voltage. The output voltage can never be lower than the internal voltage reference of 0.799 V. Above 0.799 V, the minimum controllable on-time may limit the output voltage. In this case, Equation 34 gives the minimum output voltage.

$$Voutmin = Ontimemin \times Fsmax \times (Vinmax - Ioutmin \times RDSmin) - Ioutmin \times (RL + RDSmin) \quad (34)$$

where:

Voutmin = minimum achievable output voltage

Ontimemin = minimum controllable on-time (75 ns typical. 120 ns no load)

Fsmax = maximum switching frequency, including tolerance

Vinmax = maximum input voltage

Ioutmin = minimum load current

RDSmin = minimum high-side MOSFET on-resistance (See Electrical Characteristics)

RL = series resistance of output inductor

There is also a maximum achievable output voltage, which is limited by the minimum off-time. Equation 35 gives the maximum output voltage.

$$Voutmax = Vin \times \left(1 - \frac{Offtimemax}{ts}\right) - Ioutmax \times (RDSmax + RI) - (0.7 - Ioutmax \times RDSmax) \times \left(\frac{tdead}{ts}\right) \quad (35)$$

where:

Voutmax = maximum achievable output voltage

Vin = minimum input voltage

Offtimemax = maximum off-time (90 ns typical for adequate margin)

ts = 1/Fs

Ioutmax = maximum current

RDSmax = maximum high-side MOSFET on-resistance (See Electrical Characteristics)

RI = DCR of the inductor

tdead = dead time (60 ns)

COMPENSATION

There are several industry techniques used to compensate dc-dc regulators. The method presented here is easy to calculate and yields high phase margins. For most conditions, the regulator has a phase margin between 60 and 90 degrees. The method presented here ignores the effects of the slope compensation that is internal to the TPS54618RTE-Q1. Ignoring the slope compensation usually results in the actual crossover frequency being lower than the crossover frequency used in the calculations. Use SwitcherPro software for a more accurate design.

To get started, calculate the modulator pole, fpmod, and the ESR zero, fz1 using Equation 36 and Equation 37. For Cout, the derated capacitance value is 82.5 µF. Use Equation 38 and Equation 39 to estimate a starting point for the crossover frequency, fc. For the example design, fpmod is 6.43 kHz and fzmod is 643 kHz. Equation 38 is the geometric mean of the modulator pole and the ESR zero, and Equation 39 is the mean of modulator pole and the switching frequency. Equation 38 yields 64.3 kHz and Equation 39 gives 56.7 kHz. The lower value of Equation 38 or Equation 39 is the maximum recommended crossover frequency. For this example, specify a lower fc value of 40 kHz. Next, calculate the compensation components. Use a resistor in series with a capacitor to create a compensating zero. A capacitor in parallel with these two components forms the compensating pole (if needed).

$$fp\,mod = \frac{Ioutmax}{2\pi \times Vout \times Cout} \tag{36}$$

$$fz\,mod = \frac{1}{2\pi \times Resr \times Cout} \tag{37}$$

$$f_C = \sqrt{fp\,mod \times fz\,mod} \tag{38}$$

$$f_C = \sqrt{fp\,mod \times \frac{fsw}{2}} \tag{39}$$

The compensation design takes the following steps:

1. Set up the anticipated crossover frequency. Use Equation 40 to calculate the resistor value for thecompensation network. In this example, the anticipated crossover frequency (fc) is 40 kHz. The power-stage gain (gm_{ps}) is 25 A/V and the error-amplifier gain (gm_{ea}) is 245 µA/V.

$$R3 = \frac{2\pi \times fc \times Vo \times Co}{Gm \times Vref \times VI_{gm}} \tag{40}$$

2. Place the compensation zero at the pole formed by the load resistor and the output capacitor. Calculate the compensation-network capacitor with Equation 41.

$$C4 = \frac{Ro \times Co}{R3} \tag{41}$$

3. One can add an additional pole to attenuate high-frequency noise. In this application, it is not necessary to add such a pole.

From the procedures above, the compensation network includes a 7.50-kΩ resistor and a 3300-pF capacitor.

APPLICATION CURVES

EFFICIENCY versus LOAD CURRENT

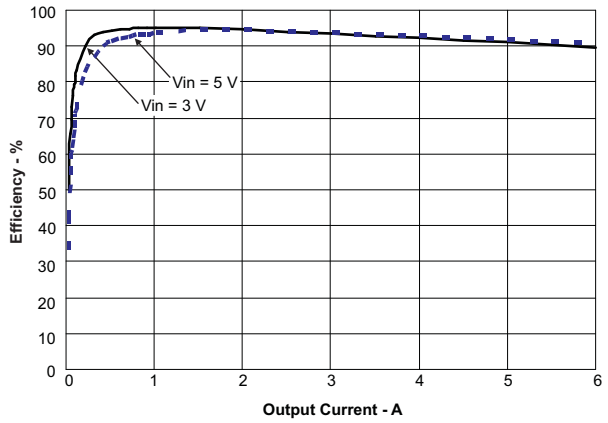


Figure 39.

EFFICIENCY versus LOAD CURRENT

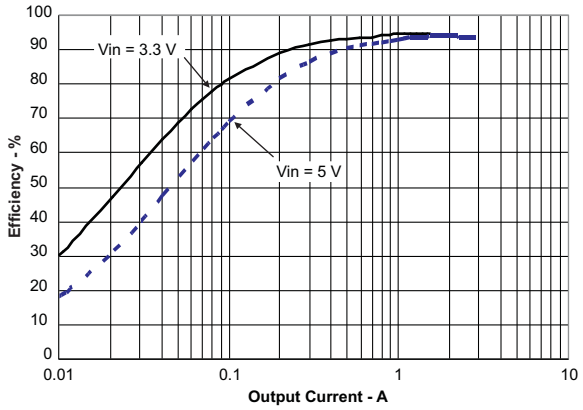


Figure 40.

TRANSIENT RESPONSE, 1.5-A STEP

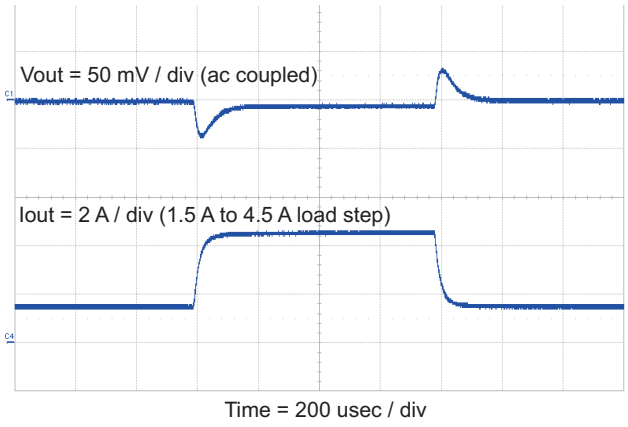


Figure 41.

POWER-UP VOUT, VIN

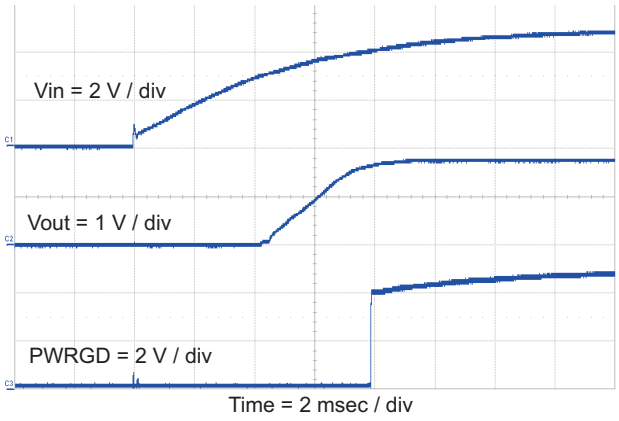


Figure 42.

POWER-UP VOUT, EN

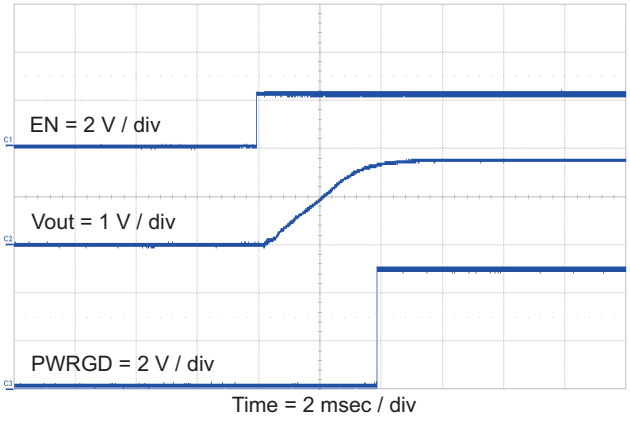


Figure 43.

OUTPUT RIPPLE, 3 A

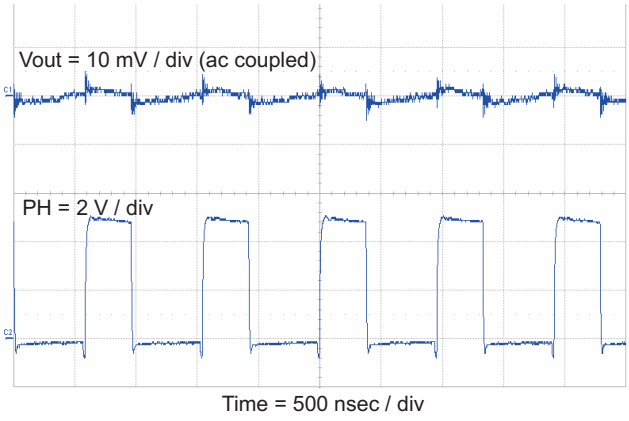


Figure 44.

INPUT RIPPLE, 3 A

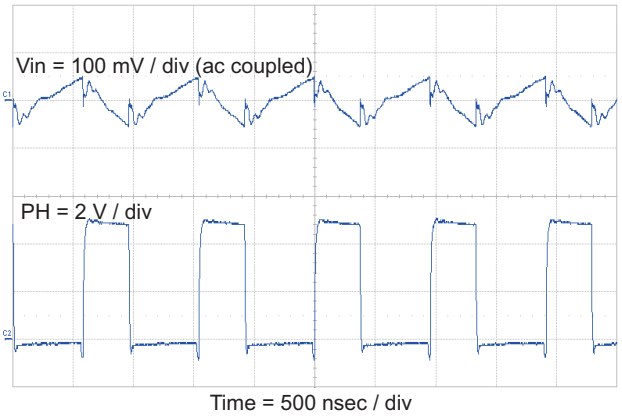


Figure 45.

CLOSED LOOP RESPONSE, VIN (5 V), 3 A

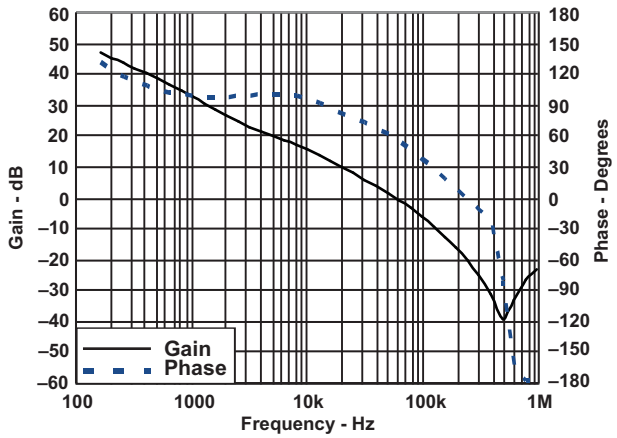


Figure 46.

LOAD REGULATION
versus
LOAD CURRENT

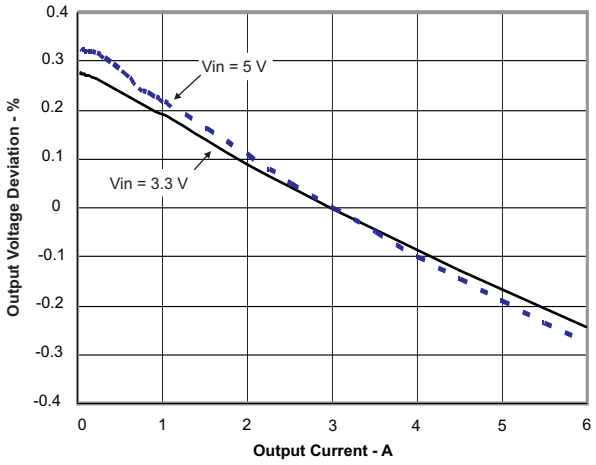


Figure 47.

REGULATION
versus
INPUT VOLTAGE

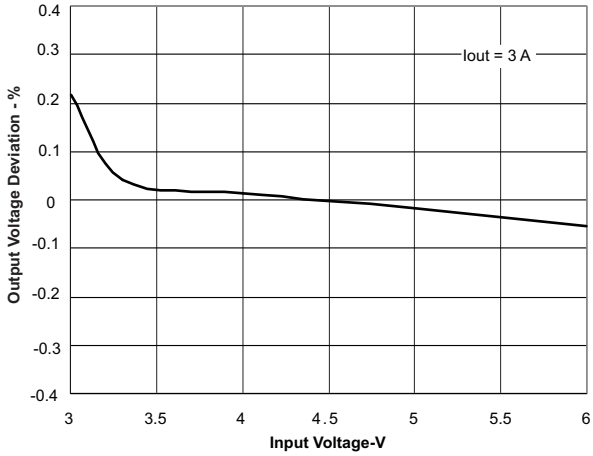


Figure 48.

POWER-DISSIPATION ESTIMATE

The following formulas show how to estimate the IC power dissipation under continuous-conduction-mode (CCM) operation. The power dissipation of the IC (Ptot) includes conduction loss (Pcon), dead time loss (Pd), switching loss (Psw), gate-drive loss (Pgd), and supply-current loss (Pq).

$$Pcon = Io^2 \times R_{DS\_on\_Temp}$$

$$Pd = f_{sw} \times Io \times 0.7 \times 40 \times 10^{-9}$$

$$Psw = 1/2 \times V_{in} \times Io \times f_{sw} \times 13 \times 10^{-9}$$

$$Pgd = 2 \times V_{in} \times f_{sw} \times 10 \times 10^{-9}$$

$$Pq = V_{in} \times 515 \times 10^{-6}$$

where:

I_O is the output current (A).
$R_{DS\_on\_Temp}$ is the on-resistance of the high-side MOSFET with given temperature (Ω).
V_{in} is the input voltage (V).
f_{sw} is the switching frequency (Hz).

So

$$Ptot = Pcon + Pd + Psw + Pgd + Pq$$

For given T_A,

$$T_J = T_A + R_{th} \times P_{tot}$$

For given T_{JMAX} = 150°C

$$T_{Amax} = T_{J\ max} - R_{th} \times P_{tot}$$

where:

P_{tot} is the total device power dissipation (W).
T_A is the ambient temperature (°C).
T_J is the junction temperature (°C).
R_{th} is the thermal resistance of the package (°C/W).
T_{JMAX} is maximum junction temperature (°C).
T_{AMAX} is maximum ambient temperature (°C).

There are additional power losses in the regulator circuit due to the inductor ac and dc losses and trace resistance that impact the overall efficiency of the regulator.

LAYOUT

Layout is a critical portion of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. Take care to minimize the loop area formed by the bypass capacitor connections and the VIN pins. See Figure 49 for a PCB layout example. Tie the GND pins and AGND pin directly to the power pad under the IC. Connect the power pad to any internal PCB ground planes using multiple vias directly under the IC. One can use additional vias to connect the top-side ground area to the internal planes near the input and output capacitors. For operation at full-rated load, the top-side ground area along with any additional internal ground planes must provide adequate heat-dissipating area.

Locate the input bypass capacitor as close to the IC as possible. Route the PH pin to the output inductor. Because the PH connection is the switching node, the location of the output inductor should be very close to the PH pin, and minimize the area of the PCB conductor to prevent excessive capacitive coupling. Locate the boot capacitor close to the device. The sensitive analog ground connections for the feedback-voltage divider, compensation components, slow-start capacitor, and connect the frequency-setting resistor to a separate analog ground trace as shown. The RT/CLK pin is particularly sensitive to noise, so locate the RT resistor as close as possible to the IC and route with minimal lengths of trace. Place the additional external components approximately as shown. It may be possible to obtain acceptable performance with alternate PCB layouts. However this layout, meant as a guideline, produces demonstrably good results.

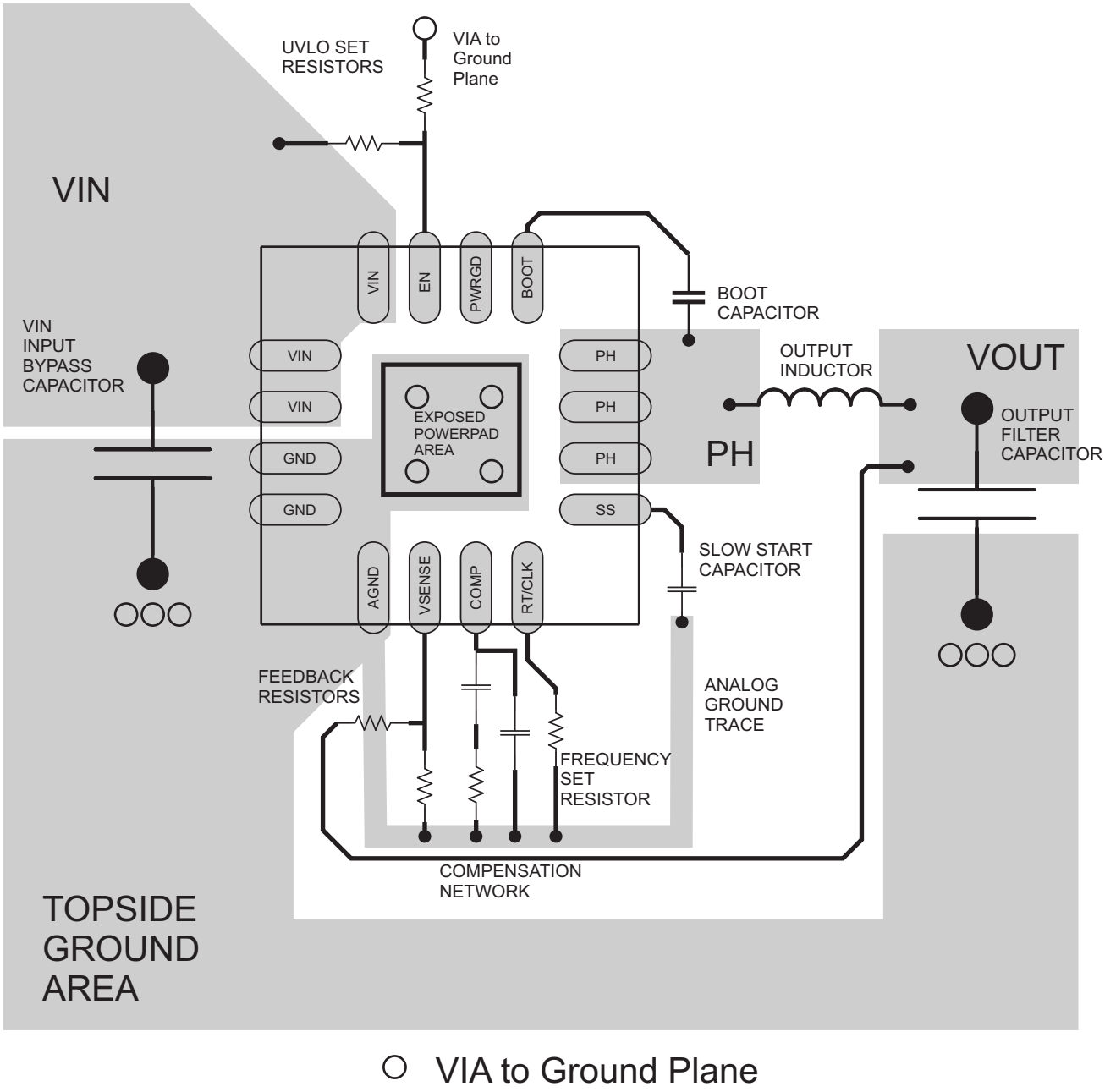


Figure 49. PCB Layout Example

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HPA02246QRTERQ1	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	618Q1	Samples
TPS54618QRTERQ1	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	618Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

OTHER QUALIFIED VERSIONS OF TPS54618-Q1 :

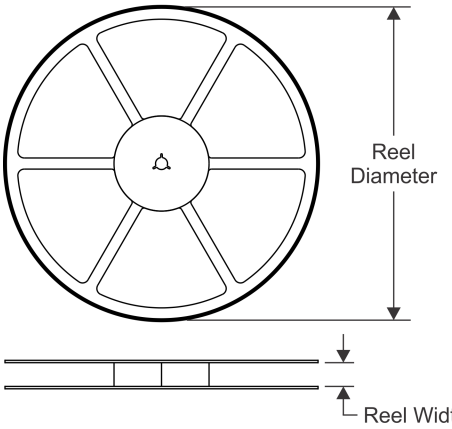
- Catalog: TPS54618

NOTE: Qualified Version Definitions:

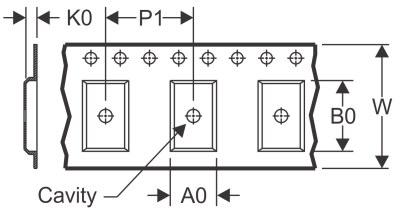
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

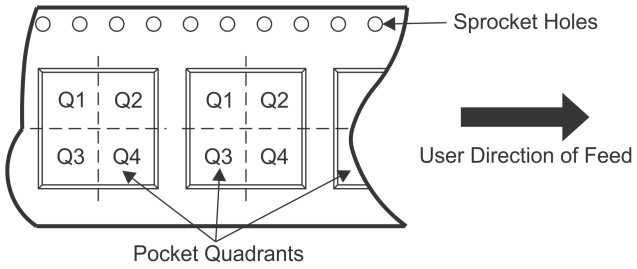


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

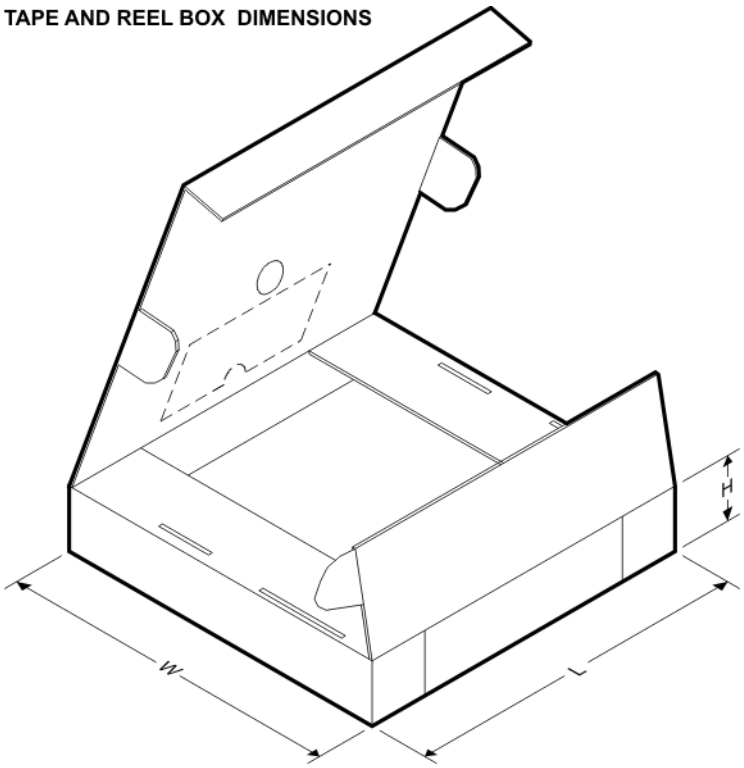
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54618QRTERQ1	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

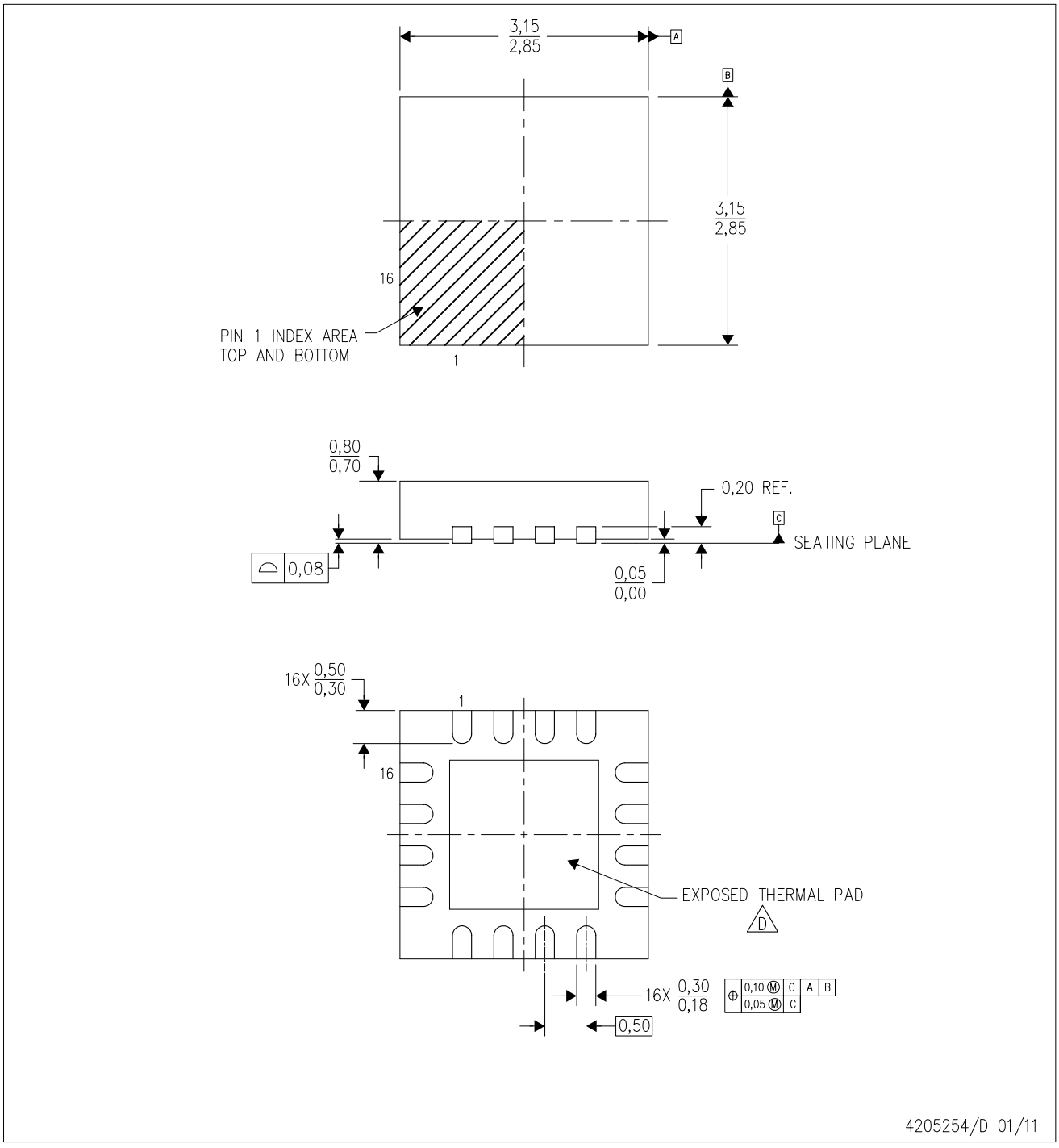
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54618QRTERQ1	WQFN	RTE	16	3000	367.0	367.0	35.0

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

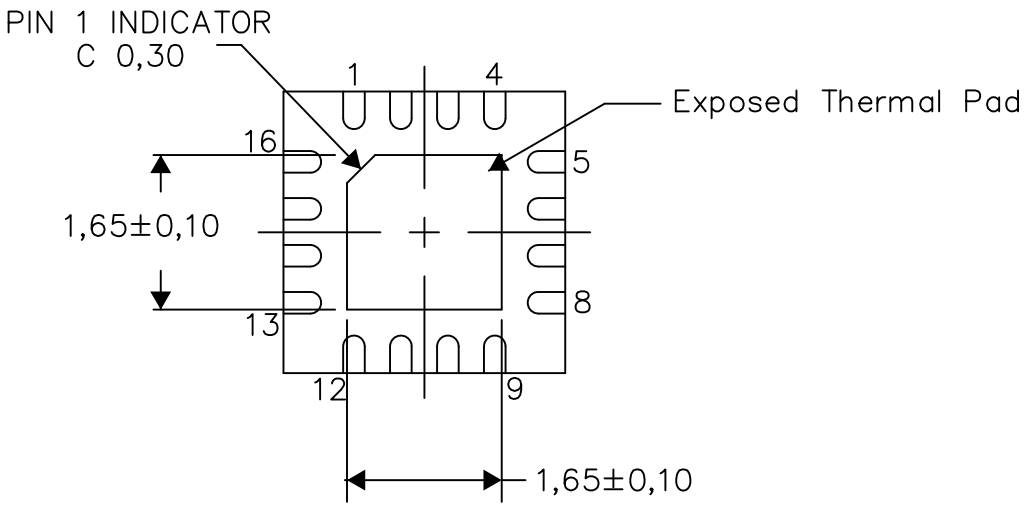
RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



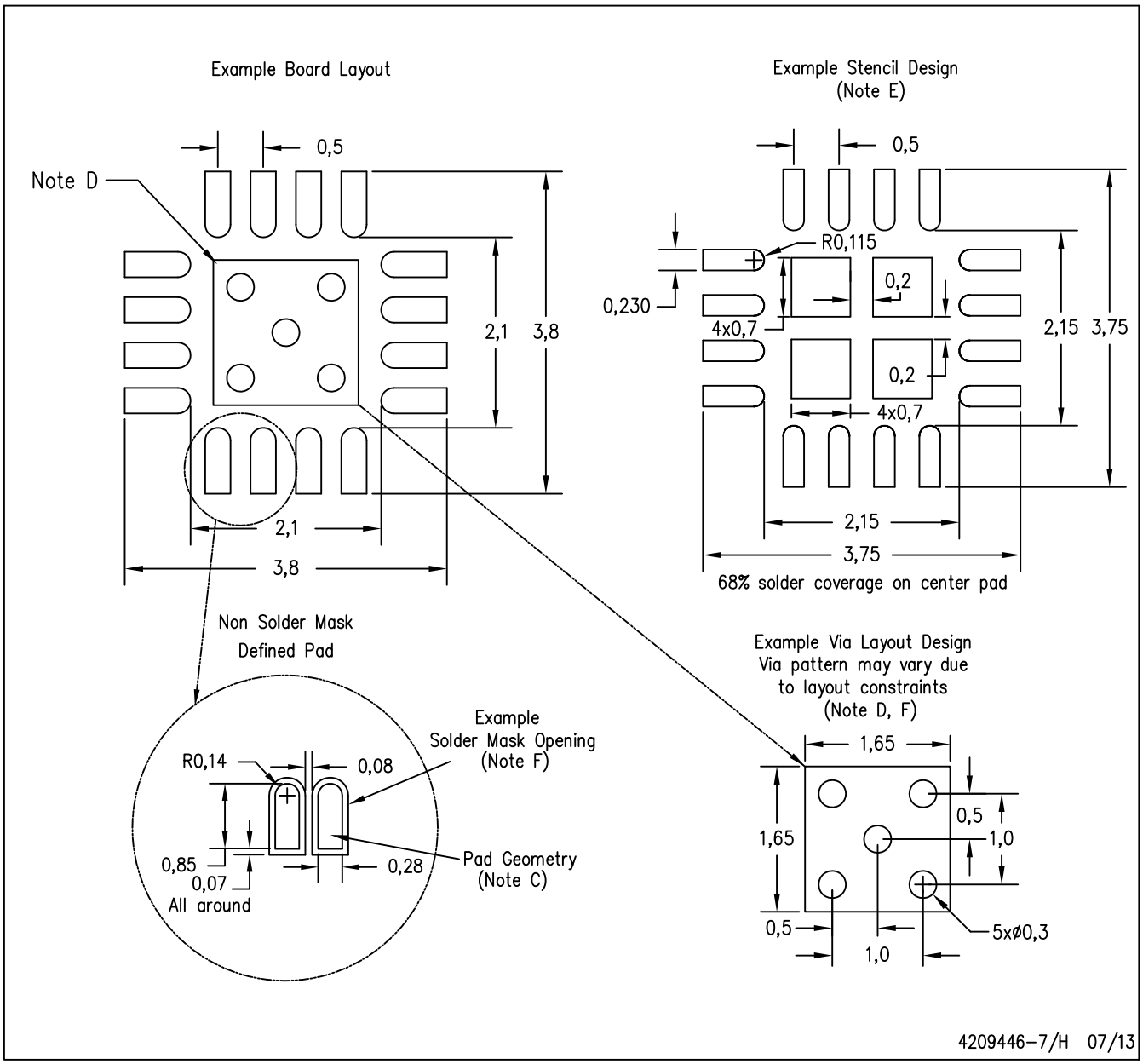
Bottom View

Exposed Thermal Pad Dimensions

4206446–4/N 07/13

NOTE: A. All linear dimensions are in millimeters

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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