TUSB7320, TUSB7340
USB 3.0 xHCI HOST CONTROLLER

Data Manual

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USB 3.0 xHCI HOST CONTROLLER

Check for Samples: TUSB7320, TUSB7340

1 INTRODUCTION

1.1 Features

- **USB 3.0 Compliant xHCI Host Controller**
  - **PCIe x1 Gen2 Interface**
  - **Four Downstream Ports**
- **Two or Four Downstream Ports**
- **Each Downstream Port**
  - **May Be Independently Enabled or Disabled**
  - **Has Adjustments for Transmit Swing, De-Emphasis, and Equalization Settings**
  - **May Be Marked as Removable/Non-Removable**
  - **Has Independent Power Control and Overcurrent Detection**
- **Requires No External Flash for Default Configuration**
  - **Optional Serial EEPROM for Custom Configuration**
- **Internal Spread Spectrum Generation**
  - **Low Cost Crystal or Oscillator Support**
- **Supports Input Frequencies Between 20 MHz and 50 MHz**
  - **Allows Use of 48-MHz System Reference Clock**
- **Best-In-Class Adaptive Receiver Equalizer Design**

1.2 Target Applications

- **Notebooks**
- **Desktop Computers**
- **Workstations**
- **Servers**
- **Add-In Cards and ExpressCard Implementations**
- **PCI Express-Based Embedded Host Controllers for HDTVs, Set-Top Boxes and Gaming Console Applications**

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2 OVERVIEW

2.1 Description

The TUSB7320 supports up to two downstream ports. The TUSB7340 is a USB 3.0 xHCI compliant host controller that supports up to four downstream ports. Both parts are available in a pin-compatible 100-pin RKM package. For the remainder of this document, the name TUSB73x0 is used to reference both the TUSB7320 and the TUSB7340.

Table 2-1. Package Information

PART	NO. DOWNSTREAM PORTS	PACKAGE
TUSB7320	2	100-pin RKM
TUSB7340	4	100-pin RKM

The TUSB73x0 interfaces to the host system via a PCIe x1 Gen 2 interface and provides SuperSpeed, high-speed, full-speed, or low-speed connections on the downstream USB ports.

A typical system view of the TUSB73x0 is shown below.

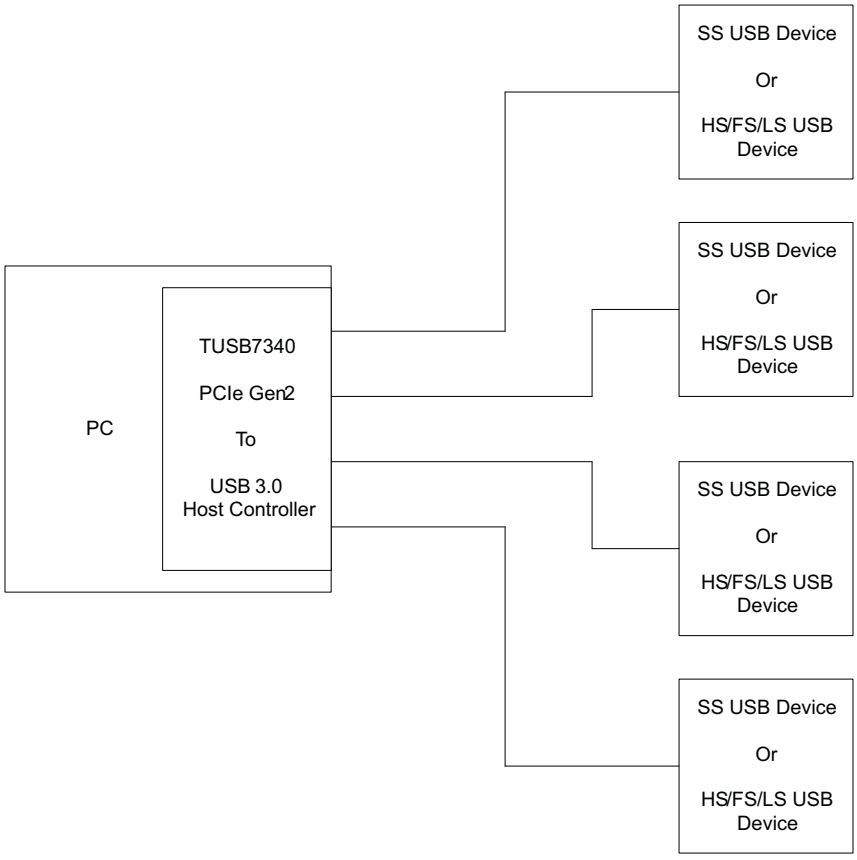

Figure 2-1. Typical Application

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2.2 Related Documents

- Universal Serial Bus 2.0 Specification
- Universal Serial Bus 3.0 Specification
- eXtensible Host Controller Interface for Universal Serial Bus (xHCI), Revision 0.96
- PCI Express Base Specification, Revision 2.1
- PCI Express Card Electromechanical Specification, Revision 2.0
- ExpressCard Standard, Release 2.0
- PCI Express Mini Card Electromechanical Specification, Revision 1.2
- PCI Bus Power Management Interface Specification, Revision 1.2
- PCI Local Bus Specification, Revision 3.0
- Guidelines for 64-Bit Global Identifier (EUI-64) Registration Authroity

2.3 Document's Conventions

Throughout this data manual, several conventions are used to convey information. These conventions are listed below:

1. To identify a binary number or field, a lower case b follows the numbers. For example: 000b is a 3-bit binary field.
2. To identify a hexadecimal number or field, a lower case h follows the numbers. For example: 8AFh is a 12-bit hexadecimal field.
3. All other numbers that appear in this document that do not have either a b or h following the number are assumed to be decimal format.
4. If the signal or terminal name has a bar above the name (for example, GRST), then this indicates the logical NOT function. When asserted, this signal is a logic low, 0, or 0b.
5. Differential signal names end with P, N, +, or – designators. The P or + designators signify the positive signal associated with the differential pair. The N or – designators signify the negative signal associated with the differential pair.
6. RSVD indicates that the referenced item is reserved.
7. In Section 4 through Section 6, the configuration space for the host controller is defined. For each register bit, the software access method is identified in an access column. The legend for this access column includes the following entries:
   - r – read access by software
   - u – updates by the host controller internal hardware
   - w – write access by software
   - c – clear an asserted bit with a write-back of 1b by software. Write of zero to the field has no effect
   - s – the field may be set by a write of one. Write of zero to the field has no effect
   - na – not accessible or not applicable

2.4 Available Options

2.5 ORDERING INFORMATION(1)

T_A	PACKAGE(2)	ORDERABLE PART NUMBER
0°C to 70°C	100-terminal (Lead-Free) (RKM) PWQFN	TUSB7320RKM
		TUSB7340RKM

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

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2.6 Terminal Assignments

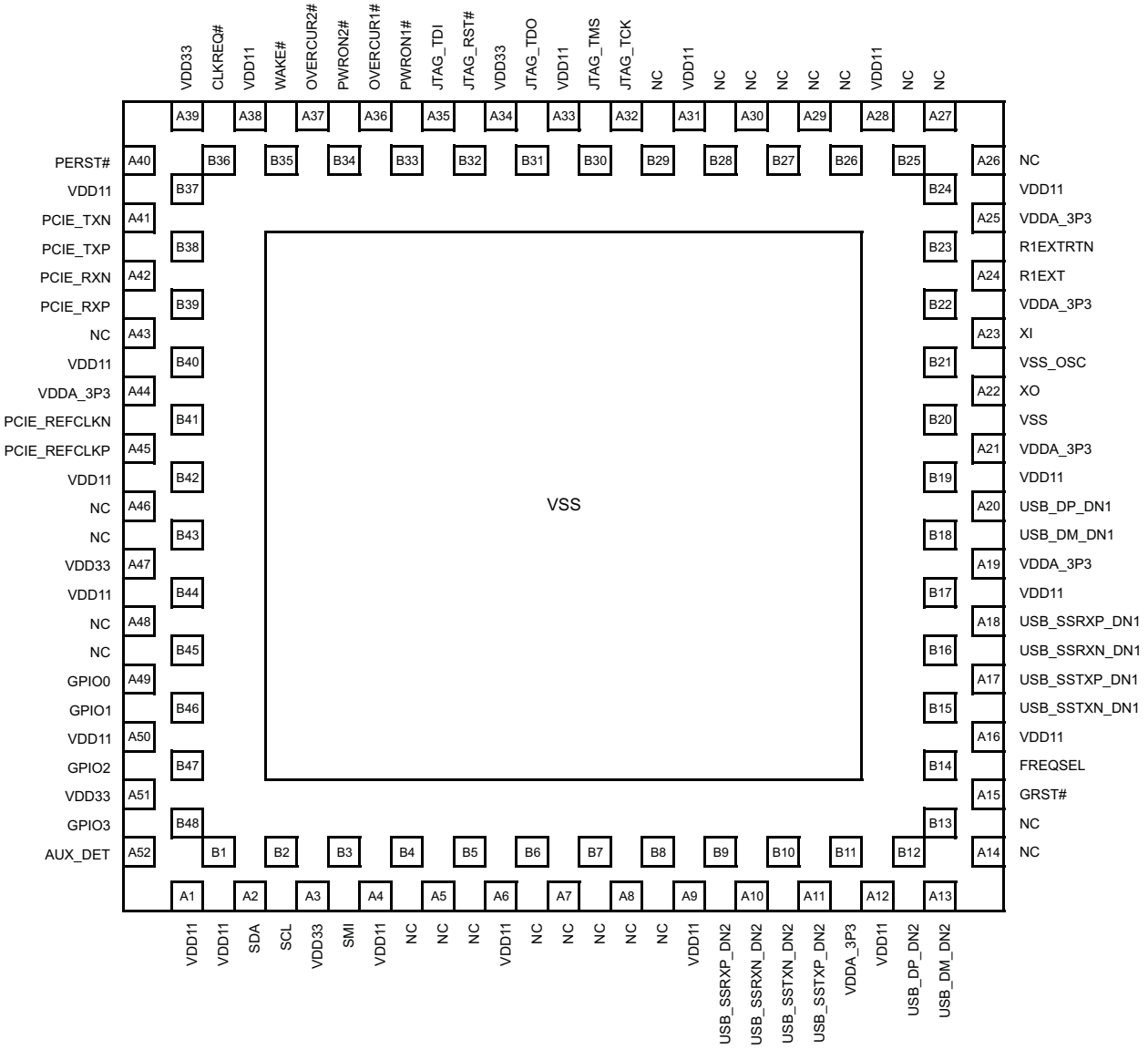

Figure 2-2. TUSB7320 RKM Package (Top View)

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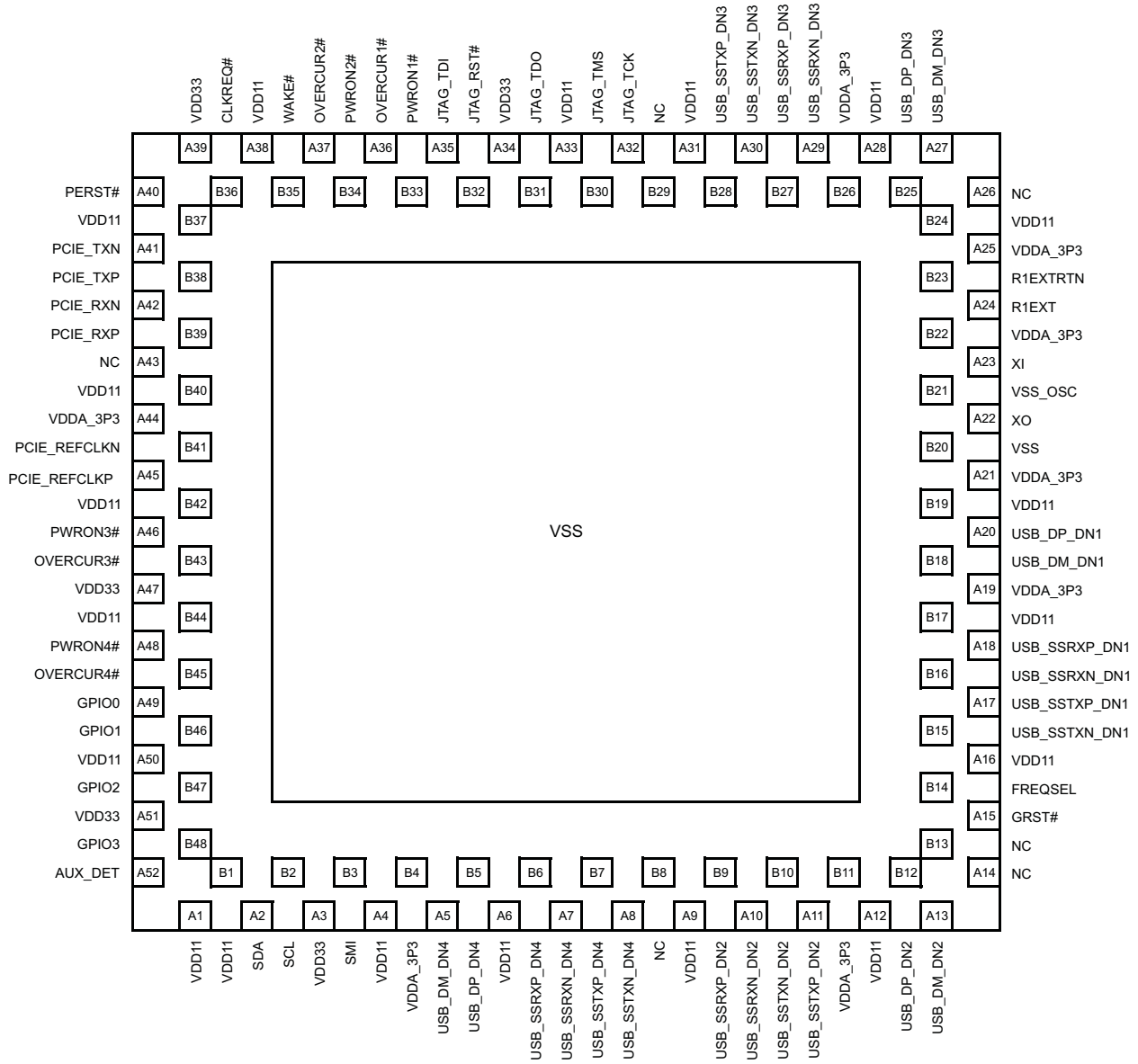

Figure 2-3. TUSB7340 RKM Package (Top View)

2.7 Terminal Descriptions

The following tables give a description of the terminals. These terminals are grouped in tables by functionality. Each table includes the terminal name, terminal number, I/O type, and terminal description.

TYPE	DESCRIPTION
I	Input
O	Output
I/O	Input/Output
PD, PU	Internal pull-down/pull-up
S	Strapping pin
P	Power supply
G	Ground

Table 2-2. Clock and Reset Signals

TERMINAL			I/O	DESCRIPTION
NAME	TUSB7320 PIN NO.	TUSB7340 PIN NO.		
GRST#	A15	A15	I PU	Global power reset. This reset brings all of the TUSB73x0 internal registers to their default states. When GRST# is asserted, the device is completely nonfunctional. GRST# should be asserted until all power rails are valid at the device.
XI	A23	A23	I	Crystal input. This terminal is the crystal input for the internal oscillator. The input may alternately be driven by the output of an external oscillator. When using a crystal a 1-MΩ feedback resistor is required between XI and XO.
XO	A22	A22	O	Crystal output. This terminal is crystal output for the internal oscillator. If XI is driven by an external oscillator this pin may be left unconnected. When using a crystal a 1-MΩ feedback resistor is required between XI and XO.
FREQSEL	B14	B14	I	Frequency select. This terminal indicates the oscillator input frequency and is used to configure the correct PLL multiplier. If the FREQSEL pin is '0', the frequency used is 48 MHz. If the FREQSEL pin is '1', refer to Table 4-100: USB Control Register Description.
PCIE_ REFCLKP PCIE_ REFCLKN	A45 B41	A45 B41	I	PCI Express Reference Clock. PCIE_REFCLKP and PCIE_REFCLKN comprise the differential input pair for the 100-MHz system reference clock.
PERST#	A40	A40	I	PCI Express Reset Input. The PERST# signal is used to signal when the system power is stable. The PERST# signal is also used to generate an internal power on reset

Table 2-3. PCI Express Signals

TERMINAL			I/O	DESCRIPTION
NAME	TUSB7320 PIN NO.	TUSB7340 PIN NO.		
PCIE_TXP	B38	B38	O	PCI Express transmitter differential pair (positive).
PCIE_TXN	A41	A41	O	PCI Express transmitter differential pair (negative).
PCIE_RXP	B39	B39	I	PCI Express receiver differential pair (positive).
PCIE_RXN	A42	A42	I	PCI Express receiver differential pair (negative).
WAKE#(1)	B35	B35	O	Wake. Wake is an active low signal that is driven low to reactivate the PCI Express link hierarchy's main power rails and reference clocks. Note: WAKE# is a failsafe I/O and can be connected to a 3.3-V auxiliary supply while VDD33 is not present.
CLKREQ#(1)	B36	B36	O	PCI Express REFCLK Request signal. Note: CLKREQ# is a failsafe I/O and can be connected to a 3.3-V auxiliary supply while VDD33 is not present.

(1) The only failsafe pins in the device are WAKE and CLKREQ#. No other pins are failsafe.

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Table 2-4. USB Downstream Signals

TERMINAL			I/O	DESCRIPTION
NAME	TUSB7320 PIN NO.	TUSB7340 PIN NO.		
USB_SSTXP_DN1	A17	A17	O	USB SuperSpeed transmitter differential pair (positive). Note: When routing, it is permissible to swap the positive and negative signals in Port 1 SSTX differential pair.
USB_SSTXN_DN1	B15	B15	O	USB SuperSpeed transmitter differential pair (negative). Note: When routing, it is permissible to swap the positive and negative signals in Port 1 SSTX differential pair.
USB_SSRXP_DN1	A18	A18	I	USB SuperSpeed receiver differential pair (positive). Note: When routing, it is permissible to swap the positive and negative signals in Port 1 SSRX differential pair.
USB_SSRXN_DN1	B16	B16	I	USB SuperSpeed receiver differential pair (negative). Note: When routing, it is permissible to swap the positive and negative signals in Port 1 SSRX differential pair.
USB_DP_DN1	A20	A20	I/O	USB High-speed differential transceiver (positive).
USB_DM_DN1	B18	B18	I/O	USB High-speed differential transceiver (negative).
PWRON1#	B33	B33	O PD	USB DS Port 1 Power On Control for Downstream Power. The terminal is used for control of the downstream power switch. If the PWRON_POLARITY bit is set to ‘1’, this pin is active high and the internal pull-down is disabled. This pin may be at low impedance when power rails are removed.
OVERCUR1#	A36	A36	I PU	USB DS Port 1 Over-Current Detection. 0: over-current detected; 1: over-current not detected
USB_SSTXP_DN2	A11	A11	O	USB SuperSpeed transmitter differential pair (positive). Note: When routing, it is permissible to swap the positive and negative signals in Port 2 SSTX differential pair.
USB_SSTXN_DN2	B10	B10	O	USB SuperSpeed transmitter differential pair (negative). Note: When routing, it is permissible to swap the positive and negative signals in Port 2 SSTX differential pair.
USB_SSRXP_DN2	B9	B9	I	USB SuperSpeed receiver differential pair (positive). Note: When routing, it is permissible to swap the positive and negative signals in Port 2 SSRX differential pair.
USB_SSRXN_DN2	A10	A10	I	USB SuperSpeed receiver differential pair (negative). Note: When routing, it is permissible to swap the positive and negative signals in Port 2 SSRX differential pair.
USB_DP_DN2	B12	B12	I/O	USB High-speed differential transceiver (positive).
USB_DM_DN2	A13	A13	I/O	USB High-speed differential transceiver (negative).
PWRON2#	B34	B34	O PD	USB DS Port 2 Power On Control for Downstream Power. The terminal is used for control of the downstream power switch. If the PWRON_POLARITY bit is set to ‘1’, this pin is active high and the internal pull-down is disabled. This pin may be at low impedance when power rails are removed.
OVERCUR2#	A37	A37	I PU	USB DS Port 2 Over-Current Detection. 0: over-current detected; 1: over-current not detected
USB_SSTXP_DN3	N/A	B28	O	USB SuperSpeed transmitter differential pair (positive). Note: When routing, it is permissible to swap the positive and negative signals in Port 3 SSTX differential pair.
USB_SSTXN_DN3	N/A	A30	O	USB SuperSpeed transmitter differential pair (negative). Note: When routing, it is permissible to swap the positive and negative signals in Port 3 SSTX differential pair.
USB_SSRXP_DN3	N/A	B27	I	USB SuperSpeed receiver differential pair (positive). Note: When routing, it is permissible to swap the positive and negative signals in Port 3 SSRX differential pair.
USB_SSRXN_DN3	N/A	A29	I	USB SuperSpeed receiver differential pair (negative). Note: When routing, it is permissible to swap the positive and negative signals in Port 3 SSRX differential pair.
USB_DP_DN3	N/A	B25	I/O	USB High-speed differential transceiver (positive).
USB_DM_DN3	N/A	A27	I/O	USB High-speed differential transceiver (negative).

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Table 2-4. USB Downstream Signals (continued)

TERMINAL			I/O	DESCRIPTION
NAME	TUSB7320 PIN NO.	TUSB7340 PIN NO.		
PWRON3#	N/A	A46	O PD	USB DS Port 3 Power On Control for Downstream Power. The terminal is used for control of the downstream power switch. If the PWRON_POLARITY bit is set to '1', this pin is active high and the internal pull-down is disabled. This pin may be at low impedance when power rails are removed.
OVERCUR3#	N/A	B43	I PU	USB DS Port 3 Over-Current Detection. 0: over-current detected; 1: over-current not detected
USB_SSTXP_DN4	N/A	B7	O	USB SuperSpeed transmitter differential pair (positive). Note: When routing, it is permissible to swap the positive and negative signals in Port 4 SSTX differential pair.
USB_SSTXN_DN4	N/A	A8	O	USB SuperSpeed transmitter differential pair (negative). Note: When routing, it is permissible to swap the positive and negative signals in Port 4 SSTX differential pair.
USB_SSRXP_DN4	N/A	B6	I	USB SuperSpeed receiver differential pair (positive). Note: When routing, it is permissible to swap the positive and negative signals in Port 4 SSRX differential pair.
USB_SSRXN_DN4	N/A	A7	I	USB SuperSpeed receiver differential pair (negative). Note: When routing, it is permissible to swap the positive and negative signals in Port 4 SSRX differential pair.
USB_DP_DN4	N/A	B5	I/O	USB High-speed differential transceiver (positive).
USB_DM_DN4	N/A	A5	I/O	USB High-speed differential transceiver (negative).
PWRON4#	N/A	A48	O PD	USB DS Port 4 Power On Control for Downstream Power. The terminal is used for control of the downstream power switch. If the PWRON_POLARITY bit is set to '1', this pin is active high and the internal pull-down is disabled. This pin may be at low impedance when power rails are removed.
OVERCUR4#	N/A	B45	I PU	USB DS Port 4 Over-Current Detection. 0: over-current detected; 1: over-current not detected

Table 2-5. I^2C Signals

TERMINAL			I/O	DESCRIPTION
NAME	TUSB7320 PIN NO.	TUSB7340 PIN NO.		
SCL	B2	B2	I/O	I^2C Clock - If no I^2C device is present, pull this line down to disable.
SDA	A2	A2	I/O	I^2C Data - If no I^2C device is present, pull this line down to disable.

Table 2-6. Test and Miscellaneous Signals

TERMINAL			I/O	DESCRIPTION
NAME	TUSB7320 PIN NO.	TUSB7340 PIN NO.		
JTAG_TCK	A32	A32	I PD	JTAG test clock
JTAG_TDI	A35	A35	I PU	JTAG test data in
JTAG_TDO	B31	B31	O PD	JTAG test data out
JTAG_TMS	B30	B30	I PU	JTAG test mode select
JTAG_RST#	B32	B32	I PD	JTAG reset. Should be pulled low for normal operation.

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Table 2-6. Test and Miscellaneous Signals (continued)

TERMINAL			I/O	DESCRIPTION
NAME	TUSB7320 PIN NO.	TUSB7340 PIN NO.		
GPIO[0] GPIO[1] GPIO[2] GPIO[3]	A49, B46, B47, B48	A49, B46, B47, B48	I/O PU	General purpose I/O
SMI	B3	B3	O	System management interrupt Note: This pin is active high and should not be pulled up/down.
R1EXT R1EXTRTN	A24, B23	A24, B23	OI	High precision external resistor used for calibration. A resister value of 9.09 KΩ ±1% accuracy is connected between the terminals R1EXT and R1EXTRTN.
AUX_DET	A52	A52	I	Auxiliary power detect. This pin indicates if the TUSB73X0 is enabled for wakeup from D3cold. Note: If this feature is implemented, AUX_DET must be pulled to VDD33 to prevent leakage.
NC	B4, A5, B5, B6, A7, B7, A8, B8, B13, A14, B25, A26, B26, A27, B27, B28, A29, B29, A30, A43, B43, B45, A46, A48	A14, B8, B13, A26, B29, A43	I/O	Pins are not connected internally. Note: TUSB7320 pins B4 and B26 may be connected to VDDA_3P3 to support a dual-layout option with the TUSB7340.

Table 2-7. Power Signals

TERMINAL			I/O	DESCRIPTION
NAME	TUSB7320 PIN NO.	TUSB7340 PIN NO.		
VDD33	A3, A34, A39, A47, A51	A3, A34, A39, A47, A51	PWR	3.3-V I/O power rail
VDDA_3P3	B11, A19, A21, A25, B22, A44	B4, B11, A19, A21, A25, B22, B26, A44	PWR	3.3-V analog power rail
VDD11	A1, B1, A4, A6, A9, A12, A16, B17, B19, B24, A28, A33, A31, A38, B37, B40, B42, B44, A50	A1, B1, A4, A6, A9, A12, A16, B17, B19, B24, A28, A33, A31, A38, B37, B40, B42, B44, A50	PWR	1.1-V core power rail
VSS	B20, A53	B20, A53	PWR	Ground. The ground pad is labeled A53 for schematic purposes.
VSS_NC	C1, C2, C3, C4	C1, C2, C3, C4	PWR	The corner pins, which are for mechanical stability of the package, are connected to ground internally. These pins may be connected to VSS or left unconnected.
VSS_OSC	B21	B21	PWR	Oscillator return. If using a crystal, the load capacitors should use this signal as the return path and it should not be connected to the PCB ground. If using an oscillator, this should be connected to PCB Ground.

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3 FEATURE/PROTOCOL DESCRIPTIONS

3.1 Power-Up/-Down Sequencing

The host controller contains both 1.1-V and 3.3-V power terminals. The following power-up and power-down sequences describe how power is applied to these terminals.

In addition, the host controller has three resets: PERST#, GRST#, and an internal power- on reset. These resets are fully described in the next section. The following power-up and power-down sequences describe how PERST# is applied to the host controller.

The application of the PCI Express reference clock (PCIE_REFCLK) is important to the power-up/-down sequence and is included in the following power-up and power-down descriptions.

3.1.1 Power-Up Sequence

1. Assert PERST# to the device.
2. Apply 1.1-V and 3.3-V voltages.
3. GRST# must remain asserted until both the 1.1-V and 3.3-V voltages have reached the minimum recommended operating voltage, see Section 11.2.
4. Apply a stable PCI Express reference clock.
5. To meet PCI Express specification requirements, PERST cannot be deasserted until the following two delay requirements are satisfied:

Wait a minimum of 100 µs after applying a stable PCI Express reference clock. The 100-µs limit satisfies the requirement for stable device clocks by the de-assertion of PERST.

Wait a minimum of 100 ms after applying power. The 100-ms limit satisfies the requirement for stable power by the de-assertion of PERST.

See the power-up sequencing diagram in Figure 3-1.

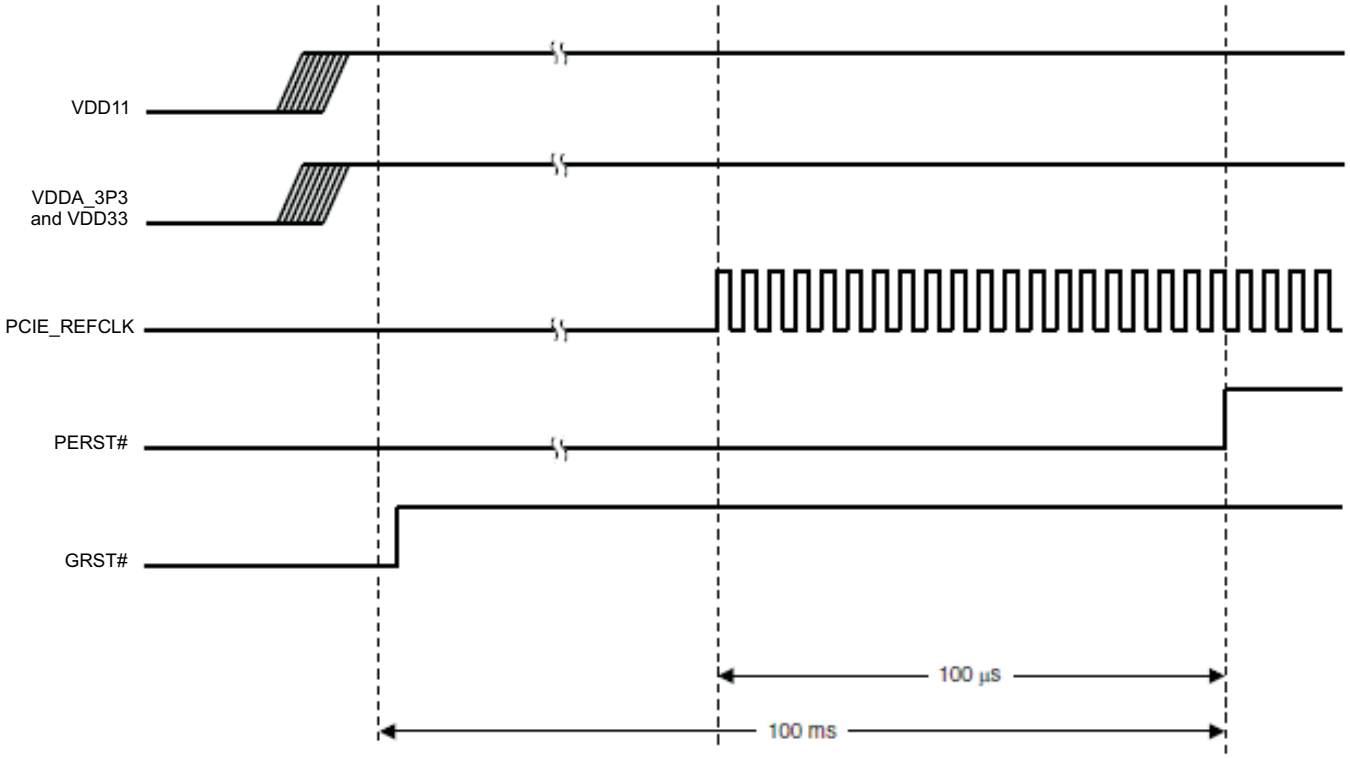

Figure 3-1. Power-Up Sequence

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3.1.2 Power-Down Sequence

1. Assert PERST# to the device.
2. Remove the reference clock.
3. Remove the 3.3-V and 1.1-V voltages

See the power power-down sequencing diagram in Figure 3-2. If the VDD33_AUX terminal is to remain powered after a system shutdown, then the host controller power-down sequence is exactly the same as shown in Figure 3-2.

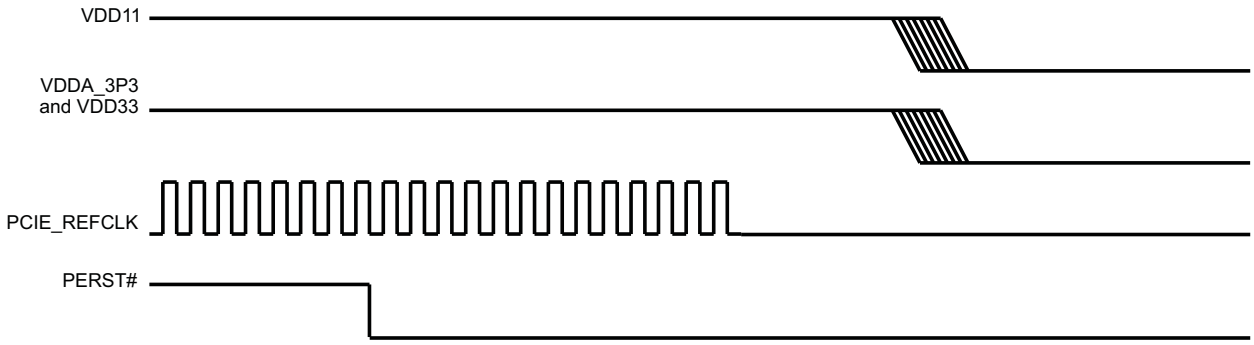

Figure 3-2. Power-Down Sequence

3.2 Two-Wire Serial-Bus Interface

The host controller provides a two-wire serial-bus interface to load subsystem identification information and specific register defaults from an external EEPROM. The serial-bus interface signals include SDA and SCL. The use of an external EEPROM is optional. The TUSB73x0 will function with the default settings. For motherboard down applications, BIOS can be used to set all of the options available on the TUSB73x0.

On a PCIe Add-in Card, an EEPROM is only needed if a any of the following is true:

- Use of a crystal other than 48 MHz.
- Mark one or more USB ports as non-removable.
- Disable one or more USB ports.
- Set a PCIe Subsystem ID and Subsystem Vendor ID.
- Change the default de-emphasis/swing/equalizer settings of the SuperSpeed USB ports.
- Change the default L0s and L1 latency values for PCIe.
- Change the default PWRON polarity to active high instead of active low.

3.2.1 Serial-Bus Interface Implementation

To enable the serial-bus interface, a pull-up resistor must be implemented on the SCL signal. At the rising edge of PERST# or GRST#, whichever occurs later in time, the SCL terminal is checked for a pull-up resistor. If one is detected, then bit 3 (SBDETECT) in the serial-bus control and status register (see Section 4.52) is set. Software may disable the serial-bus interface at any time by writing a 0b to the SBDETECT bit. If no external EEPROM is required, then the serial-bus interface is permanently disabled by attaching a pulldown resistor to the SCL signal.

The host controller implements a two-terminal serial interface with one clock signal (SCL) and one data signal (SDA). The SCL signal is a unidirectional output from the host controller and the SDA signal is

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bidirectional. Both are open-drain signals and require pull-up resistors. The host controller is a bus master device and drives SCL at approximately 60 kHz during data transfers and places SCL in a high-impedance state (0 frequency) during bus idle states. The serial EEPROM is a bus slave device and must acknowledge a slave address equal to A0h. Figure 3-3 illustrates an example application implementing the two-wire serial bus.

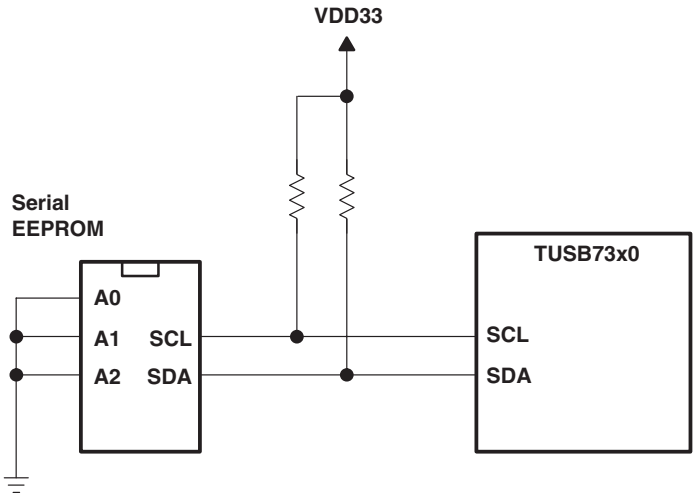

Figure 3-3. Serial EEPROM Application

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3.2.2 Serial-Bus Interface Protocol

All data transfers are initiated by the serial-bus master. The beginning of a data transfer is indicated by a start condition, which is signaled when the SDA line transitions to the low state while SCL is in the high state, as illustrated in Figure 3-4. The end of a requested data transfer is indicated by a stop condition, which is signaled by a low-to-high transition of SDA while SCL is in the high state, as shown in Figure 3-4. Data on SDA must remain stable during the high state of the SCL signal, as changes on the SDA signal during the high state of SCL are interpreted as control signals, that is, a start or stop condition.

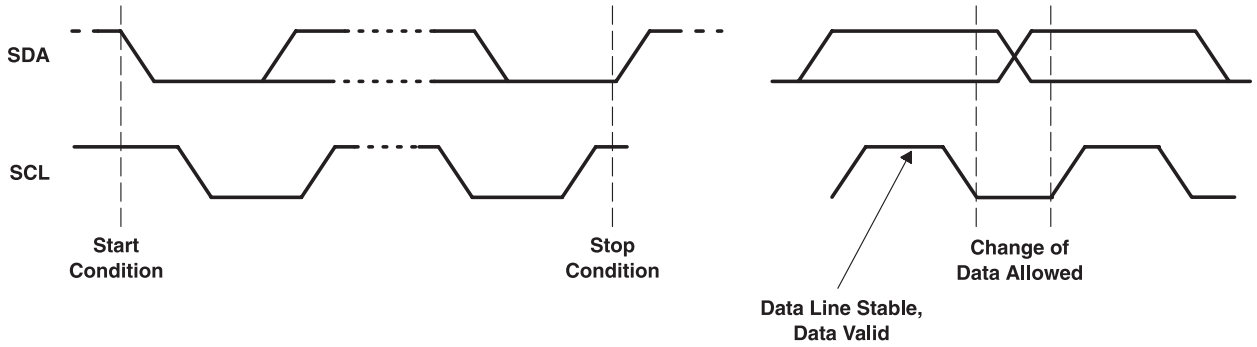

Figure 3-4. Serial-Bus Start/Stop Conditions and Bit Transfers

Data is transferred serially in 8-bit bytes. During a data transfer operation, the exact number of bytes that are transmitted is unlimited. However, each byte must be followed by an acknowledge bit to continue the data transfer operation. An acknowledge (ACK) is indicated by the data byte receiver pulling the SDA signal low, so that it remains low during the high state of the SCL signal. Figure 3-5 illustrates the acknowledge protocol.

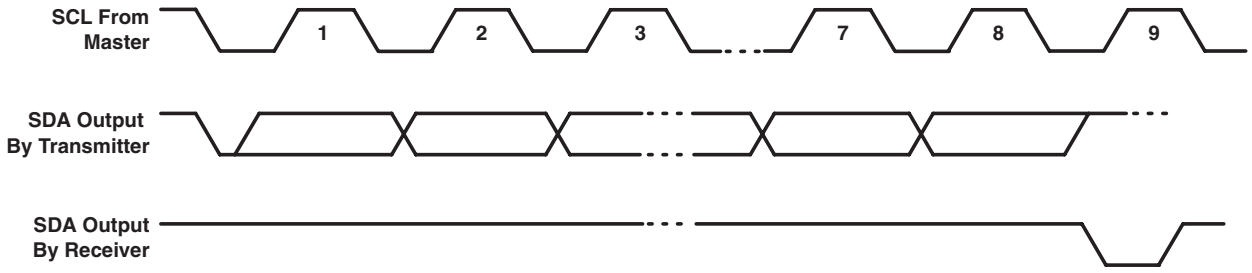

Figure 3-5. Serial-Bus Protocol Acknowledge

The host controller performs three basic serial-bus operations: single byte reads, single byte writes, and multibyte reads. The single byte operations occur under software control. The multibyte read operations are performed by the serial EEPROM initialization circuitry immediately after a PCI Express reset. See Section 11.6, *Serial-Bus EEPROM Application*, for details on how the host controller automatically loads the subsystem identification and other register defaults from the serial-bus EEPROM.

Figure 3-6 illustrates a single byte write. The host controller issues a start condition and sends the 7-bit slave device address and the R/W command bit is equal to 0b. A 0b in the R/W command bit indicates that the data transfer is a write. The slave device acknowledges if it recognizes the slave address. If no acknowledgment is received by the host controller, then bit 1 (SB_ERR) is set in the serial-bus control and status register (PCI offset BCh, see Section 4.52). Next, the EEPROM word address is sent by the host controller, and another slave acknowledgment is expected. Then the host controller delivers the data byte MSB first and expects a final acknowledgment before issuing the stop condition.

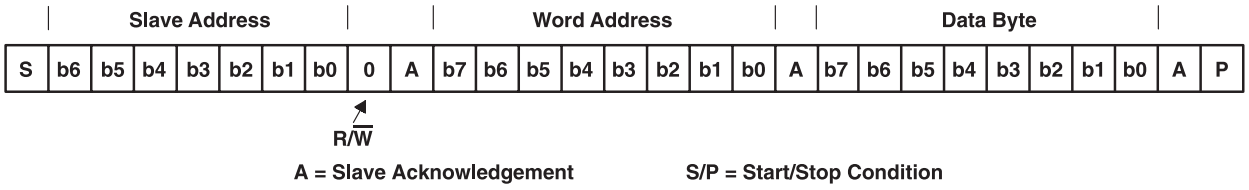

Figure 3-6. Serial-Bus Protocal - Byte Write

Figure 3-7 illustrates a single byte read. The host controller issues a start condition and sends the 7-bit slave device address and the R/W command bit is equal to 0b (write). The slave device acknowledges if it recognizes the slave address. Next, the EEPROM word address is sent by the host controller, and another slave acknowledgment is expected. Then, the host controller issues a restart condition followed by the 7-bit slave address and the R/W command bit is equal to 1b (read). Once again, the slave device responds with an acknowledge. Next, the slave device sends the 8-bit data byte, MSB first. Since this is a 1-byte read, the host controller responds with no acknowledge (logic high) indicating the last data byte. Finally, the host controller issues a stop condition.

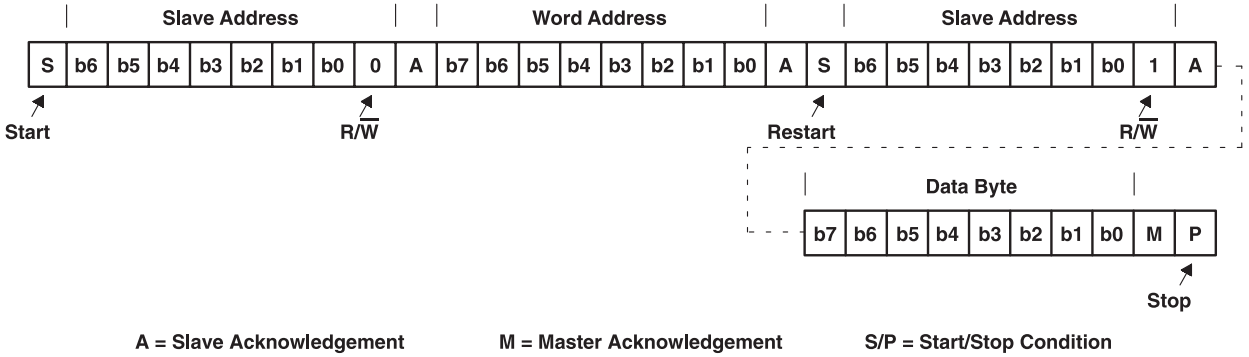

Figure 3-7. Serial-Bus Protocal - Byte Read

Figure 3-8 illustrates the serial interface protocol during a multi-byte serial EEPROM download. The serial-bus protocol starts exactly the same as a 1-byte read. The only difference is that multiple data bytes are transferred. The number of transferred data bytes is controlled by the host controller master. After each data byte, the host controller master issues acknowledge (logic low) if more data bytes are requested. The transfer ends after a host controller master no acknowledge (logic high) followed by a stop condition.

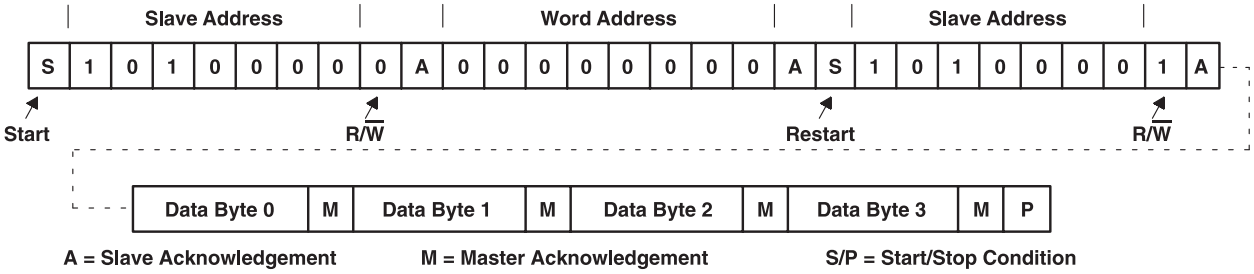

Figure 3-8. Serial-Bus Protocal - Multibyte Read

Bit 7 (PROT_SEL) in the serial-bus control and status register changes the serial-bus protocol. Each of the three previous serial-bus protocol figures illustrates the PROT_SEL bit default (logic low). When this control bit is asserted, the word address and corresponding acknowledge are removed from the serial-bus protocol. This feature allows the system designer a second serial-bus protocol option when selecting external EEPROM devices.

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3.2.3 Serial-Bus EEPROM Application

A serial EEPROM interface is implemented to pre-load several registers. The registers and corresponding bits that are loaded through the EEPROM are provided in Table 3-1.

Table 3-1. EEPROM Register Loading Map

SERIAL EEPROM WORD ADDRESS	BYTE DESCRIPTION
00h	TUSB73X0 Function Indicator (00h)
01h	Number of Bytes (19h)
02h	PCI D0h, Subsystem Vendor ID, Byte 0
03h	PCI D1h, Subsystem Vendor ID, Byte 1
04h	PCI D2h, Subsystem ID, Byte 0
05h	PCI D3h, Subsystem ID, Byte 1
06h	PCI D4h, General Control 0, Byte 0
07h	PCI D5h, General Control 0, Byte 1
08h	PCI D8h, General Control 1, Byte 0
09h	PCI DCh, General Control 2, Byte 0
0Ah	PCI E0h, USB Control, Byte 0
0Bh	PCI E1h, USB Control, Byte 1
0Ch	PCI E2h, USB Control, Byte 2
0Dh	PCI E3h, USB Control, Byte 3
0Eh	PCI E4h, De-emphasis and Swing Control, Byte 0
0Fh	PCI E5h, De-emphasis and Swing Control, Byte 1
10h	PCI E6h, De-emphasis and Swing Control, Byte 2
11h	PCI E7h, De-emphasis and Swing Control, Byte 3
12h	PCI E8h, Equalizer Control, Byte 0
13h	PCI E9h, Equalizer Control, Byte 1
14h	PCI EAh, Equalizer Control, Byte 2
15h	PCI EBh, Equalizer Control, Byte 3
16h	PCI ECh, Custom PHY Transmit/Receive Control, Byte 0
17h	PCI EDh, Custom PHY Transmit/Receive Control, Byte 1
18h	PCI EEh, Custom PHY Transmit/Receive Control, Byte 2
19h	PCI EFh, Custom PHY Transmit/Receive Control, Byte 3
1Ah	PCI 61h, Frame Length Adjustment Register
1Bh	End of List Indicator (80h)

This format must be explicitly followed for the host controller to correctly load initialization values from a serial EEPROM. All byte locations must be considered when programming the EEPROM.

The serial EEPROM is addressed by the host controller at slave address 1010 000b. This slave address is internally hardwired and cannot be changed by the system designer. Therefore, all three hardware address bits for the EEPROM are tied to VSS to achieve this address. The serial EEPROM in the sample application circuit (Figure 3-3) assumes the 1010b high-address nibble. The lower three address bits are terminal inputs to the chip, and the sample application shows these terminal inputs tied to VSS.

During an EEPROM download operation, bit 4 (ROMBUSY) in the serial-bus control and status register is asserted. After the download is finished, bit 0 (ROM_ERR) in the serial-bus control and status register may be monitored to verify a successful download.

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3.3 System Management Interrupt

The TUSB73X0 includes a System Management Interrupt (SMI) pin to allow for USB support in the BIOS of a system that implements the TUSB73X0. The SMI pin is controlled by the bits in the USB Legacy Support Control/Status Register. See Section 6.6.2 for more information. If there are no SMI events pending or if all sources for SMI are disabled, the TUSB73X0 drives the SMI pin low. When an SMI event occurs and the corresponding event is enabled, the TUSB73X0 drives the SMI pin high until the event is cleared or disabled.

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4 CLASSIC PCI CONFIGURATION SPACE

4.1 The PCI Configuration Map

The programming model of the TUSB73X0 USB 3.0 Host Controller is compliant to the standard PCI device programming model. The PCI configuration map uses the type 0 PCI header.

All bits marked with a '*' are sticky bits and are reset by a global reset (GRST) or the internally-generated power-on reset. All bits marked with a '†' are reset by a PCI Express reset (PERST), a GRST, or the internally-generated power-on reset. The remaining register bits are reset by a PCI Express hot reset, PERST, GRST, or the internally-generated power-on reset.

Table 4-1. PCI Configuration Register Map

REGISTER NAME				OFFSET
Device ID		Vendor ID		000h
Status		Command		004h
Class Code			Revision ID	008h
BIST	Header Type	Latency Timer	Cache Line Size	00Ch
Base Address Register 0				010h
Base Address Register 1				014h
Base Address Register 2				018h
Base Address Register 3				01Ch
Reserved				020h-028h
Subsystem ID		Subsystem Vendor ID		02Ch
Reserved				030h
Reserved			Capabilities Pointer	034h
Reserved				038h
Max Latency	Min Grant	Interrupt Pin	Interrupt Line	03Ch
Power Management Capabilities		Next Item Pointer	PM CAP ID	040h
PM Data (RSVD)	PMCSR_BSE	Power Management CSR		044h
MSI Message Control		Next Item Pointer	MSI CAP ID	048h
MSI Message Address				04Ch
MSI Upper Message Address				050h
Reserved		MSI Message Data		054h
Reserved				058h-05Ch
Reserved		FLADJ	SBRN	60h
Reserved				064h-06Ch
PCI Express Capabilities Register		Next Item Pointer	PCI Express Capability ID	070h
Device Capabilities				074h
Device Status		Device Control		078h
Link Capabilities				07Ch
Link Status		Link Control		080h
Reserved				084h-090h
Device Capabilities2				094h
Device Status2		Device Control2		098h
Link Capabilities2				09Ch
Link Status2		Link Control2		0A0h
Reserved				0A4h-0ACh
Serial Bus CSR	Serial Bus Slave Address	Serial Bus Index	Serial Bus Data	0B0h
GPIO Data		GPIO Control		0B4h
Reserved				0B8h-0BCh

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Table 4-1. PCI Configuration Register Map (continued)

MSI-X Message Control	Next Item Pointer	MSI-X CAP ID	0C0h
MSI-X Table Offset and BIR			0C4h
MSI-X PBA Offset and BIR			0C8h
Reserved			0CCh
Subsystem Access			0D0h
General Control 0			0D4h
General Control 1			0D8h
General Control 2			0DCh
USB Control			0E0h
Deemphasis and Swing Control			0E4h
Equalizer Control			0E8h
Custom PHY Transmit/Receive Control			0ECh
Reserved			0F0h-0FCh

4.2 Vendor ID Register

This 16-bit read only register contains the value 104Ch, which is the vendor ID assigned to Texas Instruments.

PCI register offset: 00h

Register type: Read-only

Default value: 104Ch

Table 4-2. PCI Register 00h

Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	1	0	0	0	0	0	1	0	0	1	1	0	0

4.3 Device ID Register

This 16-bit read only register contains the value 8241h, which is the device ID assigned by TI to the TUSB73X0.

PCI register offset: 02h

Register type: Read-only

Default value: 8241h

Table 4-3. PCI Register 02h

Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0	1

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4.4 Command Register

The Command register provides control over the TUSB73X0 interface to the PCIe interface

PCI register offset: 04h

Register type:Read-only, Read/Write

Default value: 0000h

Table 4-4. PCI Register 04h

Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-5. Bit Command Register Description

Bit	Field Name	Access	Description
15:11	RSVD	r	Reserved. Returns zeros when read.
10	INT_DISABLE	rw	INTx# Disable. This bit enables device specific interrupts.
9	FBB_ENB	r	Fast back-to-back enable. The host controller does not generate fast back-to-back transactions; therefore, this bit returns 0 when read.
8	SERR_ENB	rw	SERR enable bit. When this bit is set, the host controller can signal fatal and nonfatal errors on the PCI Express interface on behalf of SERR assertions detected on the PCI bus. 0 = Disable the reporting of nonfatal errors and fatal errors (default) 1 = Enable the reporting of nonfatal errors and fatal errors
7	STEP_ENB	r	Address/data stepping control. The host controller does not support address/data stepping, and this bit is hardwired to 0b.
6	PERR_ENB	rw	Controls the setting of bit 8 (DATAPAR) in the status register (offset 06h, see Section 4.5) in response to a received poisoned TLP from PCI Express. A received poisoned TLP is forwarded with bad parity to conventional PCI regardless of the setting of this bit. 0 = Disables the setting of the master data parity error bit (default) 1 = Enables the setting of the master data parity error bit
5	VGA_ENB	r	VGA palette snoop enable. The host controller does not support VGA palette snooping; therefore, this bit returns 0b when read.
4	MWI_ENB	r	Memory write and invalidate enable. The host controller does not support memory write and invalidate enable; therefore, this bit returns 0b when read.
3	SPECIAL	r	Special cycle enable. This host controller does not respond to special cycle transactions; therefore, this bit returns 0 when read.
2	MASTER_ENB	rw	Bus master enable. When this bit is set, the host controller is enabled to initiate transactions on the PCI Express interface. 0 = PCI Express interface cannot initiate transactions. The host controller must disable the response to memory and I/O transactions on the PCI interface (default). 1 = PCI Express interface can initiate transactions. The host controller can forward memory and I/O transactions from PCI secondary interface to the PCI Express interface.
1	MEMORY_ENB	rw	Memory space enable. Setting this bit enables the host controller to respond to memory transactions on the PCI Express interface. 0 = PCI Express receiver cannot process downstream memory transactions and must respond with an unsupported request (default) 1 = PCI Express receiver can process downstream memory transactions. The host controller can forward memory transactions to the PCI interface.
0	IO_ENB	r	I/O space enable. Setting this bit enables the host controller to respond to I/O transactions on the PCI Express interface. 0 = PCI Express receiver cannot process downstream I/O transactions and must respond with an unsupported request (default) 1 = PCI Express receiver can process downstream I/O transactions. The host controller can forward I/O transactions to the PCI interface.

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4.5 Status Register

The status register provides information about the PCI Express interface to the system.

PCI register offset: 06h

Register type:Read-only, Read/Clear

Default value: 0010h

Table 4-6. PCI Register 06h

Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-7. Status Register Description

Bit	Field Name	Access	Description
15	PAR_ERR	rcu	Detected parity error. This bit is set when the PCI Express interface receives a poisoned TLP. This bit is set regardless of the state of bit 6 (PERR_ENB) in the command register (offset 04h, see Section 4.4). 0 = No parity error detected 1 = Parity error detected
14	SYS_ERR	rcu	Signaled system error. This bit is set when the host controller sends an ERR_FATAL or ERR_NONFATAL message and bit 8 (SERR_ENB) in the command register (offset 04h, see Section 4.4) is set. 0 = No error signaled 1 = ERR_FATAL or ERR_NONFATAL signaled
13	MABORT	rcu	Received master abort. This bit is set when the PCI Express interface of the host controller receives a completion-with-unsupported-request status. 0 = Unsupported request not received on the PCI Express interface 1 = Unsupported request received on the PCI Express interface
12	TABORT_REC	rcu	Received target abort. This bit is set when the PCI Express interface of the host controller receives a completion-with-completer-abort status. 0 = Completer abort not received on the PCI Express interface 1 = Completer abort received on the PCI Express interface
11	TABORT_SIG	rcu	Signaled target abort. This bit is set when the PCI Express interface completes a request with completer abort status. 0 = Completer abort not signaled on the PCI Express interface 1 = Completer abort signaled on the PCI Express interface
10:9	DEVSEL_TIMING	r	DEVSEL Timing. These bits are read only zero, because they do not apply to PCI Express.
8	DATAPAR	rcu	Master data parity error. This bit is set if bit 6 (PERR_ENB) in the command register (offset 04h, see Section 4.4) is set and the host controller receives a completion with data marked as poisoned on the PCI Express interface or poisons a write request received on the PCI Express interface. 0 = No uncorrectable data error detected on the primary interface 1 = Uncorrectable data error detected on the primary interface.
7	FBB_CAP	r	Fast back-to-back capable. This bit does not have a meaningful context for a PCI Express device and is hardwired to 0b.
6	RSVD	r	Reserved. Returns zeros when read.
5	66MHZ	r	66 MHz capable. This bit does not have a meaningful context for a PCI Express device and is hardwired to 0b.
4	CAPLIST	r	Capabilities list. This bit returns 1b when read, indicating that the host controller supports additional PCI capabilities.
3	INT_STATUS	ru	Interrupt Status. This bit reflects the interrupt status of the function.
2:0	RSVD	r	Reserved. Returns zeros when read.

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4.6 Class Code and Revision ID Register

This read only register categorizes the Base Class, Sub Class, and Programming Interface of the TUSB73X0. The Base Class is 0Ch, identifying the device as a Serial Bus Controller. The Sub Class is 03h, identifying the function as a Universal Serial Bus Host Controller, and the Programming Interface is 30h, identifying the function as a USB 3.0 xHCI Host Controller. Furthermore, the TI chip revision is indicated in the lower byte (02h).

PCI register offset: 08h

Register type:Read-only

Default value: 0C03 3002h

Table 4-8. PCI Register 06h

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	1
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0

Table 4-9. Class Code and Revision ID Register Description

Bit	Field Name	Access	Description
31:24	BASECLASS	r	Base Class. This field returns 0Ch when read, which classifies the function as a Serial Bus Controller.
23:16	SUBCLASS	r	Sub Class. This field returns 03h when read, which specifically classifies the function as a Universal Serial Bus Host Controller.
15:8	PGMIF	r	Programming Interface. This field returns 30h when read, which identifies the function as a USB 3.0 xHCI Host Controller.
7:0	CHIPREV	r	Silicon Revision. This field returns the silicon revision of the function. This field is 02h.

4.7 Cache Line Size Register

This 8-bit register is read/write for legacy compatibility purposes and is not applicable to the functionality of the TUSB73X0.

PCI register offset: 0Ch

Register type:Read/Write

Default value: 00h

Table 4-10. PCI Register 0Ch

Bit No.	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0

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4.8 Latency Timer Register

This read-only register has no meaningful context for a PCI Express device and returns zeros when read.

PCI register offset: 0Dh

Register type:Read-only

Default value: 00h

Table 4-11. PCI Register 0Dh

Bit No.	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0

4.9 Header Type Register

This read only register indicates that this function has a type 0 PCI header. Bit seven of this register is zero indicating that the TUSB73X0 is not a Multifunction device.

PCI register offset: 0Eh

Register type:Read-only

Default value: 00h

Table 4-12. PCI Register 0Eh

Bit No.	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0

4.10 BIST Register

Since the TUSB73X0 does not support a built-in self test (BIST), this read only register returns the value of 00h when read.

PCI register offset: 0Fh

Register type:Read-only

Default value: 00h

Table 4-13. PCI Register 0Fh

Bit No.	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0

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4.11 Base Address Register 0

This register is used to program the memory address used to access the device control registers.

PCI register offset: 10h

Register type:Read/Write,Read-only

Default value: 0000 0004h

Table 4-14. PCI Register 10h

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Table 4-15. Base Address Register 0 Description

Bit	Field Name	Access	Description
31:16	ADDRESS	rw	Memory Address. The lower 32 bits of the 64-bit memory address field for the TUSB73X0. The TUSB73X0 uses 16 read/write bits indicating that 64 kB of memory space is required.
15:4	RSVD	r	Reserved. These bits are read-only and return zeros when read.
3	PRE_FETCH	r	Pre-fetchable. This bit is read only 0 indicating that this memory window is not prefetchable.
2:1	MEM_TYPE	r	Memory Type. This field is read only 10b indicating that this window can be located anywhere in the 64-bit address space.
0	MEM_IND	r	Memory Space Indicator. This field returns 0 indicating that memory space is used.

4.12 Base Address Register 1

This register is used to program the memory address used to access the device control registers.

PCI register offset: 14h

Register type:Read/Write

Default value: 0000 0000h

Table 4-16. PCI Register 14h

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-17. Base Address Register 1 Description

Bit	Field Name	Access	Description
31:0	ADDRESS	rw	Memory Address. T his field indicates the upper 32 bits of the 64-bit memory address for the TUSB73X0.

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4.13 Base Address Register 2

This register is used to program the memory address used to access the MSI-X Table and PBA.

PCI register offset: 18h

Register type:Read/Write, Read-only

Default value: 0000 0004h

Table 4-18. PCI Register 18h

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Table 4-19. Base Address Register 2 Description

Bit	Field Name	Access	Description
31:20	ADDRESS	rw	Memory Address. The lower 32 bits of the 64-bit memory address field for the TUSB73X0 uses 19 read/write bits indicating that 8 MB of memory space is required.
19:4	RSVD	r	Reserved. These bits are read-only and returns zeros when read.
3	PRE_FETCH	r	Pre-fetchable. This bit is read only 0 indicating that this memory window is not prefetchable.
2:1	MEM_TYPE	r	Memory Type. This field is read only 10b indicating that this window can be located anywhere in the 64-bit address space.
0	MEM_IND	r	Memory Space Indicator. This field returns 0 indicating that memory space is used.

4.14 Base Address Register 3

This register is used to program the memory address used to access the MSI-X Table and PBA.

PCI register offset: 1Ch

Register type:Read/Write

Default value: 0000 0000h

Table 4-20. PCI Register 1Ch

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-21. Table 9-3 Base Address Register 3 Description

Bit	Field Name	Access	Description
31:0	ADDRESS	rw	Memory Address. This field indicates the upper 32 bits of the 64-bit memory address for the TUSB73X0.

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4.15 Subsystem Vendor ID Register

This register, which is used for system and option card identification purposes, may be required for certain operating systems. This read-only register is a direct reflection of the Subsystem Access register, which is read/write and is initialized through the EEPROM (if present) or can be written through the Subsystem Alias Register at PCI Offset D0h.

PCI register offset: 2Ch

Register type:Read-only

Default value: 0000h

Table 4-22. PCI Register 2Ch

Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

4.16 Subsystem ID Register

This register, which is used for system and option card identification purposes, may be required for certain operating systems. This read-only register is a direct reflection of the Subsystem Access register, which is read/write and is initialized through the EEPROM (if present) or can be written through the Subsystem Alias Register at PCI Offset D0h.

PCI register offset: 2Eh

Register type:Read-only

Default value: 0000h

Table 4-23. PCI Register 2Eh

Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

4.17 Capabilities Pointer Register

This read-only register provides a pointer into the PCI configuration header where the PCI power management block resides. Since the PCI power management registers begin at 40h, this register is hardwired to 40h.

PCI register offset: 34h

Register type:Read-only

Default value: 40h

Table 4-24. PCI Register 34h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	1	0	0	0	0	0	0

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4.18 Interrupt Line Register

This read/write register is programmed by the system and indicates to the software which interrupt line the TUSB73X0 has been assigned. The default value of this register is FFh, indicating that an interrupt line has not yet been assigned to the function

PCI register offset: 3Ch

Register type:Read-only

Default value: FFh

Table 4-25. PCI Register 3Ch

Bit No.	7	6	5	4	3	2	1	0
Reset State	1	1	1	1	1	1	1	1

4.19 Interrupt Pin Register

The Interrupt Pin register is read-only 01h indicating that the TUSB73X0 uses INTA.

PCI register offset: 3Dh

Register type:Read-only

Default value: 01h

Table 4-26. PCI Register 3Dh

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	1

4.20 Min Grant Register

This read-only register has no meaningful context for a PCI Express device and returns zeros when read.

PCI register offset: 3Eh

Register type:Read-only

Default value: 00h

Table 4-27. PCI Register 3Eh

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

4.21 Max Latency Register

This read-only register has no meaningful context for a PCI Express device and returns zeros when read.

PCI register offset: 3Fh

Register type:Read-only

Default value: 00h

Table 4-28. PCI Register 3Fh

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

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4.22 Capability ID Register

This read-only register identifies the linked list item as the register for PCI Power management. The register returns 01h when read.

PCI register offset: 40h

Register type:Read-only

Default value: 01h

Table 4-29. PCI Register 40h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	1

4.23 Next Item Pointer Register

The contents of this read-only register indicate the next item in the linked list of capabilities for the TUSB73X0. This register reads 48h pointing to the MSI Capability registers.

PCI register offset: 41h

Register type:Read-only

Default value: 48h

Table 4-30. PCI Register 41h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	1	0	0	1	0	0	0

4.24 Power Management Capabilities Register

The read-only register indicates the capabilities of the TUSB73X0 related to PCI power management.

PCI register offset: 42h

Register type:Read-only

Default value: xxx3h

Table 4-31. PCI Register 42h

Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	x	1	1	1	1	1	1	x	x	x	0	0	0	0	1	1

Table 4-32. Power Management Capabilities Register Description

Bit	Field Name	Access	Description
15:11	PME_SUPPORT	r	PME# support. This five-bit field indicates the power states from which the TUSB73X0 may assert PME#. If the AUX_DET pin is ‘1’, this field is ‘11111’. If the AUX_DET pin is ‘0’, this field is ‘01111’.
10	D2_SUPPORT	r	This bit returns a 1 when read, indicating that the function supports the D2 device power state.
9	D1_SUPPORT	r	This bit returns a 1 when read, indicating that the function supports the D1 device power state.
8:6	AUX_CURRENT	r	3.3 Vaux auxiliary current requirements. If the AUX_DET pin is ‘1’, this field is 010. IF the AUX_DET pin is ‘0’, this field is ‘000’.

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Table 4-32. Power Management Capabilities Register Description (continued)

5	DSI	r	Device Specific Initialization. This bit returns 0 when read, indicating that the TUSB73X0 does not require special initialization beyond the standard PCI configuration header before a generic class driver is able to use it.
4	RSVD	r	Reserved. Returns zero when read.
3	PME_CLK	r	PME# Clock.
2:0	PM_VERSION	r	Power Mgmt Version. This field returns 3'b011 indicating Rev 1.2 compatibility.

4.25 Power Management Control/Status Register

This register determines and changes the current power state of the TUSB73X0.

PCI register offset: 44h

Register type:Read/Write, Read-only

Default value: 0008h

Table 4-33. PCI Register 44h

Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Table 4-34. Power Management Control/Status Register Description

Bit	Field Name	Access	Description
15	PME_STAT	rc	PME# Status. This bit is sticky and is only reset by a Global Reset.
14:13	DATA_SCALE	r	Data Scale. This 2-bit field returns 0's when read since the TUSB73X0 does not use the Data Register.
12:9	DATA_SEL	r	Data Select. This 4-bit field returns 0's when read since the TUSB73X0 does not use the Data Register.
8	PME_EN	rw	PME# Enable. This bit is sticky and is only reset by a Global Reset.
7:4	RSVD	r	Reserved. Returns zero when read.
3	NO_SOFT_RESET	r	No Soft Reset. This bit returns '1' indicating that no internal reset is generated and the device retains its configuration context when transitioning from the D3hot state to the D0 state.
2	RSVD	r	Reserved. Returns zero when read.
1:0	PWR_STATE	rw	Power State. This 2-bit field is used both to determine the current power state of the function and to set the function into a new power state. This field is encoded as follows:00 = D001 = D110 = D211 = D3hot.

4.26 Power Management Bridge Support Extension Register

This read-only register is not applicable to the TUSB73X0 and returns 00h when read.

PCI register offset: 46h

Register type:Read-only

Default value: 00h

Table 4-35. PCI Register 46h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

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4.27 Power Management Data Register

This read-only register is not applicable to the TUSB73X0 and returns 00h when read.

PCI register offset: 47h

Register type:Read-only

Default value: 00h

Table 4-36. PCI Register 47h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

4.28 MSI Capability ID Register

This read-only register identifies the linked list item as the register for Message Signaled Interrupts Capabilities. The register returns 05h when read.

PCI register offset: 48h

Register type:Read-only

Default value: 05h

Table 4-37. PCI Register 48h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	1	0	1

4.29 Next Item Pointer Register

The contents of this read-only register indicate the next item in the linked list of capabilities for the TUSB73X0. This register reads 70h pointing to the PCI Express Capability registers.

PCI register offset: 49h

Register type:Read-only

Default value: 70h

Table 4-38. PCI Register 49h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	1	1	1	0	0	0	0

4.30 MSI Message Control Register

The register is used to control the sending of MSI messages.

PCI register offset: 4Ah

Register type:Read/Write, Read-only

Default value: 0086h

Table 4-39. PCI Register 4Ah

Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0

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Table 4-40. MSI Message Control Register Description

Bit	Field Name	Access	Description
15:8	RSVD	r	Reserved. Returns zeros when read.
8	PVM_CAP	r	Per-vector Masking Capable. This bit is read only 0 indicating that the TUSB73X0 does not support per-vector masking.
7	64CAP	r	64 Bit Message Capability. This bit is read only 1 indicating that the TUSB73X0 supports 64 bit MSI message addressing.
6:4	MM_EN	rw	Multiple Message Enable. This bit indicates the number of distinct messages that the TUSB73X0 is allowed to generate. 000 – 1 Message (All interrupters mapped to the same message) 001 – 2 Messages (Interrupters 0, 2, 4, and 6 mapped to message 0 and Interrupters 1, 3, 5, and 7 mapped to message 1) 010 – 4 Messages (Interrupters 0 and 4 mapped to message 0, Interrupters 1 and 5 mapped to message 1, Interrupters 2 and 6 mapped to message 2, Interrupters 3 and 7 mapped to message 3) 011 – 8 Messages (Interrupter # mapped to corresponding message #) 100 – 16 Messages (Interrupter # mapped to corresponding message #) 101 – 32 Messages (Interrupter # mapped to corresponding message #) 110 – Reserved111 – Reserved
3:1	MM_CAP	r	Multiple Message Capabilities. This field indicates the number of distinct messages that TUSB73X0 is capable of generating. This field is read only ‘011’ indicating that the TUSB73X0 can signal 8 distinct messages.
0	MSI_EN	rw	MSI Enable. This bit is used to enable MSI interrupt signaling. MSI signaling must be enabled by software for the TUSB73X0 to signal an MSI 0 – MSI signaling is prohibited 1 – MSI signaling is enabled

4.31 MSI Lower Message Address Register

This register contains the lower 32 bits of the address that a MSI message is written to when an interrupt is to be signaled.

PCI register offset: 4Ch

Register type:Read/Write

Default value: 0000 0000h

Table 4-41. PCI Register 4Ch

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-42. MSI Lower Message Address Register Description

Bit	Field Name	Access	Description
31:2	ADDRESS	rw	System Specified Message Address
1:0	RSVD	r	Reserved. Return zeros when read.

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4.32 MSI Upper Message Address Register

This register contains the upper 32 bits of the address that a MSI message is written to when an interrupt is to be signaled. If this register is 0000 0000h, 32-bit addressing is used; otherwise, 64-bit addressing is used.

PCI register offset: 50h

Register type:Read/Write

Default value: 0000 0000h

Table 4-43. PCI Register 4Ch

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

4.33 MSI Message Data Register

This 16-bit register contains the data that software programmed the device to send when it sends a MSI message.

PCI register offset: 54h

Register type:Read/Write

Default value: 0000h

Table 4-44. PCI Register 54h

Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-45. MSI Message Data Register Description

Bit	Field Name	Access	Description
15:4	MSG	rw	System Specific Message. This field contains the portion of the message that the TUSB73X0 can never modify.
3:0	MSG_NUM	rw	Message Number. This portion of the message field may be modified to contain the message number if multiple messages are enabled. The number of bits that are modifiable depends on the number of messages enabled in the Message Control Register. 1 Message – No message data bits can be modified 2 messages – Bit 0 can be modified 4 messages – Bits 0:1 can be modified 8 messages – Bits 0:2 can be modified 16 messages – Bits 0:3 can be modified 32 messages – Bits 0:4 can be modified

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4.34 Serial Bus Release Number Register (SBRN)

This read only register is set to 30h to indicate that the TUSB73X0 is compliant to release 3.0 of the Universal Serial Bus Specification.

PCI register offset: 60h

Register type:Read-only

Default value: 00h

Table 4-46. PCI Register 60h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	1	1	0	0	0	0

4.35 Frame Length Adjustment Register (FLADJ)

This register is used to adjust any offset from the clock source that generates the clock that drives the SOF counter. When a new value is written to this register, the length of the frame is adjusted for all USB buses implemented by the TUSB73X0. This register is only reset by a Global Reset.

PCI register offset: 61h

Register type:Read/Write

Default value: 20h

Table 4-47. PCI Register 61h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	1	0	0	0	0	0

Table 4-48. Frame Length Adjustment Register Description

Bit	Field Name	Access	Description
7:6	RSVD	r	Reserved. Return zeros when read.
5:0	FRAME_LENGTH *	rw	Frame Length Timing Value. Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time is equal to 59488 plus the value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000.

4.36 PCI Express Capability ID Register

This read-only register identifies the linked list item as the register for PCI Express Capabilities. The register returns 10h when read.

PCI register offset: 70h

Register type:Read-only

Default value: 10h

Table 4-49. PCI Register 70h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	1	0	0	0	0

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4.37 Next Item Pointer Register

The contents of this read-only register indicate the next item in the linked list of capabilities for the TUSB73X0. This register reads C0h pointing to the MSI-X Capability registers.

PCI register offset: 71h

Register type:Read-only

Default value: C0h

Table 4-50. PCI Register 71h

Bit No.	7	6	5	4	3	2	1	0
Reset State	1	1	0	0	0	0	0	0

4.38 PCI Express Capabilities Register

This register indicates the capabilities of the TUSB73X0 related to PCI Express.

PCI register offset: 72h

Register type:Read-only

Default value: 0002h

Table 4-51. PCI Register 72h

Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Table 4-52. PCI Express Capabilities Register Description

Bit	Field Name	Access	Description
15:14	RSVD	r	Reserved. Returns zeros when read.
13:9	INT_NUM	r	Interrupt Message Number. This field is used for MSI and MSI-X support.
8	SLOT	r	Slot Implemented. This bit is not valid for the TUSB73X0 and is read only zero.
7:4	DEV_TYPE	r	Device/Port Type. This read only field returns 0000b indicating that the device is a PCI Express Endpoint.
3:0	VERSION	r	Capability Version. This field returns 0010b indicating revision two of the PCI Express capability.

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4.39 Device Capabilities Register

The Device Capabilities Register indicates the device specific capabilities of the TUSB73X0.

PCI register offset: 74h

Register type:Read-only, Hardware Update

Default value: 0000 8FC3h

Table 4-53. PCI Register 74h

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	1	0	0	0	1	1	1	1	1	1	0	0	0	0	1	1

Table 4-54. Device Capabilities Register Description

Bit	Field Name	Access	Description
31:29	RSVD	r	Reserved. Return zeros when read.
28	FLR	r	Function Level Reset. This bit is set to 0 since the TUSB73X0 has only one function.
27:26	CSPLS	ru	Captured Slot Power Limit Scale. The value in this register is programmed by the host by issuing a Set_Slot_Power_Limit Message. When a Set_Slot_Power_Limit Message is received bits 9:8 are written to this field. The value in this register specifies the scale used for the Slot Power Limit. 00 – 1.0x 01 – 0.1x 10 – 0.01x 11 – 0.001x
25:18	CSPLV	ru	Captured Slot power Limit Value. The value in this register is programmed by the host by issuing a Set_Slot_Power_Limit Message. When a Set_Slot_Power_Limit Message is received bits 7:0 are written to this field. The value in this register in combination with the Slot power Limit Scale value, specifies the upper limit of power supplied to the slot. The power limit is calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field.
17:16	RSVD	r	Reserved. Return zeros when read.
15	RBER	r	Role Based Error Reporting. This bit is hardwired to 1 indicating that the TUSB73X0 supports Role Based Error Reporting
14:12	RSVD	r	Reserved. Return zeros when read.
11:9	EP_L1_LAT	r	Endpoint L1 Acceptable Latency. This field indicates the acceptable latency for a transition from L1 to L0 State. This field can be programmed by writing to the L1_LATENCY field in the General Control Register 2. The default value for this register is the latency for the PHY to exit the L1 state. This field cannot be programmed to be less than the latency for the PHY to exit the L1 state.
8:6	EP_L0S_LAT	r	Endpoint L0s Acceptable Latency. This field indicates the acceptable latency for a transition from L0s to L0 State. This field can be programmed by writing to the L0s_LATENCY field in the General Control Register 2. The default value for this register is the latency for the PHY to exit the L0s state. This field cannot be programmed to be less than the latency for the PHY to exit the L0s state.
5	ETFS	r	Extended Tag Field Supported. This field indicates the size of the tag field and is encoded as 0.
4:3	PFS	r	Phantom Functions Supported. This field is read only 00b indicating that function numbers are not used for phantom functions.

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Table 4-54. Device Capabilities Register Description (continued)

2:0	MPSS	r	Max Payload Size Supported. This field indicates the maximum payload size that the device can support for TLPs. This field is encoded as 011b indicating the Max Payload size for a TLP is 1 Kbyte.

4.40 Device Control Register

The Device Control Register controls PCI Express device specific parameters.

PCI register offset: 78h

Register type:Read/Write

Default value: 2810h

Table 4-55. PCI Register 78h

Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	1	0	1	0	0	0	0	0	0	1	0	0	0	0

Table 4-56. Device Control Register Description

Bit	Field Name	Access	Description
15	INITIATE_FLR	rw	Initiate Function Level Reset. A write of 1b initiates Function Level Reset to the Function. The value read by software from this bit is always 0b.
14:12	MRRS	rw	Max Read Request Size. This field is programmed by host software to set the maximum size of a read request that the TUSB73X0 can generate. This field is encoded as: 000 – 128B 001 – 256B 010 – 512B (default) 011 – 1024B 100 – 2048B101 – 4096B 110 – Reserved 111 – Reserved
11	ENS	rw	Enable No Snoop. Controls the setting of the “No Snoop” flag within the TLP header for upstream memory transactions mapped to any traffic class mapped to a virtual channel other than VC0 through the Upstream Decode Windows. 0 – No snoop field is ‘0’ 1 – No snoop field is ‘1’ (default)
10	APPE	rw	Auxiliary Power PM Enable. This bit is only reset by a Global Reset.
9	PFE	r	Phantom Function Enable. Since the TUSB73X0 does not support phantom functions this bit is read only zero.
8	ETFE	rw	Extended Tag Field Enable.
7:5	MPS	rw	Max Payload Size.
4	ERO	rw	Enable Relaxed Ordering.
3	URRE	rw	Unsupported Request Reporting Enable.
2	FERE	rw	Fatal Error Reporting Enable.
1	NFERE	rw	Non-Fatal Error Reporting Enable.
0	CERE	rw	Correctable Error Reporting Enable.

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4.41 Device Status Register

The Device Status Register controls PCI Express device specific parameters.

PCI register offset: 7Ah

Register type:Read Only, Clear by a Write of One, Hardware Update

Default value: 00x0h

Table 4-57. PCI Register 7Ah

Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	x	0	0	0	0

Table 4-58. Device Status Register Description

Bit	Field Name	Access	Description
15:6	RSVD	r	Reserved. Return zeros when read.
5	PEND	ru	Transaction Pending.
4	APD	ru	AUX Power Detected. This bit indicates that AUX power is present. 0 – No AUX power detected. (AUX_DET pin is ‘0’) 1 – AUX power detected. (AUX_DET pin is ‘1’) This bit is set based upon the state of the AUX_DET pin.
3	URD	rcu	Unsupported Request Detected.
2	FED	rcu	Fatal Error Detected.
1	NFED	rcu	Non-Fatal Error Detected.
0	CED	rcu	Correctable Error Detected.

4.42 Link Capabilities Register

The Link Capabilities Register indicates the link specific capabilities of the TUSB73X0.

PCI register offset: 7Ch

Register type:Read-only

Default value: 0007 xC12h

Table 4-59. PCI Register 7Ch

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	x	x	1	1	1	0	0	0	0	0	1	0	0	1	0

Table 4-60. Link Capabilities Register Description

Bit	Field Name	Access	Description
31:24	PORT_NUM	r	Port Number. This field indicates port number for the PCI Express link. This field is read only 00h indicating that the Link is associated with port zero.
23:19	RSVD	r	Reserved. Returns zeros when read.

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Table 4-60. Link Capabilities Register Description (continued)

18	CLK_PM	r	Clock Power Management. This bit is hardwired to 1 to indicate that the TUSB73X0 supports Clock Power Management through the CLKREQ# protocol.
17:15	L1_LATENCY	r	L1 Exit Latency. This field indicates the time that it takes to transition from the L1 state to the L0 state. The value reported by this field is determined by either the L1_EXIT_LAT_ASYNC field or the L1_EXIT_LAT_COMMON field in the General Control Register 0.
14:12	L0S_LATENCY	r	L0s Exit Latency. This field indicates the time that it takes to transition from the L0s state to the L0 state. The value reported by this field is determined by either the L0s_EXIT_LAT_ASYNC field or the L0s_EXIT_LAT_COMMON field in the General Control Register 0.
11:10	ASLPMS	r	Active State Link PM Support. This field indicates the level of active state power management that the TUSB73X0 supports. The value 11b indicates support for both L0s and L1 through active state power management.
9:4	MLW	r	Maximum Link Width. This field is encoded 000001b to indicate that the TUSB73X0 only supports a 1x PCI Express link.
3:0	MLS	r	Maximum Link Speed. This field is encoded 0010b to indicate that the TUSB73X0 supports link speeds of 5 Gb/s and 2.5 Gb/s.

4.43 Link Control Register

The Link Control Register indicates is used to control link specific behavior.

PCI register offset: 80h

Register type:Read-only, Read/Write

Default value: 0000h

Table 4-61. PCI Register 80h

Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-62. Link Control Register Description

Bit	Field Name	Access	Description
15:9	RSVD	r	Reserved. Returns zeros when read.
8	EN_CPM	rw	Enable Clock Power Management.
7	ES	rw	Extended Synch.
6	CCC	rw	Common Clock Configuration. This bit is set when a common clock is provided to both ends of the PCI Express link. This bit is also used to select the L0s exit latency and L1 exit latency. 0 – Reference clock is asynchronous (L0s exit latency and L1 exit latency based on the L0s_EXIT_LAT_ASYNC and L1_EXIT_LAT_ASYNC fields in the General Control Register 0) 1 – Reference clock is synchronous (L0s exit latency and L1 exit latency based on the L0s_EXIT_LAT_COMMON and L1_EXIT_LAT_COMMON fields in the General Control Register 0)
5	RL	r	Retrain Link. This bit has no function and is read only zero.
4	LD	r	Link Disable. This bit has no function and is read only zero.
3	RCB	rw	Read Completion Boundary.
2	RSVD	r	Reserved. Returns zero when read.

Table 4-62. Link Control Register Description (continued)

1:0	ASLPMC	rw	Active State Link PM Control. This field is used to enable and disable active state PM. 00 – Active State PM Disabled 01 – L0s Entry Enabled 10 – L1 Entry Enabled 11 – L0s and L1 Entry Enable

4.44 Link Status Register

The Link Status Register indicates current state of the PCI Express Link.

PCI register offset: 82h

Register type:Read-only

Default value: 101xh

Table 4-63. PCI Register 82h

Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	1	0	0	0	0	0	0	0	1	0	0	x	x

Table 4-64. Link Status Register Description

Bit	Field Name	Access	Description
15	LINK_ABS	r	Link Autonomous Bandwidth Status. This bit has no function and is read only zero.
14	LINK_BMS	r	Link Bandwidth Management Status. This bit has no function and is read only zero.
13	DLL_ACTIVE	r	Data Link Layer Active. This bit has no function and is read only zero.
12	SCC	r	Slot Clock Configuration. This bit is ‘1’, since the TUSB73X0 uses the 100-MHz differential reference clock provided by the platform.
11	LT	r	Link Training. This bit has no function and is read only zero.
10	TE	r	Retrain Link. This bit has no function and is read only zero.
9:4	NLW	r	Negotiated Link Width. This field is read only 000001b indicating the lane width is 1x.
3:0	LS	r	Link Speed. This field indicates the negotiated link speed.

4.45 Device Capabilities 2 Register

The Device Capabilities 2 Register indicates the device specific capabilities of the TUSB73X0.

PCI register offset: 94h

Register type:Read-only

Default value: 0000 0010h

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Table 4-65. PCI Register 94h

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Table 4-66. Device Capabilities 2 Register Description

Bit	Field Name	Access	Description
31:5	RSVD	r	Reserved. Returns zeros when read.
4	CPLT_TO_DIS_SUP	r	Completion Timeout Disable Supported. This bit is read only 1b indicating that the completion timeout disable mechanism is supported.
3:0	CPLT_TO_RANGES	r	Completion Timeout Ranges Supported. This field is read only 0000b indicating that completion timeout programming is not supported.

4.46 Device Control 2 Register

The Device Control 2 Register controls PCI Express device specific parameters.

PCI register offset: 98h

Register type:Read-only, Read/Write

Default value: 0800h

Table 4-67. PCI Register 98h

Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Table 4-68. Device Control 2 Register Description

Bit	Field Name	Access	Description
15:5	RSVD	r	Reserved. Returns zeros when read.
4	CPTL_TO_DIS	rw	Completion Timeout Disable.
3:0	CPLT_TO_VALUE	r	Completion Timeout Value. This field is read only 0000b indicating that completion timeout programming is not supported.

4.47 Link Control 2 Register

The Link Control 2 Register indicates is used to control link specific behavior.

PCI register offset: A0h

Register type:Read-only, Read/Write

Default value: 0000h

Table 4-69. PCI Register A0h

Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

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Table 4-70. Link Control 2 Register Description

Bit	Field Name	Access	Description
15:13	RSVD	r	Reserved. Returns zeros when read.
12	COMPLIANCE_DEEMPH*	rw	Compliance De-Emphasis. This bit is sticky and is only reset by a Global Reset.
11	COMPLIANCE_SOS*	rw	Compliance SOS. This bit is sticky and is only reset by a Global Reset.
10	ENT_MOD_COMPLIANCE*	rw	Enter Modified Compliance. This bit is sticky and is only reset by a Global Reset.
9:7	TRANSMIT_MARGIN*	rw	Transmit Margin. This bit is sticky and is only reset by a Global Reset.
6	SEL_DEEMPH	r	Selectable De-Emphasis. This bit has no function and is read only zero.
5	HW_AUTO_SPEED_DIS	r	Hardware Autonomous Speed Disable. This bit is read only zero since this function is not supported.
4	ENTER_COMPL*	rw	Enter Compliance. This bit is sticky and is only reset by a Global Reset.
3:0	TGT_LINK_SPEED*	rw	Target Link Speed. This bit is sticky and is only reset by a Global Reset.

4.48 Link Status 2 Register

The Link Status 2 Register indicates current state of the PCI Express Link.

PCI register offset: A2h

Register type:Read-only

Default value: 000xh

Table 4-71. PCI Register A2h

Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x

Table 4-72. Link Status 2 Register Description

Bit	Field Name	Access	Description
15:1	RSVD	r	Reserved. Returns zeros when read.
0	DEEMPH_LEVEL	r	Current De-Emphasis Level.

4.49 Serial Bus Data Register

The Serial Bus Data register is used to read and write data on the serial bus interface. When writing data to the serial bus, this register must be written before writing to the Serial Bus Address register to initiate the cycle. When reading data from the serial bus, this register will contain the data read after the REQBUSY (bit 5 Serial Bus Control Register) bit is cleared. This register is reset by a PCI Express reset (PERST#), a GRST#, or the internally-generated power-on reset.

PCI register offset: B0h

Register type:Read/Write

Default value: 00h

Table 4-73. PCI Register B0h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

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4.50 Serial Bus Index Register

The value written to the Serial Bus Index register represents the byte address of the byte being read or written from the serial bus device. The Serial Bus Index register must be written before the before initiating a serial bus cycle by writing to the Serial Bus Slave Address register. This register is reset by a PCI Express reset (PERST#), a GRST#, or the internally-generated power-on reset.

PCI register offset: B1h

Register type:Read/Write

Default value: 00h

Table 4-74. PCI Register B1h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

4.51 Serial Bus Slave Address Regsiter

The Serial Bus Slave Address register is used to indicate the address of the device being targeted by the serial bus cycle. This register also indicates if the cycle will be a read or a write cycle. Writing to this register initiates the cycle on the serial interface. This register is reset by a PCI Express reset (PERST#), a GRST#, or the internally-generated power-on reset.

PCI register offset: B2h

Register type:Read/Write

Default value: 00h

Table 4-75. PCI Register B2h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

Table 4-76. Serial Bus Slave Address Register Description(1)

Bit	Field Name	Access	Description
7:1†	SLAVE_ADDR†	rw	Serial Bus Slave Address. This bit field represents the slave address of a read or write transaction on the serial interface.
0†	RW_CMD†	rw	Read/Write Command. This bit is used to determine if the serial bus cycle will be a read or a write cycle. 0 – A single byte write is requested. 1 – A single byte read is requested.

(1) Bits marked with † are reset by a PCI Express reset (PERST#), a GRST#, or the internally-generated power-on reset.

4.52 Serial Bus Control and Status Register

The Serial Bus Control and Status register is used to control the behavior of the Serial bus interface. This register also provides status information about the state of the serial bus. This register is reset by a PCI Express reset (PERST#), a GRST#, or the internally-generated power-on reset.

PCI register offset: B3h

Register type:Read/Write, Read-Only, Read/Clear

Default value: 00h

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Table 4-77. PCI Register B3h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

Table 4-78. Serial Bus Control and Status Register Description(1)

Bit	Field Name	Access	Description
7†	PROT_SEL†	rw	Protocol Select. This bit is used to select the serial bus address mode used. 0 – Slave Address and Byte Address are sent on the serial bus. 1 – Only the Slave address is sent on the serial bus.
6	RSVD	r	Reserved. Returns zero when read.
5†	REQBUSY†	r	Requested Serial Bus Access Busy. This bit is set when a serial bus cycle is in progress. 0 – No serial bus cycle 1 – Serial bus cycle in progress
4†	ROMBUSY†	r	Serial EEPROM Access Busy. This bit is set when the serial EEPROM circuitry in the TUSB73X0 is downloading register defaults from a serial EEPROM. 0 – No EEPROM activity 1 – EEPROM download in progress
3†	SBDETECT†	rwu	Serial EEPROM Detected. This bit is automatically set when a serial EEPROM is detected by the TUSB73X0. The value of this bit is used to enable the serial bus interface and to control whether or not the EEPROM load takes place. Note that a serial EEPROM is only detected once following a PERST# or a GRST#. 0 – No EEPROM present, EEPROM load process does not happen 1 – EEPROM present, EEPROM load process takes place Note that even if a serial EERPOM is not detected following PERST# or a GRST#, software can still set this bit to enable the serial bus interface. In this situation, the EEPROM load process will not happen.
2†	SBTEST†	rw	Serial Bus Test. This bit is used for internal test purposes. This bit controls the clock source for the serial interface clock. 0 – Serial bus clock at normal operating frequency ~ 100 kHz 1 – Serial bus clock frequency increased for test purposes
1†	SB_ERR†	rc	Serial Bus Error. This bit is set when an error occurs during a software initiated serial bus cycle. 0 – No error 1 – Serial bus error
0†	ROM_ERR†	rc	Serial EEPROM Load Error. This bit is set when an error occurs while downloading registers from a serial EEPROM. 0 – No Error 1 – EEPROM load error

(1) Bits marked with † are reset by a PCI Express reset (PERST#), a GRST#, or the internally-generated power-on reset.

4.53 GPIO Control Register

This register is used to control the direction of the eight GPIO pins. This register is reset by a PCI Express reset (PERST#), a GRST#, or the internally-generated power-on reset.

PCI register offset: B4h

Register type:Read/Write, Read-Only

Default value: 0000h

Table 4-79. PCI Register B4h

Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Table 4-80. GPIO Control Register Description(1)

Bit	Field Name	Access	Description
15:4	RSVD	r	Reserved. Returns zero when read.
3†	GPIO3_DIR†	rw	GPIO 3 Data Direction. This bit selects whether GPIO3 is in input or output mode. 0 – Input 1 – Output
2†	GPIO2_DIR†	rw	GPIO 2 Data Direction. This bit selects whether GPIO2 is in input or output mode. 0 – Input 1 – Output
1†	GPIO1_DIR†	rw	GPIO 1 Data Direction. This bit selects whether GPIO1 is in input or output mode. 0 – Input 1 – Output
0†	GPIO0_DIR†	rw	GPIO 0 Data Direction. This bit selects whether GPIO0 is in input or output mode. 0 – Input 1 – Output

(1) Bits marked with † are reset by a PCI Express reset (PERST#), a GRST#, or the internally-generated power-on reset.

4.54 GPIO Data Register

This register is used to read the state of the GPIO pins and to change the state of GPIO pins that are in output mode. Writing to a bit that is in input mode will be ignored. The default value at power up depends on the state of the GPIO terminals as they default to general purpose inputs. This register is reset by a PCI Express reset (PERST#), a GRST#, or the internally-generated power-on reset.

PCI register offset: B6h

Register type:Read/Write, Read-Only

Default value: 0000h

Table 4-81. PCI Register B6h

Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	x	x	x	x

Table 4-82. GPIO Data Register Description(1)

Bit	Field Name	Access	Description
15:4	RSVD	r	Reserved. Returns zero when read.
3†	GPIO3_DATA†	rw	GPIO 3 Data. This bit is used to read the state of GPIO3 or change the state of GPIO3 in output mode.
2†	GPIO2_DATA†	rw	GPIO 2 Data. This bit is used to read the state of GPIO2 or change the state of GPIO2 in output mode.
1†	GPIO1_DATA†	rw	GPIO 1 Data. This bit is used to read the state of GPIO1 or change the state of GPIO1 in output mode.
0†	GPIO0_DATA†	rw	GPIO 0 Data. This bit is used to read the state of GPIO0 or change the state of GPIO0 in output mode.

(1) Bits marked with † are reset by a PCI Express reset (PERST#), a GRST#, or the internally-generated power-on reset.

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4.55 MSI-X Capability ID Register

This read-only register identifies the linked list item as the register for MSI-X Capabilities. The register returns 11h when read.

PCI register offset: C0h

Register type:Read-Only

Default value: 11h

Table 4-83. PCI Register C0h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	1	0	0	0	1

4.56 Next Item Pointer Register

The contents of this read-only register indicate the next item in the linked list of capabilities for the TUSB73X0. This register reads 00h indicating that no additional capabilities are supported.

PCI register offset: C1h

Register type:Read-Only

Default value: 11h

Table 4-84. PCI Register C1h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

4.57 MSI-X Message Control Register

This register is used to control the sending of MSI-X messages.

PCI register offset: C2h

Register type:Read-Only, Read/Write

Default value: 0007h

Table 4-85. PCI Register C2h

Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Table 4-86. MSI-X Message Control Register Description

Bit	Field Name	Access	Description
15	MSIX_EN	rw	MSI-X Enable.
14	FUNC_MASK	rw	Function Mask.
13:11	RSVD	r	Reserved. Returns zero when read.
10:0	TABLE_SIZE	r	MSI-X Table Size. This field is set to 07h to indicate a table size of 8 entries.

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4.58 MSI-X Table Offset and BIR Register

This register indicates into which BAR and offset the MSI-X table is mapped.

PCI register offset: C4h

Register type:Read-Only

Default value: 0000 0002h

Table 4-87. PCI Register C4h

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Table 4-88. MSI-X Table Offset and BIR Register Description

Bit	Field Name	Access	Description
31:3	TABLE_OFFSET	r	Table Offset. This field is set to 000h to indicate that the MSI-X Table is at an offset of 0000h from the beginning of the BAR at offset 18h.
2:0	TABLE_BIR	r	Table BIR. This field is set to 010b to indicate that the MSI-X table is mapped into the BAR at offset 18h.

4.59 MSI-X PBA Offset and BIR Register

This register indicates into which BAR and offset the MSI-X PBA is mapped.

PCI register offset: C8h

Register type:Read-Only

Default value: 0000 1000h

Table 4-89. PCI Register C8h

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-90. MSI-X PBA Offset and BIR Register Descriptions

Bit	Field Name	Access	Description
31:3	PBA_OFFSET	r	PBA Offset. This field is set to 200h to indicate that the MSI-X PBA is at an offset of 1000h from the beginning of the BAR at offset 18h.
2:0	PBA_BIR	r	PBA BIR. This field is set to 010b to indicate that the MSI-X PBA is mapped into the BAR at offset 18h.

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4.60 Subsystem Access Register

This register is a read/write register and the contents of this register are aliased to the Subsystem Vendor ID and Subsystem ID Registers at PCI Offsets 2Ch and 2Eh. This register is reset by a PCI Express reset (PERST#), a GRST#, or the internally-generated power-on reset.

PCI register offset: D0h

Register type:Read/Write

Default value: 0000 0000h

Table 4-91. PCI Register D0h

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-92. Subsystem Access Register Description

Bit	Field Name	Access	Description
31:16†	SubsystemID†	rw	Subsystem ID. The value written to this field is aliased to the Subsystem ID Register at PCI Offset 2Eh.
15:0†	SubsystemVendorID†	rw	Subsystem Vendor ID. The value written to this field is aliased to the Subsystem Vendor ID Register at PCI Offset 2Ch.

4.61 General Control 0 Register

This register is a read/write register is used to control various functions of the TUSB73X0. This register is reset by a PCI Express reset (PERST#), a GRST#, or the internally-generated power-on reset.

PCI register offset: D4h

Register type:Read/Write

Default value: 0000 0D9Bh

Table 4-93. PCI Register D4h

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	1	1	0	1	1	0	0	1	1	0	1	1

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Table 4-94. General Control 0 Register Description

Bit	Field Name	Access	Description
31:12	RSVD	r	Reserved. Returns zeros when read.
11:9†	L1_EXIT_LAT_ASYNC†	rw	L1 Exit Latency for Asynchronous Clock. This value in this field is the value reported in the L1_LATENCY field in the Link Capabilities Register when the CCC bit in the Link Control Register is '0'. This field defaults to 110b.
8:6†	L1_EXIT_LAT_COMMON†	rw	L1 Exit Latency for Common Clock. This value in this field is the value reported in the L1_LATENCY field in the Link Capabilities Register when the CCC bit in the Link Control Register is '1'. This field defaults to 110b.
5:3†	L0s_EXIT_LAT_ASYNC†	rw	L0s Exit Latency for Asynchronous Clock. This value in this field is the value reported in the L0s_LATENCY field in the Link Capabilities Register when the CCC bit in the Link Control Register is '0'. This field defaults to 011b.
2:0†	L0s_EXIT_LAT_COMMON†	rw	L0s Exit Latency for Common Clock. This value in this field is the value reported in the L0s_LATENCY field in the Link Capabilities Register when the CCC bit in the Link Control Register is '1'. This field defaults to 011b.

4.62 General Control 1 Register

This register is a read/write register is used to control various functions of the TUSB73X0. This register is reset by a PCI Express reset (PERST#), a GRST#, or the internally-generated power-on reset.

PCI register offset: D8h

Register type:Read-Only,Read/Write

Default value: 0000 001Bh

Table 4-95. PCI Register D8h

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1

Table 4-96. General Control 1 Register Description

Bit	Field Name	Access	Description
31:6	RSVD	r	Reserved. Returns zeros when read.
5:3†	L1ASPM_ENTRY_TIMER†	rw	L1ASPM Entry Timer. This field specifies the value of the L1ASPM Entry Timer. This field defaults to '011', corresponding to a value of 8 µs.
2:0†	L0s_ENTRY_TIMER†	rw	L0s Entry timer. This field specifies the value of the L0s Entry timer. This field defaults to '011', corresponding to a value of 4 µs.

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4.63 General Control 2 Register

This register is a read/write register is used to control various functions of the TUSB73X0. This register is reset by a PCI Express reset (PERST#), a GRST#, or the internally-generated power-on reset.

Note: For Pass 1.0 of the TUSB73X0 design, this register is read only zeros and has no effect.

PCI register offset: DCh

Register type:Read-Only,Read/Write

Default value: 0000 001Bh

Table 4-97. PCI Register DCh

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1

Table 4-98. General Control 2 Register Description

Bit	Field Name	Access	Description
31:6	RSVD	r	Reserved. Returns zeros when read.
5:3†	L1_LATENCY†	rw	L1 Maximum Exit Latency. This field is used to program the maximum acceptable latency when exiting the L1 state. This is used to set the L1 Acceptable Latency field in the Device capabilities register. 000 – Less than 1µs 001 – 1 µs up to less than 2 µs 010 – 2 µs up to less than 4 µs 011 – 4 µs up to less than 8 µs (default) 100 – 8 µs up to less than 16 µs 101 – 16 µs up to less than 32 µs 110 – 32 µs to 64 µs 111 – more than 64 µs
2:0†	L0s_LATENCY†	rw	L0s Maximum Exit Latency. This field is used to program the maximum acceptable latency when exiting the L0s state. This is used to set the L0s Acceptable Latency field in the Device capabilities register. 000 – Less than 64 ns 001 – 64 ns up to less than 128 ns 010 – 128 ns up to less than 256 ns 011 – 256 ns up to less than 512 ns (default) 100 – 512 ns up to less than 1 µs 101 – 1 µs up to less than 2 µs 110 – 2 µs to 4 µs 111 – more than 4 µs

4.64 USB Control Register

This register is a read/write register is used to control USB settings in the TUSB73X0. This register is reset by a PCI Express reset (PERST#), a GRST#, or the internally-generated power-on reset.

PCI register offset: E0h

Register type:Read/Write

Default value: 0000 0000h

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Table 4-99. PCI Register E0h

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-100. USB Control Register Description(1)(2)

Bit	Field Name	Access	Description
31†	USB_SPREAD_DIS†	rw	USB Spread Spectrum Disable. When this bit is set to '1', spread spectrum generation for the USB 3.0 clock is disabled.
30*	FREQ_SEL_EN*	rw	Frequency Select Enable. When this bit is set to 1, the oscillator is restarted with the PLL multiplier value and the oscillator frequency controls set according to the value specified in the PLL_FREQ_SEL field. This bit can only be written to once after power up.
29:24*	PLL_FREQ_SEL*	rw	PLL Frequency Select. If the FREQSEL pin is '1', then the value in this field controls the Frequency Select inputs to the PLL. In addition, the frequency selector inputs to the Oscillator are set appropriately for the frequency selected. If the FREQSEL pin is '0', then this field has no effect. Once the FREQ_SEL_EN bit has been set, this field will be locked and cannot be changed. 000110 – 20 MHz 000111 – 21 MHz 001000 – 22 MHz 001001 – 23 MHz 001010 – 24 MHz 001011 – 25 MHz 001100 – 26 MHz 001101 – 27 MHz 001110 – 28 MHz 001111 – 29 MHz 010000 – 30 MHz 010001 – 31 MHz 010010 – 32 MHz 010011 – 33 MHz 010100 – 34 MHz 010101 – 35 MHz 010110 – 36 MHz 010111 – 37 MHz 011000 – 38 MHz 011001 – 38.4 MHz 011010 – 39 MHz 011011 – 40 MHz 011100 – 41 MHz 011101 – 42 MHz 011110 – 43 MHz 011111 – 44 MHz 100000 – 45 MHz 100001 – 46 MHz 100010 – 47 MHz 100011 – 48 MHz 100100 – 49 MHz 100101 – 50 MHz All other values are reserved.
23†	HIDE_MSIX†	rw	Hide MSI-X. When this bit is set, the Next Item Pointer Register (offset 71h) for the PCI Express Capability is set to 00h, and BAR2 (offset 18h) and BAR3 (offset 1Ch) are only zeros.
22*	PWRON_POLARITY*	rw	PWRONx Polarity. When this bit is '0' (default), the PWRONx# pins are active low and their internal pull-down resistors are enabled. When this bit is '1', the PWRONx# pins are active high and their internal pull-down resistors are disabled.
21:17	RSVD	r	Reserved. Returns zero when read.
16†	PPC_NOT_PRESENT†	rw	Port Power Control Not Present. When this bit is '0', the TUSB73X0 forces the PPC bit to '1' in the Host Controller Capability Parameters, indicating that the system supports port power switches. When this bit is set to '1', the TUSB73X0 forces the PPC bit to '0' in the Host Controller Capability Parameters, indicating that the system does not support port power switches.
15:12†	RSVD†	rw	Reserved. Returns zeros when read.
11†	PORT4_DIS†	rw	USB Port 4 Disable. When this bit is set to '1', port 4 of the TUSB73X0 is disabled. For the TUSB7320 Port 4 is not present and this bit has no effect.

(1) Bits marked with † are reset by a PCI Express reset (PERST#), a GRST#, or the internally-generated power-on reset
(2) Bits marked with * are reset by a GRST#

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Table 4-100. USB Control Register Description[(1)(2)] (continued)

Bit	Field Name	Access	Description
10†	PORT3_DIS†	rw	USB Port 3 Disable. When this bit is set to '1', port 3 of the TUSB73X0 is disabled. For the TUSB7320 Port 3 is not present and this bit has no effect.
9†	PORT2_DIS†	rw	USB Port 2 Disable. When this bit is set to '1', port 2 of the TUSB73X0 is disabled.
8†	PORT1_DIS†	rw	USB Port 1 Disable. When this bit is set to '1', port 1 of the TUSB73X0 is disabled.
7†	USB3_PORT4_NON_REM†	rw	USB 3.0 Port 4 Non-Removable. When this bit is set to '1', the TUSB73X0 forces the DR bit to '1' in the Port Status and Control Register corresponding to USB 3.0 Port 4. For the TUSB7320 Port 4 is not present and this bit has no effect.
6†	USB3_PORT3_NON_REM†	rw	USB 3.0 Port 3 Non-Removable. When this bit is set to '1', the TUSB73X0 forces the DR bit to '1' in the Port Status and Control Register corresponding to USB 3.0 Port 3. For the TUSB7320 Port 3 is not present and this bit has no effect.
5†	USB3_PORT2_NON_REM†	rw	USB 3.0 Port 2 Non-Removable. When this bit is set to '1', the TUSB73X0 forces the DR bit to '1' in the Port Status and Control Register corresponding to USB 3.0 Port 2.
4†	USB3_PORT1_NON_REM†	rw	USB 3.0 Port 1 Non-Removable. When this bit is set to '1', the TUSB73X0 forces the DR bit to '1' in the Port Status and Control Register corresponding to USB 3.0 Port 1.
3†	USB2_PORT4_NON_REM†	rw	USB 2.0 Port 4 Non-Removable. When this bit is set to '1', the TUSB73X0 forces the DR bit to '1' in the Port Status and Control Register corresponding to USB 2.0 Port 4. For the TUSB7320 Port 4 is not present and this bit has no effect.
2†	USB2_PORT3_NON_REM†	rw	USB 2.0 Port 3 Non-Removable. When this bit is set to '1', the TUSB73X0 forces the DR bit to '1' in the Port Status and Control Register corresponding to USB 2.0 Port 3. For the TUSB7320 Port 3 is not present and this bit has no effect.
1†	USB2_PORT2_NON_REM†	rw	USB 2.0 Port 2 Non-Removable. When this bit is set to '1', the TUSB73X0 forces the DR bit to '1' in the Port Status and Control Register corresponding to USB 2.0 Port 2.
0†	USB2_PORT1_NON_REM†	rw	USB 2.0 Port 1 Non-Removable. When this bit is set to '1', the TUSB73X0 forces the DR bit to '1' in the Port Status and Control Register corresponding to USB 2.0 Port 1.

4.65 De-Emphasis and Swing Control Register

This register is used to control the de-emphasis and transmit swing settings for each of the USB 3.0 ports when the default setting is overridden through the Custom PHY Transmit/Receive Control Register. This register is reset by a PCI Express reset (PERST#), a GRST#, or the internally-generated power-on reset.

PCI register offset: E4h

Register type:Read/Write

Default value: 0000 0000h

Table 4-101. PCI Register E4h

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Table 4-102. De-Emphasis and Swing Control Register Description(1)

Bit	Field Name	Access	Description
31:28†	PORT4_SWING†	rw	Port 4 Swing. When the PORT4_SWING_OV bit is set to '1', these bits are used to set the output swing for port 4. For details on the behavior of the swing signals refer to Table 8-1. For the TUSB7320 Port 4 is not present and these bits have no effect.
27:24†	PORT4_DE†	rw	Port 4 Deemphasis. When the PORT4_DE_OV bit is set to '1', these bits are used to set the de-emphasis value for port 4. For details on the behavior of the swing signals refer to Table 8-2. For the TUSB7320 Port 4 is not present and these bits have no effect.
23:20†	PORT3_SWING†	rw	Port 3 Swing. When the PORT3_SWING_OV bit is set to '1' these bits are used to set the output swing for port 3. For details on the behavior of the swing signals refer to Table 8-1. For the TUSB7320 Port 3 is not present and these bits have no effect.
19:16†	PORT3_DE†	rw	Port 3 Deemphasis. When the PORT3_DE_OV bit is set to '1' these bits are used to set the de-emphasis value for port 3. For details on the behavior of the swing signals refer to Table 8-2. For the TUSB7320 Port 3 is not present and these bits have no effect.
15:12†	PORT2_SWING†	rw	Port 2 Swing. When the PORT2_SWING_OV bit is set to '1', these bits are used to set the output swing for port 2.For details on the behavior of the swing signals refer to Table 8-1.
11:8†	PORT2_DE†	rw	Port 2 Deemphasis. When the PORT2_DE_OV bit is set to '1' these bits are used to set the de-emphasis value for port 2. For details on the behavior of the swing signals refer to Table 8-2.
7:4†	PORT1_SWING†	rw	Port 1 Swing. When the PORT1_SWING_OV bit is set to '1', these bits are used to set the output swing for port 1. For details on the behavior of the swing signals refer to Table 8-1.
3:0†	PORT1_DE†	rw	Port 1 Deemphasis. When the PORT1_DE_OV bit is set to '1', these bits are used to set the de-emphasis value for port 1. For details on the behavior of the swing signals refer to Table 8-2.

(1) Bits marked with † are reset by a PCI Express reset (PERST#), a GRST#, or the internally-generated power-on reset

4.66 Equalizer Control Register

This register is used to control the equalizer settings for each of the USB 3.0 ports when the default setting is overridden through the Custom PHY Transmit/Receive Control Register. This register is reset by a PCI Express reset (PERST#), a GRST#, or the internally-generated power-on reset.

PCI register offset: E8h

Register type:Read/Write

Default value: 0000 0000h

Table 4-103. PCI Register E8h

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Table 4-104. Equalizer Control Register Description(1)

Bit	Field Name	Access	Description
31:28†	PORT4_EQ_INIT†	rw	Port 4 Equalizer - Initialization Mode. When the PORT4_EQ_OV bit is set to '1', these bits are used as the source for the Equalizer init values for port 4 of the PHY. For details on the behavior of the equalizer values refer to Table 8-3. For the TUSB7320 Port 4 is not present and these bits have no effect.
27:24†	PORT4_EQ_FUNC†	rw	Port 4 Equalizer- Functional Mode. When the PORT4_EQ_OV bit is set to '1', these bits are used as the source for the Equalizer func values for port 4 of the PHY. For details on the behavior of the equalizer values refer to Table 8-3. For the TUSB7320 Port 4 is not present and these bits have no effect.
23:20†	PORT3_EQ_INIT†	rw	Port 3 Equalizer - Initialization Mode. When the PORT3_EQ_OV bit is set to '1', these bits are used as the source for the Equalizer init values for port 3 of the PHY. For details on the behavior of the equalizer values refer to Table 8-3. For the TUSB7320 Port 3 is not present and these bits have no effect.
19:16†	PORT3_EQ_FUNC†	rw	Port 3 Equalizer- Functional Mode. When the PORT3_EQ_OV bit is set to '1', these bits are used as the source for the Equalizer func values for port 3 of the PHY. For details on the behavior of the equalizer values refer to Table 8-3. For the TUSB7320 Port 3 is not present and these bits have no effect.
15:12†	PORT2_EQ_INIT†	rw	Port 2 Equalizer - Initialization Mode. When the PORT2_EQ_OV bit is set to '1', these bits are used as the source for the Equalizer init values for port 3 of the PHY. For details on the behavior of the equalizer values refer to Table 8-3.
11:8†	PORT2_EQ_FUNC†	rw	Port 2 Equalizer- Functional Mode. When the PORT2_EQ_OV bit is set to '1', these bits are used as the source for the Equalizer func values for port 3 of the PHY. For details on the behavior of the equalizer values refer to Table 8-3.
7:4†	PORT1_EQ_INIT†	rw	Port 1 Equalizer - Initialization Mode. When the PORT1_EQ_OV bit is set to '1', these bits are used as the source for Equalizer init values for port 1 of the PHY. For details on the behavior of the equalizer values refer to Error: Reference source not found.
3:0†	PORT1_EQ_FUNC†	rw	Port 1 Equalizer- Functional Mode. When the PORT1_EQ_OV bit is set to '1', these bits are used as the source for Equalizer func values for port 1 of the PHY. For details on the behavior of the equalizer values refer to Table 8-3.

(1) Bits marked with † are reset by a PCI Express reset (PERST#), a GRST#, or the internally-generated power-on reset

4.67 Custom PHY Transmit/Receive Control Register

This register is used to enable the override of the default de-emphasis, transmit swing, and receiver equalization settings for each of the USB 3.0 ports. This register is reset by a PCI Express reset (PERST#), a GRST#, or the internally-generated power-on reset.

PCI register offset: ECh

Register type:Read/Write

Default value: 0000 0000h

Table 4-105. PCI Register ECh

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Table 4-106. Custom PHY Transmit/Receive Control Register Description(1)

Bit	Field Name	Access	Description
31:27	RSVD	r	Reserved. Returns zeros when read.
26†	PORT4_EQ_OV†	rw	Port 4 Equalization Override. When this bit is set to '1', the TUSB73X0 overrides the default equalization settings for port 4 with the values in the PORT4_EQ_FUNC field and the PORT4_EQ_INIT field of the Equalizer Control Register. For the TUSB7320 Port 4 is not present and this bit has no effect.
25†	PORT4_SWING_OV†	rw	Port 4 Swing Override. When this bit is set to '1', the TUSB73X0 overrides the default swing settings for port 4 with the values in the PORT4_SWING field of the Deemphasis and Swing Control Register. For the TUSB7320 Port 4 is not present and this bit has no effect.
24†	PORT4_DE_OV†	rw	Port 4 Deemphasis Override. When this bit is set to '1', the TUSB73X0 overrides the default de-emphasis settings for port 4 with the values in the PORT4_DE field of the Deemphasis and Swing Control Register. For the TUSB7320 Port 4 is not present and this bit has no effect.
23:19	RSVD	r	Reserved. Returns zeros when read.
18†	PORT3_EQ_OV†	rw	Port 3 Equalization Override. When this bit is set to '1', the TUSB73X0 overrides the default equalization settings for port 3 with the values in the PORT3_EQ_FUNC field and the PORT3_EQ_INIT field of the Equalizer Control Register. For the TUSB7320 Port 3 is not present and this bit has no effect.
17†	PORT3_SWING_OV†	rw	Port 3 Swing Override. When this bit is set to '1', the TUSB73X0 overrides the default swing settings for port 3 with the values in the PORT3_SWING field of the Deemphasis and Swing Control Register. For the TUSB7320 Port 3 is not present and this bit has no effect.
16†	PORT3_DE_OV†	rw	Port 3 Deemphasis Override. When this bit is set to '1', the TUSB73X0 overrides the default de-emphasis settings for port 3 with the values in the PORT3_DE field of the Deemphasis and Swing Control Register. For the TUSB7320 Port 3 is not present and this bit has no effect.
15:11	RSVD	r	Reserved. Returns zeros when read.
10†	PORT2_EQ_OV†	rw	Port 2 Equalization Override. When this bit is set to '1', the TUSB73X0 overrides the default equalization settings for port 2 with the values in the PORT2_EQ_FUNC field and the PORT2_EQ_INIT field of the Equalizer Control Register.
9†	PORT2_SWING_OV†	rw	Port 2 Swing Override. When this bit is set to '1', the TUSB73X0 overrides the default swing settings for port 2 with the values in the PORT2_SWING field of the Deemphasis and Swing Control Register.
8†	PORT2_DE_OV†	rw	Port 2 Deemphasis Override. When this bit is set to '1', the TUSB73X0 overrides the default de-emphasis settings for port 2 with the values in the PORT2_DE field of the Deemphasis and Swing Control Register.
7:3	RSVD	r	Reserved. Returns zeros when read.
2†	PORT1_EQ_OV†	rw	Port 1 Equalization Override. When this bit is set to '1', the TUSB73X0 overrides the default equalization settings for port 1 with the values in the PORT1_EQ_FUNC field and the PORT1_EQ_INIT field of the Equalizer Control Register.
1†	PORT1_SWING_OV†	rw	Port 1 Swing Override. When this bit is set to '1', the TUSB73X0 overrides the default swing settings for port 1 with the values in the PORT1_SWING field of the Deemphasis and Swing Control Register.
0†	PORT1_DE_OV†	rw	Port 1 Deemphasis Override. When this bit is set to '1', the TUSB73X0 overrides the default de-emphasis settings for port 1 with the values in the PORT1_DE field of the Deemphasis and Swing Control Register.

(1) Bits marked with † are reset by a PCI Express reset (PERST#), a GRST#, or the internally-generated power-on reset

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5 PCI EXPRESS EXTENDED CONFIGURATION SPACE

5.1 The PCI Express Extended Configuration Map

Table 5-1. PCI Express Extended Configuration Register Map

Register Name		Offset
Next Capability Offset / Capability Version	PCI Express Advanced Error Reporting Capabilities ID	100h
Uncorrectable Error Status Register		104h
Uncorrectable Error Mask Register		108h
Uncorrectable Error Severity Register		10Ch
Correctable Error Status Register		110h
Correctable Error Mask Register		114h
Advanced Error Capabilities and Control Register		118h
Header Log Register		11Ch
Header Log Register		120h
Header Log Register		124h
Header Log Register		128h
Reserved		12Ch-14Fh
Next Capability Offset / Capability Version	Device Serial Number Capability ID	150h
Serial Number Register (Lower DW)		154h
Serial Number Register (Upper DW)		158h
Reserved		15C-FFFh

5.2 Advanced Error Reporting capability Register

This read-only register identifies the linked list item as the register for PCI Express Advanced Error Reporting Capabilities. The register returns 0001h when read.

PCI Express Extended Register Offset: 100h

Register type:Read-Only

Default value: 0001h

Table 5-2. PCI Express Extended Register 100h

Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

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5.3 Next Capability Offset / Capability Version Register

This read-only register identifies the next location in the PCI Express Extended Capabilities link list. The upper 12 bits in this register shall be 150h, indicating that the Device Serial Number Capability starts at offset 150h. The least significant four bits identify the revision of the current capability block as 2h.

PCI Express Extended Register Offset: 100h

Register type:Read-Only

Default value: 1502h

Table 5-3. PCI Express Extended Register 102h

Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	1	0	1	0	1	0	0	0	0	0	0	1	0

5.4 Uncorrectable Error Status Register

The Uncorrectable Error Status Register reports the status of individual errors as they occur. Software may clear these bits only by writing a 1 to the desired location.

PCI Express Extended Register Offset: 104h

Register type:Read-Only, Read/Clear

Default value: 0000 0000h

Table 5-4. PCI Express Extended Register 104h

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5-5. Custom PHY Transmit/Receive Control Register Description(1)

Bit	Field Name	Access	Description
31:21	RSVD	r	Reserved. Returns zeros when read.
20†	UR_ERROR †	rcu	Unsupported Request Error. This bit is asserted when an Unsupported Request is received.
19†	ECRC_ERROR †	rcu	Extended CRC Error. This bit is asserted when an Extended CRC error is detected.
18†	MAL_TLP †	rcu	Malformed TLP. This bit is asserted when a malformed TLP is detected.
17†	RX_OVERFLOW †	rcu	Receiver Overflow. This bit is asserted when the flow control logic detects that the transmitting device has illegally exceeded the number of credits that were issued.
16†	UNXP_CPL †	rcu	Unexpected Completion. This bit is asserted when a completion packet is received that does not correspond to an issued request.
15†	CPL_ABORT †	rcu	Completer Abort. This bit is asserted when the TUSB73X0 signals a Completer Abort.
14†	CPL_TIMEOUT †	rcu	Completion Timeout. This bit is asserted when no completion has been received for an issued request before the timeout period.

(1) Bits marked with † are reset by a PCI Express reset (PERST#), a GRST#, or the internally-generated power-on reset

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Table 5-5. Custom PHY Transmit/Receive Control Register Description(1) (continued)

13†	FC_ERROR †	rcu	Flow Control Error. This bit is asserted when a flow control protocol error is detected either during initialization or during normal operation.
12†	PSN_TLP †	rcu	Poisoned TLP. This bit is asserted when a poisoned TLP is received.
11:5	RSVD	r	Reserved. Returns zeros when read.
4†	DLL_ERROR †	rcu	Data Link Protocol Error. This bit is asserted if a data link layer protocol error is detected.
3:0	RSVD	r	Reserved. Returns zeros when read.

5.5 Uncorrectable Error Mask Register

The Uncorrectable Error Mask Register controls the reporting of individual errors as they occur. When a bit is set to one, the corresponding error condition will not be logged, and does not update any of the status bits within the Extended Error Reporting Capability block.

PCI Express Extended Register Offset: 108h

Register type:Read-Only, Read/Write

Default value: 0000 0000h

Table 5-6. PCI Express Extended Register 108h

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5-7. Bit Descriptions – Uncorrectable Error Mask Register(1)

Bit	Field Name	Access	Description
31:21	RSVD	r	Reserved. Returns zeros when read.
20†	UR_ERROR_MASK †	rw	Unsupported Request Error Mask. 0 – Error Condition is Unmasked 1 – Error Condition is Masked
19†	ECRC_ERROR_MASK †	rw	Extended CRC Error Mask. 0 – Error Condition is Unmasked 1 – Error Condition is Masked
18†	MAL_TLP_MASK †	rw	Malformed TLP Mask. 0 – Error Condition is Unmasked 1 – Error Condition is Masked
17†	RX_OVERFLOW_MASK †	rw	Receiver Overflow Mask. 0 – Error Condition is Unmasked 1 – Error Condition is Masked
16†	UNXP_CPL_MASK †	rw	Unexpected Completion Mask. 0 – Error Condition is Unmasked 1 – Error Condition is Masked
15†	CPL_ABORT_MASK †	rw	Completer Abort Mask. 0 – Error Condition is Unmasked 1 – Error Condition is Masked
14†	CPL_TIMEOUT_MASK †	rw	Completion Timeout Mask. 0 – Error Condition is Unmasked 1 – Error Condition is Masked

(1) Bits marked with † are reset by a PCI Express reset (PERST#), a GRST#, or the internally-generated power-on reset

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Table 5-7. Bit Descriptions – Uncorrectable Error Mask Register(1) (continued)

13†	FC_ERROR_MASK †	rw	Flow Control Error Mask. 0 – Error Condition is Unmasked 1 – Error Condition is Masked
12†	PSN_TLP_MASK †	rw	Poisoned TLP Mask. 0 – Error Condition is Unmasked 1 – Error Condition is Masked
11:5	RSVD	r	Reserved. Returns zeros when read.
4†	DLL_ERROR_MASK †	rw	Data Link Protocol Error Mask. 0 – Error Condition is Unmasked 1 – Error Condition is Masked
3:0	RSVD	r	Reserved. Returns zeros when read.

5.6 Uncorrectable Error Severity Register

The Uncorrectable Error Severity Register controls the reporting of individual errors as ERR_FATAL or ERR_NONFATAL. When a bit is set, the corresponding error condition will be identified as fatal. When a bit is clear, the corresponding error condition will be identified as non-fatal.

PCI Express Extended Register Offset: 10Ch

Register type:Read-Only, Read/Write

Default value: 0026 2030h

Table 5-8. PCI Express Extended Register 10Ch

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0

Table 5-9. Bit Descriptions – Uncorrectable Error Severity Register(1)

Bit	Field Name	Access	Description
31:23	RSVD	r	Reserved. Returns zeros when read.
22	RSVD	r	Reserved. Returns '1' when read.
21	RSVD	r	Reserved. Returns zeros when read.
20†	UR_ERROR_SEVR †	rw	Unsupported Request Error Severity. 0 – Error Condition is signaled using ERR_NONFATAL 1 – Error Condition is signaled using ERR_FATAL
19†	ECRC_ERROR_SEVR †	rw	Extended CRC Error Severity. 0 – Error Condition is signaled using ERR_NONFATAL 1 – Error Condition is signaled using ERR_FATAL
18†	MAL_TLP_SEVR †	rw	Malformed TLP Severity. 0 – Error Condition is signaled using ERR_NONFATAL 1 – Error Condition is signaled using ERR_FATAL
17†	RX_OVERFLOW_SEVR †	rw	Receiver Overflow Severity. 0 – Error Condition is signaled using ERR_NONFATAL 1 – Error Condition is signaled using ERR_FATAL
16†	UNXP_CPL_SEVR †	rw	Unexpected Completion Severity. 0 – Error Condition is signaled using ERR_NONFATAL 1 – Error Condition is signaled using ERR_FATAL

(1) Bits marked with † are reset by a PCI Express reset (PERST#), a GRST#, or the internally-generated power-on reset

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Table 5-9. Bit Descriptions – Uncorrectable Error Severity Register(1) (continued)

15†	CPL_ABORT_SEVR †	rw	Completer Abort Severity. 0 – Error Condition is signaled using ERR_NONFATAL 1 – Error Condition is signaled using ERR_FATAL
14†	CPL_TIMEOUT_SEVR †	rw	Completion Timeout Severity. 0 – Error Condition is signaled using ERR_NONFATAL 1 – Error Condition is signaled using ERR_FATAL
13†	FC_ERROR_SEVR †	rw	Flow Control Error Severity. 0 – Error Condition is signaled using ERR_NONFATAL1 – Error Condition is signaled using ERR_FATAL
12†	PSN_TLP_SEVR †	rw	Poisoned TLP Severity. 0 – Error Condition is signaled using ERR_NONFATAL 1 – Error Condition is signaled using ERR_FATAL
11:6	RSVD	r	Reserved. Returns zeros when read.
5	RSVD	r	Reserved. Returns ‘1’ when read.
4†	DLL_ERROR_SEVR †	rw	Data Link Protocol Error Severity. 0 – Error Condition is signaled using ERR_NONFATAL 1 – Error Condition is signaled using ERR_FATAL
3:0	RSVD	r	Reserved. Returns zeros when read.

5.7 correctable Error Severity Register

The Correctable Error Status Register reports the status of individual errors as they occur. Software may clear these bits only by writing a 1 to the desired location.

PCI Express Extended Register Offset: 110h

Register type:Read-Only, Read/Clear

Default value: 0000 0000h

Table 5-10. PCI Express Extended Register 110h

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5-11. Bit Descriptions – Correctable Error Severity Register(1)

Bit	Field Name	Access	Description
31:14	RSVD	r	Reserved. Returns zeros when read.
13†	ANFES †	rcu	Advisory Non-Fatal Error Status. This bit is asserted when an Advisory Non-Fatal Error has been reported.
12†	REPLAY_TMOUT †	rcu	Replay Timer Timeout. This bit is asserted when the replay timer expires for a pending request or completion that has not been acknowledged.
11:9	RSVD	r	Reserved. Returns zeros when read.
8†	REPLAY_ROLL †	rcu	REPLAY_NUM Rollover. This bit is asserted when the replay counter rolls over when a pending request or completion has not been acknowledged.
7†	BAD_DLLP †	rcu	Bad DLLP Error. This bit is asserted when an 8b/10b error was detected by the PHY during the reception of a DLLP.
6†	BAD_TLP †	rcu	Bad TLP Error. This bit is asserted when an 8b/10b error was detected by the PHY during the reception of a TLP.
5:1	RSVD	r	Reserved. Returns zeros when read.

(1) Bits marked with † are reset by a PCI Express reset (PERST#), a GRST#, or the internally-generated power-on reset

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Table 5-11. Bit Descriptions – Correctable Error Severity Register(1) (continued)

0†	RX_ERROR †	rcu	Receiver Error. This bit is asserted when an 8b/10b error is detected by the PHY at any time.

5.8 correctable Error Mask Register

The Correctable Error Status Register reports the status of individual errors as they occur. Software may clear these bits only by writing a 1 to the desired location.

PCI Express Extended Register Offset: 114h

Register type:Read-Only, Read/Write

Default value: 0000 2000h

Table 5-12. PCI Express Extended Register 114h

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5-13. Bit Descriptions – Correctable Error Mask Register(1)

Bit	Field Name	Access	Description
31:14	RSVD	r	Reserved. Returns zeros when read.
13†	ANFEM †	rw	Advisory Non-Fatal Error Mask. 0 – Error Condition is Unmasked 1 – Error Condition is Masked
12†	REPLAY_TMOUT_MASK †	rw	Replay Timer Timeout Mask. 0 – Error Condition is Unmasked 1 – Error Condition is Masked
11:9	RSVD	r	Reserved. Returns zeros when read.
8†	REPLAY_ROLL_MASK †	rw	REPLAY_NUM Rollover Mask. 0 – Error Condition is Unmasked 1 – Error Condition is Masked
7†	BAD_DLLP_MASK †	rw	Bad DLLP Error Mask. 0 – Error Condition is Unmasked 1 – Error Condition is Masked
6†	BAD_TLP_MASK †	rw	Bad TLP Error Mask. 0 – Error Condition is Unmasked 1 – Error Condition is Masked
5:1	RSVD	r	Reserved. Returns zeros when read.
0†	RX_ERROR_MASK †	rw	Receiver Error Mask. 0 – Error Condition is Unmasked 1 – Error Condition is Masked

(1) Bits marked with † are reset by a PCI Express reset (PERST#), a GRST#, or the internally-generated power-on reset

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5.9 Advanced Error Capabilities and control Register

The Advanced Error Capabilities and Control Register allows the system to monitor and control the advanced error reporting capabilities.

PCI Express Extended Register Offset: 118h

Register type:Read-Only, Read/Write

Default value: 0000 0050h

Table 5-14. PCI Express Extended Register 118h

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Table 5-15. Bit Descriptions – Advanced Error Capabilities and Control Register(1)

Bit	Field Name	Access	Description
31:9	RSVD	r	Reserved. Returns zeros when read.
8†	ECRC_CHK_EN †	rw	Extended CRC Check Enable. 0 – Extended CRC checking is Disabled 1 – Extended CRC checking is Enabled
7	ECRC_CHK_CAPABLE	r	Extended CRC Check Capable. This read-only bit returns a value of ‘1’ indicating that the TUSB73X0 is capable of checking extended CRC information.
6†	ECRC_GEN_EN †	rw	Extended CRC Generation Enable. 0 – Extended CRC generation is Disabled 1 – Extended CRC generation is Enabled
5	ECRC_GEN_CAPABLE	r	Extended CRC Generation Capable. This read-only bit returns a value of ‘1’ indicating that the TUSB73X0 is capable of generating extended CRC information.
4:0†	FIRST_ERR †	ru	First Error Pointer. This five bit value reflects the bit position within the Uncorrectable Error Status Register corresponding to the class of the first error condition that was detected.

(1) Bits marked with † are reset by a PCI Express reset (PERST#), a GRST#, or the internally-generated power-on reset

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5.10 Header Log Register

The Header Log Register stores the TLP header for the packet that lead to the most recently detected error condition. Offset 11Ch contains the first DWORD. Offset 128h contains the last DWORD (in the case of a 4DW TLP header. Each DWORD is stored with the least significant byte representing the earliest transmitted.

PCI Express Extended Register Offset: 11Ch, 120h, 124h, 128h

Register type:Read-Only

Default value: 0000 0000h

Table 5-16. PCI Express Extended Register 11Ch, 120, 124h, and 128h

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

5.11 Device Serial Number Capability ID Register

This read-only register identifies the linked list item as the Device Serial Number Capability. This register returns 0003h when read.

PCI Express Extended Register Offset: 150h

Register type:Read-Only

Default value: 0003h

Table 5-17. Device Serial Number Capability ID Register

Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

5.12 Next Capability Offset/Capability Version Register

This read-only register identifies the next location in the PCI Express Extended Capabilities link list. The upper 12 bits in this register are 000h, indicating that the Device Serial Number Capability is the last capability in the list. The least significant four bits identify the revision of the current capability block as 1h.

PCI Express Extended Register Offset: 152h

Register type:Read-Only

Default value: 0001h

Table 5-18. Next Capability Offset/Capability Version Register

Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

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5.13 Device Serial Number Register

This read-only register identifies the Device Serial Number for the TUSB73x0. The Device Serial Number is in the format of an IEEE defined 64-bit extended unique identifier (EUI-64). The EUI-64 consists of TI's 24-bit company ID (called an OUI-24) plus a 40 bit extension identifier. TI's OUI-24 is 080028h and is hardwired into bits 63:40 of the Device Serial Number Register. The TUSB73x0 has been assigned the range of 00 0000 0000h to 00 0FFF FFFFh for the 40-bit extension identifier. As such, bits 39:32 of the Device Serial Number Register are hardwired to 00h, and bits 31:0 of the Device Serial Number Register are defined by a value unique for each device.

PCI Express Extended Register Offset: 154h

Register type:Read-Only

Default value: 0800 2800 XXXX XXXX h

Table 5-19. Device Serial Number Register

Bit No.	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
Reset State	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Bit No.	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Reset State	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0
Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 5-20. Bit Descriptions - Device Serial Number Register(1)

Bit	Field Name	Access	Description
63:32	SERIAL_NUM_UPPER	r	Serial Number – Upper DW. The upper DW of the Serial Number is hardwired to 0800 2800h.
31:0	SERIAL_NUM_LOWER	r	Serial Number – Lower DW. The lower DW of the Serial Number is unique for each device.

(1) Bits marked with † are reset by a PCI Express reset (PERST#), a GRST#, or the internally-generated power-on reset

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6 xHCI MEMORY MAPPED REGISTER SPACE

6.1 The xHCI Register Map

The TUSB73X0 includes xHCI registers in memory mapped register space. These registers are accessible via the address programmed into the Base Address Register 0/1.

All bits marked with a '*' are sticky bits and are only reset by a Global Reset (GRST#).

Table 6-1. xHCI Register Map

Register Name	Offset
Host Controller Capability Registers	000h-01Fh
Host Controller Operational Registers	020h-49Fh
Runtime Registers	4A0h-5BFh
Doorbell Registers	5C0h-6C3h
Reserved	6C4-9BFh
xHCI Extended Capabilities Registers	9C0h-9EBh
Reserved	9ECh-FFFFFh

6.2 Host Controller Capability Registers

These registers specify the limits and capabilities of the TUSB7340. The offset in then table is from the address programmed into the Base Address Register 0.

Table 6-2. Host Controller Capability Register Map

Register Name			Offset
HC Interface Version	Reserved	Capability Length	00h
HC Structural Parameters 1			04h
HC Structural Parameters 2			08h
HC Structural Parameters 3			0Ch
HC Capability Parameters			10h
Doorbell Offset			14h
Runtime Register Space Offset			18h
Reserved			1Ch-1Fh

6.2.1 Capability Registers Length

This read only register returns 20h when read to indicate that the beginning of the Operational Register Space is at an offset of 20h from the address programmed into the Base Address Register 0.

BAR0 register offset: 00h

Register type:Read-Only

Default value: 0020h

Table 6-3. HC Capability Register 00h

Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

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6.2.2 Host Controller Interface Version Number

This read only register indicates the xHCI specification revision number supported by the TUSB73X0.

BAR0 register offset: 02h

Register type:Read-Only

Default value: 0096h

Table 6-4. HC Capability Register 02h

Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0

6.2.3 Host Controller Structural Parameters 1

This read only register defines basic structural parameters supported by the TUSB73X0.

BAR0 register offset: 04h

Register type:Read-Only

Default value: 0800 0840h

Table 6-5. HC Capability Register 04h

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0

Table 6-6. HC Structural Parameters 1 Description

Bit	Field Name	Access	Description
31:24	MAX_PORTS	r	Number of Ports. For the TUSB7340, this field is 08h to indicate that 8 ports are supported. For the TUSB7320, this field is 04h to indicate that 4 ports are supported. This field also indicates the number of sets of port registers that are addressable in the Operational Register Space.
23:19	RSVD	r	Reserved. Returns zeros when read.
18:8	MAX_INTRS	r	Number of Interrupters. This field specifies the number of Interrupters that are implemented. The TUSB73x0 implements 8 Interrupters. Each Interrupter is allocated to a vector of MSI-X.
7:0	MAX_SLOTS	r	Number of Device Slots. This field specifies the maximum number of Device Context Structures and Doorbell Array entries that are supported. The TUSB73x0 supports 64 Device Slots.

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6.2.4 Host Controller Structural Parameters 2

This read only register defines basic structural parameters supported by the TUSB73X0.

BAR0 register offset: 08h

Register type:Read-Only

Default value: 0C00 00F1h

Table 6-7. HC Capability Register 08h

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	1

Table 6-8. HC Structural Parameters 2 Description

Bit	Field Name	Access	Description
31:27	MAX_SCRATCH_BUF	r	Max Scratchpad Buffers. This field indicates the number of Scratchpad Buffers system software reserves. The TUSB73X0 uses one Scratchpad Buffer.
26	SPR	r	Scratchpad Restore. This bit is 1b to indicate that the TUSB73X0 requires the integrity of the Scratchpad Buffer space to be maintained across power events.
25:13	RSVD	r	Reserved. Returns zeros when read.
12:8	IOC_INTERVAL	r	IOC Interval. This field is 0b.
7:4	ERST_MAX	r	Event Ring Segment Table Max. This field is 1111b to indicate that the TUSB73X0 supports up to 32K Event Ring Segment Table entries.
3:0	IST	r	Isochronous Scheduling Threshold. This field is 0001b to indicate that software can add a TRB no later than 1 Microframes before that TRB is scheduled to be executed.

6.2.5 Host Controller Structural Parameters 3

This read only register defines basic structural parameters supported by the TUSB73X0.

BAR0 register offset: 0Ch

Register type:Read-Only

Default value: 07FF 00A0h

Table 6-9. HC Capability Register 0Ch

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

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Table 6-10. HC Structural Parameters 3 Description

Bit	Field Name	Access	Description
31:16	U2_EXIT_LAT	r	U2 Device Exit Latency. This field is 07FFh to indicate that the worst case latency for the TUSB73X0 to transition from U2 to U0 is 2047 µs.
15:8	RSVD	r	Reserved. Returns zeros when read.
7:0	U1_EXIT_LAT	r	U1 Device Exit Latency. This field is 0Ah to indicate that the worst case latency for the TUSB73X0 to transition a root hub Port Link State from U1 to U0 is 10 µs.

6.2.6 Host Controller Capability Parameters

This read only register defines capability parameters supported by the TUSB73X0.

BAR0 register offset: 10h

Register type:Read-Only

Default value: 0270 102Xh

Table 6-11. HC Capability Register 10h

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	1	0	0	1	1	1	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	1	1	1	1	0	0	0	0	0	1	1	0	x	1	0	1

Table 6-12. HC Capability Parameters Description

Bit	Field Name	Access	Description
31:16	XECP	r	xHCI Extended Capabilities Pointer. This field is 0270h to indicate that the beginning of the first xHCI Extended Capability is at an offset of 09C0h from the address programmed into the Base Address Register 0.
15:12	MAX_PSA_SIZE	r	Maximum Primary Stream Array Size. This field is ‘1111’ to indicate that the TUSB73X0 supports a Primary Stream Array size of 64K.
11:10	RSVD	r	Reserved. Returns zeros when read.
9	SBD	r	Secondary Bandwidth Domain Reporting. This bit is ‘0’ to indicate that the TUSB73X0 does not support Secondary Bandwidth Domain reporting.
8	FSE	r	Force Stopped Event. This bit is ‘0’ to indicate that theTUSB73X0 does not support Force Stopped Events.
7	NSS	r	No Secondary SID Support. This bit is ‘0’ to indicate that the TUSB73X0 supports Secondary Stream ID decoding.
6	LTC	r	Latency Tolerance Messaging Capability. This bit is ‘1’ to indicate that the TUSB73X0 supports Latency Tolerance Messaging.
5	LHRC	r	Light HC Reset Capability. This bit is ‘1’ to indicate that the TUSB73X0 supports Light Host Controller Resets.
4	PIND	r	Port Indicators. This bit is ‘0’ to indicate that the TUSB73X0 does not support port indicators.
3	PPC	r	Port Power Control. This value of this bit is determined by the PPC_NOT_PRESENT bit in the USB Control Register.
2	CSZ	r	Context Size. This bit is ‘1’ to indicate that the TUSB73X0 uses 64 byte Context data structures.
1	BNC	r	Bandwidth Negotiation Capability. This bit is ‘0’ to indicate that the TUSB73X0 does not implement Bandwidth Negotiation.

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Table 6-12. HC Capability Parameters Description (continued)

0	AC64	r	64-bit Addressing Capability. This bit is '1' to indicate that the TUSB73X0 implements 64-bit address memory pointers.

6.2.7 Doorbell Offset

This read only register returns 0000 05C0h when read to indicate that the beginning of the Doorbell Array is at an offset of 5C0h from the address programmed into the Base Address Register 0.

BAR0 register offset: 14h

Register type:Read-Only

Default value: 0000 05C0h

Table 6-13. HC Capability Register 14h

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	1	0	1	1	1	0	0	0	0	0	0

6.2.8 Runtime Register Space Offset

This read only register returns 0000 04A0h when read to indicate that the beginning of the Runtime Register Space is at an offset of 4A0h from the address programmed into the Base Address Register 0.

BAR0 register offset: 18h

Register type:Read-Only

Default value: 0000 04A0h

Table 6-14. HC Capability Register 18h

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	1	0	0	1	0	1	0	0	0	0	0

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6.3 Host Controller Operational Registers

These registers control the operation of the TUSB73X0. The offset in Table 6-15 is from the Operational Base, which is the address programmed into the Base Address Register 0 plus the value programmed into the Capability Registers Length (see Section 6.2.1).

Table 6-15. Host Controller Operational Register Map

Register Name	Offset
USB Command	00h
USB Status	04h
Page Size	08h
Reserved	0Ch-13h
Device Notification Control	14h
Command Ring Control	18h-1Fh
Reserved	20h-2Fh
Device Context Base Address Array Pointer	30h-37h
Configure	38h
Reserved	3Ch-3FFh
Port Register Set 1-8	400h-47Fh

6.3.1 USB Command Register

This register indicates the command to be executed by the TUSB73X0.

Operational Base register offset:00h

Register type:Read-Only,Read/Write

Default value: 0000 0000h

Table 6-16. HC Operational Register (Operational Base + 00h)

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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6.3.2 USB Command Register

This register indicates the command to be executed by the TUSB73X0.

Operational Base register offset:00h

Register type:Read-Only,Read/Write

Default value: 0000 0000h

Table 6-17. HC Operational Register (Operational Base + 00h)

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-18. USB Command Register Description

Bit	Field Name	Access	Description
31:12	RSVD	r	Reserved. Returns zeros when read.
11	EU3S	rw	Enable U3 MFINDEX Stop
10	EWE	rw	Enable Wrap Event
9	CRS	rw	Controller Restore State
8	CSS	rw	Controller Save State
7	LHCRST	rw	Light Host Controller Reset
6:4	RSVD	r	Reserved. Returns zeros when read.
3	HSEE	rw	Host System Error Enable
2	INTE	rw	Interrupter Enable
1	HCRST	rw	Host Controller Reset
0	R/S	rw	Run/Stop.

6.3.3 USB Status Register

This register indicates pending interrupts and various states of the TUSB73X0.

Operational Base register offset:04h

Register type:Read-Only, Read/Clear

Default value: 0000 0801h

Table 6-19. HC Operational Register (Operational Base + 04h)

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1

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Table 6-20. USB Status Register Description

Bit	Field Name	Access	Description
31:13	RSVD	r	Reserved. Returns zeros when read.
12	HCE	r	Host Controller Error
11	CNR	r	Controller Not Ready
10	SRE	rc	Save/Restore Error.
9	RSS	r	Restore State Status.
8	SSS	r	Save State Status.
7:5	RSVD	r	Reserved. Returns zeros when read.
4	PCD	rc	Port Change Detect
3	EINT	rc	Event Interrupt.
2	HSE	rc	Host System Error.
1	RSVD	r	Reserved. Returns zeros when read.
0	HCH	r	HC Halted.

6.3.4 Page Size Register

This register indicates the page size supported by the TUSB73X0.

Operational Base register offset:08h

Register type:Read-Only

Default value: 0000 0001h

Table 6-21. HC Operational Register (Operational Base + 08h)

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Table 6-22. Page Size Register Description

Bit	Field Name	Access	Description
31:16	RSVD	r	Reserved. Returns zeros when read.
15:0	PAGE_SIZE	r	Page Size. The TUSB73X0 supports a 4k byte page size, so this field is set to 0000 0001h.

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6.3.5 Device Notification Control Register

This register is used by software to enable or disable the reporting of the reception of specific USB Device Notification Transaction Packets.

Operational Base register offset:14h

Register type:Read-Only, Read/Write

Default value: 0000 0000h

Table 6-23. HC Operational Register (Operational Base + 14h)

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-24. Device Notification Control Register Description

Bit	Field Name	Access	Description
31:16	RSVD	r	Reserved. Returns zeros when read.
15:0	NOTE_EN	rw	Notification Enable (N0-N15).

6.3.6 Command Ring Control Register

This 64-bit register provides Command Ring control and status capabilities, and identifies the address and Cycle bit state of the Command Ring Dequeue Pointer.

Operational Base register offset:18h

Register type:Read-Only, Read/Write

Default value: 0000 0000 0000 0000h

Table 6-25. HC Operational Register (Operational Base + 18h)

Bit No.	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Table 6-26. Command Ring Control Register Description

Bit	Field Name	Access	Description
31:6	COM_RING_POINT	rw	Command Ring Pointer.
5:4	RSVD	r	Reserved. Returns zeros when read.
3	CRR	r	Command Ring Running.
2	CA	rw	Command Abort.
1	CS	rw	Command Stop.
0	RCS	rw	Ring Cycle State.

6.3.7 Device Context Base Address Array Pointer Register

This 64-bit register identifies the base address of the Device Context Base Address Array.

Operational Base register offset:30h

Register type:Read-Only, Read/Write

Default value: 0000 0000 0000 0000h

Table 6-27. HC Operational Register (Operational Base + 30h)

Bit No.	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-28. Device Context Base Address Array Pointer Register Description

Bit	Field Name	Access	Description
31:6	DCBAAP	rw	Device Context Base Address Array Pointer.
5:0	RSVD	r	Reserved. Returns zeros when read.

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6.3.8 Configure Register

This register defines runtime xHC configuration parameters.

Operational Base register offset:38h

Register type:Read-Only, Read/Write

Default value: 0000 0000h

Table 6-29. HC Operational Register (Operational Base + 38h)

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-30. Configure Register Description

Bit	Field Name	Access	Description
31:8	RSVD	r	Reserved. Returns zeros when read.
7:0	MAX_SLOTS_EN	rw	Max Device Slots Enabled.

6.3.9 Port Status and Control Register

The TUSB73X0 implements a Port Status and Control Register for each port that is implemented. The number of Port Status and Control Registers is the same as the value in the MAX_PORTS field in the Host Controller Structural Parameters 1 Register (see 6.1.3).

Operational Base register offset:400h + (10h*(n-1))), where n = Port Number

Register type:Read-Only, Read/Write, Read/Clear

Default value: X000 02A0h

Table 6-31. HC Operational Register (Operational Base + 400h + (10h*(n-1))), where n = Port Number

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	x	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0

Table 6-32. Port Status and Control Register Description

Bit	Field Name	Access	Description
31	WPR *	rc or r	Warm Port Reset. This field is only valid for USB 3.0 protocol ports. For USB 2.0 protocol ports, this bit is reserved.
30	DR	r	Device Removable. The value of this bit depends on the value programmed into the USBx_PORTy_NON_REM bit in the USB Control Register that corresponds to the port number and port type associated with this register.
29:28	RSVD	r	Reserved. Returns zeros when read.
27	WOE *	rw	Wake on Over-current Enable.

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Table 6-32. Port Status and Control Register Description (continued)

26	WDE *	rw	Wake on Disconnect Enable.
25	WCE *	rw	Wake on Connect Enable.
24	RSVD	r	Reserved. Return zero when read.
23	CEC *	rc or r	Port Config Error Change. This field is only valid for USB 3.0 protocol ports. For USB 2.0 protocol ports, this bit is reserved.
22	PLC *	rc	Port Link State Change.
21	PRC *	rc	Port Reset Change.
20	OCC *	rc	Over-current Change.
19	WRC *	rc or r	Warm Port Reset Change. This field is only valid for USB 3.0 protocol ports. For USB 2.0 protocol ports, this bit is reserved.
18	PEC *	rc	Port Enabled/Disabled Change.
17	CSC *	rc	Connect Status Change.
16	LWS	w	Port Link State Write Strobe. This bit returns a zero when read.
15:14	PIC *	rw	Port Indicator Control. Since the TUSB73X0 does not support port indicators, this field has no effect.
13:10	PORT_SPEED *	r	Port Speed
9	PP *	rw	Port Power.
8:5	PLS *	rw	Port Link State
4	PR *	rs	Port Reset.
3	OCA	r	Over-current Active.
2	RSVD	r	Reserved. Returns zero when read.
1	PED *	rc	Port Enabled/Disabled.
0	CCS *	r	Current Connect Status.

6.3.10 Port PM Status and Control Register (USB 3.0 Ports)

The TUSB73X0 implements a Port PM Status and Control Register for each port that is implemented. The number of Port PM Status and Control Registers is the same as the value in the MAX_PORTS field in the Host Controller Structural Parameters 1 Register (see Section 6.2.3).

Operational Base register offset:404h + (10h*(n-1))), where n = Port Number

Register type:Read-Only, Read/Write

Default value: 0000 0000h

Table 6-33. HC Operational Register (Operational Base + 404h + (10h*(n-1))), where n = Port Number

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-34. Port PM Status and Control Register (USB 3.0) Description

Bit	Field Name	Access	Description
31:17	RSVD	r	Reserved. Returns zeros when read.
16	FLA	rw	Force Link PM Accept.
15:8	U2_TIMEOUT*	rw	U2 Timeout.
7:0	U1_TIMEOUT*	rw	U1 Timeout.

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6.3.11 Port PM Status and Control Register (USB 2.0 Ports)

The TUSB73X0 implements a Port PM Status and Control Register for each port that is implemented. The number of Port PM Status and Control Registers is the same as the value in the MAX_PORTS field in the Host Controller Structural Parameters 1 Register (see Section 6.2.3).

Operational Base register offset:404h + (10h*(n-1))), where n = Port Number

Register type:Read-Only, Read/Write

Default value: 0000 0000h

Table 6-35. HC Operational Register (Operational Base + 404h + (10h*(n-1))), where n = Port Number

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-36. Port PM Status and Control Register (USB 2.0) Description

Bit	Field Name	Access	Description
31:28	PORT_TEST_CTRL	rw	Port Test Control.
27:16	RSVD	r	Reserved. Returns zeros when read.
15:8	L1_DEV_SLOT	rw	L1 Device Slot.
7:4	HIRD	rw	Host Initiated Resume Duration.
3	RWE	rw	Remote Wake Enable.
2:0	L1S	r	L1 Status.

6.3.12 Port Link Info Register

The TUSB73X0 implements a Port Link Info Register for each port USB 3.0 port that is implemented. For USB 2.0 ports, the Port Link Info Register is reserved and returns zeros when read. The number of Port Link Info Registers is the same as the value in the MAX_PORTS field in the Host Controller Structural Parameters 1 Register (see Section 6.2.3).

Operational Base register offset:408h + (10h*(n-1))), where n = Port Number

Register type:Read-Only

Default value: 0000 0000h

Table 6-37. HC Operational Register (Operational Base + 408h + (10h*(n-1))), where n = Port Number

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Table 6-38. Port Link Info Register Description

Bit	Field Name	Access	Description
31:16	RSVD	r	Reserved. Returns zeros when read.
15:0	LINK_ERROR_COUNT	r	Link Error Count.

6.4 Host Controller Runtime Registers

These registers are used to read the current microframe and to control the interrupters of the TUSB73X0. The offset in Table 6-39 is from the Runtime Base, which is the address programmed into the Base Address Register 0 plus the value programmed into the Runtime Register Space Offset (see Section 6.2.8).

Table 6-39. Host Controller Runtime Register Map

Register Name	Offset
Microframe Index	00h
Reserved	04h-1Fh
Interrupter Register Set 0	20h-3Fh
Interrupter Register Set 1	40h-5Fh
Interrupter Register Set 2	60h-7Fh
Interrupter Register Set 3	80h-9Fh
Interrupter Register Set 4	A0h-BFh
Interrupter Register Set 5	C0h-DFh
Interrupter Register Set 6	E0h-FFh
Interrupter Register Set 7	100h-11Fh

6.4.1 Microframe Index Register

This register is used by the system software to determine the current periodic frame. The register value is incremented every 125 microseconds.

Runtime Base register offset:00h

Register type:Read-Only

Default value: 0000 0000h

Table 6-40. HC Runtime Register (Runtime Base + 00h)

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-41. Microframe Index Register Description

Bit	Field Name	Access	Description
31:14	RSVD	r	Reserved. Returns zeros when read.
13:0	MICROFRAME_IDX	r	Microframe Index.

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6.4.2 Interrupter Management Register

The TUSB73X0 implements 8 Interrupter Management Registers, one for each Interrupter implemented.

Runtime Base register offset:20h + (20h*Interrupter), where Interrupter = 0 through 7

Register type:Read-Only,Read/Write

Default value: 0000 0000h

Table 6-42. HC Runtime Register (Runtime Base + 20h + (20h*Interrupter)), where Interrupter = 0 through 7

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-43. Interrupter Management Register Description

Bit	Field Name	Access	Description
31:2	RSVD	r	Reserved. Returns zeros when read.
1	IE	rw	Interrupt Enable.
0	IP	rc	Interrupt Pending.

6.4.3 Interrupter Moderation Register

The TUSB73X0 implements 8 Interrupter Moderation Registers, one for each Interrupter implemented.

Runtime Base register offset:24h + (20h*Interrupter), where Interrupter = 0 through 7

Register type:Read/Write

Default value: 0000 0FA0h

Table 6-44. HC Runtime Register (Runtime Base + 24h + (20h*Interrupter)), where Interrupter = 0 through 7

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0	0

Table 6-45. Interrupter Management Register Description

Bit	Field Name	Access	Description
31:16	IMODC	rw	Interrupt Moderation Counter.
15:0	IMODI	rw	Interrupt Moderation Interval.

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6.4.4 Event Ring Segment Table Size Register

The TUSB73X0 implements 8 Event Ring Segment Table Size Registers, one for each Interrupter implemented.

Runtime Base register offset:28h + (20h*Interrupter), where Interrupter = 0 through 7

Register type:Read-Only,Read/Write

Default value: 0000 0000h

Table 6-46. HC Runtime Register (Runtime Base + 28h + (20h*Interrupter)), where Interrupter = 0 through 7

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-47. Event Ring Segment Table Size Register Description

Bit	Field Name	Access	Description
31:16	RSVD	r	Reserved. Returns zeros when read.
15:0	ERSTS	rw	Event Ring Segment Table Size.

6.4.5 Event Ring Segment Table Base Address Register

The TUSB73X0 implements 8 Event Ring Segment Table Base Address Registers, one for each Interrupter implemented.

Runtime Base register offset:30h + (20h*Interrupter), where Interrupter = 0 through 7

Register type:Read-Only,Read/Write

Default value: 0000 0000 0000 0000h

Table 6-48. HC Runtime Register (Runtime Base + 30h + (20h*Interrupter)), where Interrupter = 0 through 7

Bit No.	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Table 6-49. Event Ring Segment Table Base Address Register Description

Bit	Field Name	Access	Description
63:4	ERST_BASE	rw	Event Ring Segment Table Base Address.
3:0	RSVD	r	Reserved. Returns zeros when read.

6.4.6 Event Ring Dequeue Pointer Register

The TUSB73X0 implements 8 Event Ring Dequeue Pointer Registers, one for each Interrupter implemented.

Runtime Base register offset:38h + (20h*Interrupter), where Interrupter = 0 through 7

Register type:Read/Write, Read/Clear

Default value: 0000 0000 0000 0000h

Table 6-50. HC Runtime Register (Runtime Base + 38h + (20h*Interrupter)), where Interrupter = 0 through 7

Bit No.	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-51. Event Ring Dequeue Pointer Register Description

Bit	Field Name	Access	Description
64:4	ERDP	rw	Event Ring Dequeue Pointer.
3	EHB	rc	Event Handler Busy.
2:0	DESI	rw	Dequeue ERST Segment Index.

6.5 Host Controller Doorbell Registers

The TUSB73X0 supports an array of 65 Doorbell Registers, one for the host controller plus one for each Device Slot supported. The address of the first Doorbell Register is the address programmed into the Base Address Register 0 plus the value programmed into the Doorbell Offset (see Section 6.2.7).

Doorbell Base register offset:00h + (04h*Device Slot), where Device Slot = 0 through 64

Register type:Read-Only, Read/Write

Default value: 0000 0000h

Table 6-52. HC Doorbell Register (Doorbell Base + (04h*Device Slot)), where Device Slot = 0 through 64

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-53. Interrupter Management Register Description

Bit	Field Name	Access	Description
31:16	DB_STREAM_ID	rw	Doorbell Stream ID. This field returns zeros when read.
15:8	RSVD	r	Reserved. Returns zeros when read.
7:0	DB_TARGET	rw	Doorbell Target. This field returns zeros when read.

6.6 xHCI Extended Capabilities Registers

These registers are used for the xHCI Extended Capabilities in the TUSB73X0. The offset in Table 6-54 is from the xHCI Extended Capabilities Base, which is the address programmed into the Base Address Register 0 plus the value programmed into the xHCI Extended Capabilities Pointer field in the Host Controller Capability Parameters (see Section 6.2.6).

Table 6-54. xHCI Extended Capabilities Register Map

Register Name	Offset
Legacy Support Capability	00h-07h
Reserved	08h-0Fh
xHCI Supported Protocol Capability (USB 2.0)	10h-1Bh
Reserved	1Ch-1Fh
xHCI Supported Protocol Capability (USB 3.0)	20h-2Bh

6.6.1 USB Legacy Support Capability Register

This register is used to coordinate the ownership of the host controller between BIOS and the operating system.

xHCI Extended Capabilities Base register offset:00h

Register type:Read-Only, Read/Write

Default value: 0000 0201h

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Table 6-55. xHCI Extended Capabilities Register (xHCI Extended Capabilities Base + 00h)

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1

Table 6-56. USB Legacy Support Capability Register Description

Bit	Field Name	Access	Description
31:25	RSVD	r	Reserved. Returns zeros when read.
24	HC_OS_SEMA	rw	HC OS Owned Semaphore.
23:17	RSVD	r	Reserved. Returns zeros when read.
16	HC_BIOS_SEMA	rw	HC BIOS Owned Semaphore.
15:8	NEXT_CAP	r	Next Capability Pointer. This field is 04h, indicating that the xHCI Supported Protocol Capability for USB 2.0 starts at offset 10h from the xHCI Extended Capabilities Base.
7:0	CAPABILITY_ID	r	Capability ID. This field is 01h, identifying this capability as a USB Legacy Support Capability.

6.6.2 USB Legacy Support Control/Status Register

This register is used by BIOS software to enable System Management Interrupts.

xHCI Extended Capabilities Base register offset:04h

Register type:Read-Only, Read/Clear

Default value: 0000 0000h

Table 6-57. xHCI Extended Capabilities Register (xHCI Extended Capabilities Base + 04h)

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-58. USB Legacy Support Control/Status Register Description

Bit	Field Name	Access	Description
31	SMI_BAR	rc	SMI on BAR.
30	SMI_PCI_COM	rc	SMI on PCI Command.
29	SMI_OS_CHANGE	rc	SMI on OS Ownership Change.
28:21	RSVD	r	Reserved. Returns zeros when read.
20	SMI_HOST_SYS_ERR	r	SMI on Host System Error.
19:17	RSVD	r	Reserved. Returns zeros when read.
16	SMI_EVENT_INT	r	SMI on Event Interrupt.
15	SMI_BAR_EN	rw	SMI on BAR Enable.
14	SMI_PCI_COM_EN	rw	SMI on PCI Command Enable.

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Table 6-58. USB Legacy Support Control/Status Register Description (continued)

13	SMI_OS_EN	rw	SMI on OS Ownership Enable.
12:5	RSVD	r	Reserved. Returns zeros when read.
4	SMI_HOST_SYS_ERR_EN	rw	SMI on Host System Error Enable.
3:1	RSVD	r	Reserved. Returns zeros when read.
0	USB_SMI_EN	rw	USB SMI Enable.

6.6.3 xHCI Supported Protocol Capability Register (USB 2.0)

This register indicates that the Supported Protocol Capability is for USB 2.0.

xHCI Extended Capabilities Base register offset:10h

Register type:Read-Only

Default value: 0200 0402h

Table 6-59. xHCI Extended Capabilities Register (xHCI Extended Capabilities Base + 10h)

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0

Table 6-60. xHCI Supported Protocol Capability Register (USB 2.0) Description

Bit	Field Name	Access	Description
31:24	MAJOR_REV	r	Major Revision. This field is 02h, since this Supported Protocol Capability is for release 2.0 of the USB specification.
23:16	MINOR_REV	r	Minor Revision. This field is 00h, since this Supported Protocol Capability is for release 2.0 of the USB specification.
15:8	NEXT_CAP	r	Next Capability Pointer. This field is 04h, indicating that the xHCI Supported Protocol Capability for USB 3.0 starts at offset 20h from the xHCI Extended Capabilities Base.
7:0	CAPABILITY_ID	r	Capability ID. This field is 02h, identifying this capability as a Supported Protocol Capability.

6.6.4 xHCI Supported Protocol Name String Register (USB 2.0)

This read only register is set to 2042 5355h, indicating that the Supported Protocol Capability is for USB 2.0.

xHCI Extended Capabilities Base register offset:14h

Register type:Read-Only

Default value: 2042 5355h

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Table 6-61. xHCI Extended Capabilities Register (xHCI Extended Capabilities Base + 14h)

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	1	0	0	0	0	0	0	1	0	0	0	0	1	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	1	0	1	0	0	1	1	0	1	0	1	0	1	0	1

6.6.5 xHCI Supported Protocol Port Register (USB 2.0)

This register indicates how many USB 2.0 ports are supported and what their port numbers are.

xHCI Extended Capabilities Base register offset:18h

Register type:Read-Only

Default value: 0001 0X01h

Table 6-62. xHCI Extended Capabilities Register (xHCI Extended Capabilities Base + 18h)

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	x	x	0	0	0	0	0	0	0	0	1

Table 6-63. xHCI Supported Protocol Capability Register (USB 2.0) Description

Bit	Field Name	Access	Description
31:19	RSVD	r	Reserved. Returns zeros when read.
18	IHI	r	Integrated Hub Implemented. This field is ‘0’ to indicate that the root hub to external port mapping adheres to the default mapping in the xHCI Specification.
17	HSO	r	High-speed Only. This field is ‘0’ to indicate that the USB 2.0 ports are Low-, Full-, and High-speed capable.
16	L1C	r	L1 Capability. This field is ‘1’ to indicate that the TUSB73X0 supports the USB 2.0 Link Power Management L1 state.
15:8	COMPATIBLE_PORT_CNT	r	Compatible Port Count. For the TUSB7340 , this field is 04h to indicate that four USB 2.0 ports are supported. For the TUSB7320, this field is 02h to indicate that two USB 2.0 ports are supported.
7:0	COMPATIBLE_PORT_OFF	r	Compatible Port Offset. This field is 01h to indicate that the first USB 2.0 port is port 1.

6.6.6 xHCI Supported Protocol Capability Register (USB 3.0)

This register indicates that the Supported Protocol Capability is for USB 3.0.

xHCI Extended Capabilities Base register offset:20h

Register type:Read-Only

Default value: 0300 0002h

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Table 6-64. xHCI Extended Capabilities Register (xHCI Extended Capabilities Base + 20h)

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Table 6-65. xHCI Supported Protocol Capability Register (USB 3.0) Description

Bit	Field Name	Access	Description
31:24	MAJOR_REV	r	Major Revision. This field is 03h, since this Supported Protocol Capability is for release 3.0 of the USB specification.
23:16	MINOR_REV	r	Minor Revision. This field is 00h, since this Supported Protocol Capability is for release 3.0 of the USB specification.
15:8	NEXT_CAP	r	Next Capability Pointer. This field is 00h, indicating that this is the last capability.
7:0	CAPABILITY_ID	r	Capability ID. This field is 02h, identifying this capability as a Supported Protocol Capability.

6.6.7 xHCI Supported Protocol Name String Register (USB 3.0)

This read only register is set to 2042 5355h, indicating that the Supported Protocol Capability is for USB 3.0.

xHCI Extended Capabilities Base register offset:24h

Register type:Read-Only

Default value: 2042 5355h

Table 6-66. xHCI Extended Capabilities Register (xHCI Extended Capabilities Base + 24h)

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	1	0	0	0	0	0	0	1	0	0	0	0	1	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	1	0	1	0	0	1	1	0	1	0	1	0	1	0	1

6.6.8 xHCI Supported Protocol Port Register (USB 3.0)

This register indicates how many USB 3.0 ports are supported and what their port numbers are.

xHCI Extended Capabilities Base register offset:28h

Register type:Read-Only

Default value: 0000 0X0Xh

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Table 6-67. xHCI Extended Capabilities Register (xHCI Extended Capabilities Base + 28h)

Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reset State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	x	x	0	0	0	0	0	0	x	x	1

Table 6-68. xHCI Supported Protocol Capability Register (USB 3.0) Description

Bit	Field Name	Access	Description
31:19	RSVD	r	Reserved. Returns zeros when read.
18	IHI	r	Integrated Hub Implemented. This field is ‘0’ to indicate that the root hub to external port mapping adheres to the default mapping in the xHCI Specification.
17	HSO	r	High-speed Only. This field is not applicable to USB 3.0 and is ‘0’.
16	L1C	r	L1 Capability. This field is not applicable to USB 3.0 and is ‘0’.
15:8	COMPATIBLE_PORT_CNT	r	Compatible Port Count. For the TUSB7340 , this field is 04h to indicate that four USB 3.0 ports are supported. For the TUSB7320, this field is 02h to indicate that two USB 3.0 ports are supported.
7:0	COMPATIBLE_PORT_OFF	r	Compatible Port Offset. For the TUSB7340 , this field is 05h to indicate that the first USB 3.0 port is port 5. For the TUSB7320, this field is 03h to indicate that the first USB 3.0 port is port 3.

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7 MSI-X MEMORY MAPPED REGISTER SPACE

7.1 The MSI-X Table and PBA in Memory Mapped Register Space

The TUSB73X0 includes the MSI-X Table and PBA in memory mapped register space. These registers are accessible via the address programmed into the Base Address Register 2/3.

Table 7-1. MSI-X Table and PBA Register Map

Register Name	Offset
Entry 0 Message Address	0000h
Entry 0 Message Upper Address	0004h
Entry 0 Message Data	0008h
Entry 0 Vector Control	000Ch
Entry 1 Message Address	0010h
Entry 1 Message Upper Address	0014h
Entry 1 Message Data	0018h
Entry 1 Vector Control	001Ch
Entry 2 Message Address	0020h
Entry 2 Message Upper Address	0024h
Entry 2 Message Data	0028h
Entry 2 Vector Control	002Ch
Entry 3 Message Address	0030h
Entry 3 Message Upper Address	0034h
Entry 3 Message Data	0038h
Entry 3 Vector Control	003Ch
Entry 4 Message Address	0040h
Entry 4 Message Upper Address	0044h
Entry 4 Message Data	0048h
Entry 4 Vector Control	004Ch
Entry 5 Message Address	0050h
Entry 5 Message Upper Address	0054h
Entry 5 Message Data	0058h
Entry 5 Vector Control	005Ch
Entry 6 Message Address	0060h
Entry 6 Message Upper Address	0064h
Entry 6 Message Data	0068h
Entry 6 Vector Control	006Ch
Entry 7 Message Address	0070h
Entry 7 Message Upper Address	0074h
Entry 7 Message Data	0078h
Entry 7 Vector Control	007Ch
Reserved	0080h-0FFFh
Pending Bits 7 through 0	1000h
Reserved	1001h-1FFFh

Refer to the PCI Local Bus Specification, Revision 3.0 for descriptions of these registers.

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8 PHY CONTROL

8.1 Output Voltage Swing Control

The output swing of each transmitter can be independently set to one of a number of settings via the SWING bits in the De-Emphasis and Swing Control Register, see Section 4.65.

Reducing the output amplitude decreases the current drawn in direct proportion to the reduction in swing, thereby saving power.

Table 8-1. Differential Output Swing

Swing Value	AC-Coupled Amplitude
0000	2.7
0001	147
0010	222
0011	298
0100	373
0101	449
0110	525
0111	600
1000	702
1001	777
1010	853
1011	928
1100	1050
1101	1082
1110	1164
1111	1253

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8.2 De-Emphasis Control

De-emphasis provides a means to compensate for high frequency attenuation in the attached media. It causes the output amplitude to be smaller for bits which are not preceded by a transition than for bits which are. Fifteen different de-emphasis settings are provided via the PORTx_DE bits in the De-Emphasis and Swing Control Register, see Section 4.65.

Table 8-2. Differential Output De-Emphasis

Value	Amplitude Reduction	
	%	dB
0000	0	0
0001	5.33	-0.48
0010	9.52	-0.87
0011	13.8	-1.29
0100	18.1	-1.73
0101	22.5	-2.21
0110	27.0	-2.73
0111	31.4	-3.28
1000	36.2	-3.9
1001	40.8	-4.55
1010	45.4	-5.26
1011	50.2	-6.05
1100	55.0	-6.93
1101	59.7	-7.90
1110	64.5	-8.99
1111	69.3	-10.27

8.3 Adaptive Equalizer

All receive channels in this macro family incorporate an adaptive equalizer, which can compensate for channel insertion loss by attenuating the low frequency components with respect to the high frequency components of the signal, thereby reducing inter-symbol interference.

The equalizer can be configured via the Portx_EQ bits of the Equalizer Control Register, Section 4.66. Table 8-3 summarizes the options, which are:

- *No adaptive equalization*. The equalizer provides a flat response at the maximum gain. This setting may be appropriate if jitter at the receiver occurs predominantly as a result of crosstalk rather than frequency dependent loss.
- *Fully adaptive equalization*. Both the low frequency gain and zero position of the equalizer are determined algorithmically by analyzing the data patterns and transition positions in the received data. FTC refers to the algorithm that controls the zero position. In the FTC normal mode, the zero is decreased in frequency when more equalization is needed; in the FTC reversed mode, the zero is increased in frequency when more equalization is needed. The fully adaptive with FTC reversed setting should be used for most applications.
- *Hold*. The equalizer state is held at its current gain level and zero point.
- *Initialize*. The equalizer is initialized to a mid-point gain level, with the zero set to a frequency appropriate for the receiver data rate.
- *Partially adaptive equalization*. The low frequency gain of the equalizer is determined algorithmically by analyzing the data patterns and transition positions in the received data. The zero position is fixed in one of eight zero positions. For any given application, the optimal setting is a function of the loss characteristics of the channel and the spectral density of the signal as well as the data rate, which means it is not possible to identify the best setting by data rate alone, although generally speaking, the lower the line rate, the lower the zero frequency that will be required.

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When enabled, the receiver equalization logic analyzes data patterns and transition times to determine whether the low frequency gain of the equalizer should be increased or decreased. For the fully adaptive setting (***EQ*** = 0001), if the low frequency gain reaches the minimum value, the zero frequency is then reduced. Likewise, if it reaches the maximum value, the zero frequency is then increased.

The decision logic is implemented as a voting algorithm with a relatively long analysis interval. The slow time constant that results reduces the probability of incorrect decisions but allows the equalizer to compensate for the relatively stable response of the channel.

Table 8-3. Receiver Equalizer Configuration

EQ Value	Amplitude Reduction	
	Low Frequency Gain	Zero Frequency
0000	Maximum	-
0001	Fully Adaptive, FTC Normal	
0010	Fully Adaptive, FTC Reversed	
0011	Hold	
0100	Initialize	
0101		
0110		
0111		
1000	Partially Adaptive	365 MHz
1001		275 MHz
1010		195 MHz
1011		140 MHz
1100		105 MHz
1101		75 MHz
1110		55 MHz
1111		50 MHz

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9 INPUT CLOCK

9.1 Clock Source Requirements

The TUSB73x0 supports an external oscillator source or a crystal unit. The frequency of the clock source may be 20 MHz – 50 MHz. The FREQSEL pin is used to indicate the oscillator input frequency. If the FREQSEL pin is pulled low, the oscillator input frequency is 48 MHz. If the FREQSEL pin is pulled high, the value in the PLL_FREQ_SEL field controls the selected frequency. After the PLL_FREQ_SEL field is set appropriately the FREQ_SEL_EN bit should be set. When the FREQ_SEL_EN bit is set high, the oscillator is restarted with the PLL multiplier value and the oscillator frequency controls set according to the value specified in the PLL_FREQ_SEL field. The register values may be programmed via EEPROM or PCI Express access; refer to Table 4-100. If a clock is provided to XI instead of a crystal, XO is left open and VSSOSC should be connected to the PCB ground plane. Otherwise, if a crystal is used, the connection needs to follow the guidelines below.

Since XI and XO are coupled to other leads and supplies on the PCB, it is important to keep them as short as possible and away from any switching leads. It is also recommended to minimize the capacitance between XI and XO. This can be accomplished by connecting the VSSOSC lead to the two external capacitors CL1 and CL2 and shielding them with the clean ground lines. The VSSOSC should not be connected to PCB ground when using a crystal.

Load capacitance (Cload) of the crystal varying with the crystal vendors is the total capacitance value of the entire oscillation circuit system as seen from the crystal. It includes two external capacitors CL1 and CL2.

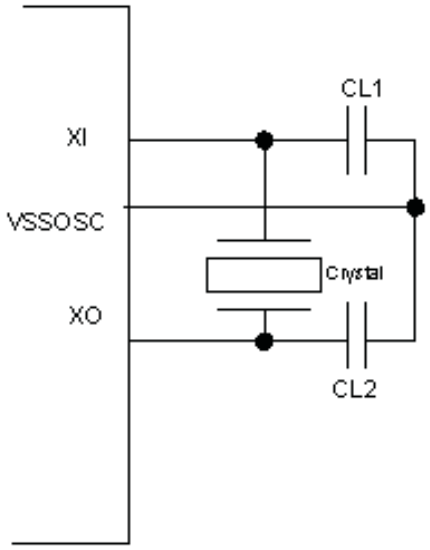

Figure 9-1. Oscillation Circuit

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9.2 External clock

When using an external clock source, the reference clock should have a ±100 PPM or better frequency stability and have less than 50-ps absolute peak to peak jitter or less than 25-ps peak to peak jitter after applying the USB 3.0 jitter transfer function. XI should be tied to the clock source and XO should be left floating. The input clock must be 1.8-V LVCMOS; this input is not 3.3-V tolerant. When AUX_DET is high and the TUSB73x0 is in D3cold the TUSB73x0 utilizes an internal ring oscillator to support wake from D3cold eliminating the need to keep the external clock active while in D3cold.

Table 9-1. Input Clock Specification

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Frequency Tolerance	Operational Temperature			±50	ppm
Frequency Stability	1 year aging			±100	ppm
Rise / Fall Time	20% - 80%			6	ns
Reference Clock R_J with JTF (1 sigma) (1)(2)			0.8		ps
Reference Clock T_J with JTF (total p-p) (2)(3)			25		ps
Reference Clock Jitter (absolute p-p) (4)			50		ps

(1) Sigma value assuming Gaussian distribution.
(2) After application of JTF.
(3) Calculated as 14.1 x R_J+D_J
(4) Absolute phase jitter (p-p)

Table 9-2. Input Clock 1.8-V DC Characteristics

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
VIH	High-level input voltage	0.65 V_{DDS}			V
VIL	Low-level input voltage			0.35 V_{DDS}	V
VOH	I_O = -2 mA, V_{DDS} = 1.62 to 1.98 V, driver enabled, pullup or pulldown disabled	V_{DDS}-0.45			V
	I_O = -2 mA, V_{DDS} = 1.4 to 1.6 V, driver enabled, pullup or pulldown disabled	0.75 V_{DDS}			
VOL	I_O = 2 mA, driver enabled, V_{DDS} = 1.62 to 1.98 V, pullup or pulldown disabled			0.45	V
	I_O = 2 mA, V_{DDS} = 1.4 to 1.6 V, driver enabled, pullup or pulldown disabled			0.25 V_{DDS}	

9.3 External crystal

An external 1-MΩ feedback resistor is required between XI and XO when using a crystal. See the table below for additional crystal specifications.

Table 9-3. Crystal Specification

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Frequency Tolerance	Operational Temperature			±50	ppm
Frequency Stability	1 year aging			±100	ppm
Load Capacitance		12		24	pF
ESR				50	Ω

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10 PCI EXPRESS POWER MANAGEMENT

10.1 Power Management

PCI power management (PM) features include active-state link PM, PME mechanisms, and all conventional PCI D states. If the active-state link PM is enabled, the link automatically saves power when idle using the L0s and L1 states.

10.2 PCI Express Link Power Management States

PCI Express defines Link power management states, replacing the bus power management states that were defined by the *PCI Bus Power Management Interface Specification*. Link states are not visible to PCI-PM legacy compatible software, and are either derived from the power management D-states of the corresponding components connected to that Link or by ASPM protocols.

Table 10-1. PCI Express Link Power Management States

Link States	Description
L0	Active state. All PCI Express transactions and other operations are enabled.
L0s	A low resume latency, energy saving "standby" state.
L1	Higher latency, lower power "standby" state.
L2	Auxiliary-powered Link, deep-energy-saving state.
L3	Link Off state. When no power is present, the component is in the L3 state.

Link States	Description	PM SW Directed	Ref Clk	Vaux
L0	Fully active	Yes (D0)	On	On/Off
L0s	Standby	No	On	On/Off
L1	Low power standby	Yes (D1-D3hot)	On	On/Off
L2/L3 Ready	Staging for power removal	Yes	On	On/Off
L2	Low power sleep	Yes	Off	On
L3	No power	N/A	Off	Off

10.3 PCI Express Power Management D-States

PCI Express supports all PCI-PM device power management states. The TUSB73x0 supports the D0, D1, D2, and D3 states (both D3hot and D3cold).

Table 10-2. PCI Express Power Management D-States

Power Management States	Description
D0	Normal operation state. The device is completely active and responsive in this state. The link may be L0 or L0s.
D1	Light sleep state. I Configuration and message requests are accepted. Intermediate state intended to provide some power savings but yields a quicker restore time. The link state is L1.
D2	Deep sleep state. Configuration and message requests are accepted. Intermediate state intended to provide some power savings but yields a quicker restore time. The link state is L1.
D3hot	Disabled State. Configuration and message requests are accepted. Link state should be L1, PERST# is deasserted, and reference clock active depending on state of CLKREQ#.
D3cold	Power-off state. Link state should be L2. PERST# is active and no reference clock is present.

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10.4 Power Management Event (PME)

Power Management Events are generated by Functions as a means of requesting a PM state change. Power Management Events are typically utilized to revive the system or an individual Function from a low power state.

Before using any wakeup mechanism, a Function must be enabled by software to do so by setting the PME_EN bit in the PMCSR, see Section 4.25. The PME_Status bit is sticky, and the value of the PME_Status bit is maintained through reset if aux power is available and the device is enabled for wakeup events.

10.4.1 PME Support

The 5-bit PME_support field in the PMC (Power Management Capabilities) register, Section 4.24, indicates the power states in which the TUSB73X0 may send a PME Message. A value of 0b for any bit indicates that it is not capable of sending PME Message while in that power state. Note that the default value of the Bit15 of the PME_support for D3cold is "HwInit" and depends on the AUX_DET pin strapping. If the AUX_DET is pulled high, bit 15 set to 1b.

Table 10-3. PME Support

Pin Name	Support Wake from D3cold/D3hot	Support Wake from D3hot only
3.3V 1.1V	Power rails must be maintained to support D3cold and D3hot states.	Power rails must be maintained to support D3hot states, but may be removed for D3cold.
AUX_DET	Pulled high.When AUXDET is pulled high, bit 15 of the Power Management Capabilities register is set to 1b.	Pulled low. When AUXDET is pulled low, bit 15 of the Power Management Capabilities register is cleared, or 0b.
GRST#	Must not be asserted during D3cold and D3hot states for WAKE# to function correctly. Should be asserted if power rails fall below specified operating conditions.	Must not be asserted during D3hot state, but should assert if power rails fall below specified operating conditions.
WAKE#	Connected to WAKE# of the system chipset and is pulled high on the system board. WAKE# is used for wakeup from D3cold. In band PME message is used for wakeup from D3hot.	WAKE# is not used. In band PME message is used for wakeup from D3hot.
CLKREQ#	Connected to CLKREQ# of the system chipset and is pulled high.	Connected to CLKREQ# of the system chipset and is pulled high.
OVERCUR(X:1)#	Must remain pulled high during D3cold and D3hot states. Should not be pulled high if power is removed.	Must remain pulled high during D3hot state. Should not be pulled high if power is removed.

If an EEPROM is used for configuration, power should also be maintained during D3cold and D3hot states.

The assertion of PERST# transitions the TUSB7340 from D3hot to D3cold. PERST# must be asserted if the power rails fall below the specified operation conditions.

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11 ELECTRICAL CHARACTERISTICS

See the PCIe and USB specifications refered to in Section 2.2 for the electrical characteristics of those interfaces.

11.1 ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
VDD33	Supply voltage range		-0.5 to 3.6	V
VDDA_3P3			-0.5 to 3.6	V
VDD11			-0.3 to 1.4	V
V_I	Input voltage range	PCI Express (RX)	0 to 1.2	V
		PCI Express REFCLK (single-ended)	-0.5 to VDD33 + 0.5	V
		REFCLK (differential)	-0.3 to 1.15	V
		Miscellaneous 3.3 V IO	-0.5 to VDD33 + 0.5	V
V_O	Output voltage range	PCI Express (TX)	0.8 to 1.2	V
		Miscellaneous 3.3 V IO	-0.5 to VDD33 + 0.5	V
V_{ESD}	HBM Human-Body ESD Rating	R = 1.5 kΩ, C = 100 pF	2000	V
	Charged-Device Model ESD Rating		500	
T_{stg}	Storage temperature range		-65 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

11.2 RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD33	Supply voltage range	3	3.3	3.6	V
VDDA_3P3		3	3.3	3.6	
VDD11(1)		0.99	1.1	1.21	V
T_A	Operating free-air temperature range	0		70	°C
T_J	Operating junction temperature range	-40		105	°C

(1) A 1.05-V supply may be used as long as minimum supply conditions are met.

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11.3 THERMAL INFORMATION

THERMAL METRIC		RKM	UNITS
		100 PINS	
θ_{JA}	Junction-to-ambient thermal resistance(1)	25.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(2)	9.5	
θ_{JB}	Junction-to-board thermal resistance(3)	15.2	
ψ_{JT}	Junction-to-top characterization parameter(4)	0.1	
ψ_{JB}	Junction-to-board characterization parameter(5)	7.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(6)	0.4	

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(5) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

11.4 3.3-V I/O ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		OPERATION	TEST CONDITIONS	MIN	MAX	UNIT
V_{IH}	High-level input voltage(1)	VDD33		2	VDD33	V
V_{IL}	Low-level input voltage(1)	VDD33		0	0.8	V
			JTAG pins only	0	0.55	
V_I	Input voltage			0	VDD33	V
V_O	Output voltage(2)			0	VDD33	V
t_t	Input transition time (t_{rise} and t_{fall})			0	25	ns
V_{hys}	Input hysteresis(3)				0.13 VDD33	V
V_{OH}	High-level output voltage	VDD33	I_{OH} = -4 mA	2.4		V
V_{OL}	Low-level output voltage	VDD33	I_{OL} = 4 mA		0.4	V
I_{OZ}	High-impedance, output current(2)	VDD33	V_I = 0 to VDD33		±20	µA
I_{OZP}	High-impedance, output current with internal pullup or pulldown resistor(4)	VDD33	V_I = 0 to VDD33		±225	µA
I_I	Input current(5)	VDD33	V_I = 0 to VDD33		±15	µA

(1) Applies to external inputs and bidirectional buffers.
(2) Applies to external outputs and bidirectional buffers.
(3) Applies to PERST, GRST, and PME.
(4) Applies to GRST (pullup) and most GPIO (pullup).
(5) Applies to external input buffers.

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11.5 POWER CONSUMPTION FOR TUSB7320 (1) (2)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		VDD11	VDD33	UNIT
P_{2SS}	2 Devices connected SuperSpeed transfer	507	112	mA
P_{1SS}	1 Device connected SuperSpeed transfer	392	112	mA
P_{D0}	PCI D0 – No device connnected	156	40	mA
P_{D3}	PCI D3 – No device connnected	56	3.5	mA

(1) All 1.1-V power rails connected together.
(2) All 3.3-V power rails connected together.

11.6 POWER CONSUMPTION FOR TUSB7340 (1) (2)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		VDD11	VDD33	UNIT
P_{4SS}	4 Devices connected SuperSpeed transfer	880	115	mA
P_{3SS}	3 Devices connected SuperSpeed transfer	740	115	mA
P_{2SS}	2 Devices connected SuperSpeed transfer	597	115	mA
P_{1SS}	1 Device connected SuperSpeed transfer	420	115	mA
P_{D0}	PCI D0 – No device connnected	168	42	mA
P_{D3}	PCI D3 – No device connnected	63	13.2	mA

(1) All 1.1-V power rails connected together.
(2) All 3.3-V power rails connected together.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TUSB7320RKMR	ACTIVE	WQFN	RKM	100	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TUSB7320RKMT	ACTIVE	WQFN	RKM	100	250	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	
TUSB7340RKMR	ACTIVE	WQFN	RKM	100	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TUSB7340RKMT	ACTIVE	WQFN	RKM	100	250	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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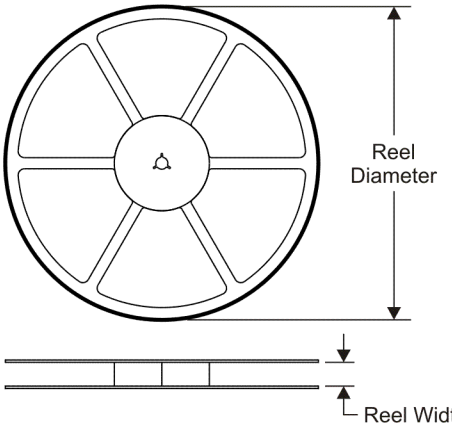
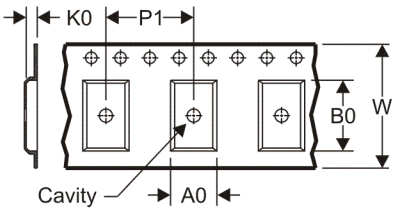
TAPE AND REEL INFORMATION

REEL DIMENSIONS

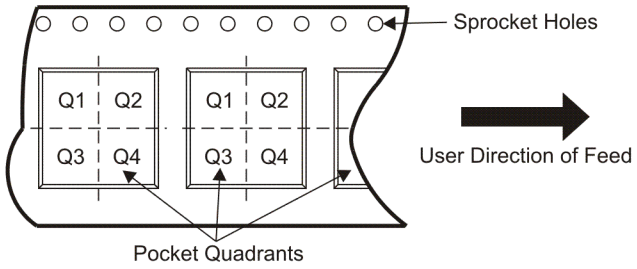


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

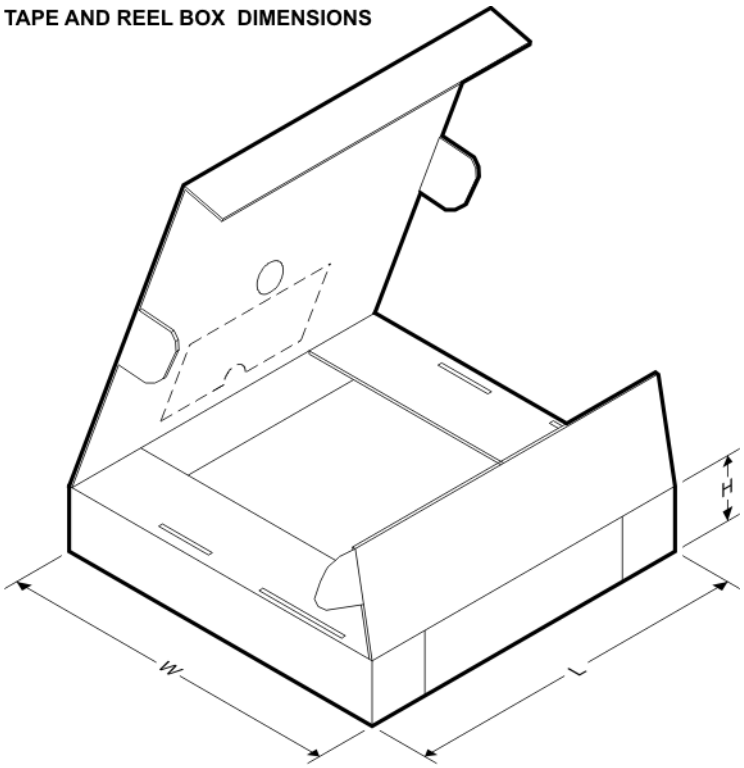
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB7320RKMR	WQFN	RKM	100	3000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
TUSB7320RKMT	WQFN	RKM	100	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
TUSB7340RKMR	WQFN	RKM	100	3000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
TUSB7340RKMT	WQFN	RKM	100	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2

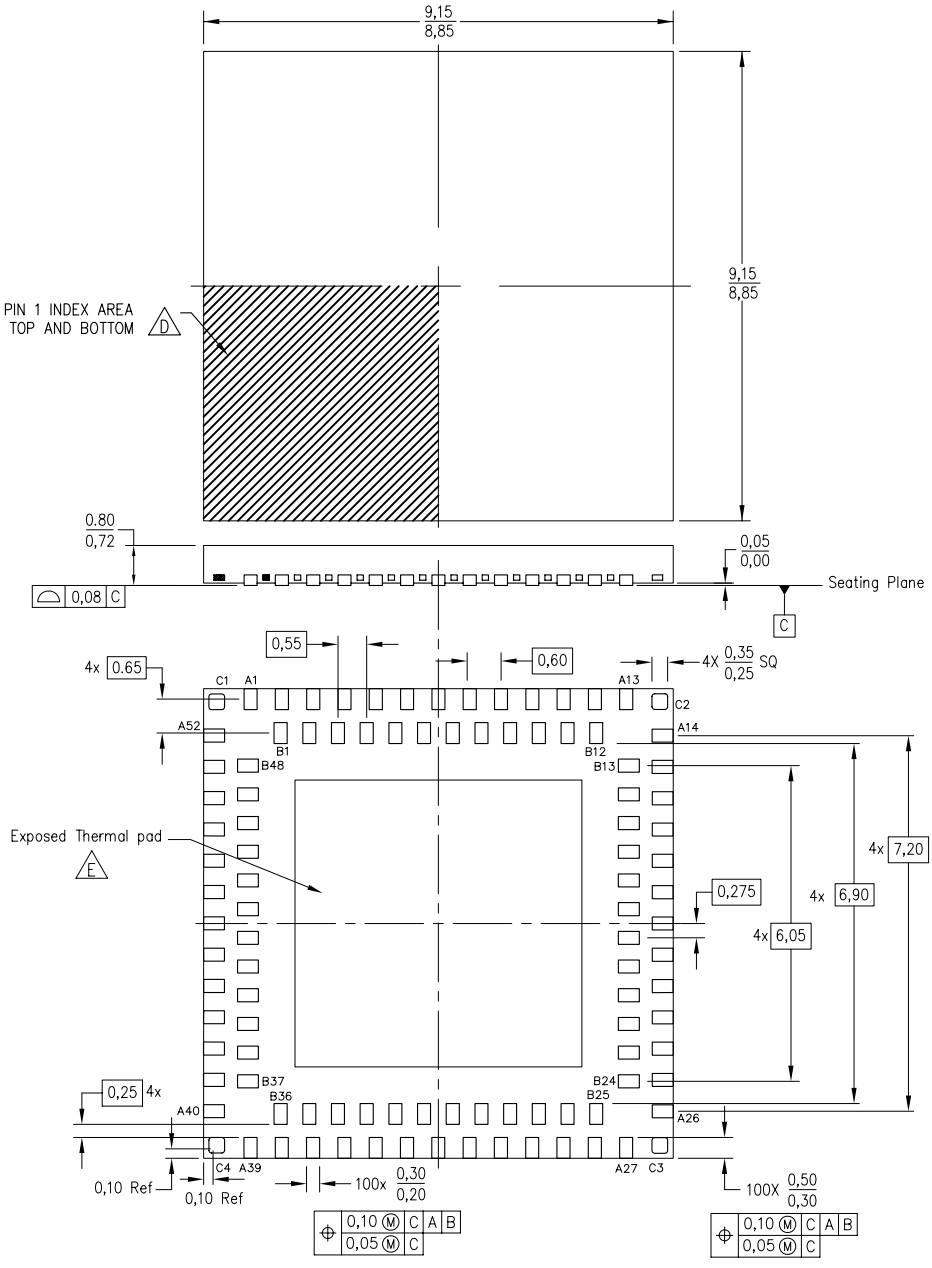
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB7320RKMR	WQFN	RKM	100	3000	346.0	346.0	33.0
TUSB7320RKMT	WQFN	RKM	100	250	190.5	212.7	31.8
TUSB7340RKMR	WQFN	RKM	100	3000	346.0	346.0	33.0
TUSB7340RKMT	WQFN	RKM	100	250	190.5	212.7	31.8

RKM (S–PWQFN–N100) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) staggered multi–row package configuration.
D. Pin A1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin A1 identifiers are either a molded, marked, or metal feature.
E. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

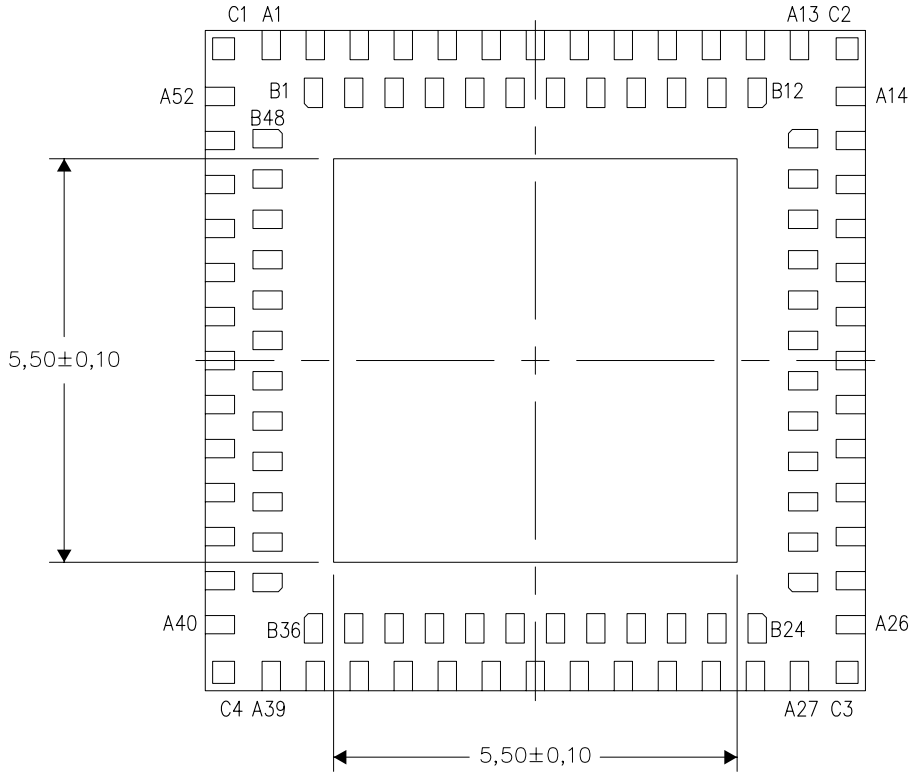
RKM (S–PWQFN–N100) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



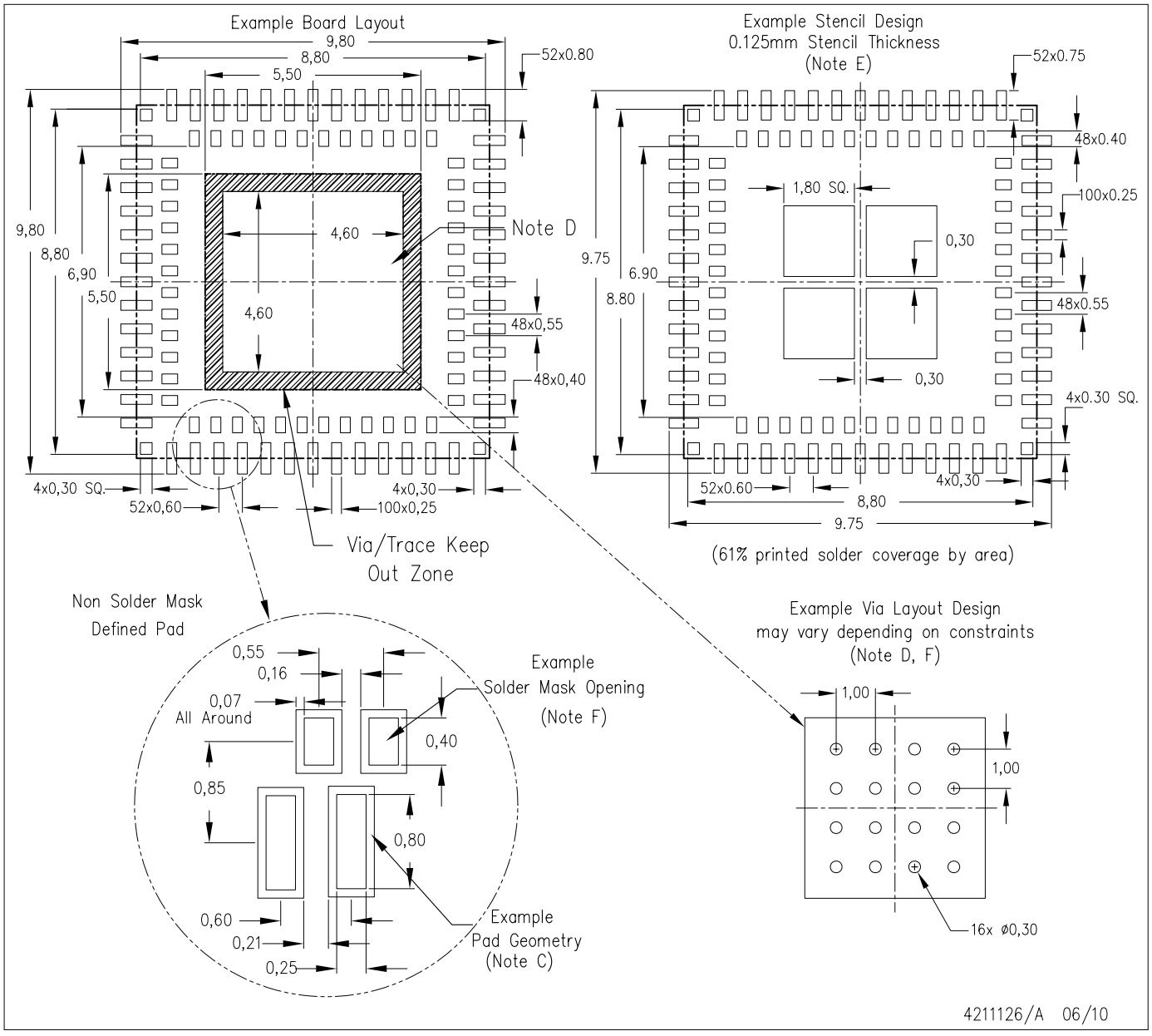
Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

4211101/B 06/10

RKM (S–PWQFN–N100) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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