

Preliminary User's Manual

IE-78K0-NS-P04

IE-780828-NS-EM4

**Emulation Board and Probe Board
for IE-78K0-NS-A**

**Target device
μPD780828B(A) Subseries**



This equipment complies with the EMC protection requirements.

Warning

This is a 'Class A' (EN 55022: 1994) equipment. This equipment can cause radio frequency noise when used in the residential area. In such cases, the user/operator of the equipment may be required to take appropriate countermeasures under his responsibility.

Caution

This equipment should be handled like a CMOS semiconductor device. The user must take all precautions to avoid build-up of static electricity while working with this equipment. All test and measurement tools including the workbench must be grounded. The user/operator must be grounded using the wrist strap. The In-Circuit Emulator probe target connector plug and/or its adapter pins should not be touched with bare hands.

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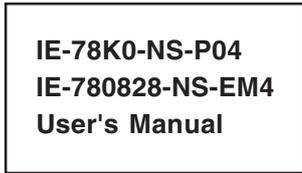
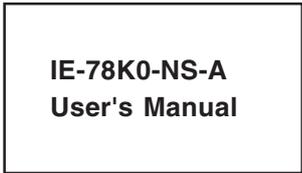
Introduction

Product Overview The IE-78K0-NS-P04 and the IE-780828-NS-EM4, when combined with the IE-78K0-NS-A, are used to debug the following target devices that belong to the 78K/0 Series of 8-bit single-chip microcontrollers.

- μ PD780828B(A) Subseries

Target Readers This manual is intended for engineers who will use the IE-78K0-NS-P04 and the IE-780828-NS-EM4 with the IE-78K0-NS-A to perform system debugging. Engineers who use this manual are expected to be thoroughly familiar with the target device's functions and use methods and to be knowledgeable about debugging.

Organization When using the IE-78K0-NS-P04 and the IE-780828-NS-EM4, refer not only to this manual (supplied with the IE-780828-NS-EM4) but also the manual that is supplied with the IE-78K0-NS-A.



- Basic specifications
- System configuration
- Part names
- External interface functions

- General
- Parts names
- Installation
- Differences between target devices and target interface circuits

Purpose This manual's purpose is to explain various debugging functions that can be performed when using the IE-78K0-NS-P04 and the IE-780828-NS-EM4.

Terminology

The meanings of certain terms used in this manual are listed below.

Term	Meaning
Emulation device	This is a general term that refers to the device in the emulator that is used to emulate the target device. It includes the emulation CPU.
Emulation CPU	This is the CPU block in the emulator that is used to execute user-generated programs.
Target device	This is a device (a μ PD780828B(A) Subseries chip) that is the target for emulation.
Target system	This includes the target program and the hardware provided by the user. When defined narrowly, it includes only the hardware.
IE system	This refers to the combination of the IE-78K0-NS-A, the IE-78K0-NS-P04 and the IE-780828-NS-EM4.

Conventions

Data significance weight : Higher digits on the left and lower digits on the right

Note : Footnote for item marked with **Note** in the text.

Caution : Information requiring particular attention

Remark : Supplementary information

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Document Name	Document Number	
	English	Japanese
IE-78K0-NS-A	To be prepared	To be prepared
IE-78K0-NS-P04, IE-780828-NS-EM4.	This manual	To be prepared
ID78K0-NS Integrated Debugger Reference Windows Based	U12900E	U12900J

Caution: The documents listed above are subject to change without notice. Be sure to use the latest documents when designing.

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[MEMO]

Chapter 1 General

The IE-78K0-NS-P04 and the IE-780828-NS-EM4 are development tools for efficient debugging of hardware or software when using one of the following target devices that belong to the 78K/0 Series of 8-bit single-chip microcontrollers.

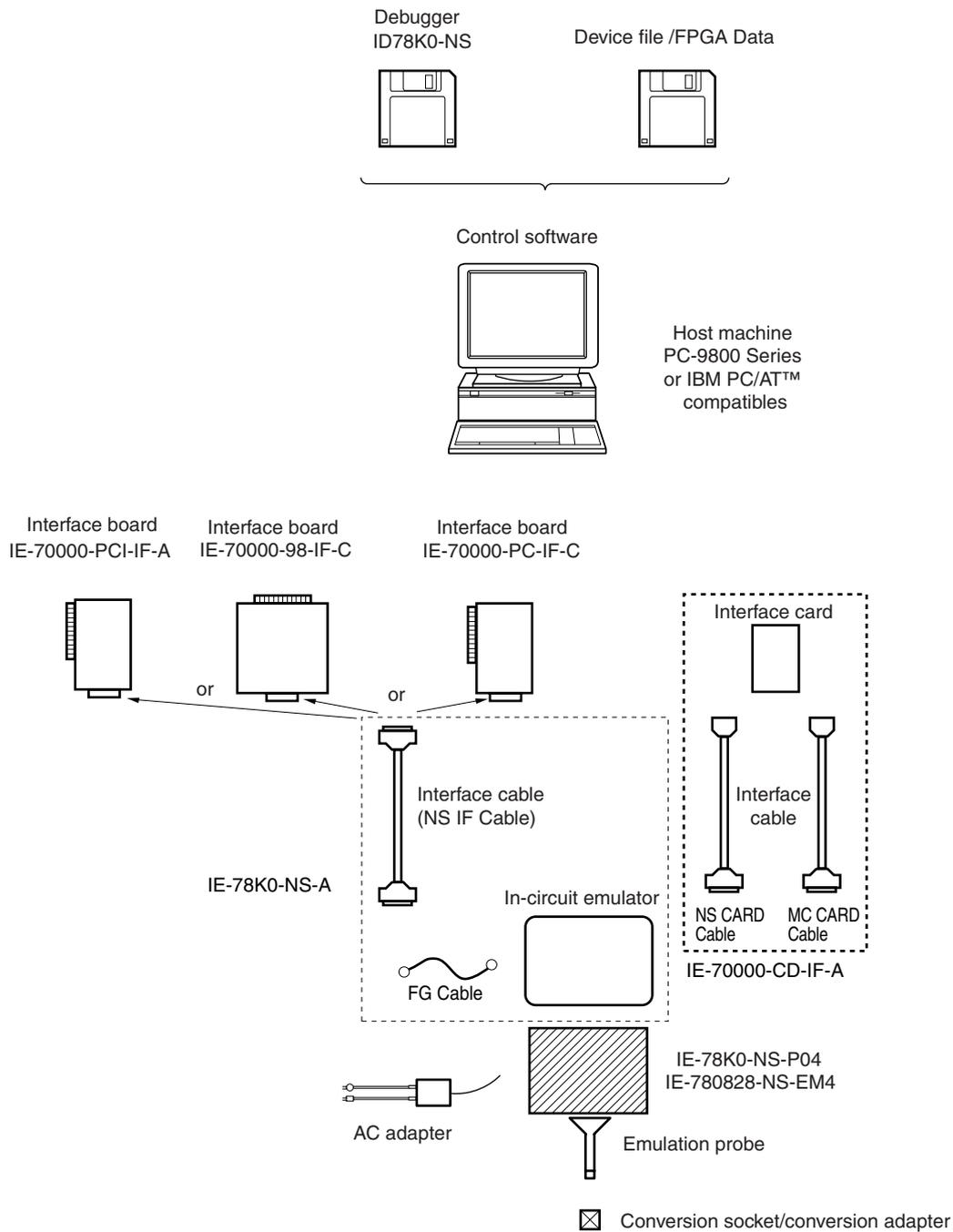
This chapter describes the emulation board's and probe board's system configuration and basic specifications.

- Target device
 - μ PD780828B(A) Subseries

1.1 System Configuration

Figure 1-1 illustrates the IE-78K0-NS-P04 / IE-780828-NS-EM4's system configuration.

Figure 1-1: System Configuration



Note: The packages, emulation probes, and conversion sockets/conversion adapters are listed below.

Package	Emulation Probe	Conversion Socket/ Conversion Adapter
80-pin plastic QFP (GC-8BT - type)	NP-80GC-TQ	NQPACK080SB YQPACK080SB HQPACK080SB YQSOCKET080SBF

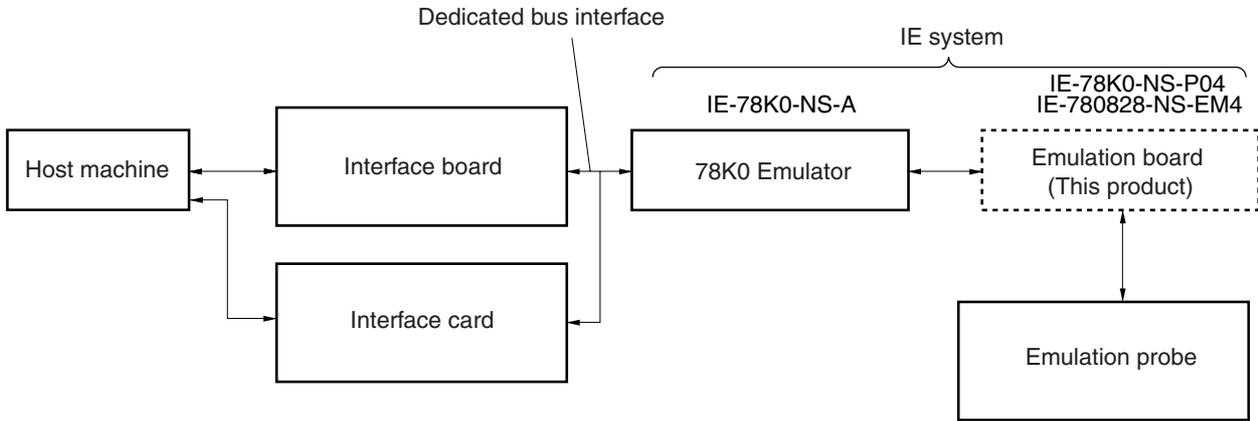
The NP-80GC-TQ is a product of Naito Densai Machidaseisakusho Co., Ltd.

The sockets are products of TOKYO ELETECH CORPORATION.

1.2 Hardware Configuration

Figure 1-2 shows the IE-78K0-NS-P04/IE-780828-NS-EM4's position in the basic hardware configuration.

Figure 1-2: Basic Hardware Configuration



1.3 Basic Specifications

The IE-78K0-NS-P04/IE-780828-NS-EM4's basic specifications are listed in Table 1-1.

Table 1-1: Basic Specifications

Parameter	Description
Target device	μPD780828B(A) Subseries
System clock	Main system clock: 8.38 MHz Subsystem clock: not available on device
Clock supply	External: Pulse input Internal: Mounted on emulation board
Voltage support	4.0 to 5.5 V (same as target device)

1.4 Notes on Use of IE-78K0-NS-P04 and IE-780828-NS-EM4

- (1) Ensure that the power supply for the IE-78K0-NS-A and the target system is OFF before connecting or disconnecting to/from the IE-78K0-NS-A and the target device, or changing switch settings, etc.
- (2) When carrying out target device emulation using the IE-78K0-NS-P04 and IE-780828-NS-EM4 in conjunction with the IE-78K0-NS-A, there are certain differences from the operation of the actual device (see **Differences from Target Device**).
- (3) The target system V_{DD} must be between 4.0 V and 5.5 V.
- (4) **Power on sequence:**
 1. Power on IE-78K0-NS-A
 2. Power on target hardware
 3. Start debugger ID78K0-NS
- (5) **Power off sequence:**
 1. Exit from debugger ID78K0-NS
 2. Power off target hardware
 3. Power off IE-78K0-NS-A.

[Memo]

Chapter 2 Part Names

This chapter introduces the parts of the IE-78K0-NS-P04 and the IE-780828-NS-EM4.

The packaging boxes of the IE-78K0-NS-P04 and the IE-780828-NS-EM4 contain the following items:

2.1 Package Components

IE-78K0-NS-P04 Components

The IE-78K0-NS-P04 comprises the following components. Please check that all these items are included in the package.

- | | |
|-------------------------------|-----|
| (1) IE-78K0-NS-P04 | x 1 |
| (2) Parts holder (with cover) | x 2 |
| (3) Registration Card | x 1 |
| (4) Readme First | x 1 |
| (5) List of Contents | x 1 |

IE-780828-NS-EM4 Components

The IE-780828-NS-EM4 comprises the following components. Please check that all these items are included in the package.

- | | |
|---|-----|
| (1) IE-780828-NS-EM4 | x 1 |
| (2) LCD-split resistor network | x 1 |
| (3) Screws Set | x 1 |
| (4) Registration Card | x 1 |
| (5) Readme First | x 1 |
| (6) List of Contents | x 1 |
| (7) Floppy Disk with Device
File and FPGA Data | x 1 |
| (8) User's Manual (this manual) | x 1 |

2.3 Parts of the IE-780828-NS-EM4

Figure 2-2: IE-780828-NS-EM4 External View and Part Names

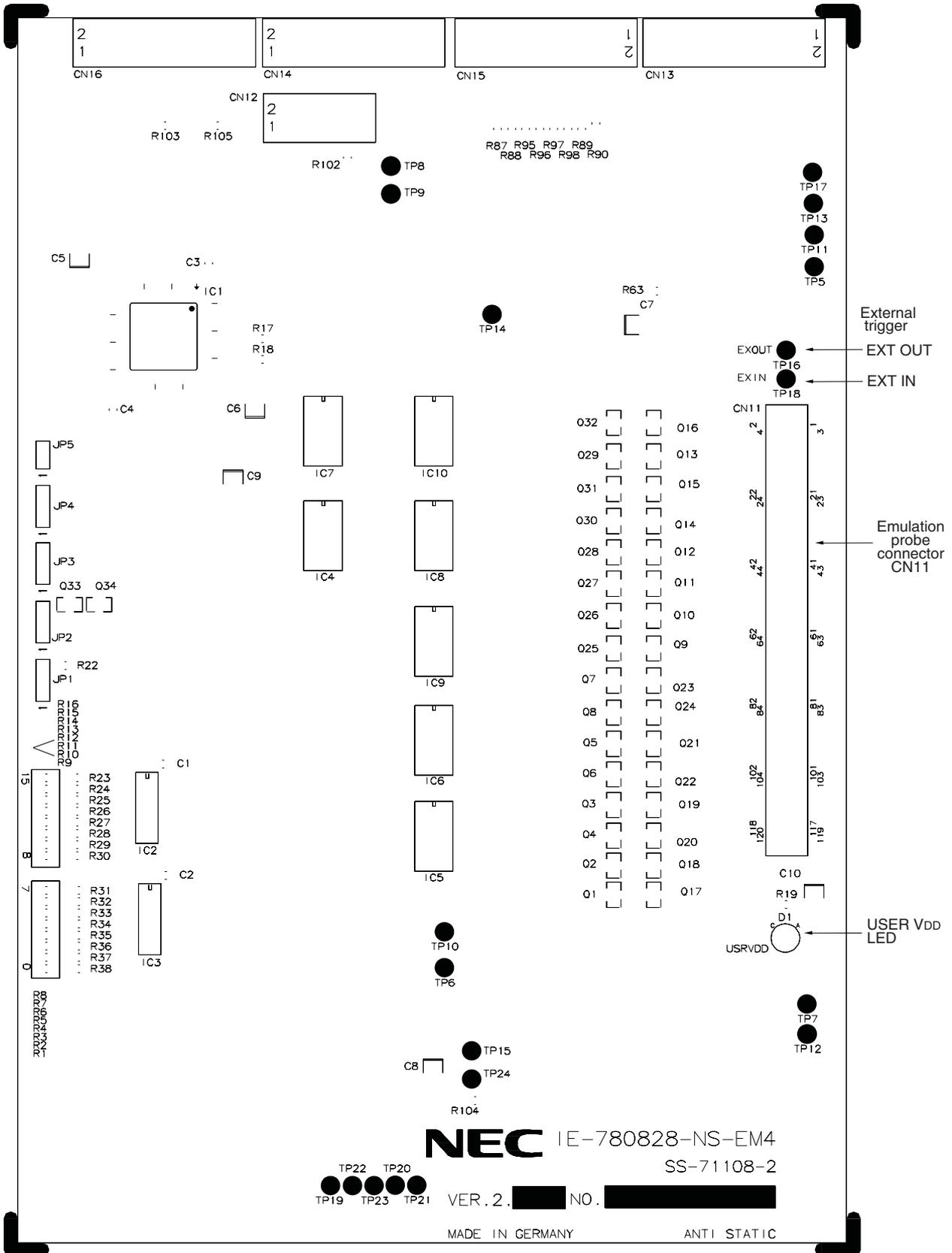


Table 2-1: Names of IE-78K0-NS-P04 and IE-780828-NS-EM4 Parts

Name	Description (IE-78K0-NS-P04)	Name	Description (IE-780828-NS-EM4)
CN1	Emulator connections	CN5	Emulation board connectors (IE-78K0-NS-P04)
CN2		CN6	
CN3		CN7	
CN4		CN8	
CN5	Probe board connectors (IE-78K0-NS-P04)	CN9	
CN6		CN10	
CN7		CN11	Probe connector
CN8		JP1	Disconnect USER-Reset
CN9		JP2	CAN TxD driver buffer type
CN10		JP3	CAN RxD receive buffer type
CN11	Test connector (only for internal use by NEC)		
CN12			
CN13			
CN14			
CN15			
CN16			
CN17			
CN18			
JP1	Analog reference voltage		
JP2	GND-pin of A/D Converter		
JP3	Reserved (only for internal use by NEC)		
JP4	JTAG mode selection (only for internal use by NEC)		
JP5	FPGA mode selection		
JP6	JTAG mode selection (only for internal use by NEC)		
JP7	LVREF1		
JP8	LVREF0		
JP9	Future Function		

[Memo]

Chapter 3 Installation

This chapter describes the method for the connection of the IE-78K0-NS-P04, the IE-780828-NS-EM4 and the emulation probe.

- Installation of the IE-78K0-NS-P04
- Installation of the IE-780828-NS-EM4
- Installation of the emulation probe
- Setting of the jumpers for the clock selection

The power supply of the IE-78K0-NS-A and the target system must be switched off when connecting or disconnecting any item.

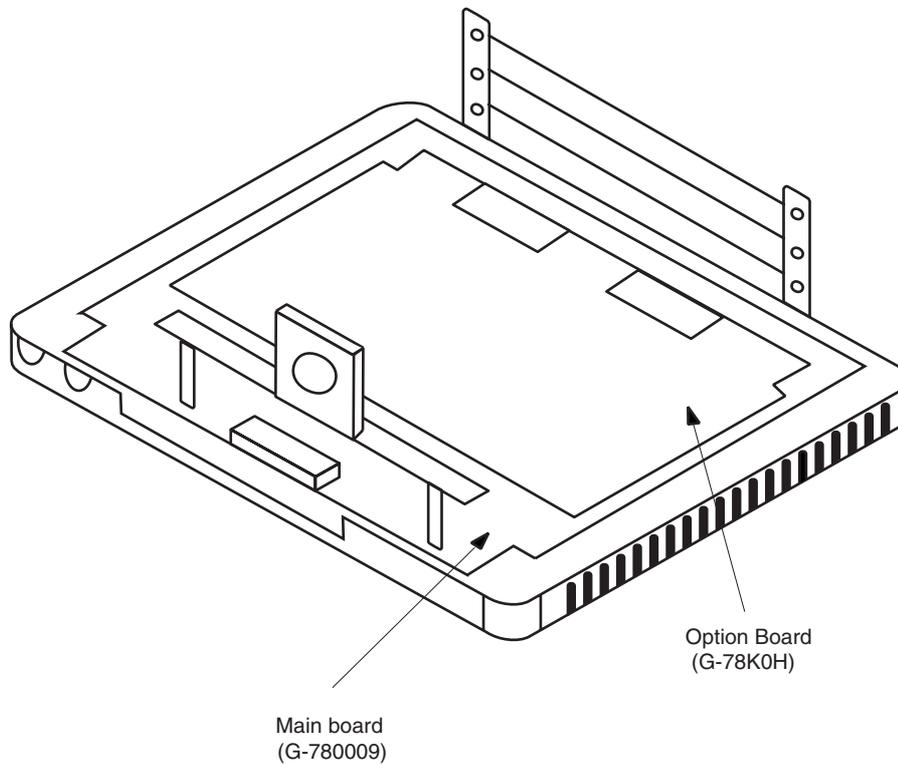
Caution: Usage of incorrect connection methods may damage the IE system.

3.1 Installation Procedure

<1> Remove the 4 screws at the sides of the IE-78K0-NS-A and open the top of the cover.

<2> Remove the screws on the option board (G-78K0H) and remove the option board.

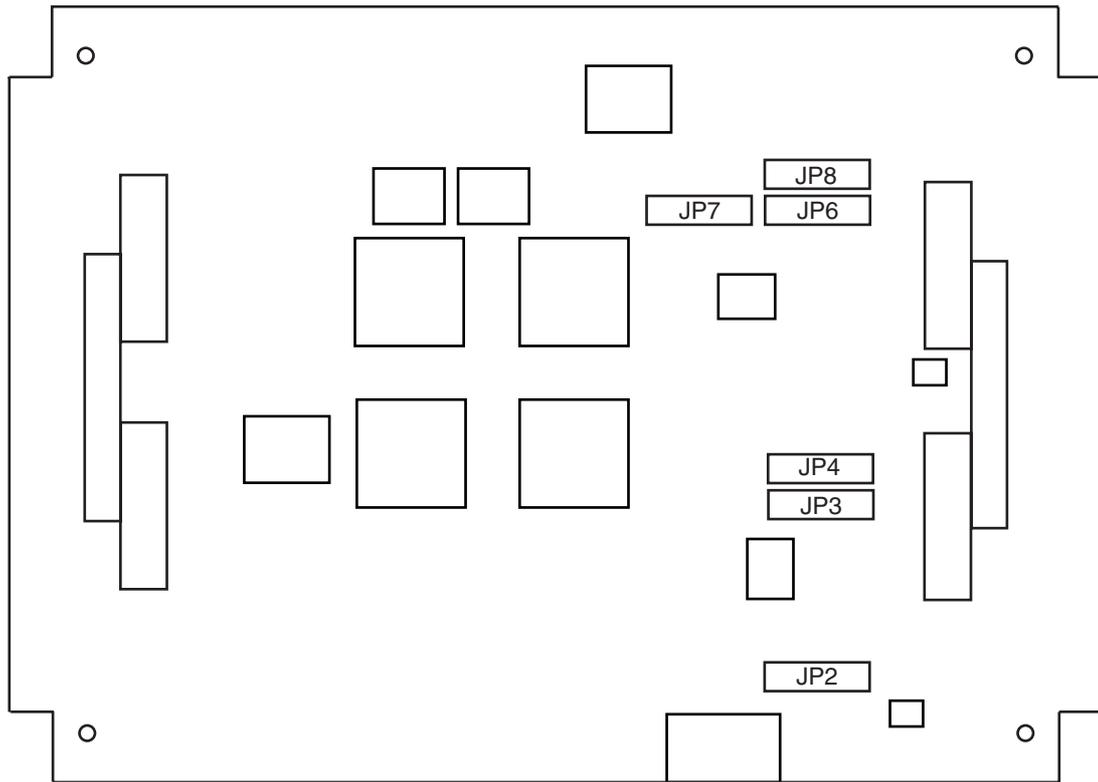
Figure 3-1: IE-78K0-NS-A inside



<3> Setup the jumper's on the **main board** (G-780009).

It is necessary to set some jumpers on the main board for the clock selection. An example for the jumper setting will be given in the chapter clock setting.

Figure 3-2: Main Board (G-780009) Jumper Positioning



Jumper JP2

Table 3-1: Flash ROM Mode

Jumper Position	Function
(1-2)	Internal use
(2-3)	Internal use (default)

Jumper JP3

Table 3-2: Internal Mode 1

Jumper Position	Function
(1-2)	Internal use (default)
(2-3)	Internal use

Jumper JP4

Table 3-3: Internal Mode 2

Jumper Position	Function
(1-2)	Internal use (default)
(2-3)	Internal use

Jumper JP6

Table 3-4: Main Clock Selection

Jumper Position	Function
(1-2)	Not selectable
(3-4)	EM1/P04 board selection (default)
(5-6)	EM4 board selection

Jumper JP7

Table 3-5: Main Clock Doubler Selection

Jumper Position	Function
(1-2)	Main board selection (default)
(3-4)	EM board selection 1
(5-6)	EM board selection 2

Jumper JP8

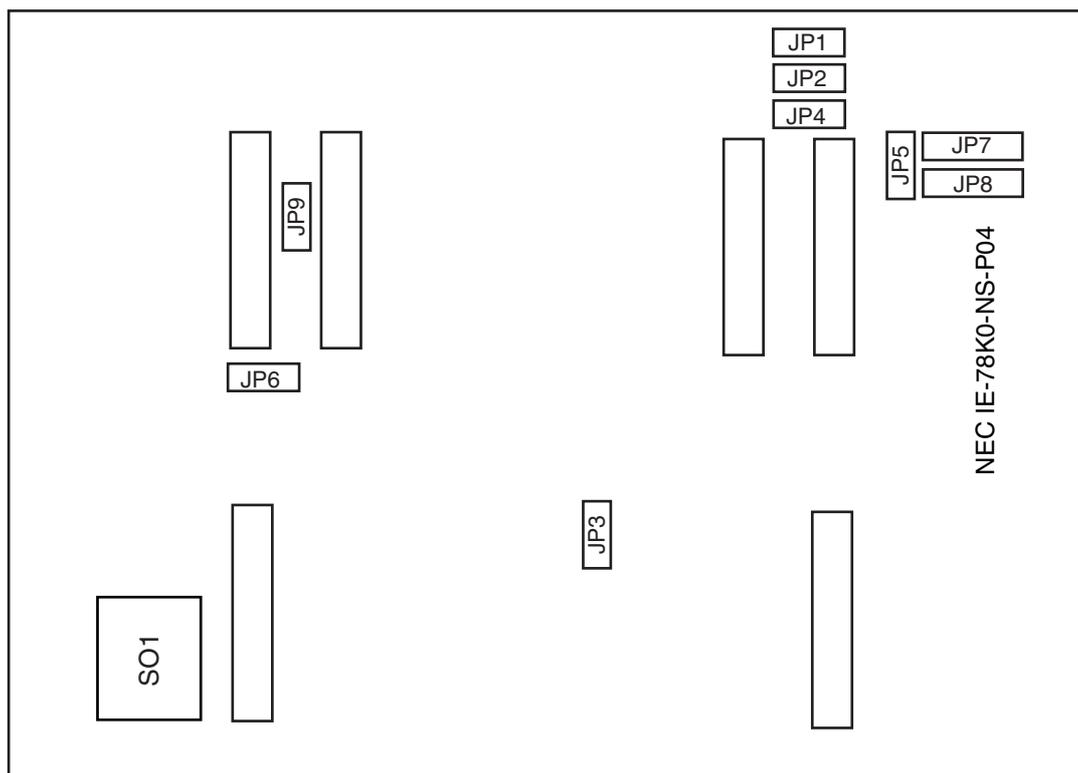
Table 3-6: Sub Clock Selection

Jumper Position	Function
(1-2)	On EM board (default)
(3-4)	On target system
(5-6)	On main board

<4> Connect the option board (G-78K0H) to the main board (G-780009).

<5> Setup of the **emulation board (IE-78K0-NS-P04)**

Figure 3-3: Emulation Board (IE-78K0-NS-P04) Jumper Positioning



Jumper JP1

Table 3-7: Reference Voltage Pin of AD-Converter

Jumper Position	AAV _{REF}	Function
Open	Target	Connected to target selected reference voltage (default)
Close	GND	Reference voltage

Remark: Close jumper JP1 when the AD-converter is not used.

Jumper JP2

Table 3-8: Ground Voltage Pin of AD-Converter

Jumper Position	AAV _{ss}	Function
Open	Target	Connected to target selected ground base (default)
Close	GND	Internal digital ground

Remark: Close jumper JP2 when the AD-converter is not used.

Jumper JP3**Table 3-9: JTAG Mode**

Jumper Position	JTAG	Function
Open	Pull-up	Reserved (Internal use) (default)
Close	GND	Reserved (Internal use)

Jumper JP4**Table 3-10: JTAG Mode**

Jumper Position	JTAG	Function
Open	Pull-up	Reserved (Internal use)
Close	GND	Reserved (Internal use) (default)

Jumper JP5**Table 3-11: FPGA Mode Selection**

Jumper Position	ESN	Function
Open	Pull-up	Asynchronous peripheral mode (FPGA s are loaded by IE) (default)
Close	GND	Reserved (Internal use)

Jumper JP6**Table 3-12: JTAG Mode**

Jumper Position	JTAG	Function
(1-2)	Pull-up	Reserved (Internal use)
(2-3)	GND	Reserved (Internal use) (default)

Jumper JP7**Table 3-13: Reference Voltage Setting**

Jumper Position	LV _{REF1}	Function
(1-2)	V _{CC}	Reserved (Internal use) (default)
(2-3)	LV _{DD}	Reserved (Internal use)

Jumper JP8

Table 3-14: Reference Voltage Setting

Jumper Position	LV _{REF0}	Function
(1-2)	V _{CC}	Reserved (Internal use) (default)
(2-3)	LV _{DD}	Reserved (Internal use)

Jumper JP9

Table 3-15: Future Function

Jumper Position		Function
Open	Pull-up	Reserved (Internal use) (default)
Close	GND	Reserved (Internal use)

Socket SO1

The LCD-controller/driver of the emulated device (μPD780828B(A) series) has internal split resistors for the LCD voltage level. Therefore the LCD-split resistor network (delivered with IE-780828-NS-EM4) has to be connected to SO1 of the IE-78K0-NS-P04.

LED Indicator

Table 3-16: LED Indicator D1, D2, D3

LED	Condition	Function
LED1 green	Blinking	FPGA download ongoing
LED1 green	On	FPGA download complete
LED1 green	Off	FPGA not programmed
LED2 yellow	Blinking	Not used
LED2 yellow	On	V _{cc} on
LED2 yellow	Off	V _{cc} off
LED3 red	Blinking	Not used
LED3 red	On	Not used
LED3 red	Off	Not used

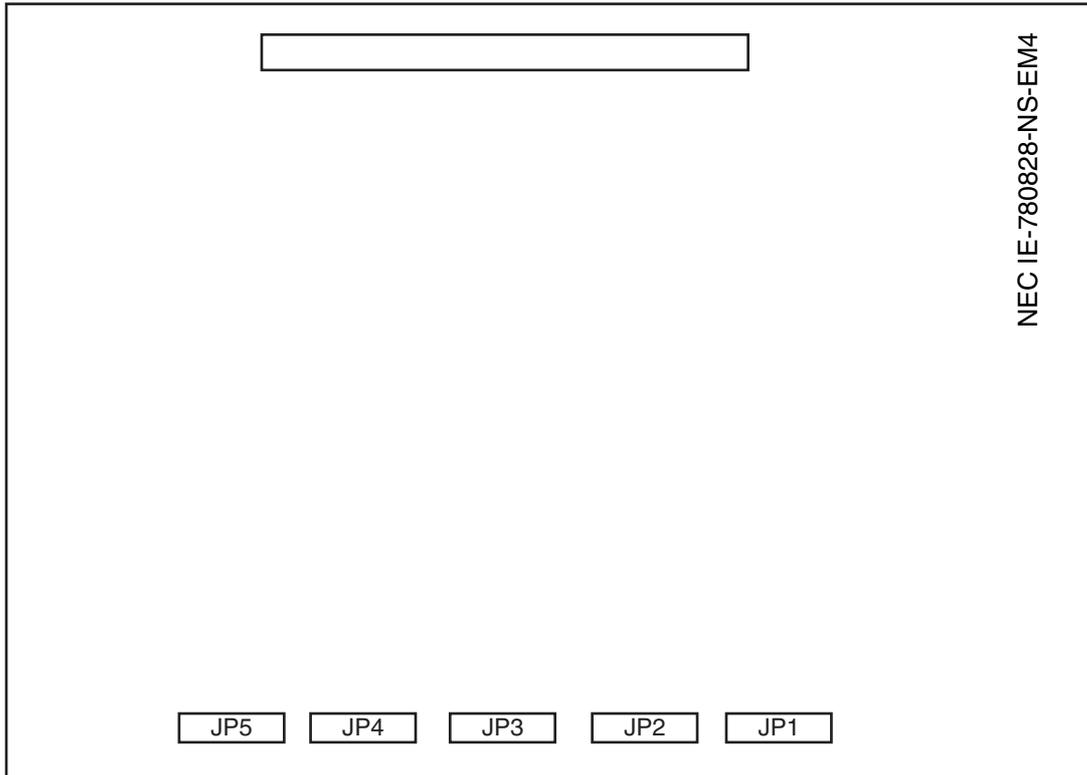
Remark: Not used LED's are reserved for future functions.

<6> Connect the emulation board (IE-78K0-NS-P04) to the option board (G-78K0H).

<7> When user clock as main clock is used, the main system clock can be mounted by using a parts holder or a crystal oscillator (see chapter clock setting).

<8> Setup of the **probe board (IE-780828-NS-EM4)**

Figure 3-4: Emulation Board (IE-780828-NS-EM4) Jumper Positioning



Jumper JP1

Table 3-17: User $\overline{\text{RESET}}$ mode

Jumper Position	User $\overline{\text{RESET}}$	Function
(1-2)	To probe	User Reset (IE) connected to the probe (default)
(2-3)	Pull-up	User Reset (IE) pull-up by resistor (10K)

Jumper JP2

Table 3-18: DCAN Out Transmit Buffer Selection

Jumper Position	DCAN out	Function
(1-2)	Pin emulator	Reserved
(2-3)	FPGA	DCAN transmit line from FPGA via transistor to probe (default)

Jumper JP3

Table 3-19: DCAN in Buffer Type Selection

Jumper Position	DCAN in	Function
(1-2)	Pin emulator	Original buffer (default)
(2-3)	FPGA	Buffer type different /timing optimized (limitation $\text{USRV}_{\text{DD}} \geq 4.5 \text{ V}$)

Jumper JP4

Table 3-20: Stepper Motor Power Selection

Jumper Position	Stepper Motor Power	Function
(1-2)	SMV_{DD}	External power supply via SMV_{DD} pin(default)
(2-3)	LV_{DD}	Internal power supply

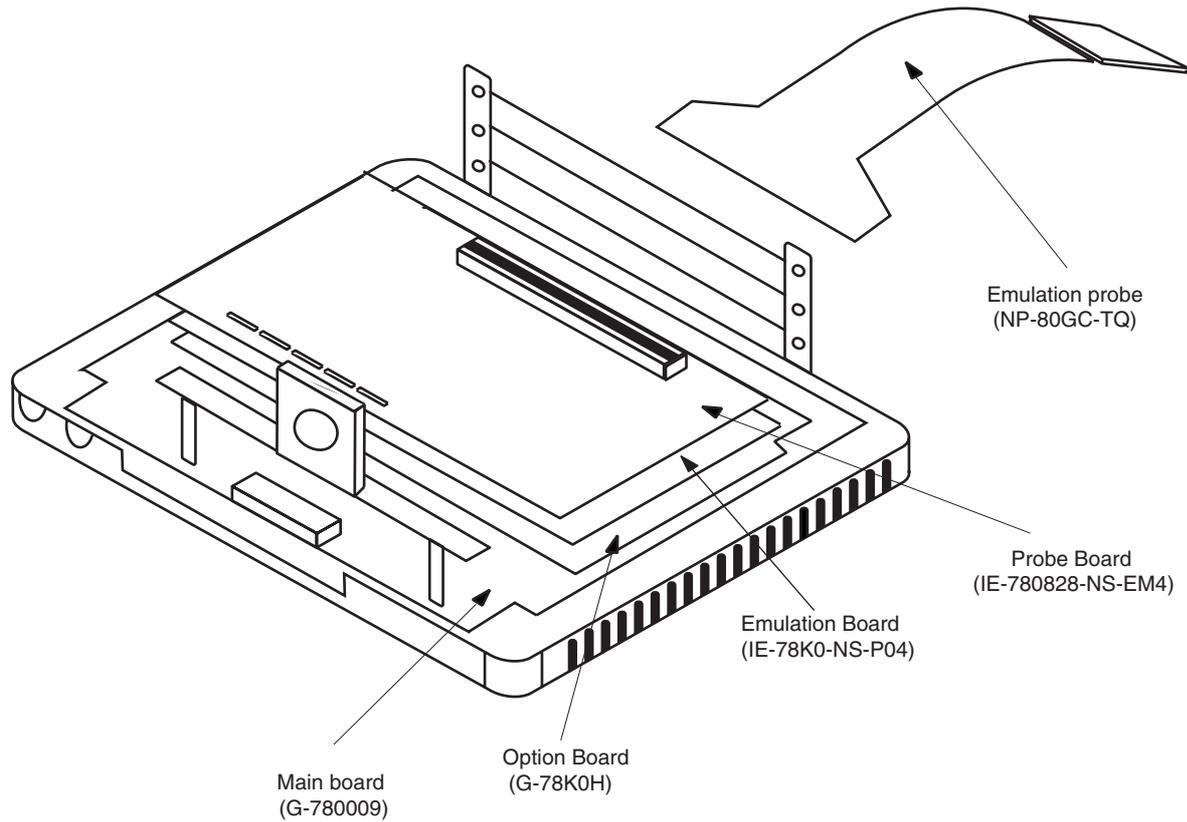
Jumper JP5

Table 3-21: Stepper Motor Power Selection

Jumper Position	Stepper Motor Power	Function
Open	SMV_{DD}	External power supply via SMV_{DD} pin(default)
Closed	USRV_{DD}	Internal power supply

- <9> Connect the probe board (IE-780828-NS-EM4) to the emulation board (IE-78K0-NS-P04)
- <10> Remove the top and the bottom plate by removing the screws.
- <11> Connect the probe (NP-80GC-TQ) to CN11 of the probe board (IE-780828-NS-EM4).
- <12> Connect the cover and tighten the 4 screws.

Figure 3-5: Connection of Boards



3.2 Clock Settings

3.2.1 Overview of clock settings

Main system clock

Select from (1) to (3) below as the main system clock and subsystem clock to be used during debugging.

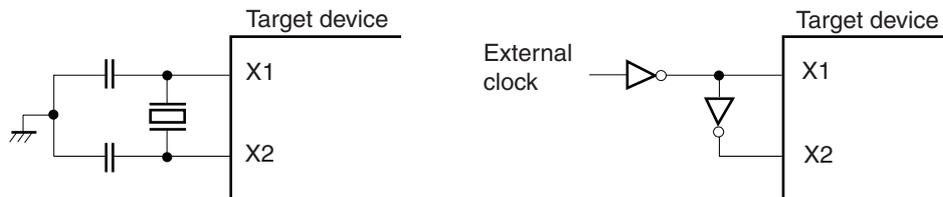
- (1) Clock that is already mounted on emulation board
- (2) Clock that is mounted by user
- (3) External clock

If the target system includes an internal clock, select either “(1) Clock that is already mounted on emulation board” or “(2) Clock that is mounted by user”. An internal clock connects the target device to an oscillator and uses the target device’s internal oscillation circuit. An example of an external circuit is shown in part (a) of Figure 3-2. During emulation, the oscillator that is mounted on the target system is not used. Instead, it uses the clock that is mounted on the emulation board which is installed for the IE-78K0-NS-A.

If the target system includes an external clock, select “(3) External clock”.

An external clock supplies a clock signal from outside of the target device and does not use the target device’s internal oscillation circuit. An example of an external circuit is shown in part (b) of Figure 3-2.

Figure 3-6: External Circuits Used as System Clock Oscillation Circuit

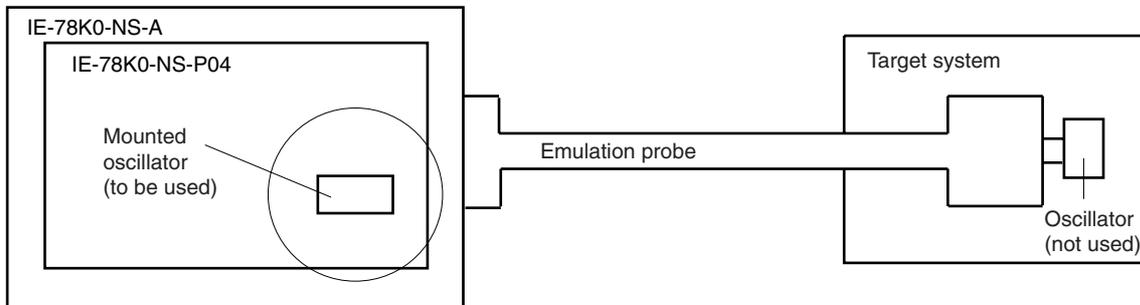


3.2.2 Main System Clock Selections

(1) Clock that is already mounted on emulation board

A crystal resonator is already mounted on the emulation board. Its frequency is 8.0000 MHz.

Figure 3-7: When Using Clock That Is Already Mounted on Emulation Board

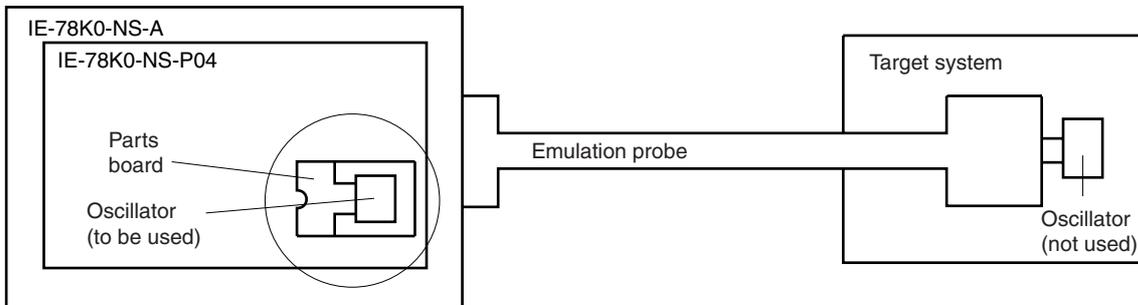


Remark: The clock that is supplied by the IE-78K0-NS-P04 oscillator (encircled in the figure) is used.

(2) Clock that is mounted by user

The user is able to mount any clock supported by the set specifications on the IE-78K0-NS-P04. First mount the oscillator on the parts holder, then attach the parts board to the IE-78K0-NS-P04. This method is useful when using a different frequency from that of the pre-mounted clock.

Figure 3-8: When Using User-mounted Clock

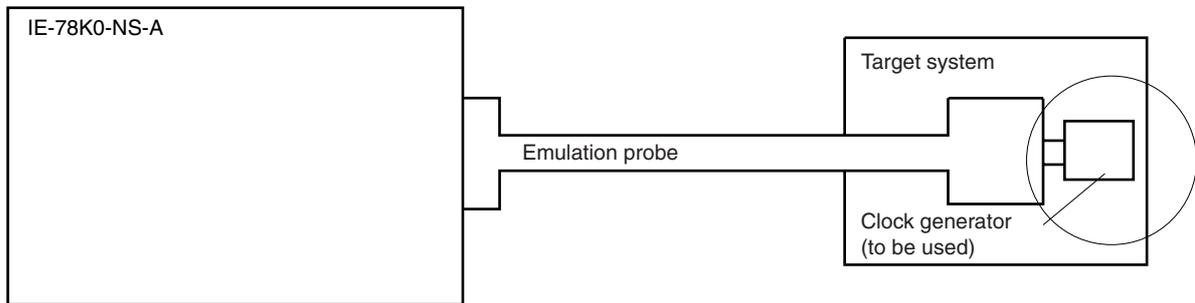


Remark: The clock that is supplied by the IE-78K0-NS-P04 oscillator (encircled in the figure) is used.

(3) External clock

An external clock connected to the target system can be used via the emulation probe.

Figure 3-9: When Using an External Clock



Remark: The clock supplied by the target system’s clock generator (encircled in the figure) is used.

3.2.3 Subsystem Clock

The IE-78K0-NS-P04 supports the using of a subclock for the emulation. But this function is **not** supported by the μPD780828B(A) series.

3.2.4 Main system clock settings

Table 3-22: Main System Clock Settings

Frequency of Main System Clock		IE-78K0-NS-P04	CPU Clock Source Selection (ID-78K0-NS)
When using clock that is already mounted on emulation board	8.0000 MHz	Shortcut 6-8	Internal
When using clock mounted by user	Other than 8.0000 MHz	Includes oscillator circuit	External
When using external clock		Shortcut 6-8	

Caution:When using an an user defined clock or external clock, open the configuration dialog when starting the integrated debugger (ID78K0-NS) and select “External” in the area (Clock) for selecting the CPU’s clock source (this selects the user’s clock).

Remark: The IE-78K0-NS-P04 factory settings are those listed above under “when using clock that is already mounted on emulation board”.

(1) When using clock that is already mounted on emulation board

When the IE-78K0-NS-P04 is shipped, an 8.0000-MHz crystal resonator is already mounted in the IE-78K0-NS-P04 X4 socket. When using the factory-set mode settings, there is no need to make any other hardware settings.

When starting the integrated debugger (ID78K0-NS), open the configuration dialog and select “Internal” in the area (Clock) for selecting the CPU’s clock source (this selects the emulator’s internal clock).

(2) When using clock mounted by user

The settings described under either (a) or (b) are required, depending on the type of clock to be used. When starting the integrated debugger (ID78K0-NS), open the configuration dialog and select “Internal” in the area (Clock) for selecting the CPU’s clock source (this selects the emulator’s internal clock).

(a) When using a ceramic oscillator or crystal resonator

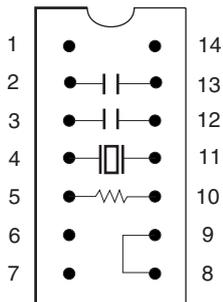
- Items to be prepared
 - Parts holder (supplied with IE-78K0-NS-P04)
 - Ceramic oscillator or crystal resonator
 - Resistor Rx
 - Capacitor CA
 - Capacitor CB
 - Solder kit

<Steps>

<1> Solder onto the supplied parts board (as shown below) the target ceramic oscillator or crystal resonator, resistor Rx, capacitor CA, and capacitor CB (all with suitable oscillation frequency).

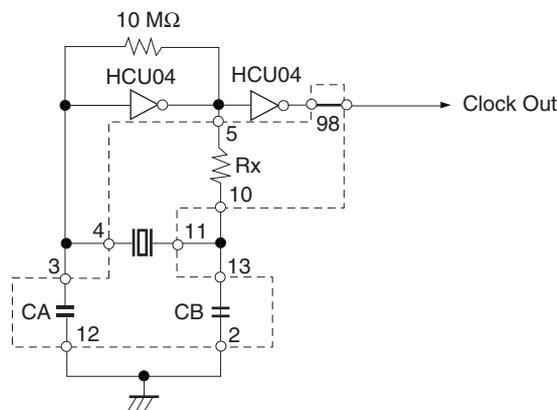
Figure 3-10: Connections on Parts Board

Parts holder



Pin No.	Connection
2-13	Capacitor CB
3-12	Capacitor CA
4-11	Ceramic oscillator or crystal resonator
5-10	Resistor Rx
8-9	Short

Circuit diagram

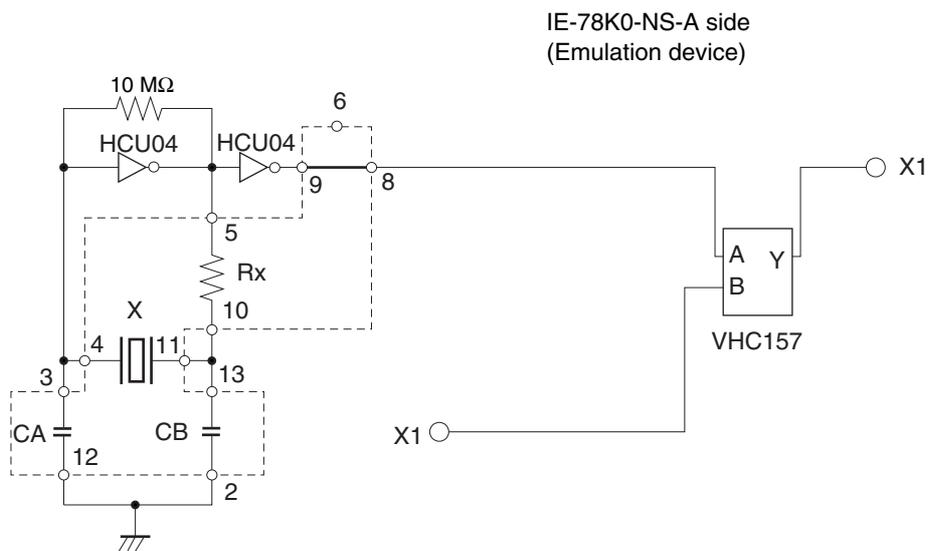


Remark: The sections enclosed in broken lines indicate parts that are attached to the parts board.

- <2> Prepare the IE-78K0-NS-P04.
- <3> Remove the parts holder inserted in the socket (marked "X2") on the IE-78K0-NS-P04.
- <4> Connect the parts holder (from <1> above) to the socket (X2) from which the part holder was removed. Check the pin 1 mark to make sure the board is mounted in the correct direction.
- <5> Make sure that the parts board mounted in the X2 socket on the emulation board is wired as shown in Figure 3-10 above.
- <6> Install the IE-78K0-NS-P04 and the IE-780828-NS-EM4 in the IE-78K0-NS-A.

The above steps configure a circuit and enable clock output to be supplied from the mounted oscillator to the emulation device.

Figure 3-11: IE-78K0-NS-A side (Emulation Device)

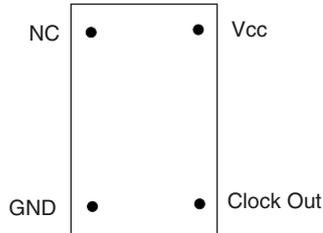


Remark: The sections enclosed in broken lines indicate parts that are attached to the parts holder.

(b) When using a crystal oscillator

- Items to be prepared
- Crystal oscillator (see pinouts shown in Figure 3-7)

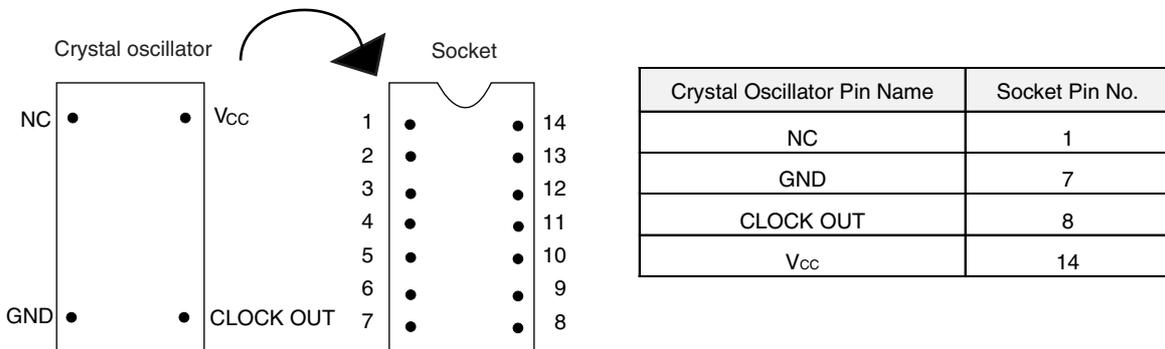
Figure 3-12: Crystal Oscillator



<Steps>

- <1> Prepare the IE-78K0-NS-P04.
- <2> Remove the parts holder inserted in the socket (marked "X2") on the IE-78K0-NS-P04.
- <3> Connect the parts board (from <2> above) to the socket (X2) from which the parts holder was removed. Insert the crystal oscillator into the socket so as to align the pins as shown in the figure below.

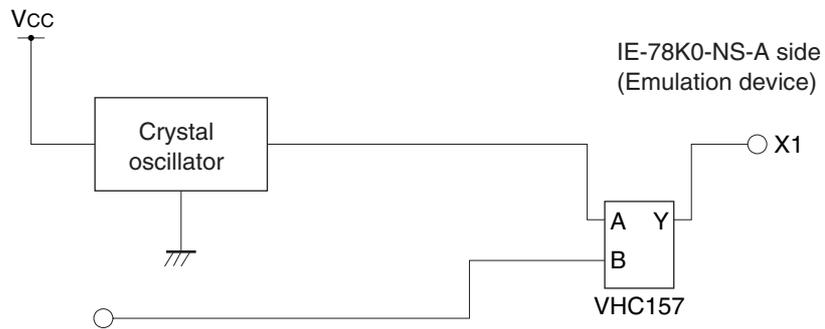
Figure 3-13: Pin Alignment of Crystal Oscillator and Socket



- <4> Install the IE-78K0-NS-P04 and the IE-780828-NS-EM4 in the IE-78K0-NS-A.

The above steps configure a circuit and enable clock output to be supplied from the mounted oscillator to the emulation device.

Figure 3-14: IE-78K0-NS-A side (Emulation Device)



(3) When using an external clock

No hardware settings are required for this situation.

Make sure that the parts holder with a shortcut between 6 and 8 is in the socket (marked "X2"). When starting the integrated debugger (ID78K0-NS), open the configuration dialog and select "External" in the area (Clock) for selecting the CPU's clock source (this selects the user's clock).

3.2.5 Examples of Main System Clock Setting

(1) Standard Clock 8.000 MHz offered by the Emulation Board (IE-78K0-NS-P04)

Main Board: JP6 - (3-4)
JP7 - (1-2)
Emulation Board: X2 with shortcut between 6 - 8
ID78K0-NS: Internal

(2) Clock mounted by the User on the Emulation Board

User related Clock
Main Board: JP6 - (3-4)
JP7 - (1-2)
Emulation Board: X2 with parts holder and crystal resonator, ceramic resonator or crystal oscillator
ID78K0-NS: External

(3) External Clock on the Target Hardware

Main Board: JP6 - (3-4)
JP7 - (1-2)
Emulation Board: X2 with shortcut between 6 - 8
ID78K0-NS: External

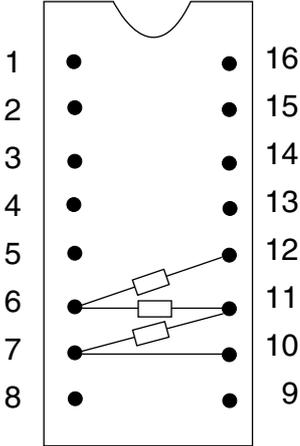
3.3 Subsystem Clock Setting

The IE-78K0-NS-P04 supports the using of a subclock for the emulation. But this function is not supported by the μ PD780828B(A) series.

3.4 LCD Resistor Network

In order to use the LCD during the emulation it is necessary to connect the resistor network (delivered with the IE-780828-NS-EM4) to the socket SO1 on the IE-78K0-NS-P04.

Figure 3-15: LCD-split resistor Network



3.5 Jumper Settings

When using the IE-78K0-NS-P04 and the IE-780828-NS-EM4, set the jumpers as shown below.

Table 3-23: Jumper Settings on IE-78K0-NS-A

	JP2	JP3	JP4	JP6	JP7	JP8
Short	2-3	1-2	1-2	3-4	1-2	3-4

Table 3-24: Jumper Settings on IE-78K0-NS-P04

JP1	JP2	JP3	JP4	JP5	JP6	JP7	JP8	JP9
Open	Open	Open	Closed	Open	2-3	1-2	1-2	Open

Table 3-25: Jumper Settings on IE-780828-NS-EM4

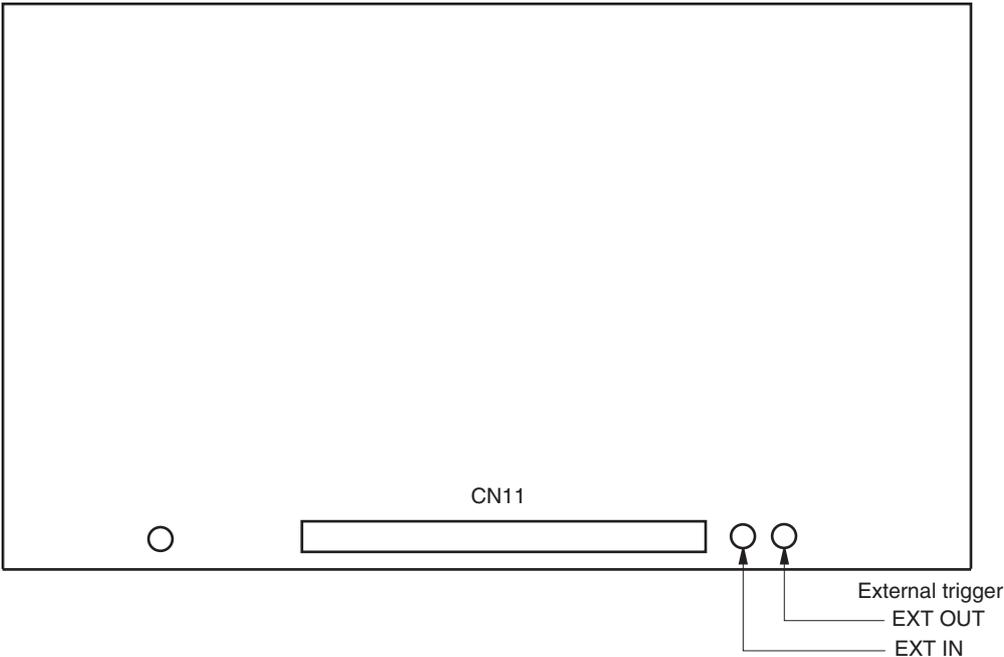
JP1	JP2	JP3	JP4	JP5
1-2	2-3	1-2	1-2	Open

3.6 External Trigger

To set up an external trigger, connect the IE-780828-NS-EM4's check pin, EXTOUT, and EXTIN as shown below.

See the in-circuit emulator (IE-78K0-NS-A) User's Manual for description of related use methods and pin characteristics.

Figure 3-16: External Trigger Input Position



[Memo]

Chapter 4 Differences among Target Devices and Target Interface Circuits

This chapter describes differences between the target device and the IE-78K0-NS-P04 / IE-780828-NS-EM4 target interface circuit.

Although the target device is a CMOS circuit, the IE-78K0-NS-P04/IE-780828-NS-EM4's target interface circuit consists of an emulation chip, TTL, CMOS-IC, and other components.

When connected the IE system with the target system for debugging, the IE system performs emulation so as to operate as the actual target device would operate on the target system.

However, some minor differences exist since the operations are performed via the IE system's emulation.

4.1 Input/Output Signals

<1> Signal which are input or output from the gate array.

<2> Signals those are input or output from the μ PD78P0308.

<3> Signals that are input or output from the μ PD780009 emulation CPU

<4> Other signals

The IE system circuit is used as follows for above-mentioned signals.

(1) Signals which are input or output from the gate array

P00 to P03
P10/ANI0 to P14/ANI4
P34 to P37
P40 to P47
P61 to P65
P80 to P87
P90 to P97
AV_{DD}/AV_{REF}
AV_{SS}
CRxD

(2) Signals those are input or output from the μ PD78P0308

S0 to S27
COM0 to COM4
V_{LCD}

(3) Signals that are input or output from the μ PD780009 emulation CPU

X1
RESET

(4) Other signals

P20 to P27
P50 to P57
P60
V_{DD0}, V_{DD1}
V_{SS0}, V_{SS1}
SMV_{DD}
SMV_{SS}
X2
CTxD
V_{PP}/Test

Figure 4-1: Equivalent Circuit 1 from Emulation Circuit

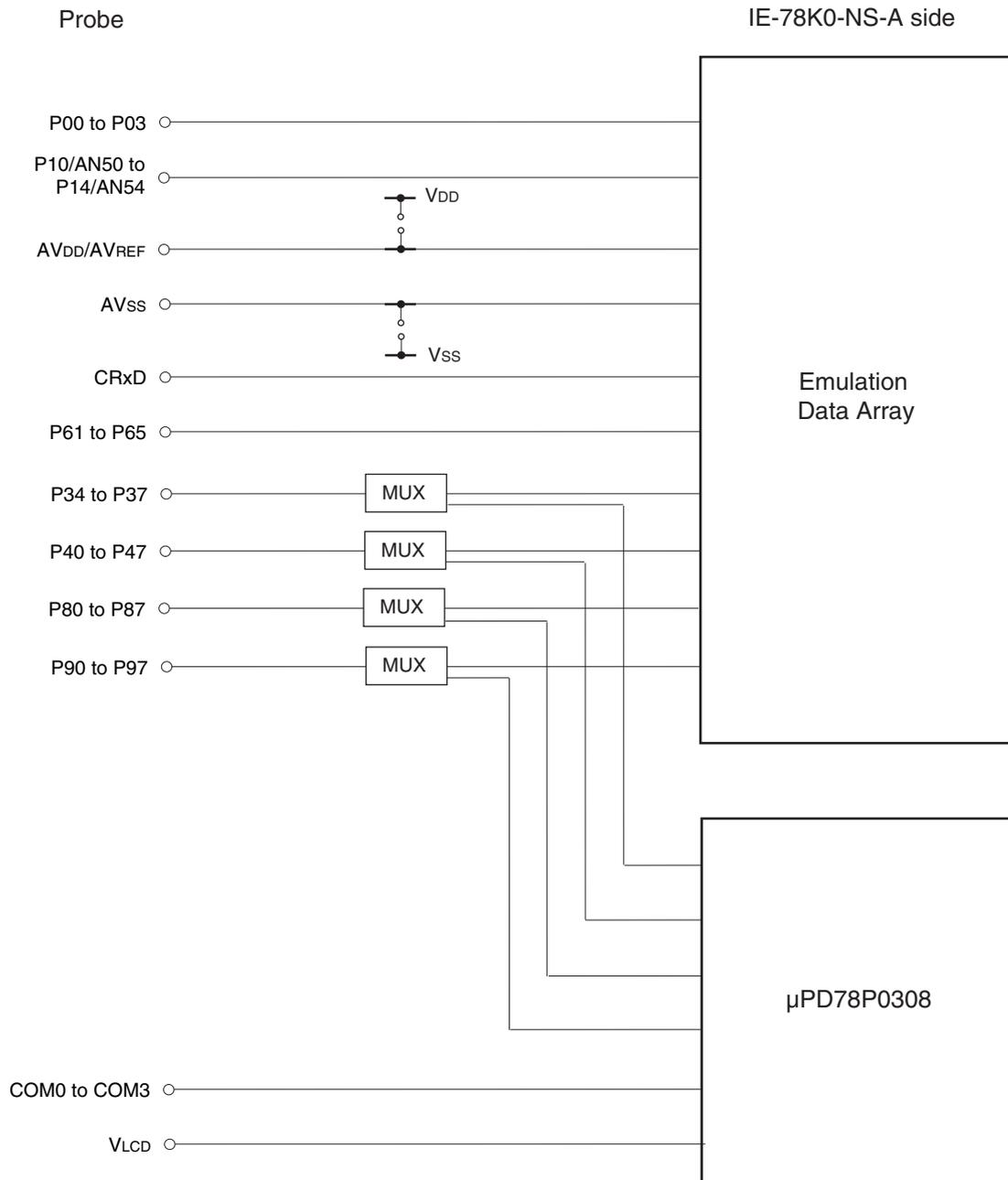


Figure 4-2: Equivalent Circuit 2 from Emulation Circuit

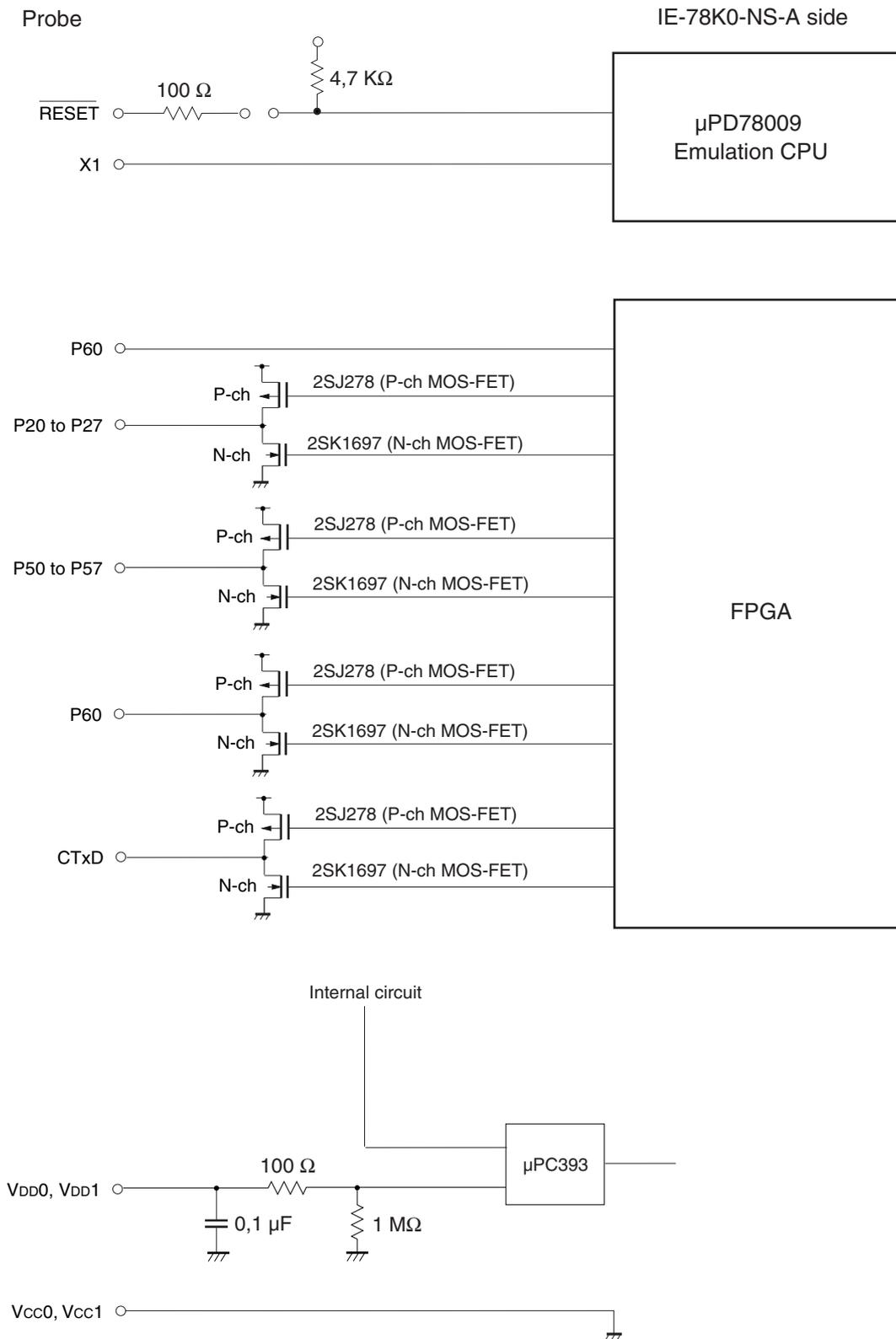


Figure 4-3: Equivalent Circuit 3 from Emulation Circuit



4.2 Differences in Port Functions

(1) Port 3.6, Port 4, Port 6.0 to 6.3 and Port 9.2 of the device are normal CMOS inputs with no hysteresis. The emulator has pins with hysteresis.

(2) The LCD-segment signals S0-S27 are input/output ports of type 17A/17B at the device. The emulator drives these signals by an analog switch.

(3) The power fail detection is implemented as analogue comparator instead of a digital comparator on the device.

4.3 Differences in SFR-Registers

Caution: 1. The emulator has a register to emulate the powerfail detection which is not existing at the real chip. The name of the register is DAM0 (SFR-Adr: 0xFF9C). This register has to be set to the value 0x01 by the user program.

2. The emulator has a register for the emulation of the LCD-function. The name of the register is LCDTM (SFR-Adr: 0xFF4A). This register has to be set to the value 0x02 by the user program.

4.4 Target Interface Circuit

The purpose of the target interface circuit is to have the same operations as the target device performed in the IE-78K0-NS-A. It comprises the emulation device and various dates (CMOS, TTL and othes ICs).

When debugging is performed with the target system connected to the IE-78K0-NS-A, the IE-78K0-NS-A target interface circuit performs emulation as though the actual target device were operating in the target system.

The target device has a CMOS LSI configuration. The target interface circuit emulator device also has a CMOS LSI configuration, and is virtually identical to the target device in terms of DC characteristics and AC characteristics (when operating on $V_{DD} = 4.0$ to 5.5 V).

However, where emulation device signal input/output is performed via gates in the target interface circuit, DC and AC characteristics differ from those of the target device.

In particular, regarding AC characteristics, there is a date delay time (which differs from date to date) each time a gate is passed through.

The above points must be taken into consideration when designing the target system.

Caution: When the IE-78K0-NS-A and IE-78K0-NS-P04 and IE-780828-NS-EM4 are connected to the target system, 4.0 to 5.5 V must be supplied as the target system power supply (V_{DD}).

[Memo]

Chapter 5 Restrictions

1. Starting up the IE system without target board connected makes initial values for ports-indefinite.
2. The RESET value of the CANES register is not correct. As workaround the CANES register has to be reset by software.
3. Meter Controller/Driver
 Since an external transistor is used for the output driver, the electrical specifications of driver capability vary as follows:

Table 5-1: Output Current per Terminal (effective value)

	Device	ICE
High-level output current	-80 mA	-150 mA
Low-level output current	80 mA	250 mA

Note: For the device output current, see the data sheet.

4. Sound Generator
 Since an external transistor is used for the output driver, the electrical specifications of driver capability vary as follows:

Table 5-2: Output Current of P61 (SGO) (effective value)

	Device	ICE
High-level output current	-20 mA	-150 mA
Low-level output current	20 mA	250 mA

Note: For the device output current, see the data sheet.

5. LCD Controller/Driver
 It is necessary to set the LCDTM register (the ICE dedicated register).
6. Power Fail Detector
 It is necessary to set the DAM0 register (dedicated register when the the ICE is used).
7. The voltage level of V_{PP} cannot be detected during self-programming. The feedback information bit V_{PP} of the FLPMC register will be always read as 1.

[Memo]

Appendix A IE-78K0-NS-P04, IE-780828-NS-EM4 Product Specifications

Product name : IE-78K0-NS-P04, IE-780828-NS-EM4
 Operating temperature : 0 to 50 °C
 Humidity : 10 to 80% RH (no condensation)
 Storage temperature : -15 to +60 °C
 Power supply : Power supply capacity : DC 200mA (MAX.) 1.0 W +5 V

Table A-1: Connectors on IE-78K0-NS-P04 Board and IE-780828-NS-EM4 Board

Name	Description (IE-78K0-NS-P04)	Name	Description (IE-780828-NS-EM4)
CN1	Emulator connections	CN5	Emulation board connectors (IE-78K0-NS-P04)
CN2		CN6	
CN3		CN7	
CN4		CN8	
CN5	Probe board connectors (IE-78K0-NS-P04)	CN9	
CN6		CN10	
CN7		CN11	Probe connector
CN8		JP1	Disconnect USER-Reset
CN9		JP2	CAN TxD driver buffer type
CN10		JP3	CAN RxD receive buffer type
CN11	Test connector (only for internal use by NEC)	JP4	Choose stepper motor power
CN12		JP5	Choose stepper motor power
CN13			
CN14			
CN15			
CN16			
CN17			
CN18			
JP1	Analog reference voltage		
JP2	GND-pin of A/D Converter		
JP3	Reserved (only for internal use by NEC)		
JP4	JTAG mode selection (only for internal use by NEC)		
JP5	FPGA mode selection		
JP6	JTAG mode selection (only for internal use by NEC)		
JP7	LVREF1		
JP8	LVREF0		
JP9	Future Function		

[Memo]

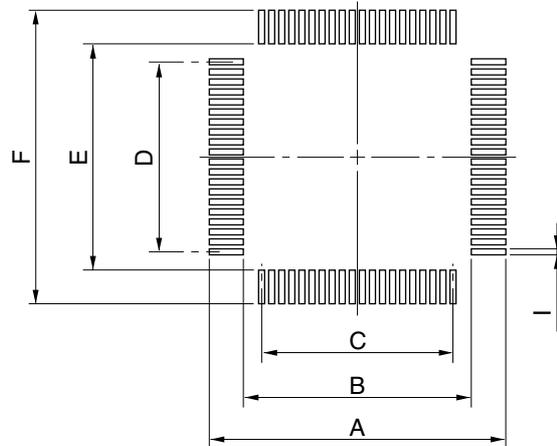
Appendix B Conversion Socket Adapter Package Drawings and recommended Board Mounting Pattern

The following sockets and socket adapters are available for the connection of the probe or device:

- Soldering socket : NQPACK080SB
- Probe adapter : YQPACK080SB
- High adapter : YQSOCKET080SB-F
- Device Lid : HQPACK080SB

Figure B-1: 80GC Package Drawings (Reference)

(2) Pad drawing (in mm)



Item	Millimeters	Inches
A	19.7	0.776
B	15.0	0.591
C	$0.65 \pm 0.02 \times 19 = 12.35 \pm 0.05$	$0.026^{+0.001}_{-0.002} \times 0.748 = 0.486^{+0.003}_{-0.002}$
D	$0.65 \pm 0.02 \times 19 = 12.35 \pm 0.05$	$0.026^{+0.001}_{-0.002} \times 0.748 = 0.486^{+0.003}_{-0.002}$
E	15.0	0.591
F	19.7	0.776

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).

[Memo]

Appendix C Pin Correspondence Tables of Emulation Probe

Table C-1: Connector CN11 to Emulation Probe

No.	Signal Name	Function	No.	Signal Name	Function
1	GND01		2	GND02	
3	NC01		4	NC02	
5	NC03		6	NC04	
7	SMVDD	SMVDD	8	GND	SMVss
9	CRxD	CRxD	10	CTxD	CTxD
11	GND03		12	GND04	
13	SM43_P56	A14/SM43/P56	14	SM44_P57	A15/SM44/P57
15	GND	Vss	16	USRVDD	VDD
17	SM41_P54	A12/SM41/P54	18	SM42_P55	A13/SM42/P55
19	NC	X2	20	X1L1	X1
21	SM33_P52	A10/SM33/P52	22	SM34_P53	A11/SM34/P53
23	NC	IC/VPP	24	SW(27)	S27/TIO50/P34
25	GND05		26	GND06	
27	SM31_P50	A8/SM31/P50	28	SM32_P51	A9/SM32/P51
29	SW(26)	S26/SCK3/P35	30	SW(25)	S25/SO3/P36
31	NC05		32	NC06	
33	NC07		34	NC08	
35		Reset	36	NC09	
37	GND	AVss	38	NC10	
39	GND07		40	GND08	
41	ACHSP4[1]	SGOA/PCL/P61	42	ACHSP4[0]	SGO/SGOF/P60
43	AANI[0]	ANI0/P10	44	AANI[1]	ANI1/P11
45	ACHSP4[3]	TxD0/P63/WR_	46	ACHSP4[3]	RxD0/P62/RD_
47	AANI[2]	AN12/P12	48	AANI[3]	ANI3/P13
49	ACHSP4[5]	TI21/P65/WAIT	50	ACHSP4[4]	TI20/P64/ASTB
51	AANI[4]	ANI4/P4	52	AVREF0	AVREF
53	GND09		54	GND10	
55	BCHSP2[2]	INTP2/P02	56	BCHSP2[3]	P03
57	GND	Vss	58	USRVDD	VDD
59	BCHSP[0]	INTP00/P00	60	BCHSP2[1]	INTP1/P01/TCL
61	SW_R(4)	AD3/P43/S4	62	SW_R(5)	AD2/P42/S5
63	SW_R(2)	AD5/P45/S2	64	SW_R(3)	AD4/P44/S3
65	SW_R(6)	AD1/P41/S6	66	SW_R(7)	AD0/P40/S7
67	GND11		68	GND12	
69	SW_R(0)	AD7/P47/S0	70	SW_R(1)	AD6/P46/S1
71	SW(8)	P87/S8	72	SW(9)	P86/S9
73	COM[2]	COM2	74	COM[3]	COM3
75	SW(10)	P85/S10	76	SW(11)	P84/S11
77	COM[0]	COM0	78	COM[1]	COM1
79	SW(12)	P93/S12	80	SW(13)	P82/S13

Remark: The meaning of the symbols and figures in the Emulation Probe column is as follows:
 GND: Ground clip
 NC: Not connected
 1–80: Emulation probe tip pin numbers

Table C-2: Connector CN11 to Emulation Probe

No.	Signal Name	Function	No.	Signal Name	Function
81	GND13		82	GND14	
83	VLC[0]	VLCD	84	NC11	
85	SW(14)	P81/S14	86	NC12	
87	NC13		88	NC14	
89	NC15		90	NC16	
91	SM23_P26	SM23/P26	92	SM24_P27	SM24/P27
93	SW(24)	S24/S13/P37	94	SW(23)	S23/TI22/P90
95	GND15		96	GND16	
97	SM21_P24	SM21/P4	98	SM22_P25	SM22/P25
99	SW(22)	S22/TIO51/P91	100	SW(21)	S21/TPO/P92
101	SM13_P22	SM13/P22	102	SM14_P23	SM14/P23
103	SW(20)	S20/P93	104	SW(19)	S19/P94
105	SM11_P20	SM11/P20	106	SM12_P21	SM12/P21
107	SW(18)	S18/P95	108	SW(17)	S17/P96
109	GND17		110	GND18	
111	GND	SMVss	112	SMVDD	SMVDD
113	SW(16)	S16/P97	114	SW(15)	S15/P80
115	NC17		116	NC18	
117	NC19		118	NC20	
119	GND19		120	GND20	

Remark: The meaning of the symbols and figures in the Emulation Probe column is as follows:
 GND: Ground clip
 NC: Not connected
 1–80: Emulation probe tip pin numbers

[Memo]

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