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RENESAS

User's Manual

IE-703114-MC-EM1

In-Circuit Emulator Option Board

Target Device
V850E/IA2

Document No. U16533EJ1V0UM00 (1st edition)
Date Published September 2003 N CP(K)

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- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
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J03.4

INTRODUCTION

Target Readers

This manual is intended for users who wish to design and develop application systems using the V850E/IA2.

Purpose

This manual is intended to give users an understanding of the basic specifications and the proper operation of the IE-703114-MC-EM1.

Organization

This manual is broadly divided into the following parts.

- Overview
- Names and functions of components
- Factory settings
- Cautions
- Differences between target device and target interface circuit

How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electrical engineering, logic circuits, and microcontrollers.
The IE-703114-MC-EM1 is used connected to the IE-V850E-MC in-circuit emulator. This manual explains the basic setup procedure and switch settings of the IE-703114-MC-EM1. For the names and functions of the IE-V850E-MC, and the connection of parts, refer to the **IE-V850E-MC, IE-V850E-MC-A User's Manual (U14487E)**, which is a separate volume.

To broadly understand the basic specifications and operation methods
→ Read this manual in the order of the **CONTENTS**.

To know the operation methods and command functions of the IE-V850E-MC, and IE-703114-MC-EM1
→ Read the user's manual of the debugger (sold separately) that is used.

Conventions

Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numerical representation:	Binary ··· ×××× or ××××B
	Decimal ··· ××××
	Hexadecimal ··· ××××H
Prefix indicating the power of 2 (address space, memory capacity):	
	K (kilo): 2^{10} = 1,024
	M (mega): 2^{20} = $1,024^2$

Terminology The meanings of terms used in this manual are listed below.

Target device	This is the device to be emulated.
Target system	The system (user-built system) to be debugged. This includes the target program and hardware configured by the user.
Emulation CPU	This is the device that performs emulation of the target device in the IE-V850E-MC.

Related Documents When using this manual, refer to the following manuals.
The related documents indicated in this publication may include preliminary versions.
However, preliminary versions are not marked as such.

○ **Documents related to development tools (user's manuals)**

Product Name		Document Number
IE-V850E-MC, IE-V850E-MC-A (In-Circuit Emulator)		U14487E
IE-703114-MC-EM1 (In-Circuit Emulator Option Board)		This manual
V850E/IA2 Hardware		U15195E
V850 Series Development Tools (Tutorial Guide)		U14218E
CA850 (Ver.2.50 or Later) (C Compiler Package)	Operation	U16053E
	C Language	U16054E
	PM plus	U16055E
	Assembly Language	U16042E
ID850 (Ver.2.50) (Integrated Debugger)	Operation	To be prepared
SM850 (Ver.2.50) (System Simulator)	Operation	To be prepared
SM850 (Ver.2.00 or Later) (System Simulator)	External Part User Open Interface Specifications	U14873E
RX850 (Ver.3.13 or Later) (Real-Time OS)	Basics	U13430E
	Installation	U13410E
	Technical	U13431E
RX850 Pro (Ver.3.13) (Real-Time OS)	Basics	U13773E
	Installation	U13774E
	Technical	U13772E
RD850 (Ver. 3.01) (Task Debugger)		U13737E
RD850 Pro (Ver. 3.01) (Task Debugger)		U13916E
AZ850 (Ver. 3.10) (System Performance Analyzer)		U14410E
V850 Series Development Tools (Supporting 32-Bit OS) (Application Note)	Tutorial Guide (Windows® Based)	U16544E

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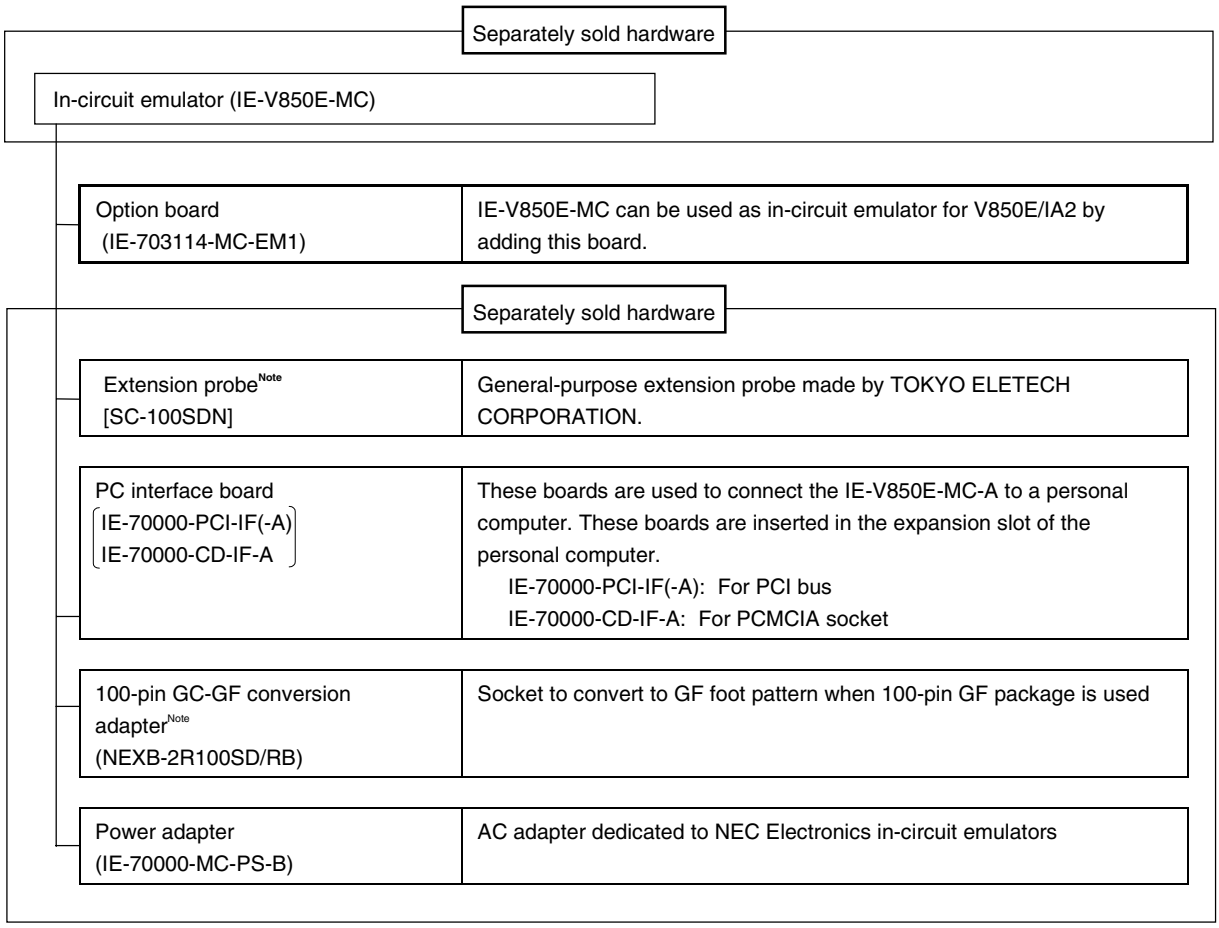
CHAPTER 1 OVERVIEW

The IE-703114-MC-EM1 is an option board for the in-circuit emulator IE-V850E-MC. By connecting the IE-703114-MC-EM1 to the IE-V850E-MC, hardware and software can be debugged efficiently in system development using the V850E/IA2.

In this manual, the basic setup procedures and switch settings of the IE-703114-MC-EM1 when connecting it to the IE-V850E-MC are described. For the names and functions of the parts of the IE-V850E-MC, and for the connection of parts, refer to the **IE-V850E-MC, IE-V850E-MC-A User's Manual (U14487E)** which is a separate volume.

1.1 Hardware Configuration



Note For further information, contact Daimaru Kogyo Co., Ltd.
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1.2 Hardware Specifications (When Connected to IE-V850E-MC)

Table 1-1. Hardware Specifications

Parameter		Value
Target device		μPD703114GC-xxx-8EU (mask ROM version 0.5 mm pitch) μPD70F3114GC-8EU (flash memory version 0.5 mm pitch) μPD703114GF-xxx-3BA (mask ROM version 0.65 mm pitch) μPD70F3114GF-3BA (flash memory version 0.65 mm pitch)
Target interface voltage		V_{DD} = RV_{DD} = AV_{DD0} = AV_{DD1} = 5.0 V ±10% REGIN = 3.0 to 3.6 V
Maximum operating frequency		40 MHz
External dimensions (Refer to **APPENDIX A DIMENSIONS**)	Height	28 mm
	Length	229 mm
	Width	96 mm
Power consumption		9.1 W (Max.)
Weight		190 g

- Extremely lightweight and compact.
- Higher equivalence with target device can be achieved by omitting buffer between signal cables.
- 8-bit external trace can be performed by connecting external logic probe (included).
- The following pins can be masked.
  $\overline{\text{RESET}}$, NMI, $\overline{\text{WAIT}}$

1.3 System Specifications of IE-703114-MC-EM1 (When Connected to IE-V850E-MC)

Table 1-2. System Specifications of IE-703114-MC-EM1 (When Connected to IE-V850E-MC)

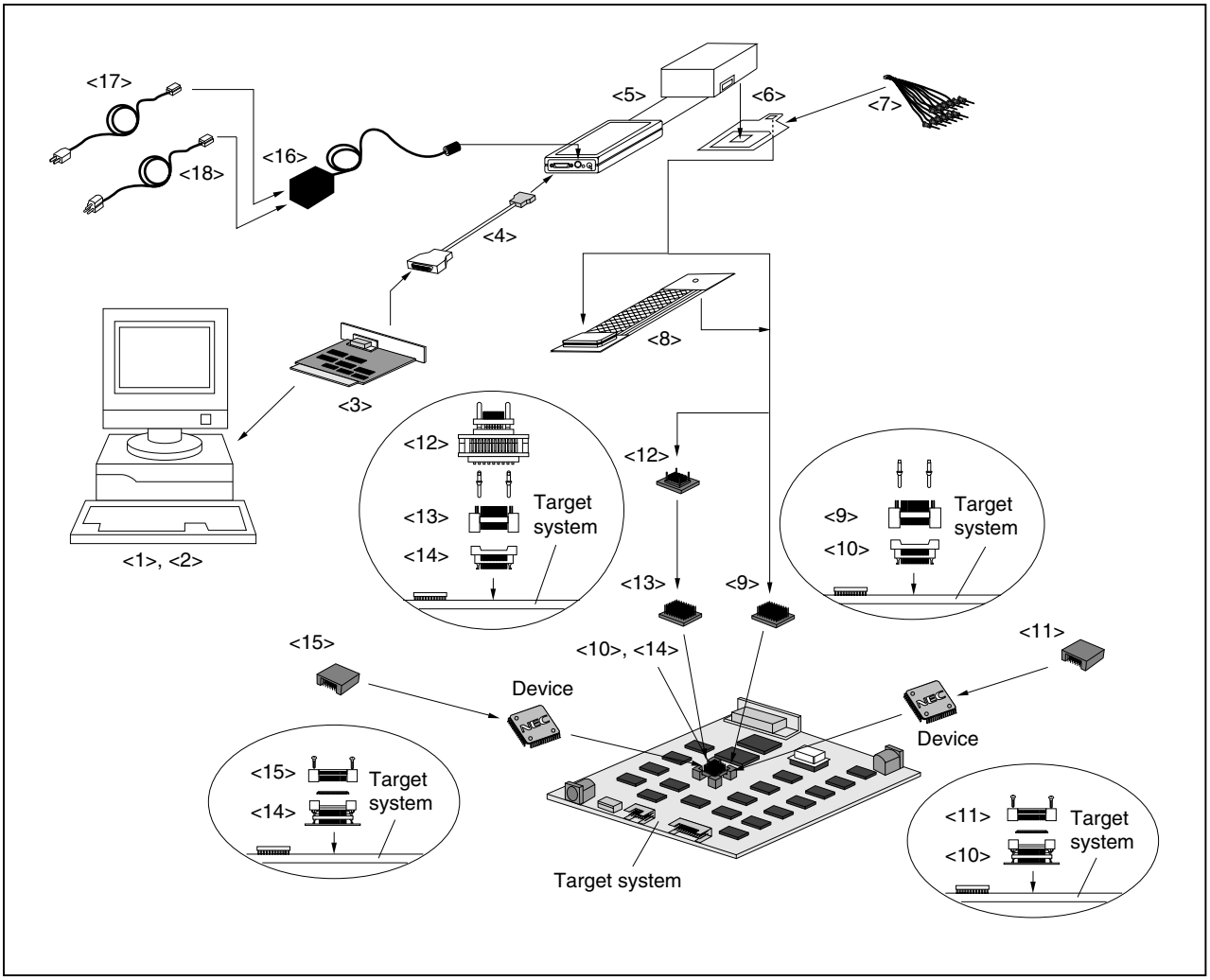
Parameter		Specification
Emulation memory capacity	Internal ROM	128 KB
	External memory	4 MB
Execution/pass detection coverage	Targeting internal ROM	128 KB
Program execution function	Real-time execution function	Go, Execution from cursor position, Automatic Go, Execution up to cursor position, Restart, Return-out
	Non real-time execution function	Step-in, Next-over, Slow motion
Break function		Event detection break, software break, forcible break, break by Come function, break when condition is satisfied during step execution, fail-safe break
Trace function	Trace conditions	All trace, section trace, qualify trace
	Memory capacity	168 bit × 32 K frames
Other functions		Mapping function, event function, snapshot function, stub function, register manipulation function, memory manipulation function, time measurement function, real-time RAM sampling function

Caution Some of the functions may not be supported depending on the debugger used.

1.4 System Configuration

The system configuration when connecting the IE-703114-MC-EM1 to the IE-V850E-MC, which is then connected to a personal computer (PC-9800 series, PC/AT™ or compatibles) is shown below.

Figure 1-1. System Configuration



Remark 1. <1> Personal computer (PC-9800 series, PC/AT or compatible)
<2> Debugger (sold separately), device file[Note]
<3> PC interface board (IE-70000-PCI-IF(-A), IE-70000-CD-IF-A: Sold separately)
<4> PC interface cable (included with IE-V850E-MC)
<5> In-circuit emulator (IE-V850E-MC: Sold separately)
<6> In-circuit emulator option board (IE-703114-MC-EM1)
<7> External logic probe (included)
<8> Extension probe (SC-100SDN: Sold separately)
<9> Connector for GC package emulator connection (YQPACK100SD: Included)
<10> Connector for GC package target connection (NQPACK100SD: Included)
<11> GC package device mount cover (HQPACK100SD: Included)
<12> GF package conversion adapter (NEXB-2R100SD/RB: Sold separately)

<13> Connector for GF package emulator connection (YQPACK100RB: Included with NEXB-2R100SD/RB)
<14> Connector for GC package target connection (NQPACK100RB: Included with NEXB-2R100SD/RB)
<15> GF package device mount cover (HQPACK100RB: Included with NEXB-2R100SD/RB)
<16> Power adapter (IE-70000-MC-PS-B: Sold separately)
<17> 100-V AC power cable (sold separately: Included with IE-70000-MC-PS-B)
<18> 220-V AC power cable (sold separately: Included with IE-70000-MC-PS-B)

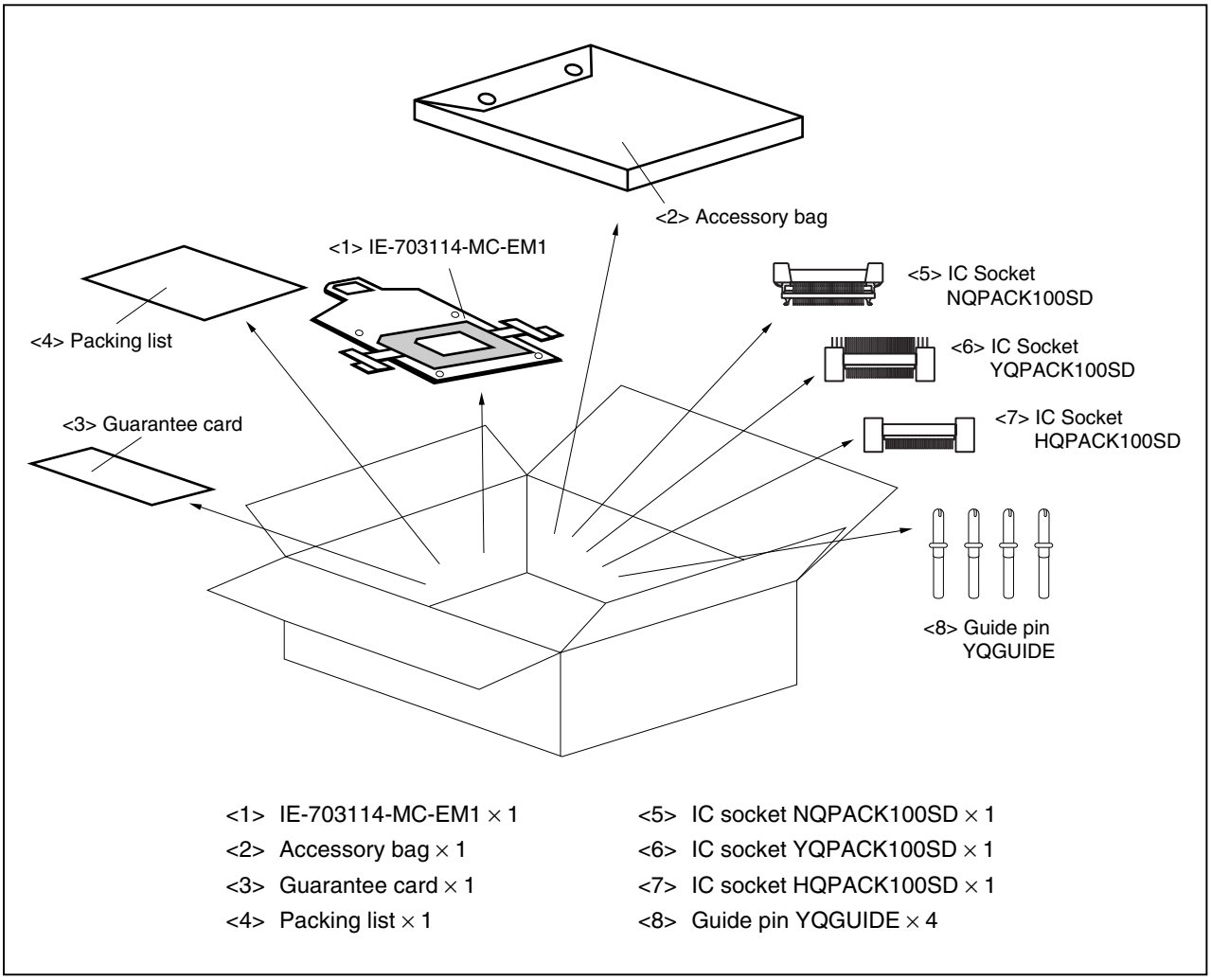
Remark 2. The circled areas in the above figure are the enlargements of the connectors for target connection.

Note Obtain the device file from the website of NEC Electronics (http://www.necel.com/micro/)..

1.5 Contents in Carton

The carton of the IE-703114-MC-EM1 contains the main unit, guarantee card, packing list, and accessory bag. Make sure that the accessory bag contains this manual and connector accessories. In case of missing or damaged items, contact an NEC Electronics sales representative or distributor.

Figure 1-2. Contents in Carton



Check that the accessory bag contains this manual, a packing list, an external logic probe, and a restriction document.

1.6 Connection Between IE-V850E-MC and IE-703114-MC-EM1

The procedure for connecting the IE-V850E-MC and IE-703114-MC-EM1 is described below.

Caution Do not break or bend connector pins.

<1> Remove the pod cover (lower) of the IE-V850E-MC.
<2> Set the PGA socket lever of the IE-703114-MC-EM1 to the OPEN position as shown in Figure 1-3 (b).
<3> Connect the IE-703114-MC-EM1 to the PGA socket at the rear of the pod (refer to Figure 1-3 (c)). When connecting, position the IE-V850E-MC and IE-703114-MC-EM1 so that they are horizontal.
Spacers can be connected to fix the pod (refer to **APPENDIX D MOUNTING PLASTIC SPACER**).
<4> Set the PGA socket lever of the IE-703114-MC-EM1 to the CLOSE position as shown in Figure 1-3 (b).
<5> Fix the IE-703114-MC-EM1 between the pod cover (lower) with the nylon rivets supplied with the IE-V850E-MC.

Figure 1-3. Connection Between IE-V850E-MC and IE-703114-MC-EM1 (1/2)

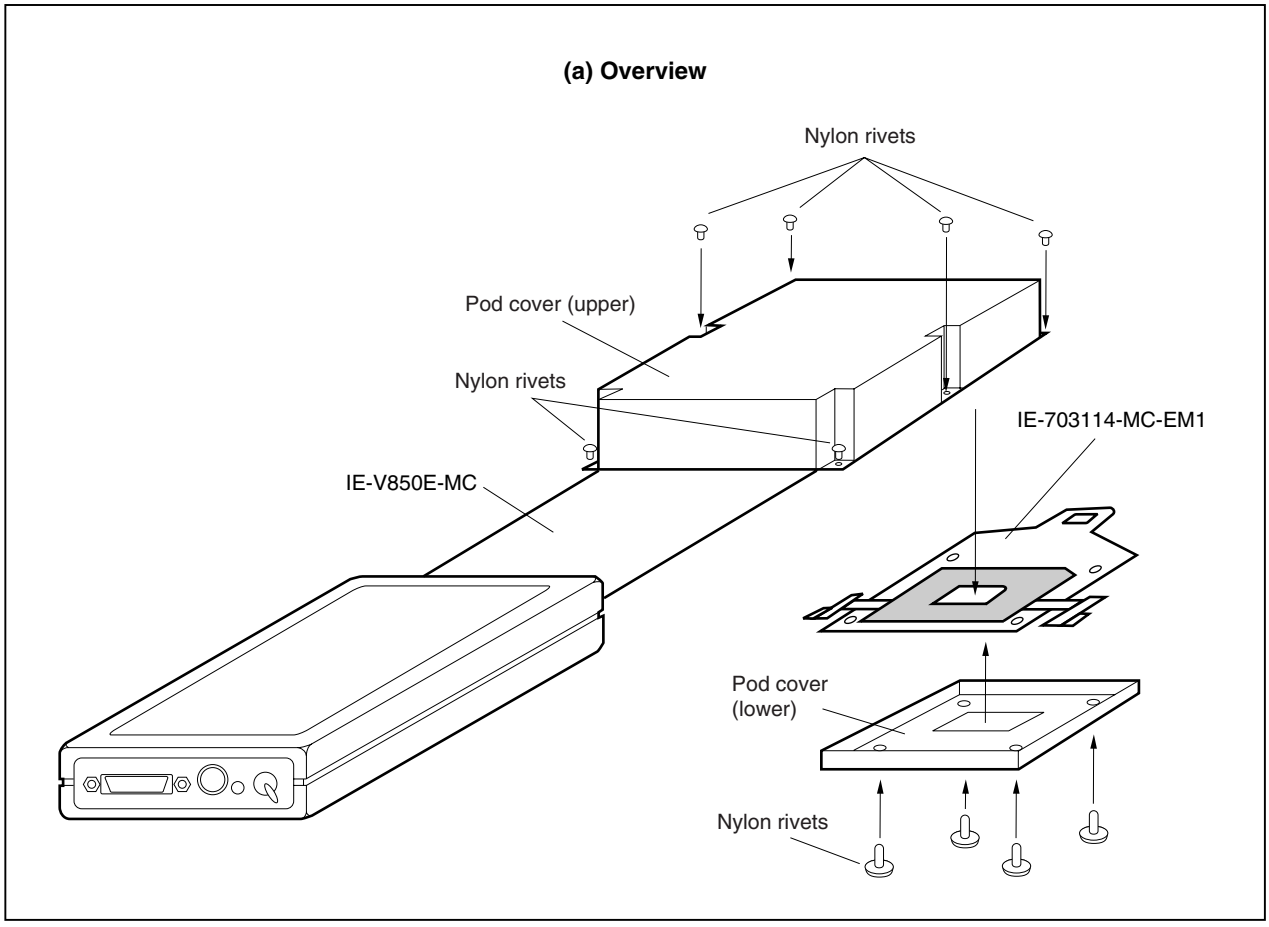
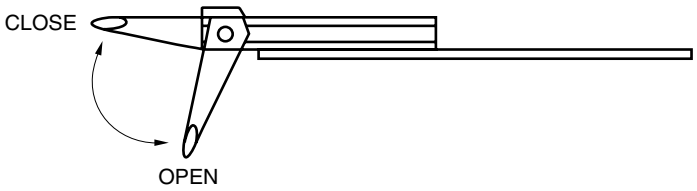
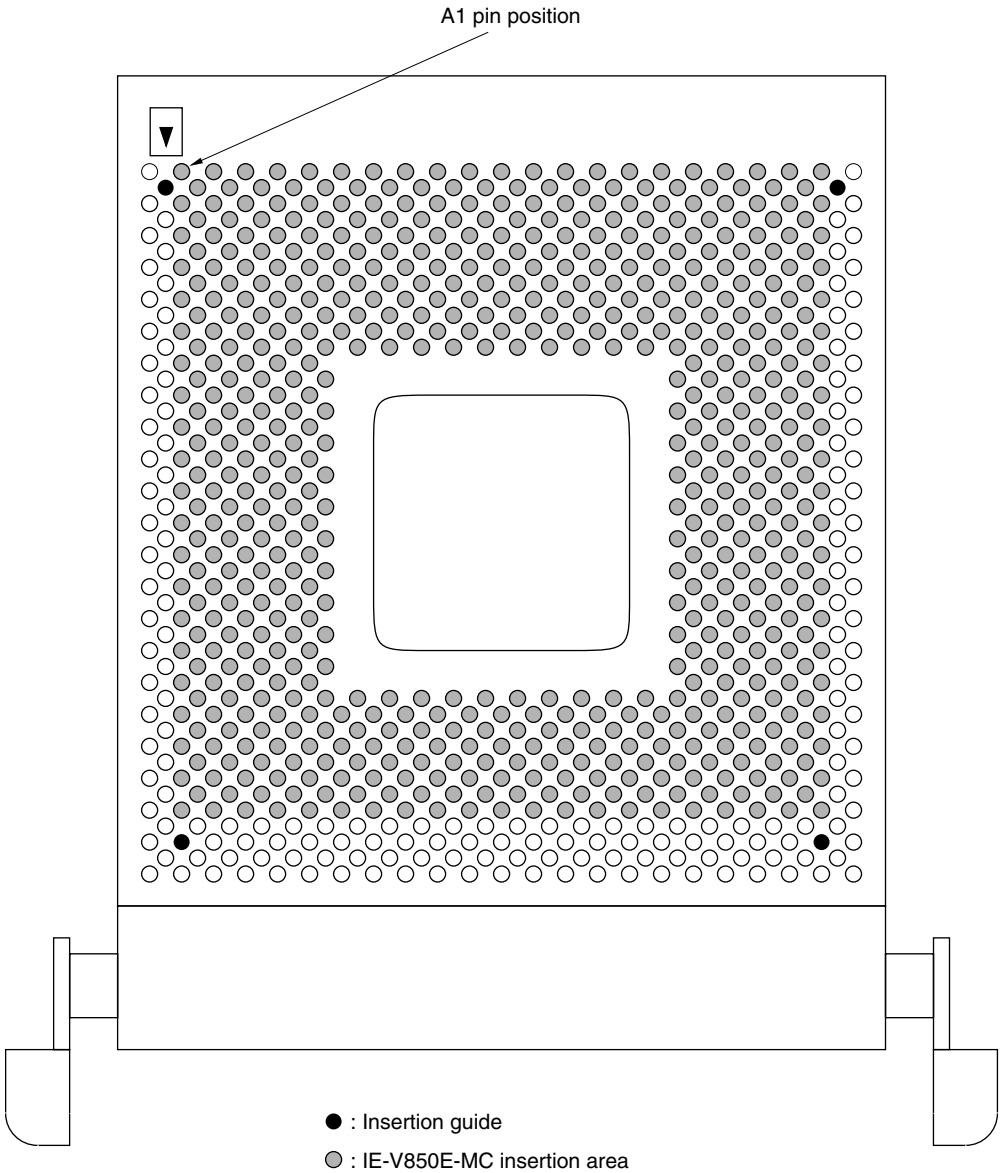


Figure 1-3. Connection Between IE-V850E-MC and IE-703114-MC-EM1 (2/2)

(b) PGA socket lever of IE-703114-MC-EM1



(c) Connecting part (IE-703114-MC-EM1)

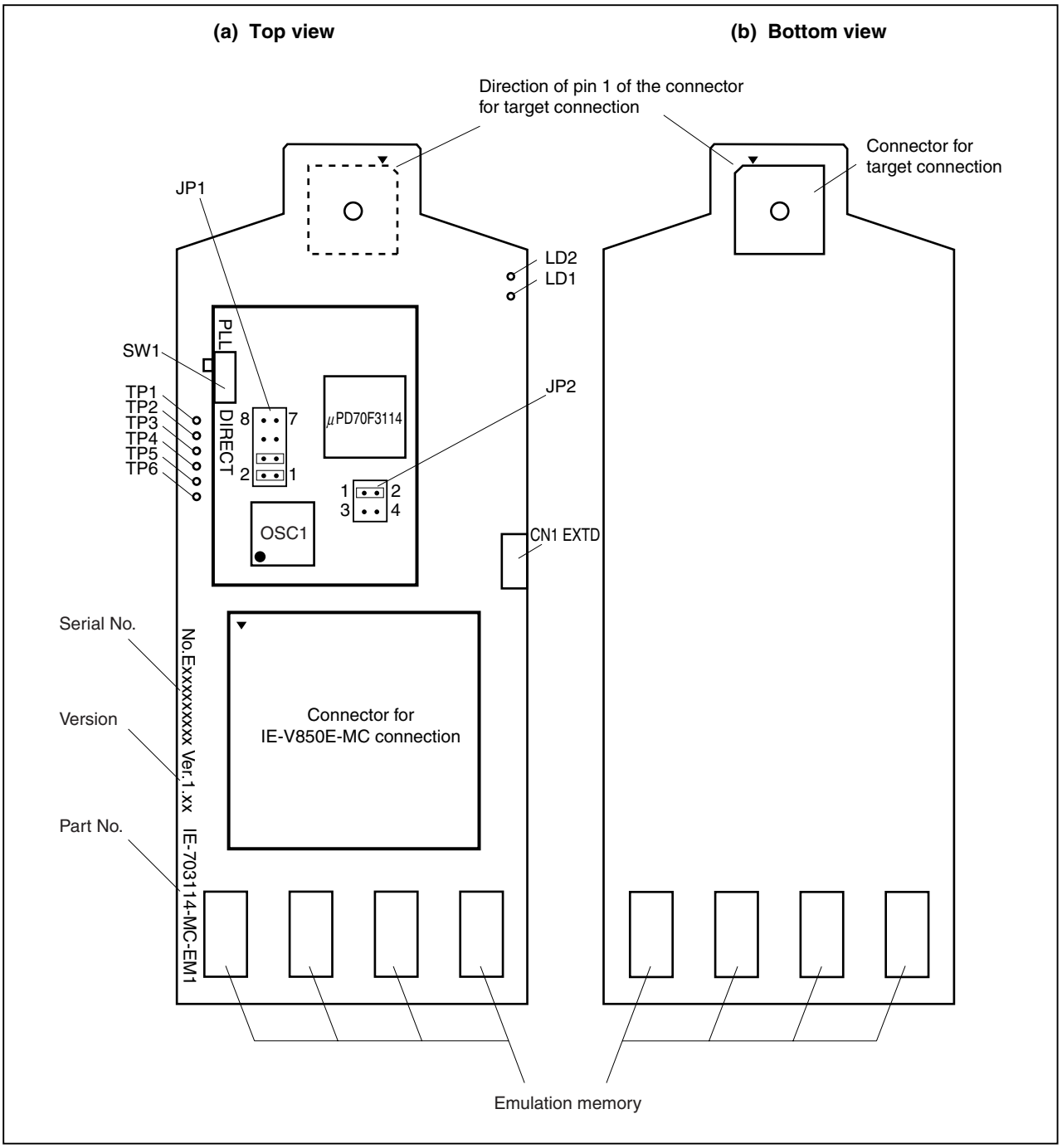


CHAPTER 2 NAMES AND FUNCTIONS OF COMPONENTS

This chapter describes the names, functions, and switch settings of components comprising the IE-703114-MC-EM1. For the details of the pod, jumper, and switch positions, etc., refer to the **IE-V850E-MC**, **IE-V850E-MC-A User's Manual (U14487E)**.

2.1 Component Names and Functions of IE-703114-MC-EM1

Figure 2-1. IE-703114-MC-EM1



(1) Test pins (TP1 to TP6)

To leave the DMA cycle in the tracer, or to set a break, connect these pins to the external logic probe.

- TP1: GND
- TP2: Test pin for product shipment test
- TP3: DMAAK0
- TP4: DMAAK1
- TP5: DMAAK2
- TP6: DMAAK3

(2) SW1

This is a switch for clock mode switching (for details, refer to **2.2 Clock Settings**).

(3) JP1

This is a jumper for switching the clock supply source (for details, refer to **2.2 Clock Settings**).

(4) JP2

This is a jumper for switching the power supply (for details, refer to **2.4 Power Supply Settings**).

(5) CN1 EXTD

Connects the external logic probe (included).

(6) LD1 (CKSEL: Green)

This is an LED for indicating the level input to the CKSEL pin. When the target system is not connected, this is lit or extinguished according to the SW1 setting.

LED Status	When Used as Standalone Unit	When Used in Target System Connection
Lit	SW1 = DIRECT	The CKSEL signal from the target system is high
Extinguished	SW1 = PLL	The CKSEL signal from the target system is low

(7) LD2 (RUN: Yellow)

This is an LED for indicating if a user program is being executed or not.

LED Status	
Lit	User program is being executed.
Extinguished	User program is halted.

(8) Connector for IE-V850E-MC connection

This is a connector for connecting the IE-V850E-MC.

(9) Connector for target connection

This is a connector for connecting the target system or the extension probe.

(10) Emulation memory

This is a memory that replaces the memory/memory mapped I/O on the target system (for details, refer to **2.5 Emulation Memory**).

2.2 Clock Settings

2.2.1 Clock settings outline

The following 3 clock setting methods are available.

For details, refer to **2.2.2 Clock setting methods**.

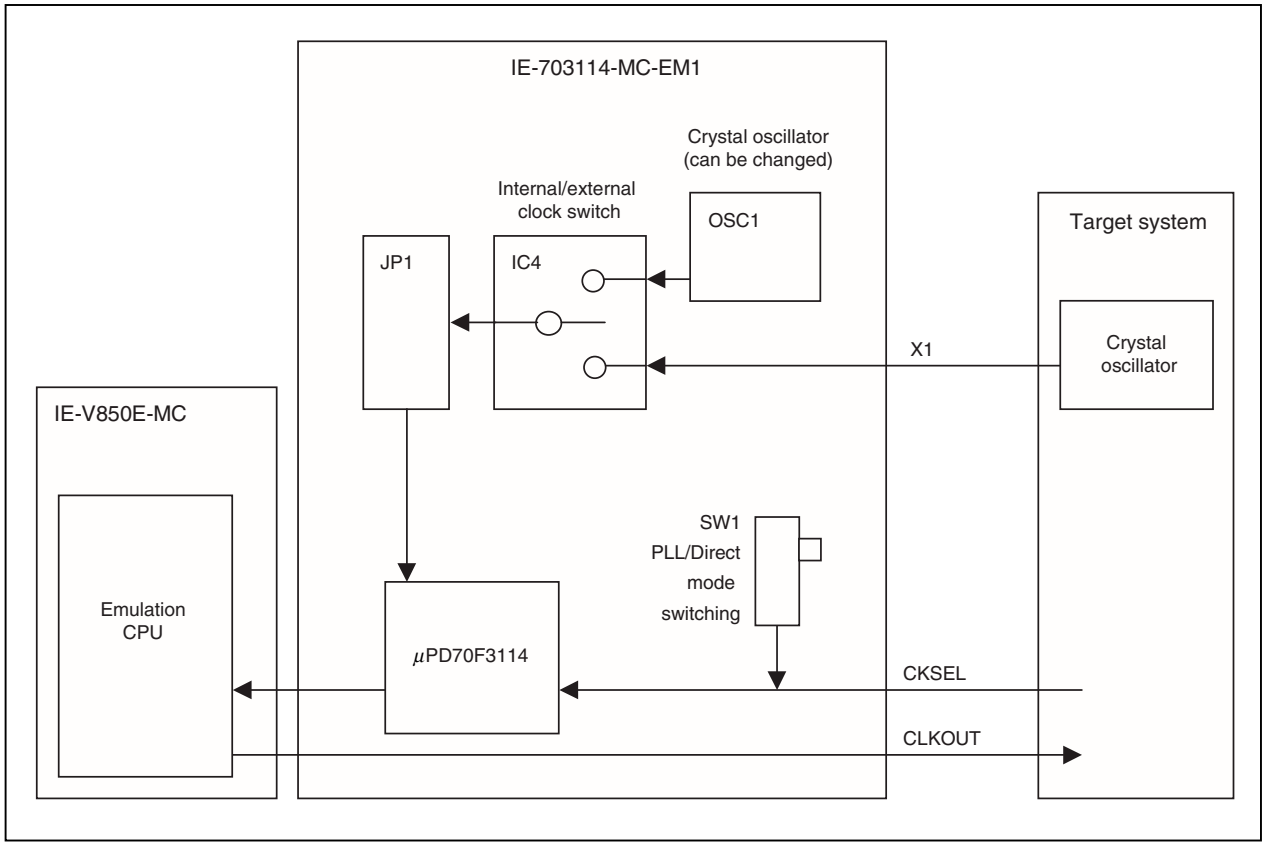
(1) Use the crystal oscillator mounted on OSC1 of the IE-703114-MC-EM1 as the internal clock.

(2) Change the crystal oscillator mounted on OSC1 of the IE-703114-MC-EM1 the replacement oscillator as the internal clock.

(3) Use the crystal oscillator on the target system as an external clock (clock input from target system).

Caution When using an external clock, input the clock generated by the crystal oscillator to the X1 pin. When a clock generated by a crystal/ceramic resonator is used, the emulator does not operate normally.

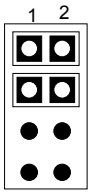
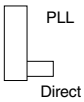
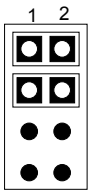
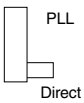
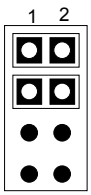
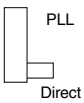
Figure 2-2. Clock Setting Outline



2.2.2 Clock setting methods

A list of the hardware settings when setting the clock is shown below.

Table 2-1. List of Hardware Settings When Setting Clock

Type of Clock Used	Clock Source Selection[Note 1]	OSC1 Crystal Oscillator	JP1 Setting	Clock Mode	SW1	CKSEL Pin[Note 2]
(1) Use crystal oscillator (OSC1) mounted on IE-703114-MC-EM1 as internal clock.	Internal	Factory settings (4.000 MHz)		PLL		Low-level input
				Direct		High-level input
(2) Change crystal oscillator (OSC1) mounted on IE-703114-MC-EM1 and use new oscillator as the internal clock.	Internal	Change (to other than 4.000 MHz)		PLL		Low-level input
				Direct		High-level input
(3) Use the crystal oscillator on the target system as an external clock.	External	Crystal oscillator can be either mounted or not mounted		PLL		Low-level input
				Direct		High-level input

Notes 1. Select the clock source in the clock source selection area in the configuration dialog box on the debugger.

2. The input setting for the CKSEL pin is made only when a target system is connected. Leave this pin open when operating the emulator on a standalone basis. The emulator operates according to the SW1 setting.

3. When changing the crystal oscillator on the emulator, choose an oscillator that satisfies the conditions described below.

Power supply voltage	5 V
Output level	CMOS
Type	8-pin type
Pin positions	Pin 1: NC, Pin 4: GND, Pin 5: OUT, Pin 8: V_{DD}

4. For cautions related to using an external clock, refer to the V850E/IA2 Hardware User's Manual (U15195E).

Caution Settings other than those described above are prohibited.

(1) Using the crystal oscillator (OSC1) mounted on the IE-703114-MC-EM1 as the internal clock

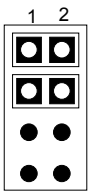
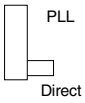
<1> Mount the 4.000 MHz crystal oscillator mounted at factory shipment in the OSC1 socket of the IE-703114-MC-EM1 (with the default settings).

<2> Change JP1 as indicated in Table 2-2 (with the default settings).

<3> Set the SW1 and CKSEL pins according to the clock mode to be used, as shown in Table 2-2.

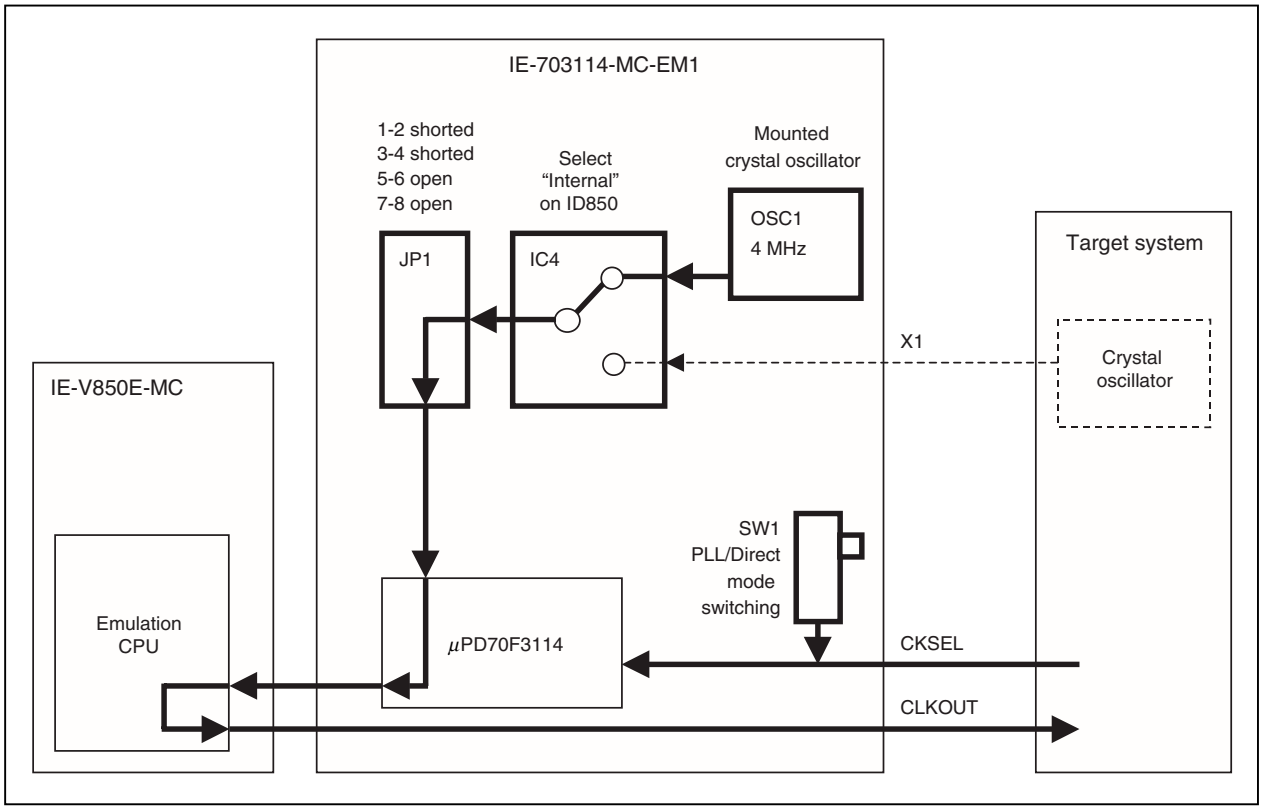
<4> To start up the integrated debugger (ID850), select “Internal” in the clock source selection area in the configuration dialog box (selection of clock in emulator).

Table 2-2. Settings When Using Mounted Internal Clock

Type of Clock Used	Clock Source Selection	OSC1 Crystal Oscillator	JP1 Setting	Clock Mode	SW1	CKSEL Pin[Note]
Use crystal oscillator (OSC1) mounted on IE-703114-MC-EM1 as internal clock.	Internal	Factory setting (4.000 MHz)		PLL		Low-level input
				Direct		High-level input

Note The input setting for the CKSEL pin is made only when a target system is connected. Leave this pin open when operating the emulator on a standalone basis.

Figure 2-3. Outline When Using Mounted Internal Clock



(2) Changing the crystal oscillator (OSC1) mounted on the IE-703114-MC-EM1 and using the new oscillator as the internal clock

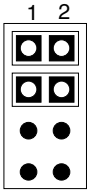
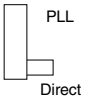
<1> Remove the crystal oscillator (OSC1) that is mounted on the IE-703114-MC-EM1 and mount the oscillator to be used.

<2> Set JP1 as shown in Table 2-3 (factory settings).

<3> Set the SW1 and CKSEL pins according to the clock mode to be used, as shown in Table 2-3.

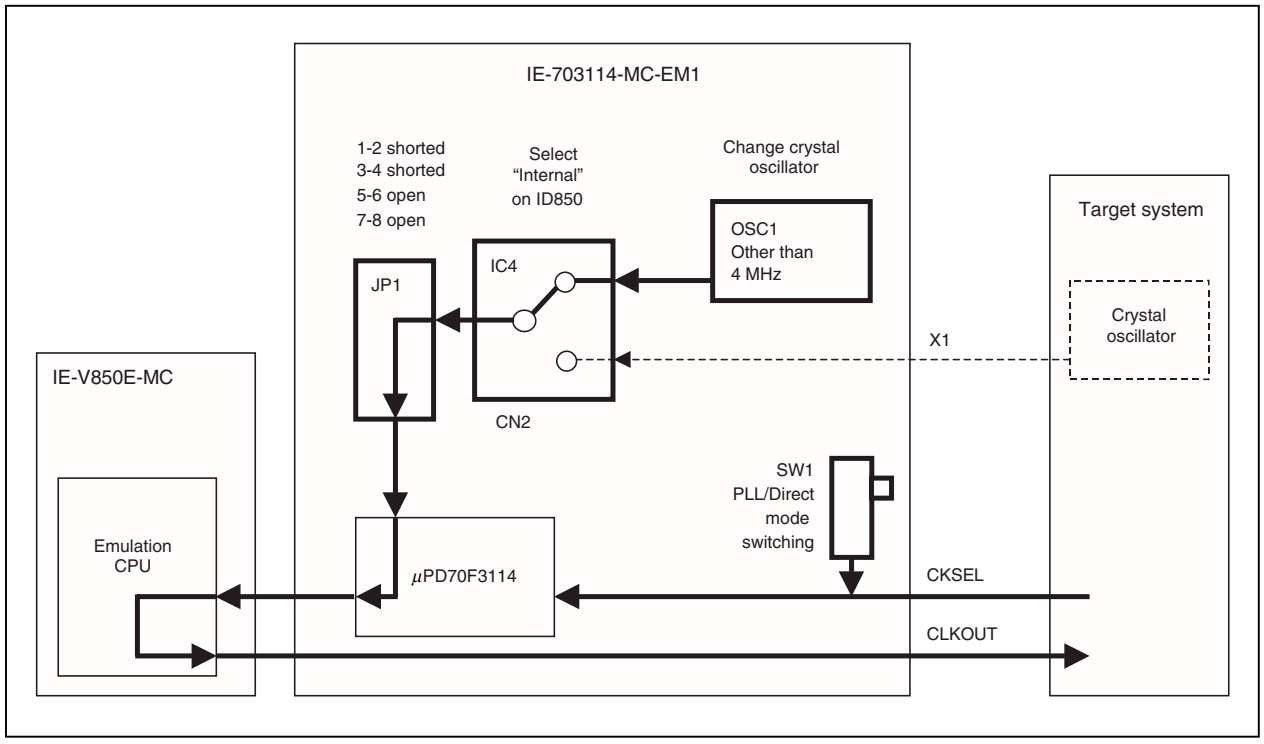
<4> Select “Internal” in the clock source selection area in the configuration dialog box on the integrated debugger (ID850).

Table 2-3. Settings When Changing Mounted Internal Clock

Type of Clock Used	Clock Source Selection	OSC1 Crystal Oscillator	JP1 Setting	Clock Mode	SW1	CKSEL pin[Note]
Change the crystal oscillator mounted on IE-703114-MC-EM1 and use the new oscillator as the internal clock.	Internal	Change (to other than 4.000 MHz)	1 2  7 8	PLL		Low-level input
				Direct		High-level input

Note The input setting for the CKSEL pin is made only when a target system is connected. Leave this pin open when operating the emulator on a standalone basis.

Figure 2-4. Outline When Changing Mounted Crystal Oscillator and Using New Oscillator as Internal Clock



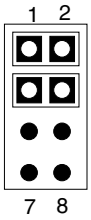
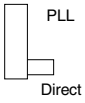
(3) Using the target system crystal oscillator as an external clock

<1> Set JP1 as shown in Table 2-4 (factory setting).

<2> Set the SW1 and CKSEL pins according to the clock mode to be used, as shown in Table 2-4.

<3> Select “External” in the clock source selection area in the configuration dialog box on the integrated debugger (ID850).

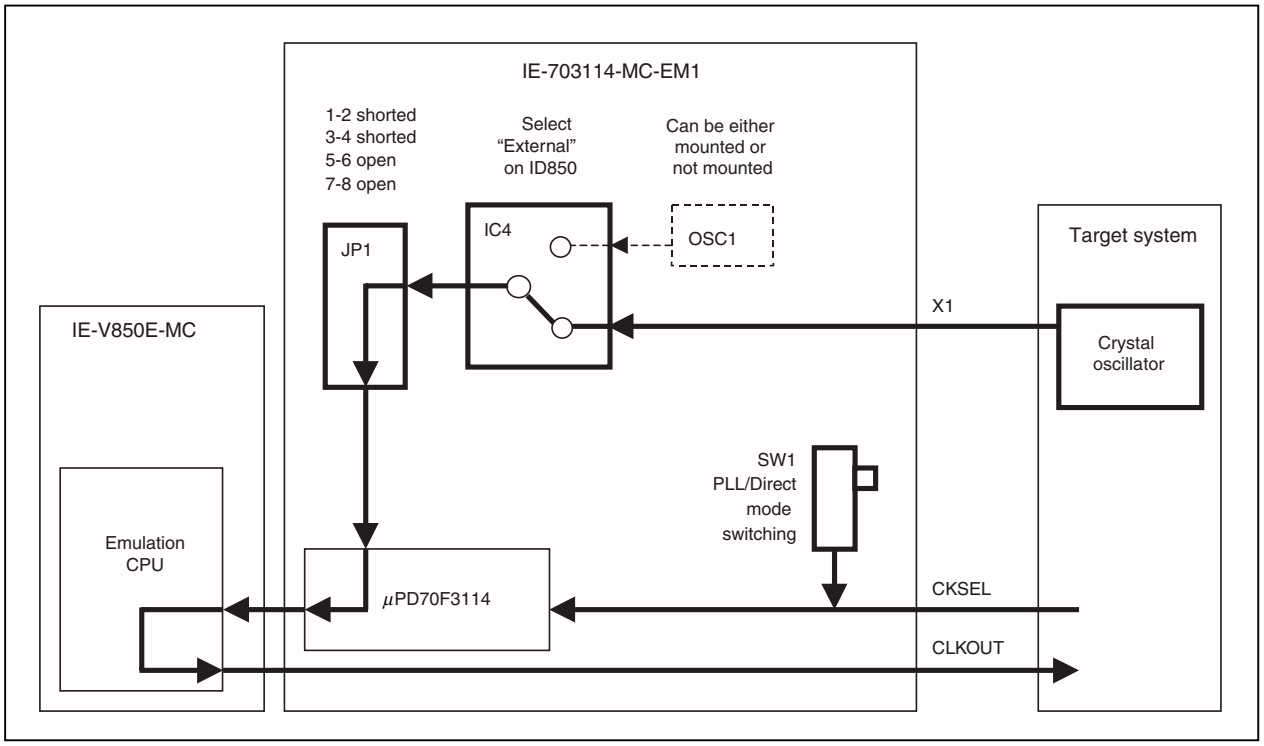
Table 2-4. Settings When Using External Clock

Type of Clock Used	Clock Source Selection	OSC1 Crystal Oscillator	JP1 Setting	Clock Mode	SW1	CKSEL Pin[Note]
Use crystal oscillator on target system as external clock.	External	Crystal oscillator can be either mounted or not mounted		PLL		Low-level input
				Direct		High-level input

Note The input setting for the CKSEL pin is made only when a target system is connected. Leave this pin open when operating the emulator on a standalone basis.

Caution Be sure to input a clock generated by a crystal oscillator to the X1 pin.
When a clock generated by a crystal/ceramic resonator is used, the emulator does not operate normally.

Figure 2-5. Outline When Using Crystal Oscillator on Target System as External Clock



2.3 Operation Mode Setting

The IE-703114-MC-EM1 supports single-chip mode and ROMless mode, similar to the V850E/IA2. Set these as follows.

Set as follows in the configuration dialog box mask setting area in accordance with the operation mode used when the integrated debugger (ID850) is activated.

Operation in ROMless mode: Select Mode00
Operation in single-chip mode: Select Mode02

Caution In ROMless mode, be sure to start mapping emulation memory from address 0H if the emulator is not connected to the target system.

Emulation of the MODE pin cannot be performed since the input level to the MODE pin is implemented using the debugger pin mask function in the IE-703114-MC-EM1.

For the settings of the pins on the target system, refer to the **V850E/IA2 Hardware User's Manual (U15195E).**

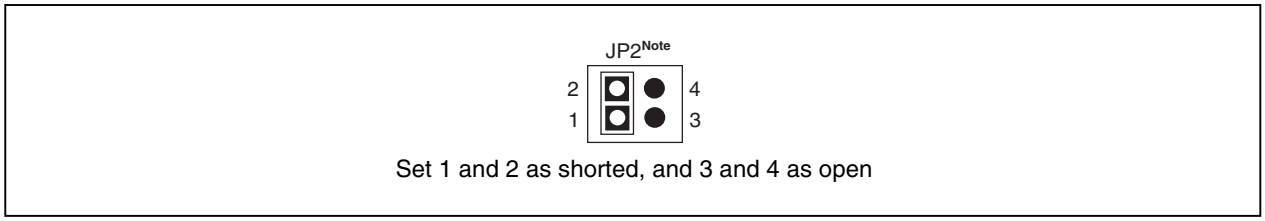
2.4 Power Supply Settings

2.4.1 JP2 setting

When JP2 is set as shown in Figure 2-6, the IE-703114-MC-EM1 detects the power supply on the target board and automatically switches whether the emulator operates on VDD from the target system or the emulator's internal power supply. (Factory setting)

Caution If the JP2 setting is incorrect, the emulator may be damaged.

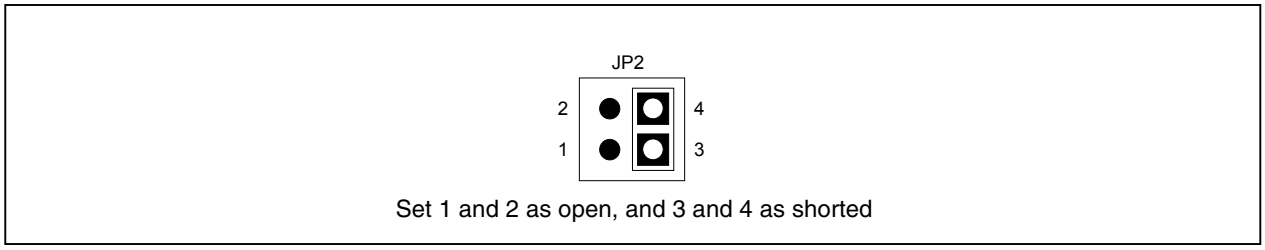
Figure 2-6. JP2 Setting (Automatic Switching Setting)



Note A relay is used for switching the power supply. Depending on the combinations with the target system, the relay may repeatedly turn on/off, making a continuous switching sound, when the target system is turned off. In such a case, set JP2 as shown in Figure 2-7.

When JP2 is set as shown in Figure 2-7, V_{DD} is always supplied from the target system. Note that, with this setting, the emulator does not operate when the target system is not connected.

Figure 2-7. JP2 setting (When Power from Target System Is Used)



2.5 Emulation Memory

This is a substitute memory used to emulate the memory or memory mapped I/O on the target system (capacity: 4 MB).

The emulation memory is mounted on the IE-703114-MC-EM1.

2.5.1 Wait setting for emulation memory

The data wait, address wait, and idle state for the emulation memory are set as follows.

(1) ID850

Select from the following three types on the configuration screen.

Selection	Wait Type	Emulation Memory Access	External Memory Access
WAIT MASK	Data wait	Fixed to 0 waits	Depends on DWC 0, 1 register setting WAIT signal masked
	Address wait	Fixed to 0 waits	Depends on AWC register setting
	Idle state	Fixed to 0 cycles	Depends on BCC register setting
1 WAIT ACCESS	Data wait	Fixed to 1 wait	Depends on DWC 0, 1 register setting and WAIT signal status
	Address wait	Fixed to 0 waits	Depends on AWC register setting
	Idle state	Fixed to 0 cycles	Depends on BCC register setting
TARGET WAIT	Data wait	Depends on DWC 0, 1 register setting However, 1 wait when set to 0 waits	Depends on DWC, 0, 1 register setting and WAIT signal status
	Address wait	Fixed to 0 waits	Depends on ASC register setting
	Idle state	Depends on BCC register setting	Depends on BCC register setting

(2) MULTI

Select mask or unmask for WAIT and EMWAIT using the “Pinmask” command.

Selection	Wait Type	Emulation Memory Access	External Memory Access
WAIT: Mask EMWAIT: Mask	Data wait	Fixed to 0 waits	Depends on DWC 0, 1 register setting WAIT signal masked
	Address wait	Fixed to 0 waits	Depends on AWC register setting
	Idle state	Fixed to 0 cycles	Depends on BCC register setting
WAIT: Unmask EMWAIT: Mask	Data wait	Fixed to 1 wait	Depends on DWC 0, 1 register setting and WAIT signal status
	Address wait	Fixed to 0 waits	Depends on AWC register setting
	Idle state	Fixed to 0 cycles	Depends on BCC register setting
WAIT: Unmask EMWAIT: Unmask	Data wait	Depends on DWC 0, 1 register setting However, 1 wait when set to 0 waits	Depends on DWC 0, 1 register setting and WAIT signal status
	Address wait	Fixed to 0 waits	Depends on AWC register setting
	Idle state	Depends on BCC register setting	Depends on BCC register setting

2.5.2 Cautions related to emulation memory

(1) Number of data waits required for emulation memory access

The number of data waits that must be inserted for emulation memory access varies depending on the operating frequency of the emulator.

4 MHz ≤ Operating frequency < 25 MHz	0 waits
25 MHz ≤ Operating frequency < 40 MHz	1 wait
40 MHz = Operating frequency	2 waits

(2) Bus sizing

Make the bus sizing 16 bits (set BSn0 in the BSC register to 1).

An 8-bit bus cannot be used.

(3) $\overline{\text{WAIT}}$ pin

The number of data waits for the emulation memory is not affected by the $\overline{\text{WAIT}}$ pin.

(4) Address wait

Address waits cannot be inserted in the emulation memory.

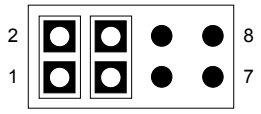
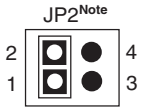
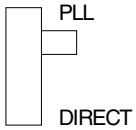
When address waits need to be inserted, set as follows.

Number of data waits for CS space of emulation memory	=	Number of address waits for external memory or external I/O	+	Number of data waits for external memory or external I/O

This setting is effective to make the access speed to the emulation memory equal to that of the external memory or external I/O to measure the performance, etc.

For how to insert waits in the emulation memory, refer to **2.5.1 Wait setting for emulation memory**.

CHAPTER 3 FACTORY SETTINGS

Item	Setting	Remark
JP1		Settings other than those shown here are prohibited.
JP2		Setting that detects the power supply on the target board and switches automatically whether the emulator operates on V_{DD} from the target system or on the emulator's internal power supply.
SW1		Set to PLL mode.
Crystal oscillator (OSC1)	4.000 MHz crystal oscillator is mounted.	The frequency can be changed by changing the crystal resonator.

CHAPTER 4 CAUTIONS

4.1 Cautions Related to Pin Termination

The following shows the pins that need special processing in the emulator.

For the detailed circuit configuration, refer to **CHAPTER 5 DIFFERENCES BETWEEN TARGET DEVICE AND TARGET INTERFACE CIRCUIT**.

(1) Pins that cannot be emulated

The following pins are left open in the emulator, so they cannot be emulated.

Evaluate them by using the target device.

Table 4-1. Pins That Cannot Be Emulated

Pin Name 1	Pin Name 2	Package	Pin No.
MODE0	–	GC (14 × 14)	12
		GF (14 × 20)	14
MODE1	V_{PP}	GC (14 × 14)	62
		GF (14 × 20)	64
REGIN	–	GC (14 × 14)	16
		GF (14 × 20)	18
X2	–	GC (14 × 14)	18
		GC (14 × 14)	20

(2) $\overline{\text{RESET}}$ pin

The $\overline{\text{RESET}}$ pin is connected (pulled-up) to V_{DD} via a 33 kΩ resistor.

(3) X1 pin

When using an external clock, the X1 pin is pulled down via a 33 kΩ resistor.

The input to the clock generator is delayed by up to 13.2 ns because it passes through 74HC157 first.

When using an internal clock, this pin is pulled down via a 33 kΩ resister and left open.

(4) CKSEL pin

Pull-up/pull-down can be switched by SW1.

When “PLL” is selected by SW1, this pin is pulled down via a 33 kΩ resistor. When “DIRECT” is selected, it is pulled up via a 33 kΩ resistor.

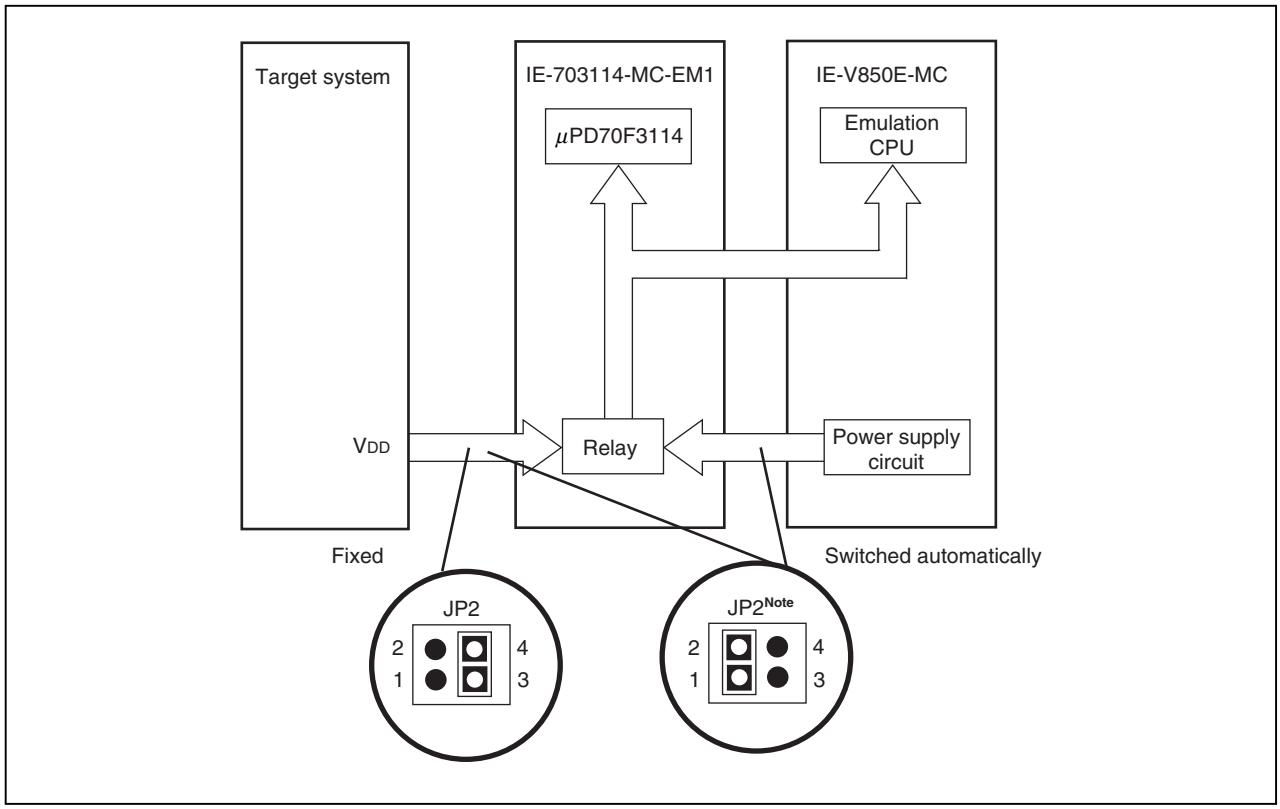
(5) V_{DD} pin

(1) V_{DD} in the target system is used to operate the circuit in the emulator.

(2) When JP2 is set as “1 and 2 open” and “3 and 4 shorted”, the evaluation chip in the emulator operates on V_{DD} from the target system.

(3) When JP2 is set as “1 and 2 open” and “3 and 4 open”, the emulator recognizes the target system power is off and operates with the 3.3 V power supply.

Figure 4-1. Schematic Diagram of Power Supply Flow



4.2 Cautions Related to Internal RAM

In the emulator, the internal RAM is mapped at the 12 KB space 0xFFFC000 to 0xFFFEFFF.

Since the V850E/IA2 is mapped at the 6 KB space 0xFFFC000 to 0xFFFD7FF, the target system is not mapped at the higher 6 KB space in the internal RAM (0xFFFD800 to 0xFFFEFFF).

Therefore, measures must be taken such as setting access breaks beforehand because if the higher 6 KB space is accessed, the emulator cannot issue a fail-safe break.

CHAPTER 5 DIFFERENCES BETWEEN TARGET DEVICE AND TARGET INTERFACE CIRCUIT

This chapter describes the equivalent circuits in the emulator for signals of the emulator connected to the target system. Note that, depending on the processing within the emulator, some pins cannot be emulated (refer to CHAPTER 4 CAUTIONS).

Figures 5-1 to 5-8 show the equivalent circuits.

Tables 5-1 to 5-8 list the pins corresponding to each equivalent circuit.

Figure 5-1. Pin Equivalent Circuit 1

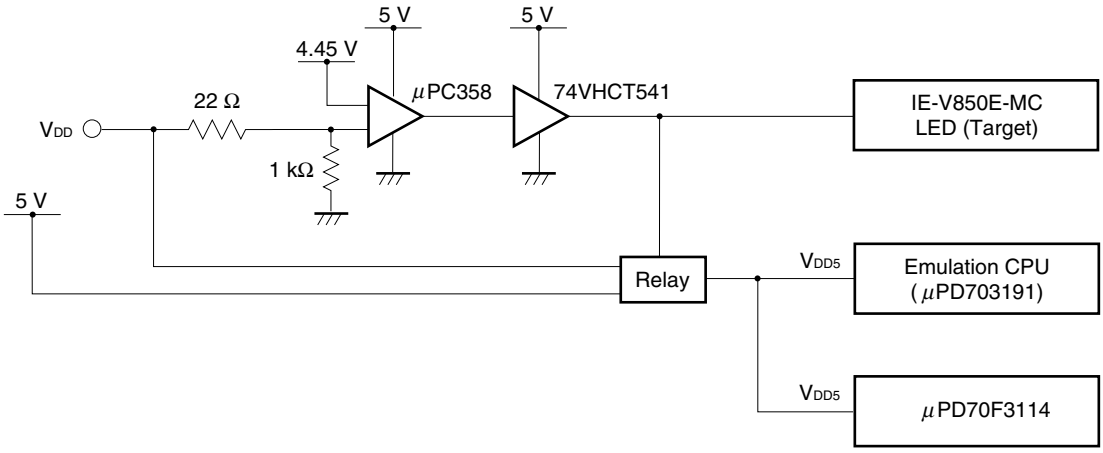


Table 5-1. Corresponding Pins (Pin Equivalent Circuit 1)

Pin Name 1	Package	Pin No.
V_{DD}	GC (14 × 14)	39, 64, 86
	GF (14 × 20)	41, 66, 88

Figure 5-2. Pin Equivalent Circuit 2

Table 5-2. Corresponding Pins (Pin Equivalent Circuit 2)

Pin Name 1	Pin Name 2	Package	Pin No.	Pin Name 1	Pin Name 2	Package	Pin No.
PDL0	AD0	GC (14 × 14)	40	PDL14	AD14	GC (14 × 14)	54
		GF (14 × 20)	42			GF (14 × 20)	56
PDL1	AD1	GC (14 × 14)	41	PDL15	AD15	GC (14 × 14)	55
		GF (14 × 20)	43			GF (14 × 20)	57
PDL2	AD2	GC (14 × 14)	42	PDH0	A16	GC (14 × 14)	56
		GF (14 × 20)	44			GF (14 × 20)	58
PDL3	AD3	GC (14 × 14)	43	PDH1	A17	GC (14 × 14)	57
		GF (14 × 20)	45			GF (14 × 20)	59
PDL4	AD4	GC (14 × 14)	44	PDH2	A18	GC (14 × 14)	58
		GF (14 × 20)	46			GF (14 × 20)	60
PDL5	AD5	GC (14 × 14)	45	PDH3	A19	GC (14 × 14)	59
		GF (14 × 20)	47			GF (14 × 20)	61
PDL6	AD6	GC (14 × 14)	46	PDH4	A20	GC (14 × 14)	60
		GF (14 × 20)	48			GC (14 × 14)	62
PDL7	AD7	GC (14 × 14)	47	PDH5	A21	GC (14 × 14)	61
		GF (14 × 20)	49			GC (14 × 14)	63
PDL8	AD8	GC (14 × 14)	48	PCT0	$\overline{\text{LWR}}$	GC (14 × 14)	65
		GF (14 × 20)	50			GF (14 × 20)	67
PDL9	AD9	GC (14 × 14)	49	PCT1	$\overline{\text{UWR}}$	GC (14 × 14)	66
		GF (14 × 20)	51			GF (14 × 20)	68
PDL10	AD10	GC (14 × 14)	50	PCT4	$\overline{\text{RD}}$	GC (14 × 14)	67
		GF (14 × 20)	52			GF (14 × 20)	69
PDL11	AD11	GC (14 × 14)	51	PCT6	ASTB	GC (14 × 14)	68
		GF (14 × 20)	53			GF (14 × 20)	70
PDL12	AD12	GC (14 × 14)	52	PCM0	$\overline{\text{WAIT}}$	GC (14 × 14)	69
		GF (14 × 20)	54			GF (14 × 20)	71
PDL13	AD13	GC (14 × 14)	53	PCM1	CLKOUT	GC (14 × 14)	70
		GF (14 × 20)	55			GC (14 × 14)	72

Figure 5-3. Pin Equivalent Circuit 3

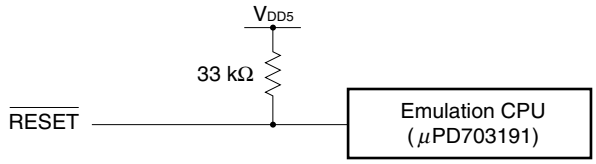


Table 5-3. Corresponding Pins (Pin Equivalent Circuit 3)

Pin Name 1	Package	Pin No.
$\overline{\text{RESET}}$	GC (14 × 14)	19
	GF (14 × 20)	21

Figure 5-4. Pin Equivalent Circuit 4

Table 5-4. Corresponding Pins (Pin Equivalent Circuit 4)

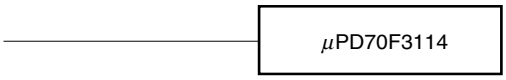
Pin Name 1	Pin Name 2	Package	Pin No.
AV_{SS1}	$\overline{\text{LWR}}$	GC (14 × 14)	3
		GF (14 × 20)	5
V_{SS3}	$\overline{\text{UWR}}$	GC (14 × 14)	13, 63
		GF (14 × 20)	15, 65
CV_{SS}	$\overline{\text{RD}}$	GC (14 × 14)	20
		GF (14 × 20)	22
V_{SS}	ASTB	GC (14 × 14)	38, 87
		GF (14 × 20)	40, 89
AV_{SS0}	$\overline{\text{WAIT}}$	GC (14 × 14)	95
		GF (14 × 20)	97

Figure 5-5. Pin Equivalent Circuit 5

Table 5-5. Corresponding Pins (Pin Equivalent Circuit 5)

Pin Name 1	Pin Name 2	Package	Pin No.
MODE0	–	GC (14 × 14)	12
		GF (14 × 20)	14
MODE1	V_{PP}	GC (14 × 14)	62
		GF (14 × 20)	64
REGIN	–	GC (14 × 14)	16
		GF (14 × 20)	18
X2	–	GC (14 × 14)	18
		GC (14 × 20)	20

Figure 5-6. Pin Equivalent Circuit 6



Remark For the corresponding pin names, refer to Table 5-6.

Table 5-6. Corresponding Pins (Pin Equivalent Circuit 6) (1/3)

Pin Name 1	Pin Name 2	Pin Name 3	Pin Name 4	Package	Pin No.
AV_{DD0}	–	–	–	GC (14 × 14)	94
				GF (14 × 20)	96
ANI00	–	–	–	GC (14 × 14)	96
				GF (14 × 20)	98
ANI01	–	–	–	GC (14 × 14)	97
				GF (14 × 20)	99
ANI02	–	–	–	GC (14 × 14)	98
				GF (14 × 20)	100
ANI03	–	–	–	GC (14 × 14)	99
				GF (14 × 20)	1
ANI04	–	–	–	GC (14 × 14)	100
				GF (14 × 20)	2
ANI05	–	–	–	GC (14 × 14)	1
				GF (14 × 20)	3
AV_{DD1}	–	–	–	GC (14 × 14)	2
				GF (14 × 20)	4
ANI10	–	–	–	GC (14 × 14)	4
				GF (14 × 20)	6
ANI11	–	–	–	GC (14 × 14)	5
				GF (14 × 20)	7
ANI12	–	–	–	GC (14 × 14)	6
				GF (14 × 20)	8
ANI13	–	–	–	GC (14 × 14)	7
				GF (14 × 20)	9
ANI14	–	–	–	GC (14 × 14)	8
				GF (14 × 20)	10
ANI15	–	–	–	GC (14 × 14)	9
				GF (14 × 20)	11
ANI16	–	–	–	GC (14 × 14)	10
				GF (14 × 20)	12
ANI17	–	–	–	GC (14 × 14)	11
				GF (14 × 20)	13
RV_{DD}	–	–	–	GC (14 × 14)	14
				GF (14 × 20)	16
REGOUT	–	–	–	GC (14 × 14)	15
				GF (14 × 20)	17
SI0	P40	–	–	GC (14 × 14)	22
				GF (14 × 20)	24
SO0	P41	–	–	GC (14 × 14)	23
				GF (14 × 20)	25
$\overline{SCK0}$	P42	–	–	GC (14 × 14)	24
				GF (14 × 20)	26
RXD0	P30	–	–	GC (14 × 14)	25
				GF (14 × 20)	27

Table 5-6. Corresponding Pins (Pin Equivalent Circuit 6) (2/3)

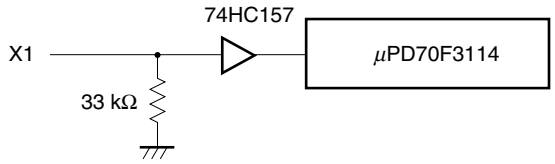
Pin Name 1	Pin Name 2	Pin Name 3	Pin Name 4	Package	Pin No.
TXD0	P31	–	–	GC (14 × 14)	26
				GF (14 × 20)	28
SI1	RXD1	P32	–	GC (14 × 14)	27
				GF (14 × 20)	29
SO1	TXD1	P33	–	GC (14 × 14)	28
				GF (14 × 20)	30
$\overline{\text{SCK1}}$	$\overline{\text{ASCK1}}$	P34	–	GC (14 × 14)	29
				GF (14 × 20)	31
TI2	INTP20	P20	–	GC (14 × 14)	30
				GF (14 × 20)	32
TO21	INTP21	P21	–	GC (14 × 14)	31
				GF (14 × 20)	33
TO22	INTP22	P22	–	GC (14 × 14)	32
				GF (14 × 20)	34
TO23	INTP23	P23	–	GC (14 × 14)	33
				GF (14 × 20)	35
TO24	INTP24	P24	–	GC (14 × 14)	34
				GF (14 × 20)	36
TCLR2	INTP25	P25	–	GC (14 × 14)	35
				GF (14 × 20)	37
TI3	INTP30	TCLR3	P26	GC (14 × 14)	36
				GF (14 × 20)	38
TO3	INTP31	P27	–	GC (14 × 14)	37
				GF (14 × 20)	39
TIUD10	TO10	P10	–	GC (14 × 14)	71
				GF (14 × 20)	73
TCUD10	INTP100	P11	–	GC (14 × 14)	72
				GF (14 × 20)	74
TCLR10	INTP101	P12	–	GC (14 × 14)	73
				GF (14 × 20)	75
NMI	P00	–	–	GC (14 × 14)	74
				GF (14 × 20)	76
ESO0	INTP0	P01	–	GC (14 × 14)	75
				GF (14 × 20)	77
ESO1	INTP1	P02	–	GC (14 × 14)	76
				GF (14 × 20)	78
ADTRG0	INTP2	P03	–	GC (14 × 14)	77
				GF (14 × 20)	79
ADTRG1	INTP3	P04	–	GC (14 × 14)	78
				GF (14 × 20)	80
INTP4	TO3OFF	P05	–	GC (14 × 14)	79
				GF (14 × 20)	81
TO000	–	–	–	GC (14 × 14)	80
				GF (14 × 20)	82

Table 5-6. Corresponding Pins (Pin Equivalent Circuit 6) (3/3)

Pin Name 1	Pin Name 2	Pin Name 3	Pin Name 4	Package	Pin No.
TO001	–	–	–	GC (14 × 14)	81
				GF (14 × 20)	83
TO002	–	–	–	GC (14 × 14)	82
				GF (14 × 20)	84
TO003	–	–	–	GC (14 × 14)	83
				GF (14 × 20)	85
TO004	–	–	–	GC (14 × 14)	84
				GF (14 × 20)	86
TO005	–	–	–	GC (14 × 14)	85
				GF (14 × 20)	87
TO010	–	–	–	GC (14 × 14)	88
				GF (14 × 20)	90
TO011	–	–	–	GC (14 × 14)	89
				GF (14 × 20)	91
TO012	–	–	–	GC (14 × 14)	90
				GF (14 × 20)	92
TO013	–	–	–	GC (14 × 14)	91
				GF (14 × 20)	93
TO014	–	–	–	GC (14 × 14)	92
				GF (14 × 20)	94
TO015	–	–	–	GC (14 × 14)	93
				GF (14 × 20)	95

Figure 5-7. Pin Equivalent Circuit 7

(a) When using an external clock



(b) When using an internal clock

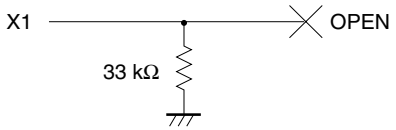
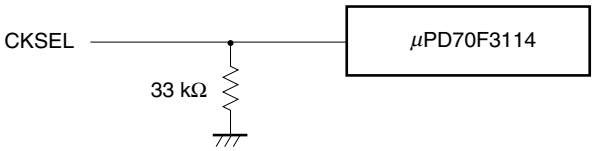


Table 5-7. Corresponding Pins (Pin Equivalent Circuit 7)

Pin Name 1	Package	Pin No.
X1	GC (14 × 14)	17
	GF (14 × 20)	19

Figure 5-8. Pin Equivalent Circuit 8

(a) When selecting PLL via SW1



(b) When selecting DIRECT via SW1

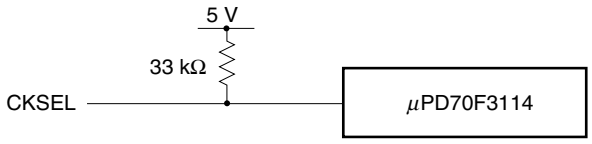
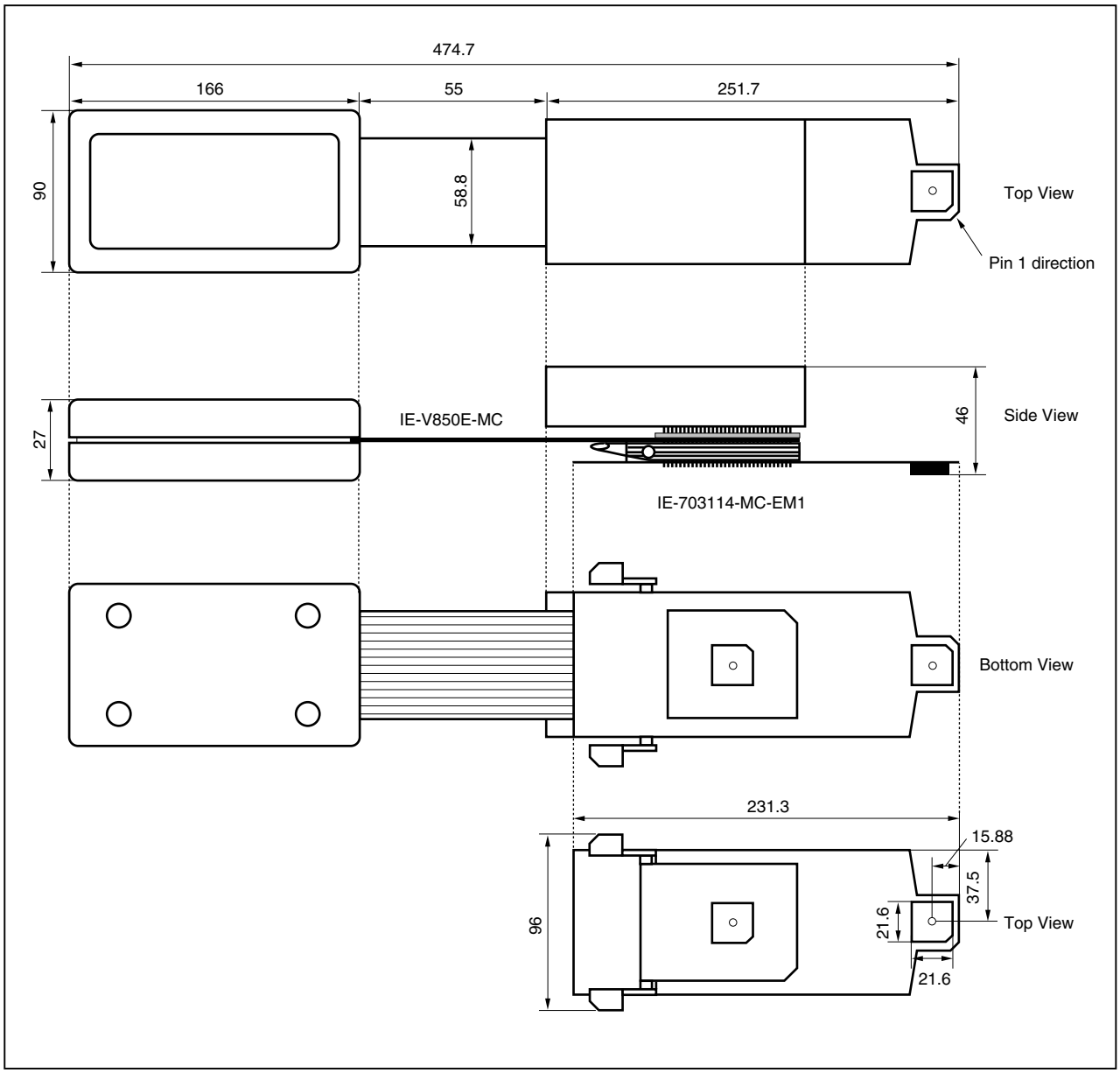


Table 5-8. Corresponding Pins (Pin Equivalent Circuit 8)

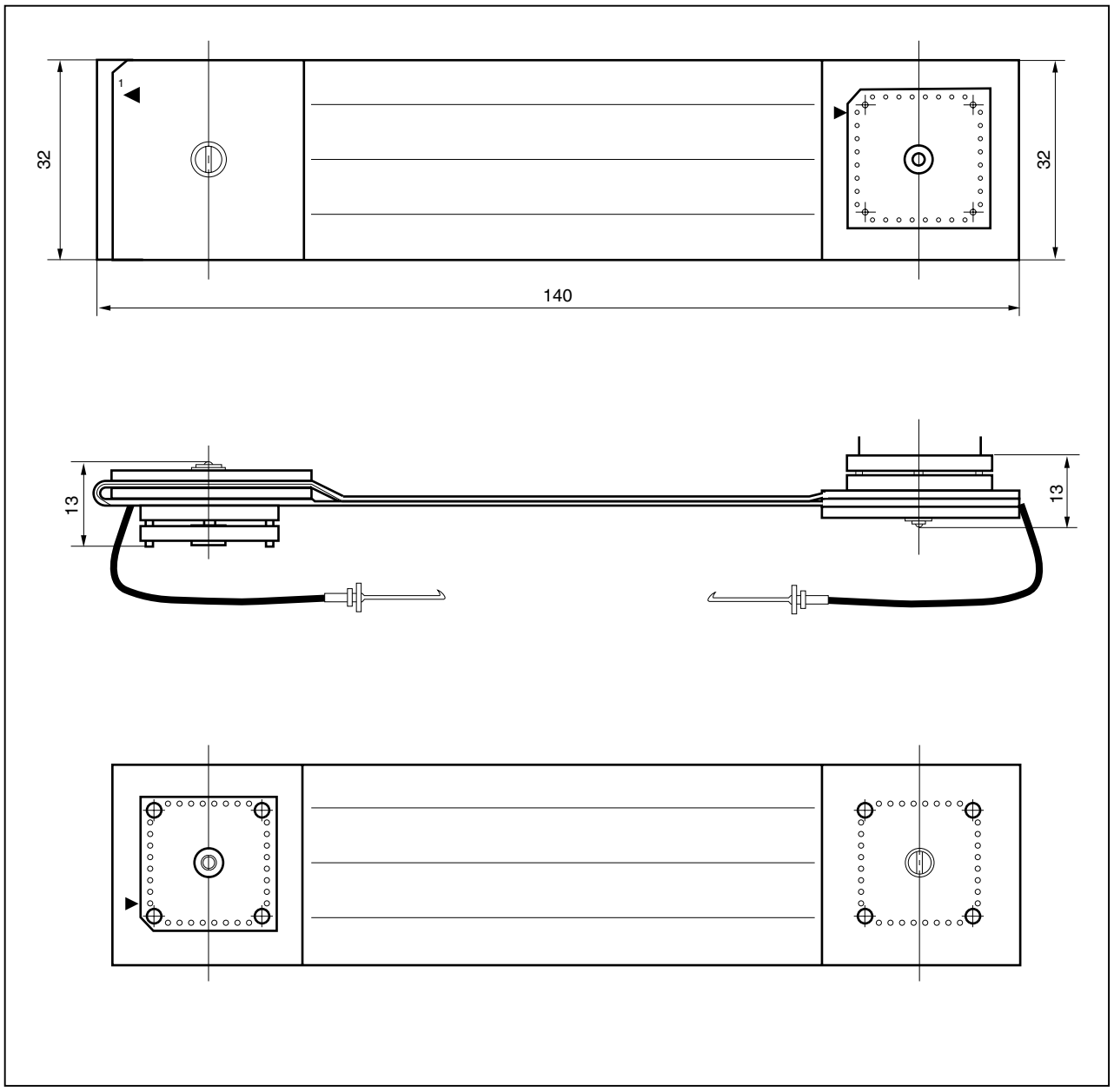
Pin Name 1	Package	Pin No.
CKSEL	GC (14 × 14)	21
	GF (14 × 20)	23

APPENDIX A DIMENSIONS

(1) IE-V850E-MC + IE-703114-MC-EM1 (Unit: mm)

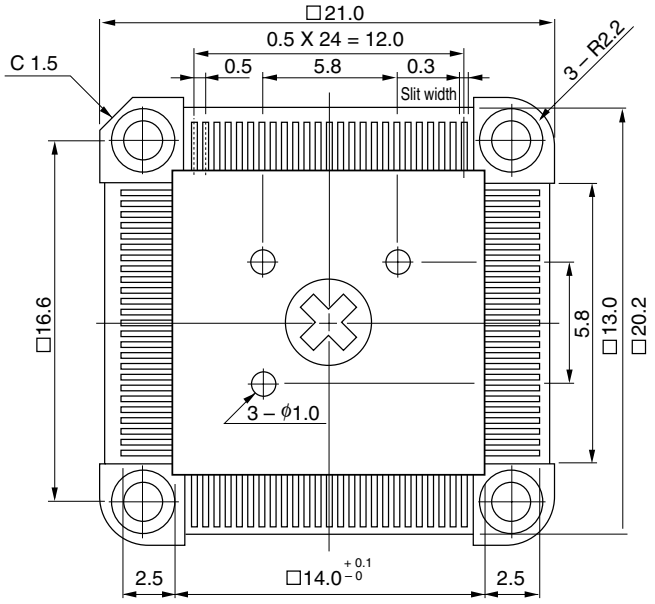


(2) SC-100SDN (Unit: mm)

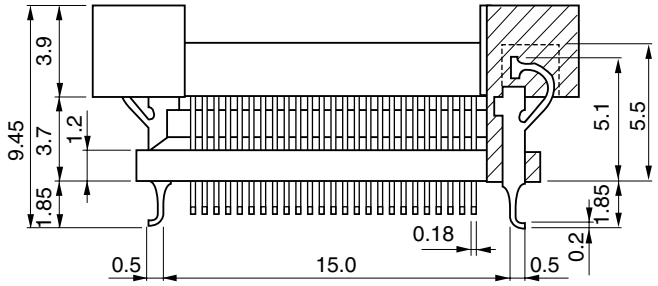


(3) NQPACK100SD (Unit: mm)

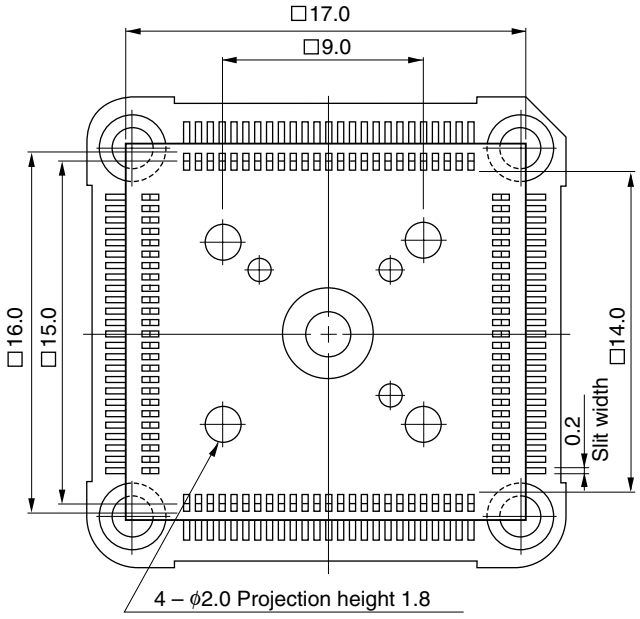
[Top view]



[Side view]

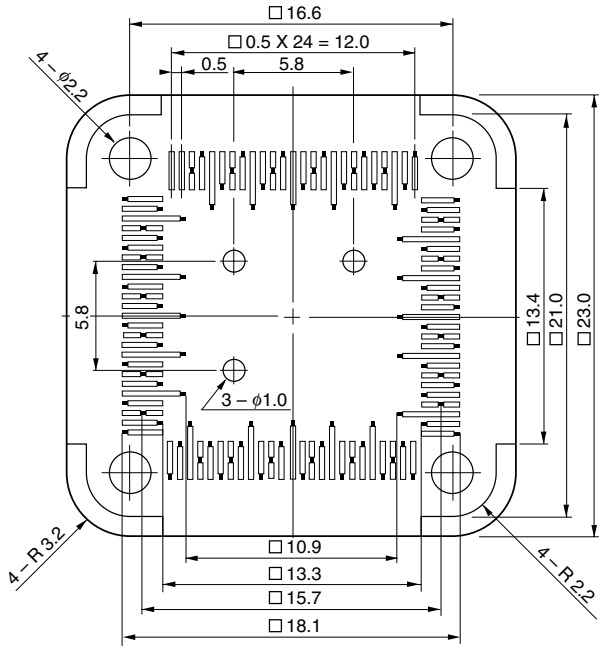


[Bottom view]

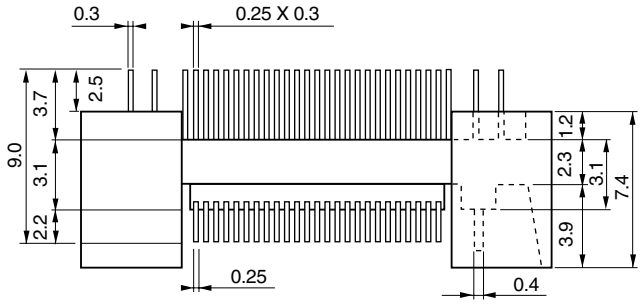


(4) YQPACK100SD (Unit: mm)

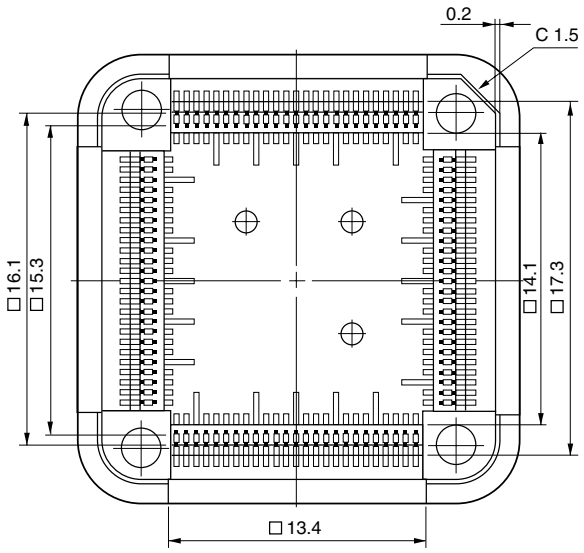
[Top view]



[Side view]

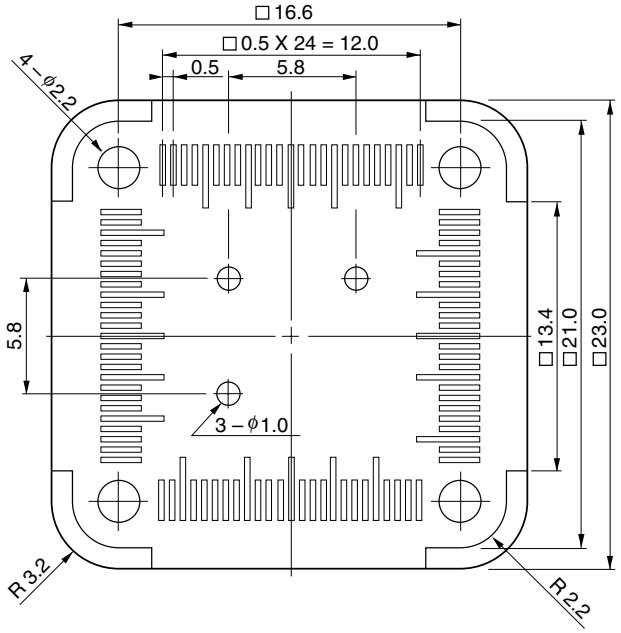


[Bottom view]

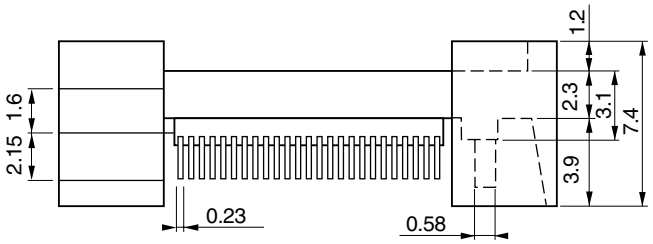


(5) HQPACK100SD (Unit: mm)

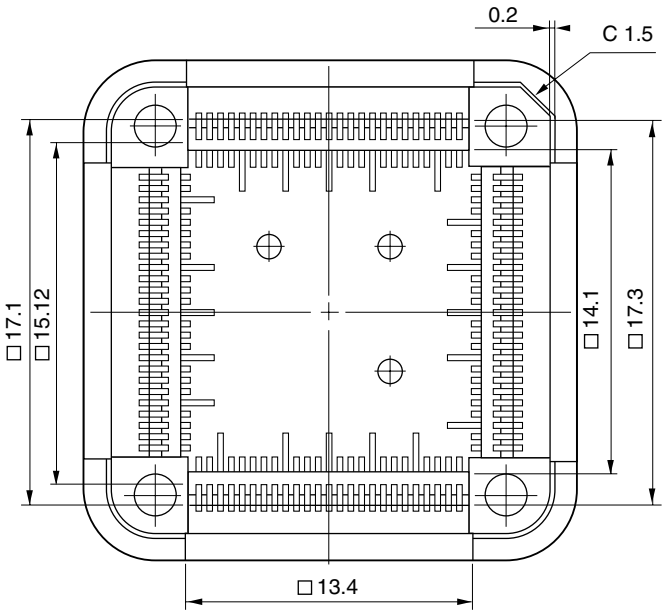
[Top view]



[Side view]

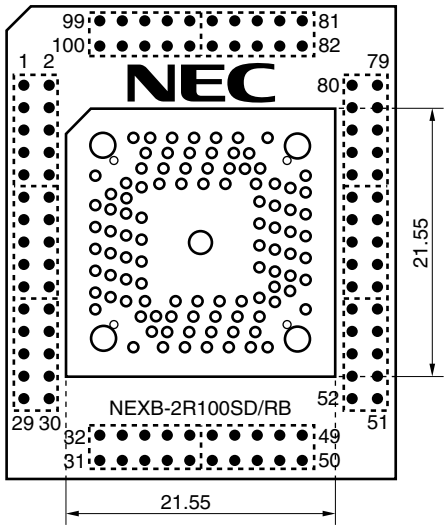


[Bottom view]

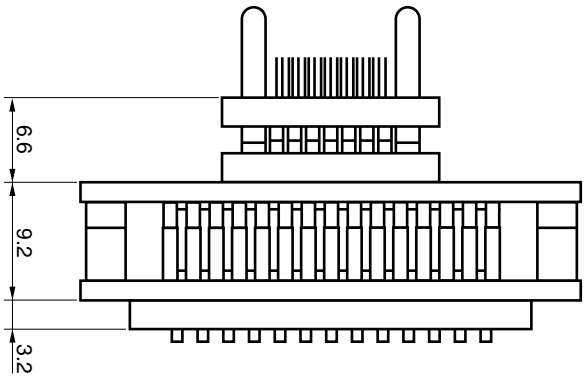


(6) NEXB-2R100SD/RB (Unit: mm)

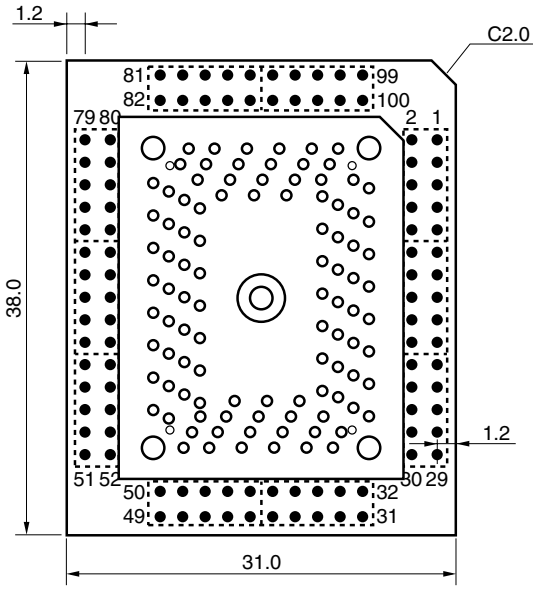
[Top view]



[Side view]

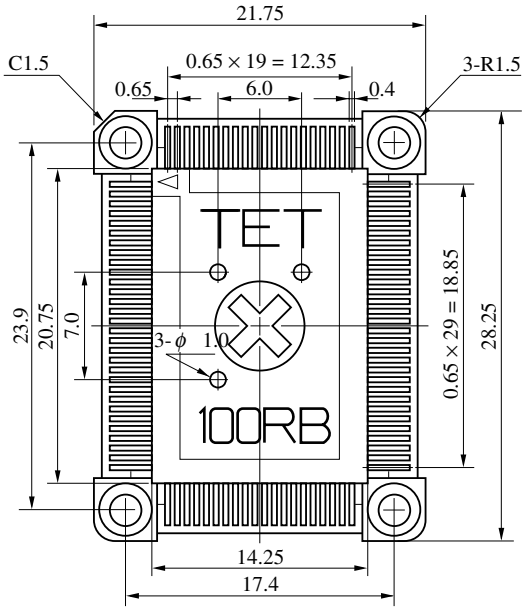


[Bottom view]

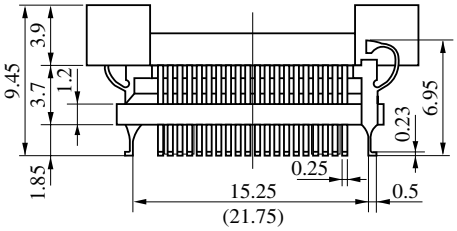


(7) NQPACK100RB (Unit: mm)

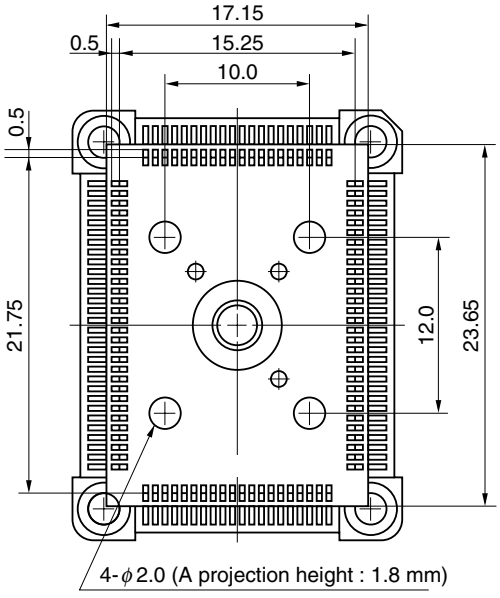
[Top view]



[Side view]

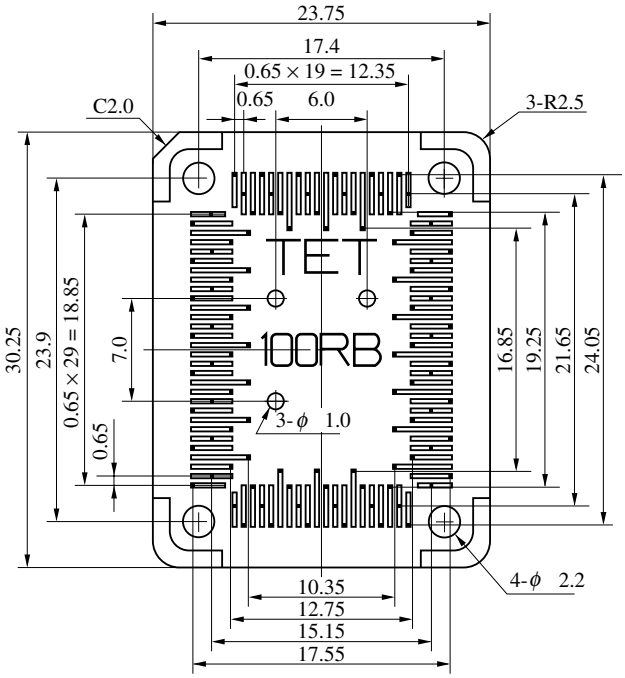


[Bottom view]

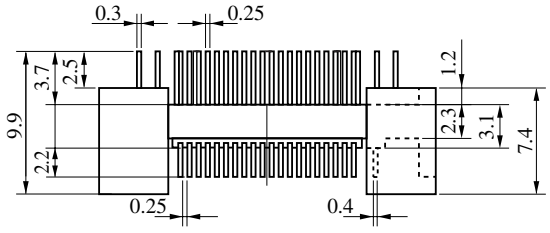


(8) YQPACK100RB (Unit: mm)

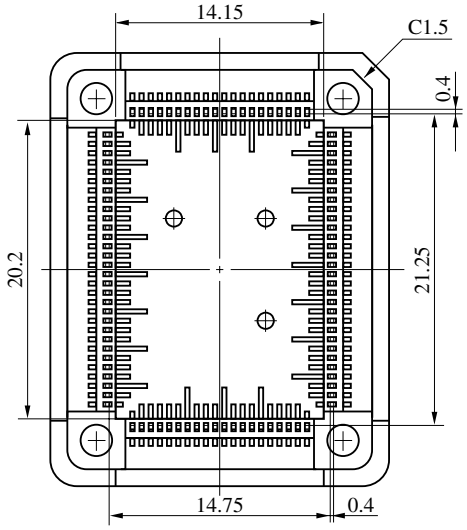
[Top view]



[Side view]

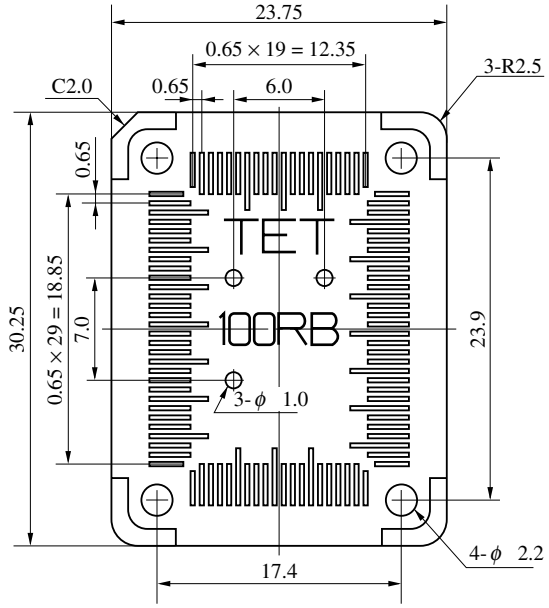


[Bottom view]

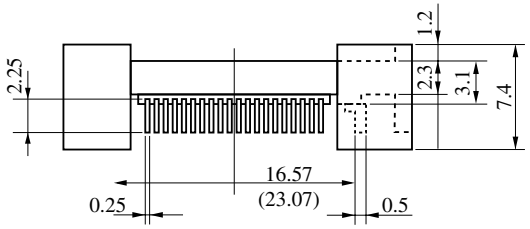


(9) HQPACK100RB (Unit: mm)

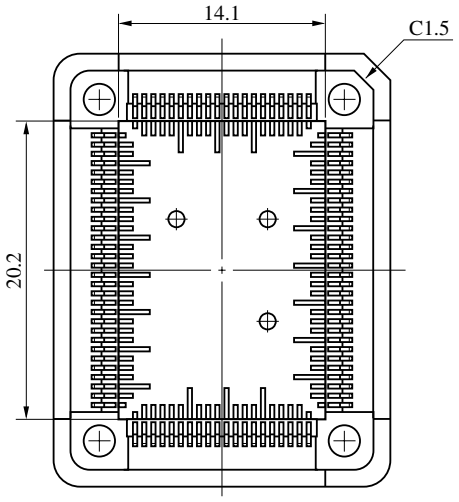
[Top view]



[Side view]



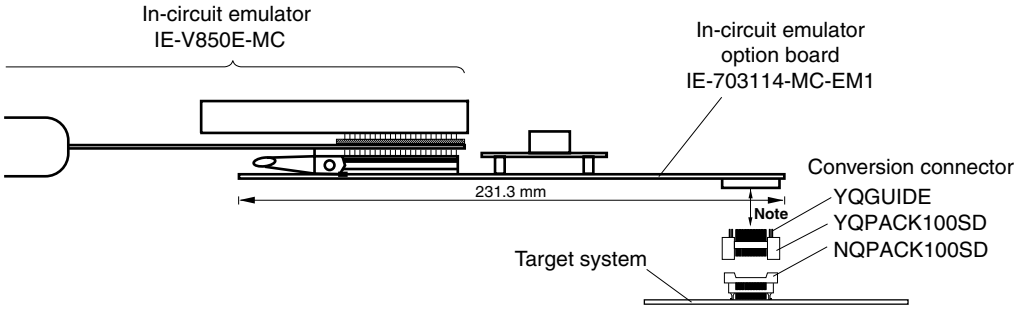
[Bottom view]



The following shows a diagram of the conditions when connecting the in-circuit emulator option board to the conversion connector. Follow the configuration below and consider the shape of parts to be mounted on the target system when designing a system.

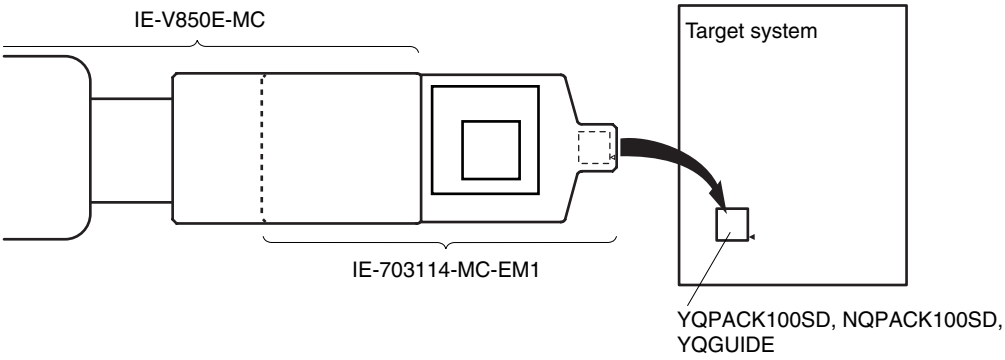
Figure A-1. 100-Pin Plastic LQFP (Fine Pitch) (14 × 14)

Side view



Note YQSOCKET100SDN (sold separately) can be inserted here to adjust the height (height: 3.2 mm).

Top view



Connection condition diagram

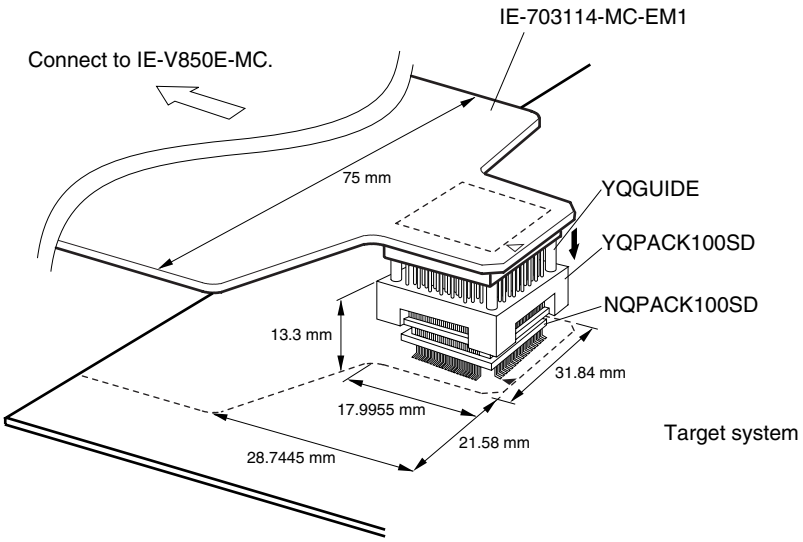
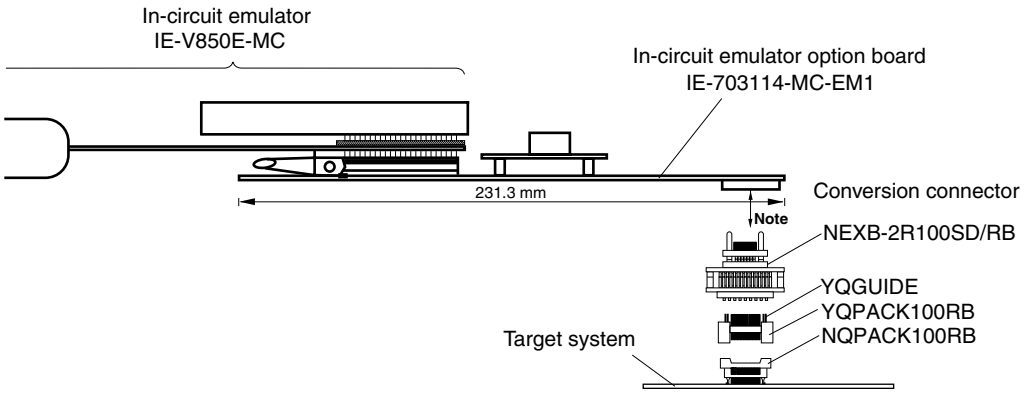


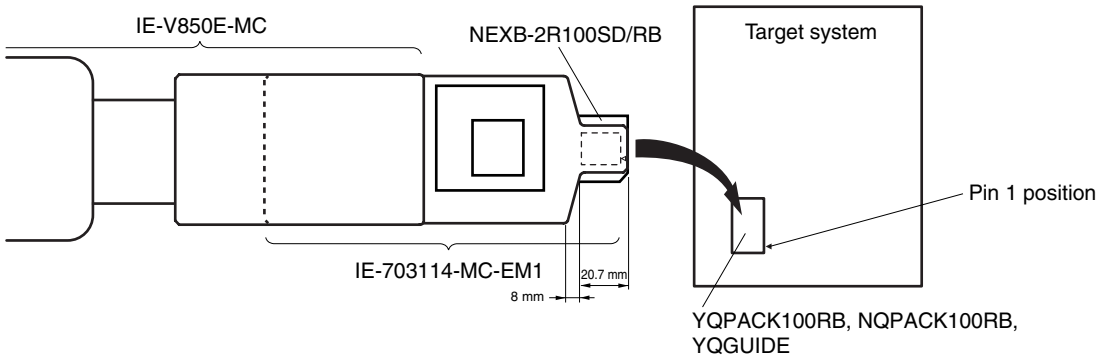
Figure A-2. 100-Pin Plastic QFP (14 × 20)

Side view

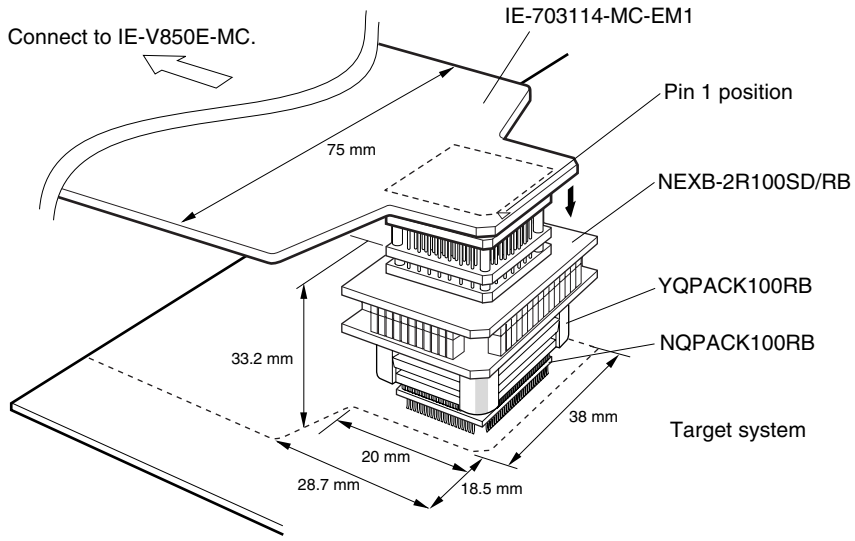


Note YQSOCKET100SDN (sold separately) can be inserted here to adjust the height (height: 3.2 mm).

Top view

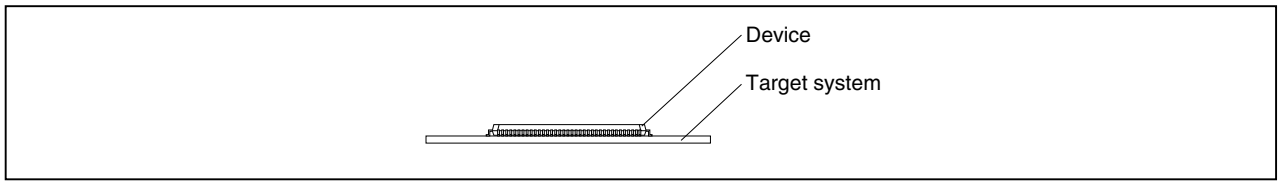


Connection condition diagram

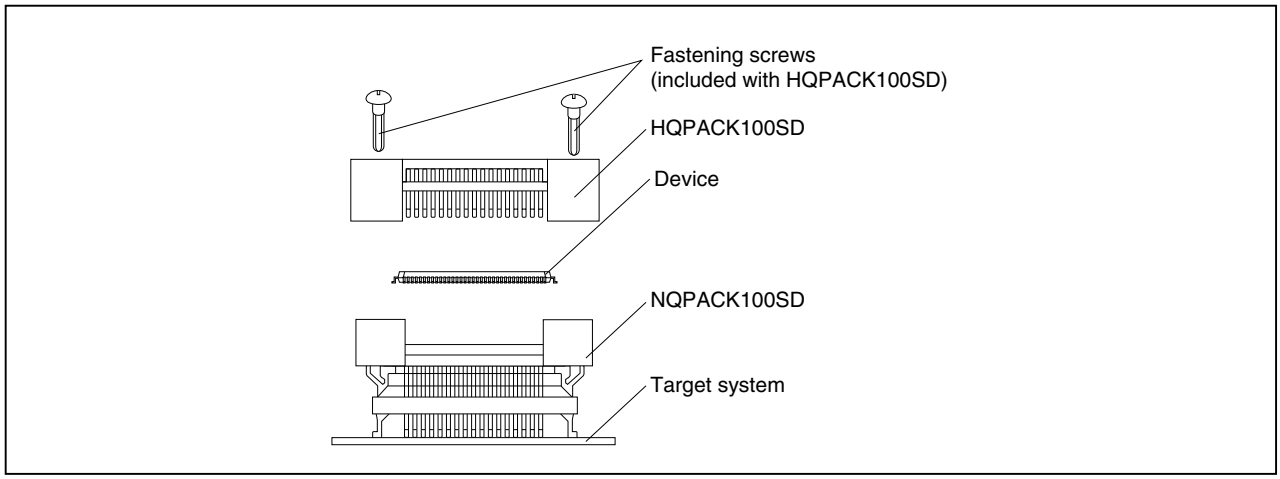


APPENDIX B EXAMPLE OF USE OF CONNECTOR FOR TARGET CONNECTION

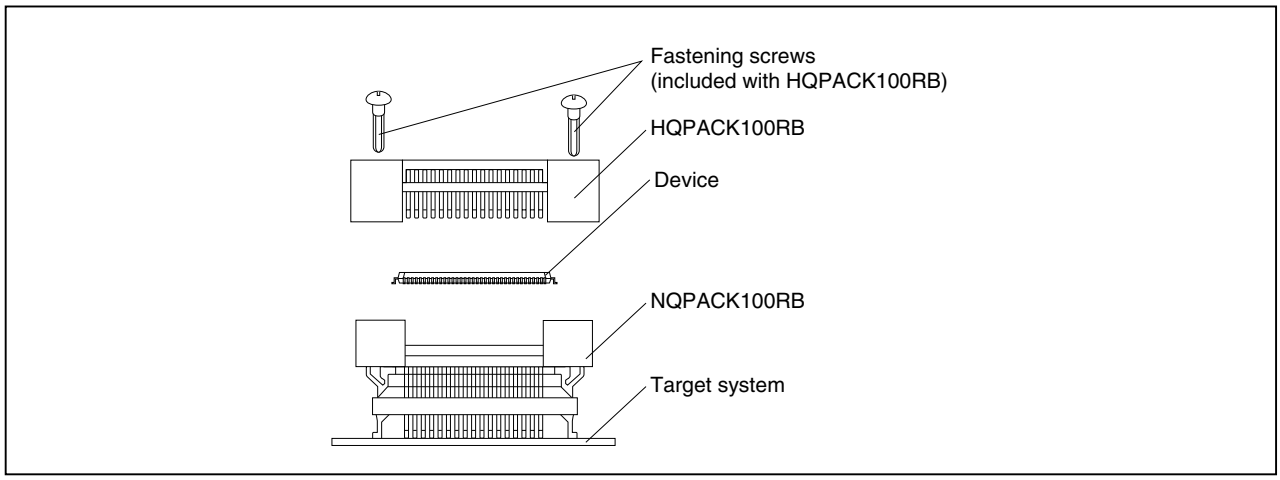
(1) When directly connecting device to target system (connector for target connection is not used)



(2) When using device using connector for target connection (GC package)



(3) When using device using connector for target connection (GF package)



APPENDIX C CONNECTORS FOR TARGET CONNECTION

C.1 Usage

(1) When mounting NQPACK100SD or NQPACK100RB on target system

<1> Coat the tip of the four projections (points) at the bottom of the NQPACK100SD or NQPACK100RB with two-component type epoxy adhesive (cure time longer than 30 min.) and bond the NQPACK100SD or NQPACK100RB to the target system. If not bonded properly, the pad of the printed circuit board may peel off when the emulator is removed from the target system. If the leads of the NQPACK100SD is not can be easily, aligned with the pads of the target system perform step <2> to adjust the position.

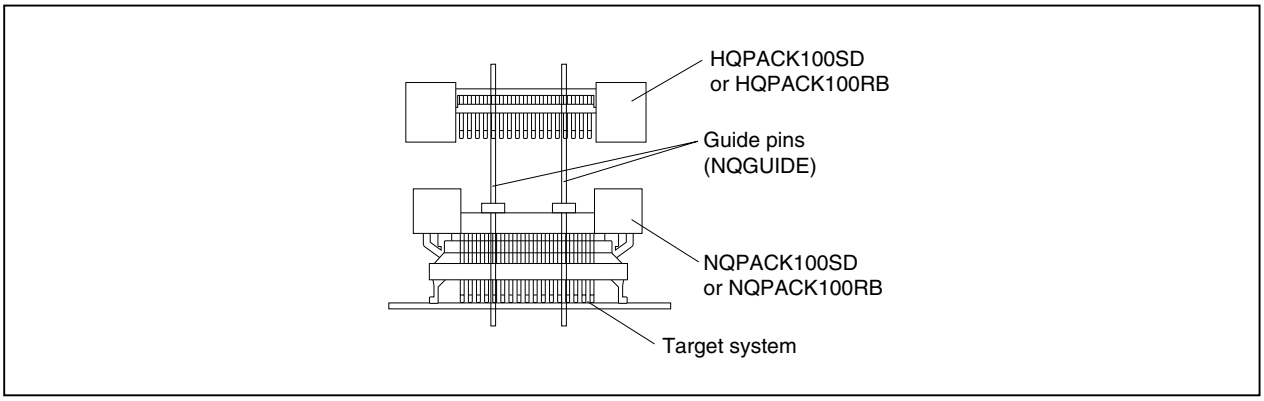
<2> To adjust the position, insert the guide pins for position adjustment (NQGUIDE) provided with the NQPACK100SD or NQPACK100RB into the pin holes on the upper side of NQPACK100SD or NQPACK100RB (refer to Figure C-1). The diameter of a hole is ϕ = 1.0 mm. There are three non-through holes (refer to **APPENDIX A DIMENSIONS**).

<3> After setting the HQPACK100SD or HQPACK100RB, solder the NQPACK100SD or HQPACK100RB to the target system. By following this sequence, adherence of flux or solder sputtering on the contact pins of the NQPACK100SD or HQPACK100RB can be avoided.

Recommended soldering conditions… Reflow: 240°C, 20 seconds max.
Partial heating: 240°C, 10 seconds max. (per pin row)

<4> Remove the guide pins.

Figure C-1. Mounting NQPACK100SD or NQPACK100RB



Remark NQPACK100SD or NQPACK100RB: Connector for target connection
HQPACK100SD or NQPACK100RB: Cover for device installation

(2) When mounting device

Caution Check for abnormal conditions such as resin burr or bent pins before mounting a device on the NQPACK100SD or NQPACK100RB. Moreover, check that the hold pins of the HQPACK100SD or HQPACK100RB are not broken or bent before mounting the HQPACK100SD or HQPACK100RB. If there are broken or bent pins, fix them with a thin, flat plate such as a blade.

<1> Make sure that the NQPACK100SD or NQPACK100RB is clean and the device pins are parallel (flat) before mounting a device on the NQPACK100SD or NQPACK100RB. Then, after mounting the NQPACK100SD or NQPACK100RB on the target board, fix the device and the HQPACK100SD or HQPACK100RB (refer to Figure C-2).

<2> Using the screws provided with the HQPACK100SD or HQPACK100RB (four locations: M2 × 6 mm), secure the HQPACK100SD or HQPACK100RB, device, and NQPACK100SD or NQPACK100RB.
Tighten the screws in a crisscross pattern with the screwdriver provided or a driver with a torque gauge (avoid tightening only one screw strongly). Tighten the screws with 0.55 kg·f·cm (0.054 N·m) max. torque. Excessive tightening may diminish conductivity.
At this time, each pin is fixed inside the plastic dividers by the contact pin of the NQPACK100SD or NQPACK100RB and the hold pin of the HQPACK100SD or HQPACK100RB (refer to Figure C-3). Thus, pins cannot cause shorting with the pins of neighboring devices.

Figure C-2. Mounting Device

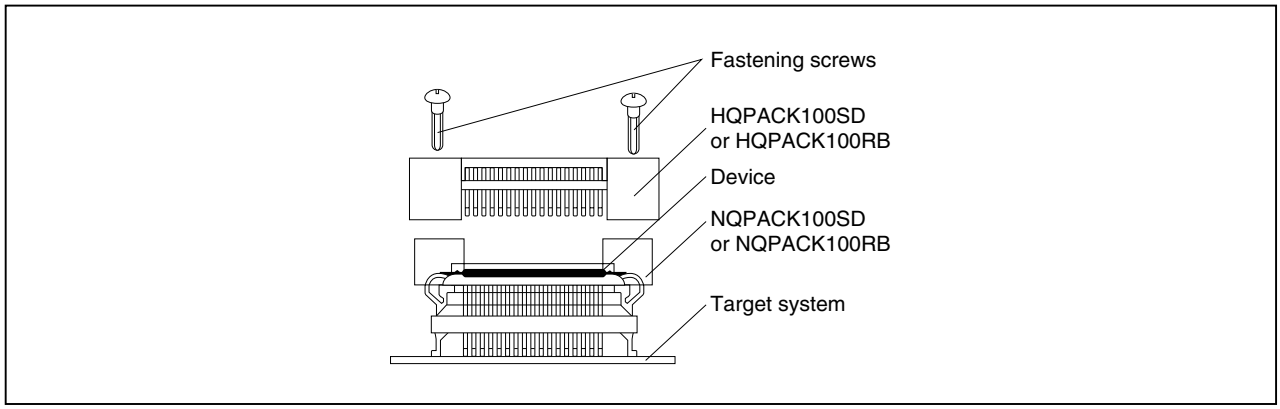
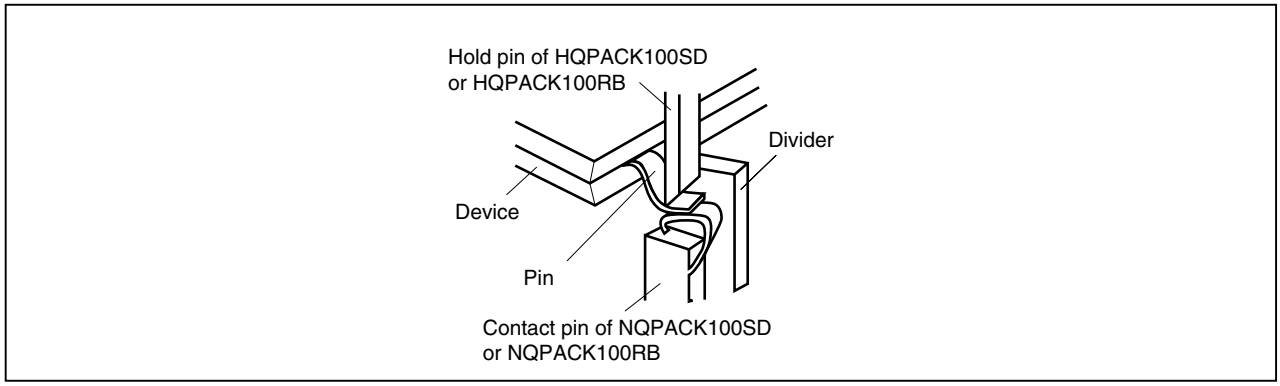


Figure C-3. NQPACK100SD or NQPACK100RB and Device Pin



C.2 Cautions on Handling Connectors

(1) When taking connectors out of the case, remove the sponge while holding the main unit.

(2) When soldering the NQPACK100SD or NQPACK100RB to the target system, cover it with the HQPACK100SD or HQPACK100RB for protection against splashing flux.

Recommended soldering conditions… Reflow: 240°C, 20 seconds max.
Partial heating: 240°C, 10 seconds max. (per pin row)

(3) Check for abnormal conditions such as resin burr or bent pins before mounting a device on the NQPACK100SD or NQPACK100RB. Moreover, when covering with the HQPACK100SD or HQPACK100RB, check that the hold pins of the HQPACK100SD or HQPACK100RB are not broken or bent before mounting the HQPACK100SD or HQPACK100RB. If there are broken or bent pins, fix them with a thin, flat plate such as a blade.

(4) When securing the YQPACK100SD or YQPACK100RB (connector for emulator connection) or HQPACK100SD or HQPACK100RB to the NQPACK100SD or NQPACK100RB with screws, tighten the four screws temporarily with the screwdriver provided or a driver with a torque gauge, then tighten the screws in a crisscross pattern (with 0.054 N·m max. torque).

Excessive tightening of only one screw may diminish conductivity.
If the conductivity is diminished after screw-tightening, stop tightening, remove the screws and make sure the NQPACK100SD or NQPACK100RB is clean and the device pins are parallel (flat).

(5) Device pins are not strong. Repeatedly connecting to the NQPACK100SD or NQPACK100RB may cause pins to bend. When mounting a device on NQPACK100SD or NQPACK100RB, check and adjust bent pins.

APPENDIX D MOUNTING PLASTIC SPACER

This chapter describes the mounting method for the plastic spacer supplied with the IE-V850E-MC.

When using the emulator connected to the target system, mount the plastic spacer as shown in Figure D-1 to fix the pod horizontally.

- **Mounting plastic spacer on IE-V850E-MC**

<1> Remove the nylon rivet from the rear part of the pod.

<2> Tighten the plastic spacer with the plastic screw supplied.

<3> To adjust the height, use a spacer other than the included spacer or a stand.

Figure D-1. Mounting Method of Plastic Spacer