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RENESAS

User's Manual

IE-V850E1-CD-NW

PCMCIA Card Type On-Chip Debug Emulator

Document No. U16647EJ1V0UM00 (1st edition)
Date Published June 2003 N CP(K)

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- Product release schedule
- Availability of related technical literature
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J03.4

INTRODUCTION

Target Readers

This manual is intended for users who design and develop application systems using the IE-V850E1-CD-NW. It is assumed that the target readers are familiar with the functions and usage methods of the devices and have knowledge of debuggers.

Purpose

The purpose of this manual is to describe the proper operation of the IE-V850E1-CD-NW and its basic specifications.

Organization

This manual is divided into the following parts.

- Overview
- Names and functions of components
- Cautions on designing target system
- Cautions on use

How to Read This Manual

It is assumed that the reader of this manual has general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.
This manual explains the basic setup procedure and switch settings.

To learn about the basic specifications and operation methods
→ Read this manual in the order of the **CONTENTS**.

To learn the operation methods and command functions, etc., of the IE-V850E1-CD-NW
→ Read the user's manual of the debugger (included) that is used.

Conventions

Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeral representation:	Binary ··· xxxx or xxxxB
	Decimal ··· xxxx
	Hexadecimal ··· xxxxH

Prefix indicating the power of 2 (address space, memory capacity):

K (kilo):	$2^{10} = 1024$
M (mega):	$2^{20} = 1024^2$

Terminology

The meanings of terms used in this manual are listed below.

Target device	The device that is targeted for emulation.
Target system	The system (user-built system) that is targeted for debugging. This includes the target program and user-configured hardware.
On-chip debug unit	Generic term of macros indicating RCU (run control unit), TEU (trigger event unit), and TRCU (trace control unit). It may be referred to as DCU (debug control unit).
KEL connector	The following products provided by KEL Corporation. 8830E-026-170S (26-pin straight type) 8830E-026-170L (26-pin right-angle type)
MICTOR connector	The following products provided by Tyco Electronic AMP K.K. 2-7670074-2 (38-pin straight type)

Related Documents

When using this manual, refer to the following manuals.
The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

○ **Documents related to development tools (user's manuals)**

Document Name		Document Number
IE-V850E1-CD-NW PCMCIA Card Type On-Chip Debug Emulator		This manual
CA850 Ver. 2.40 C Compiler Package	Operation	U16053E
	C Language	U16054E
	Assembly Language	U16042E
PM Plus Ver. 5.10		U16559E
ID850NWC Ver. 2.51 Integrated Debugger	Operation	To be prepared

Caution The documents listed above are subject to change without notice. Be sure to use the latest documents when designing.

CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1 OVERVIEW

The IE-V850E1-CD-NW is an emulator to be connected to a target device with an on-chip debug unit to efficiently debug hardware and software.

1.1 Features

- General-purpose usage available in microcontrollers with a V850E1 or V850ES Series on-chip debug unit
- N-Wire interface is adopted for connection between microcontroller and this emulator
- Debugging is possible with microcontroller mounted in the system to be developed
- Small PC card type emulator requiring no power supply unit ideal for debugging in the field
- Downloading program into the flash memory possible using flash self-programming function
- Usage as a flash programmer possible using flash programmer software (under development)
- The following shows the dimensions and weight of the IE-V850E1-CD-NW.

Parameter		Value
External dimensions (refer to **APPENDIX B PACKAGE DRAWINGS**)	Height	5.0 mm
	Width	54.0 mm
	Depth	85.6 mm
Weight		Approximately 32 g

1.2 Function Specifications

Table 1-1. Function Specifications

Parameter	Specification
Target device	Microcontroller with V850E1, V850ES Series on-chip debug unit Microcontroller with Nx85ET core
Target voltage	2.0 to 5.0 V
Target OS	Windows™ 98, Windows Me, Windows 2000, Windows NT™ 4.0, Windows XP
Target host machine	PC-9821 series, PC-98NX series, IBM PC/AT™ compatibles with PC card slot conforming to PCMCIA2.1/JEIDA standard Ver. 4.2
Hardware resources used by host machine	I/O address: 100 H to 3FFH (only 20H bytes are available, specifying either 220H, 260H, 2E0H, 320H, or 3E0H as the base address) Interrupts, others: Not used
N-Wire interface (on-chip debug unit execution control block)	Number of interface signal pins: 5 Function of interface signal pins (in and out below indicates the direction when seen from the target device) • DCK (in): Clock input • DMS (in): Mode select input • DI (in): Data input • DDO (out): Data output • $\overline{\text{DRST}}$ (in): On-chip debug unit reset input
Flash writing interface	Required when the target device includes flash memory. Number of interface signal pins: 1 Function of interface signal pins (in and out below indicates the direction when seen from the target device) • FLMD0 (in): Used when writing to the flash memory from the integrated debugger
Reset interface	May be required when $\overline{\text{DRST}}$ of the target device is an alternate-function pin and the initial value of the OCDM0 bit in the device changes according to the reset source (refer to **3.2.8 $\overline{\text{RESET}}$**) Number of interface signal pins: 1 Function of interface signal pins (in and out below indicates the direction when seen from the target device) • $\overline{\text{RESET}}$ (in): System reset
Interface for target power supply detection	Monitors the power supply of the target system Supply V_{DD} for on-chip debugging • V_{DD} (in): V_{DD} for on-chip debugging
On-chip debug function	Depends on the type of the on-chip debug unit in the target system (refer to Table 1-2)
Connectors for IE connection (connectors for mounting target system)	KEL connector (product of KEL Corporation) • 8830E-026-170S (26-pin straight type) • 8830E-026-170L (26-pin right-angle type) MICTOR connector (product of Tyco Electronic AMP K.K.) • 2-7670074-2 (36-pin straight type) 2.54 mm pitch general-purpose connector
IE connection cable	500 mm
Operating environment	Temperature: +0 to +40°C, humidity: 10 to 80%RH (no condensation)
Storage environment	Temperature: −15 to +60°C, humidity: 10 to 80%RH (no condensation)

Table 1-2. On-Chip Debug Unit and Debug Function

Debug Function	On-Chip Debug Unit Name			
	RCU0 (NB85E901)	RCU1	RCU2 (Under Development)	Nx85ET Core (RCU0 + TEU + TRCU)[Note 1]
Internal ROM/flash memory security function	10-byte ID code authentication			
Event detection break function	Break before execution or Access break × 2 (selectable)			Break before execution × 2, Break after execution × 2, Access break × 4
Software break function	2000 points 0 to 8 points can be assigned to the internal ROM/flash memory area at one time[Note 2]			
Forced break function	Provided			
Execution function	Go (free-run), execution from cursor position, restart, step execution			
RM, DMM function[Note 3]	Provided			
Register manipulation function	Provided			
Mask function	Not provided	Resolution: 100 ns, Maximum measurement time: 3 min. 30 sec.		Not provided
Trace function	Not provided		Provided[Note 4]	Not provided[Note 5]

Notes 1. The Nx85ET core is a CPU core in which RCU, TEU, and TRCU macros are incorporated.

2. The number of points depends on the device. This function cannot be used when the flash self-programming function is used.

3. RM (RAM Monitor): Function that read the contents of the memory during program execution
DMM (Dynamic Memory Modification): Function that rewrites the contents of the RAM during program execution

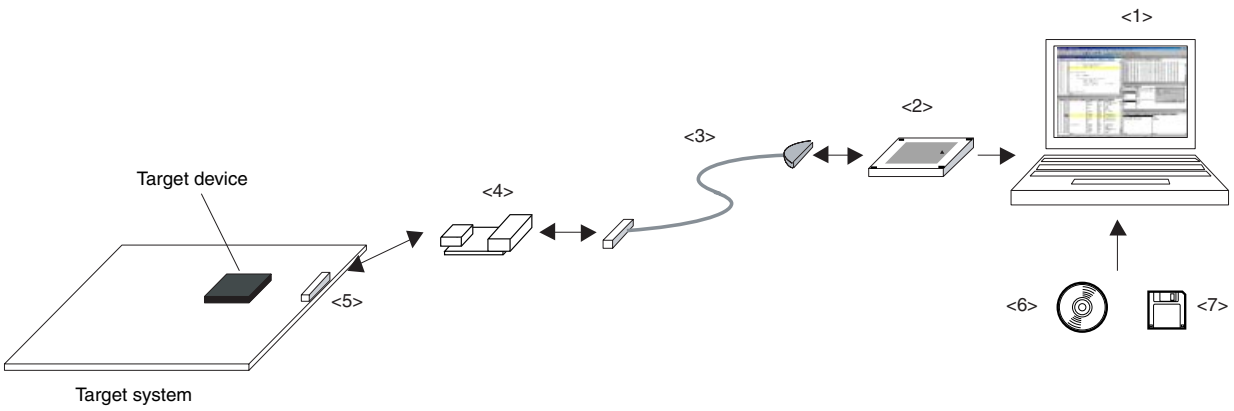
4. The latest 8 trace conditions are traced.
The trace conditions (branch source, branch destination, write access) can be set.

5. The trace function of the Nx85ET core is realized by using the trace interface. This emulator does not feature a trace interface, so the trace function cannot be used.

1.3 System Configuration

The following shows the system configuration when connecting the IE-V850E1-CD-NW.

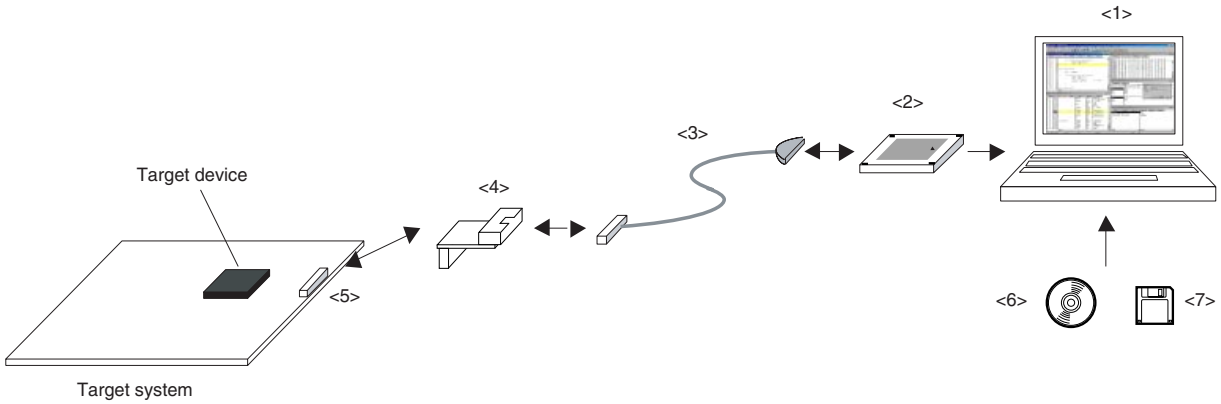
Figure 1-1. System Configuration 1 (Recommended)



Remark <1> Host machine (with PC card slot)
<2> IE-V850E1-CD-NW
<3> IE connection cable (included)
<4> Connector conversion board: KEL Adapter (included with this product)
<5> IE connector: KEL connector[Note 1]
8830E-026-170S (included)
8830E-026-170L (sold separately)
<6> CD-ROM (included)
Integrated debugger: ID850NWC
N-Wire checker
Device driver
Document
<7> Device file[Note 2]

Notes 1. Product of KEL Corporation
2. The device file can be downloaded from the website of NEC Electronics (URL: http://www.necel.com/micro/)

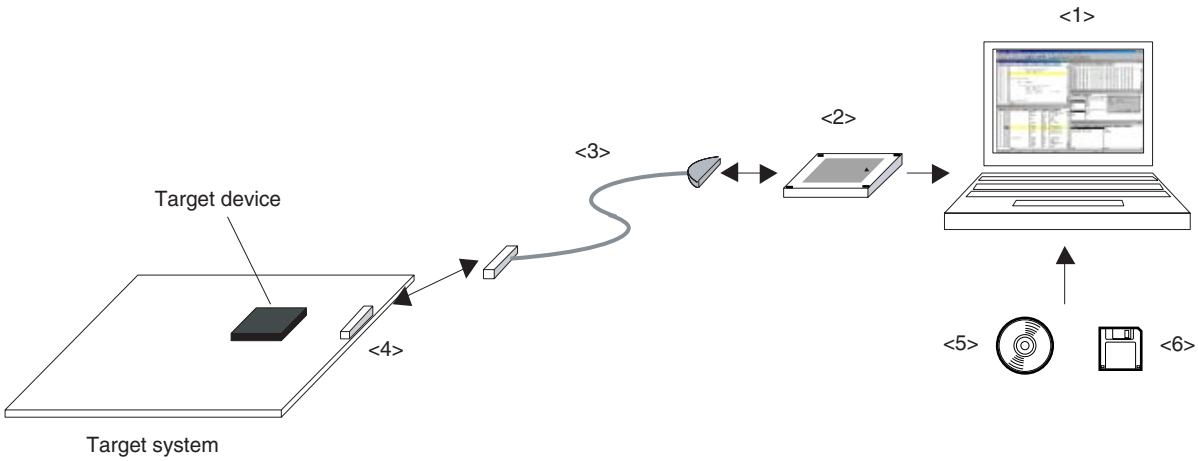
Figure 1-2. System Configuration 2



Remark <1> Host machine (with PC card slot)
<2> IE-V850E1-CD-NW
<3> IE connection cable (included)
<4> Connector conversion board: MICTOR Adapter (sold separately)[Note 1]
<5> IE connector: MICTOR connector[Note 2]
2-7670074-2 (sold separately)
<6> CD-ROM (included)
Integrated debugger: ID850NWC
N-Wire checker
Device driver
Document
<7> Device file[Note 3]

Notes 1. Product of Lightwell Co., Ltd.
B-137 (right-angle product), B-137A (straight product)
2. Product of Tyco Electronic AMP K.K.
3. The device file can be downloaded from the website of NEC Electronics
(URL: http://www.necel.com/micro/)

Figure 1-3. System Configuration 3



Remark <1> Host machine (PC card slot mounted)
<2> IE-V850E1-CD-NW
<3> IE connection cable (included)
<4> IE connector: 2.54-mm pitch 20-pin general purpose connector
<5> CD-ROM (included)
Integrated debugger: ID850NWC
N-Wire checker
Device driver
Document
<6> Device file[Note]

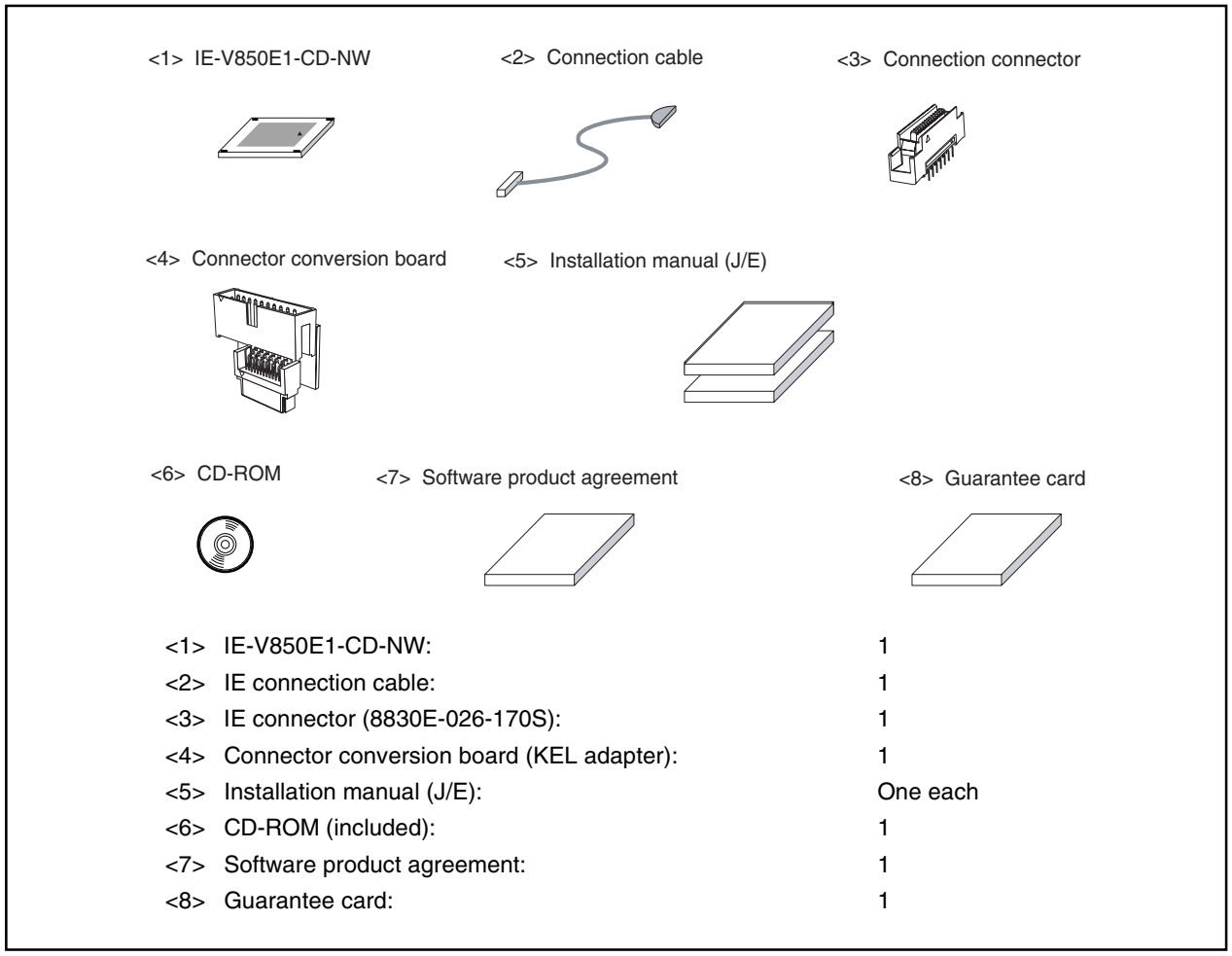
Note The device file can be downloaded from the website of NEC Electronics (URL: http://www.necel.com/micro/)

1.4 Contents in Carton

The carton of the IE-V850E1-CD-NW contains the following. Check for any missing items. If there are missing or damaged items, please contact an NEC Electronics sales representative or an NEC Electronics distributor.

Return the guarantee card included in the carton after filling in all the items.

Figure 1-4. Contents in Carton



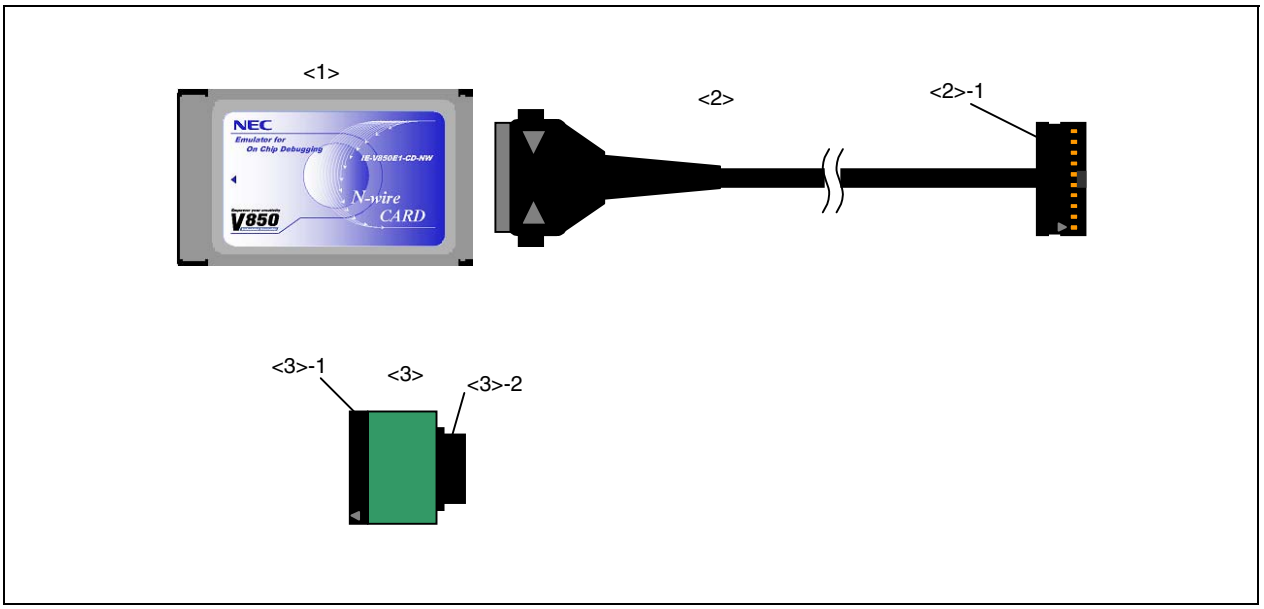
<1>	IE-V850E1-CD-NW:	1
<2>	IE connection cable:	1
<3>	IE connector (8830E-026-170S):	1
<4>	Connector conversion board (KEL adapter):	1
<5>	Installation manual (J/E):	One each
<6>	CD-ROM (included):	1
<7>	Software product agreement:	1
<8>	Guarantee card:	1

CHAPTER 2 NAMES AND FUNCTIONS OF COMPONENTS

This chapter describes the names and functions of components, and connections with related devices of the IE-V850E1-CD-NW.

2.1 Names and Functions of Components

Figure 2-1. Names of Components



<1> IE-V850E1-CD-NW

<2> IE connection cable (included)
<2>-1: HIF3BA-20-20D-2, 54C (product of Hirose Electric Co., Ltd.)

<3> Connector conversion board (KEL adapter) (included)
<3>-1: HIF3FC-20PA-2, 54DS (product of Hirose Electric Co., Ltd.)
<3>-2: 8802-026-170L (product of KEL Corporation)

2.2 Connection

The following describes the connection between the IE-V850E1-CD-NW and related devices.

(1) Connecting the IE connection cable

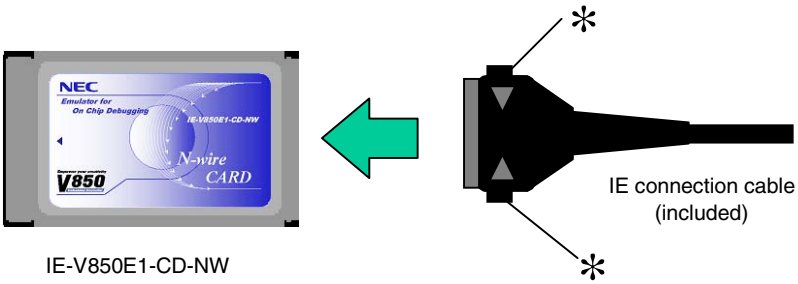
Connect the IE connection cable to the IE-V850E1-CD-NW before connecting the IE-V850E1-CD-NW to the host machine.

At this time, do not connect the IE connection cable and the IE connector on the target.

Connect the IE connection cable to the IE-V850E1-CD-NW pressing the portions indicated by ∗, as shown in Figure 2-1.

The portions indicated by ∗ must also be pressed when disconnecting the IE connection cable.

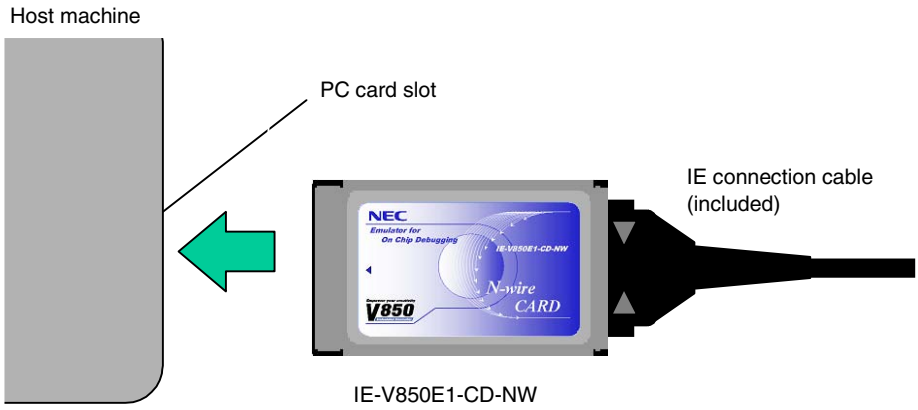
Figure 2-2. Connecting IE Connection Cable



(2) Inserting the IE-V850E1-CD-NW

Insert the IE-V850-CD-NW in the PC card slot on the host machine.

Figure 2-3. Installing IE-V850E1-CD-NW



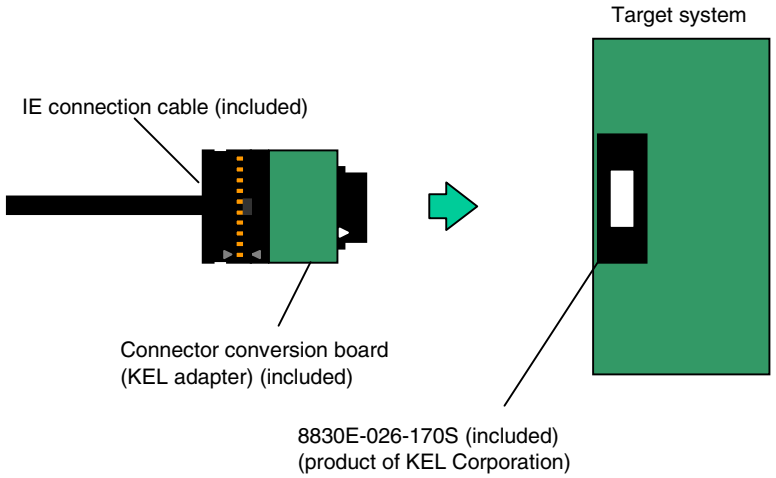
(3) How to connect to the target system differs depending on the IE connector type.

Caution Be sure to turn off the power to the target system before connecting to or disconnecting from the target system.

<1> When the 8830E-026-170S (included) is used as the IE connector

Connect the IE connection cable to the connector conversion board (included) and connect it to the target system. At this time, align the position of pin 1 (mark △) of both sides.

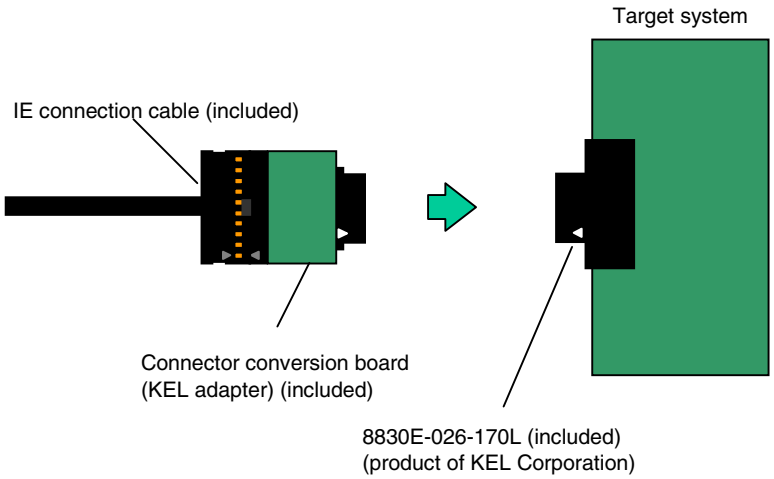
Figure 2-4. Connecting to Target System (1)



<2> When the 8830E-026-170L (sold separately) is used as the IE connector

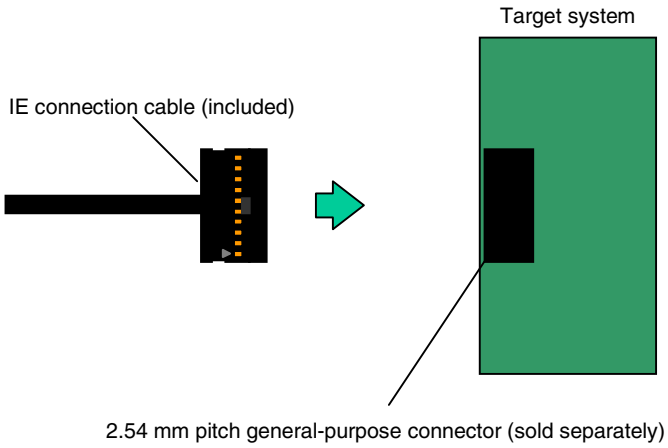
Connect the IE connection cable to the connector conversion board (included) and connect it to the target system. At this time, align the position of pin 1 (mark △) of both sides.

Figure 2-5. Connecting to Target System (2)



<3> When the 2.54 mm pitch general-purpose connector (sold separately) is used as the IE connector
Connect the IE connection cable to the target system. At this time, align the position of pin 1 (mark ▲) of both sides.

Figure 2-6. Connecting to Target System (3)



2.3 Startup/Termination

The following describes the procedures for startup and termination.

To operate the IE-70000-MC-NW-A, a dedicated debugger is required. For details, refer to the **ID850NWC Integrated Debugger Ver.2.51 or Later Operation (Windows Based) User's Manual (U16525E)**.

(1) Startup procedure

<1> Apply power to the host machine and start the OS.
Install the integrated debugger, device file, and driver, if they have not been installed. (See **APPENDIX A** for the installation procedure of the driver, and the **ID850NWC Integrated Debugger Ver. 2.51 or Later Operation (Windows Based) User's Manual (U16525E)** for the installation procedure of the integrated debugger and device file.)

<2> Apply power to the target system.

<3> Start the integrated debugger.

<4> If the target device includes internal ROM/flash memory, flash security ID code authentication must be performed in the integrated debugger. (See **APPENDIX C** for details of the ID code.)

(2) Termination procedure

<1> Terminate the debugger.

<2> Shutdown the power to the target system.

<3> Shutdown the OS in the host machine and shutdown the power to the host machine.

CHAPTER 3 NOTES ON TARGET SYSTEM DESIGN

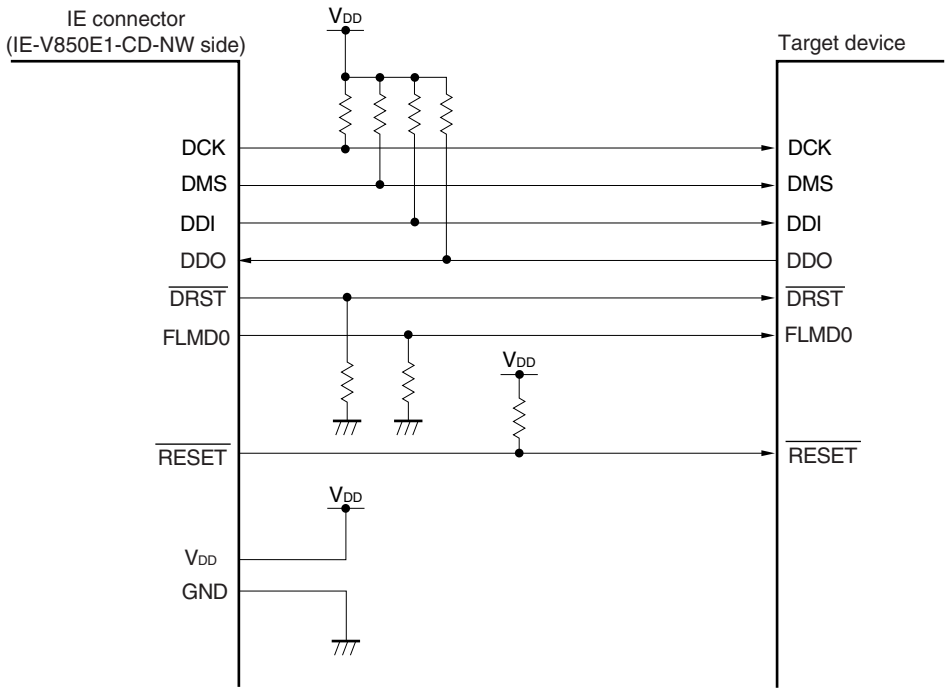
To debug the target system with the IE-V850E1-CD-NW connected, a circuit to connect the IE-V850E1-CD-NW is required on the target system.

For details, refer to the user's manual of the target device.

3.1 Connection Circuit Example

The following shows a connection circuit example of the target system required when connecting the IE-V850E1-CD-NW. For details, refer to the user's manual of the target device.

Figure 3-1. Connection Circuit Example



Cautions 1. Keep the pattern length as short as possible. (Do not exceed 100 mm.)

2. V_{DD} of the IE connector is used for detecting whether the target board is powered on.

3. The DCK, DMS, DDI, DDO, and $\overline{\text{DRST}}$ pins may function alternately as general-purpose ports. Therefore handle these pins in accordance with the specifications of each target device.

4. Make sure that the signals driven from the IE-V850E1-CD-NW and the signals generated on the target system do not conflict.

5. FLMD0 is connected only when the target device incorporates flash memory.

6. $\overline{\text{RESET}}$ may be required when both of the following conditions are satisfied.

- **$\overline{\text{DRST}}$ of the target device has an alternate function**
- **The IE-V850E1-CD-NW is connected to a target system that only uses the POC reset function, without using the $\overline{\text{RESET}}$ pin function**

7. Supply the on-chip debug power supply for V_{DD}.

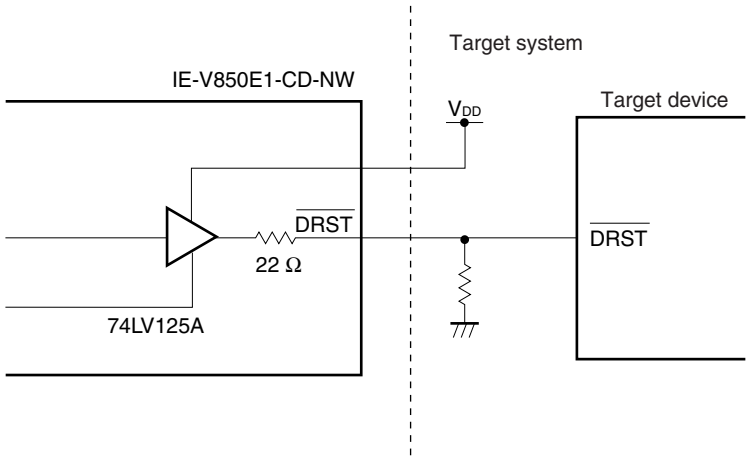
3.2 Interface Signals

This section describes the interface signals.

3.2.1 $\overline{\text{DRST}}$

This is the reset input signal for the on-chip debug unit. This is a negative logic signal for initializing the debug control unit asynchronously. Barring a problem arising from the specifications of the target device, pull down this signal to low level.

Figure 3-2. $\overline{\text{DRST}}$ Pin Connection Example



Upon detection of V_{DD} of the target system following integrated debugger startup by the IE-V850E1-CD-NW, the $\overline{\text{DRST}}$ signal changes from low level to high level to start the on-chip debug unit of the target device.

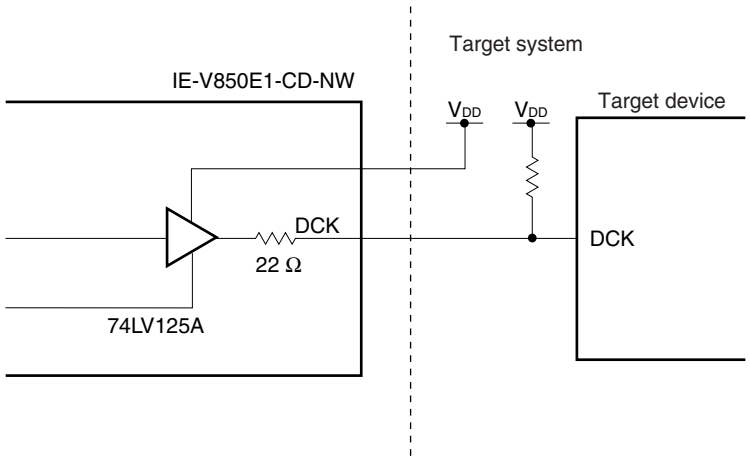
The change of the $\overline{\text{DRST}}$ signal from low level to high level also resets the CPU.

When debugging is started by starting up the integrated debugger, CPU reset always occurs.

3.2.2 DCK

This is the clock input signal. This signal supplies a 20 MHz clock from the IE-V850E1-CD-NW. The DMS and DDI signals are sampled in synchronization with the rising edge of the DCK signal in the on-chip debug unit, and the data DDO signal is output in synchronization with the falling edge of the DCK signal. Barring a problem arising from the specifications of the target device, pull up this signal to high level.

Figure 3-3. DCK Pin Connection Example



3.2.3 DMS

This is the transfer mode selection signal. The state machine in the debug unit changes according to the level of the DMS signal. This signal is sampled in synchronization with the rising edge of the DCK signal in the on-chip debug unit.

Barring a problem arising from the specifications of the target device, pull up this signal to high level. The connection example for this signal is the same as that shown in **Figure 3-3 DCK Pin Connection Example**.

3.2.4 DDI

This is the data input signal. This signal is sampled in synchronization with the rising edge of the DCK signal in the on-chip debug unit.

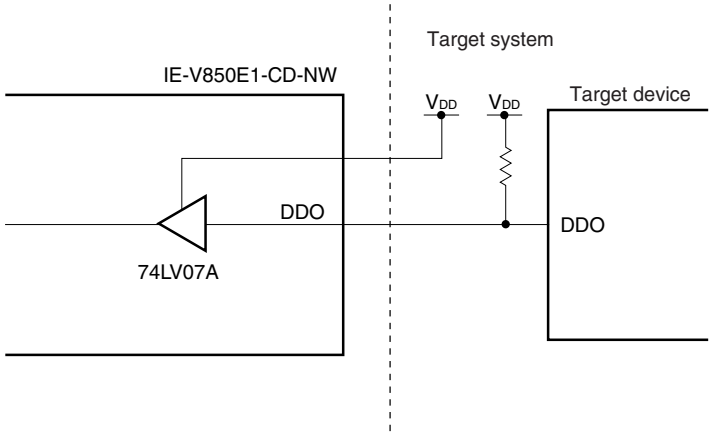
Barring a problem arising from the specifications of the target device, pull up this signal to high level. The connection example for this signal is the same as that shown in **Figure 3-3 DCK Pin Connection Example**.

3.2.5 DDO

This is the data output signal. This signal is output in synchronization with the falling edge of the DCK signal from the on-chip debug unit.

Barring a problem arising from the specifications of the target device, pull up this signal to high level.

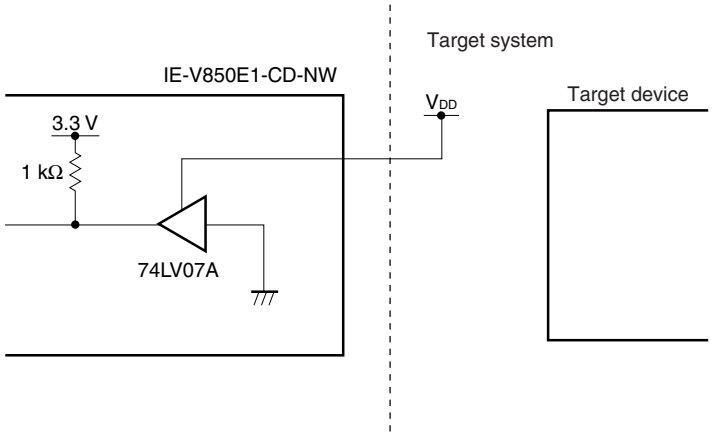
Figure 3-4. DDO Pin Connection Example



3.2.6 V_{DD}

This signal is used for detection of V_{DD} of the target system. The interface with the target system (detection range) is 2.0 V to 5.0 V. If V_{DD} from the target system is not detected, the $\overline{\text{DRST}}$, DCK, DMS, DDI, FLMD0, and $\overline{\text{RESET}}$ pins go to a high-impedance state.

Figure 3-5. V_{DD} Pin Connection Example



3.2.7 FLMD0

This is the flash mode signal. It is used only when the target device incorporates flash memory.

The flash self-programming function is used for the download function for downloading to the flash memory using the integrated debugger. The FLMD0 pin must be made high level during flash self-programming.

There are two methods for controlling the FLMD0 pin from the IE-V850E1-CD-NW. Either one can be selected for use.

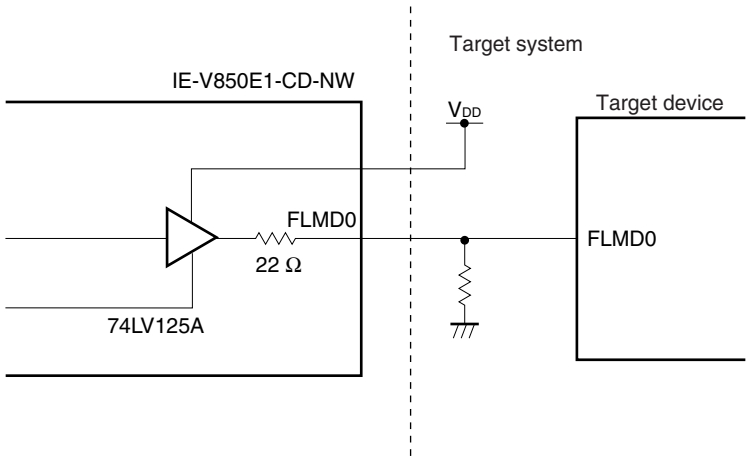
<1> Control from IE-V850E1-CD-NW

Connect the FLMD0 pin from the IE-V850E1-CD-NW to the FLMD0 pin of the target device.

In the normal mode, nothing is driven from the IE-V850E1-CD-NW.

When, during a break, the download function, etc., of the integrated debugger is executed, the FLMD0 pin from the IE-V850E1-CD-NW is controlled to be high level. Barring a problem arising from the specifications, pull down the FLMD0 pin to low level.

Figure 3-6. FLMD0 Pin Connection Example <1>



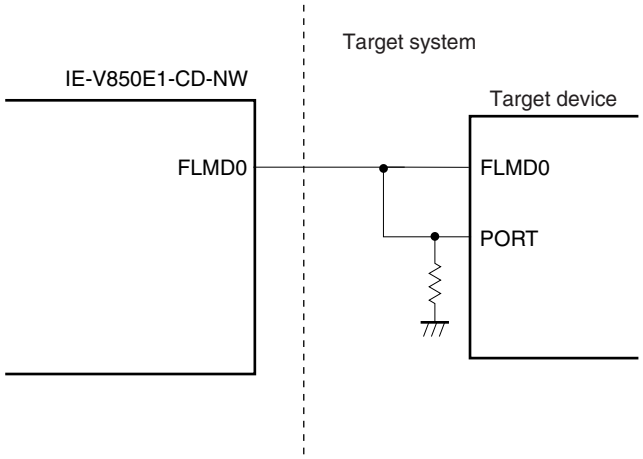
<2> Control from port

Connect an unused port of the target device to the FLMD0 pin.

The same port pin (PORT in Figure 3-7) can be used with no problem to realize the flash self-programming function in the user program using a similar method. Barring a problem arising from the specifications, pull down this pin to low level.

Perform settings to make the port pin high level prior to executing the download function and make the port pin low level or high impedance after executing the download function, through the integrated debugger console. (For details, refer to the **ID850NWC Integrated Debugger Ver. 2.51 or Later Operation (Windows Based) User's Manual (U16525E)**.)

Figure 3-7. FLMD0 Pin Connection Example <2>

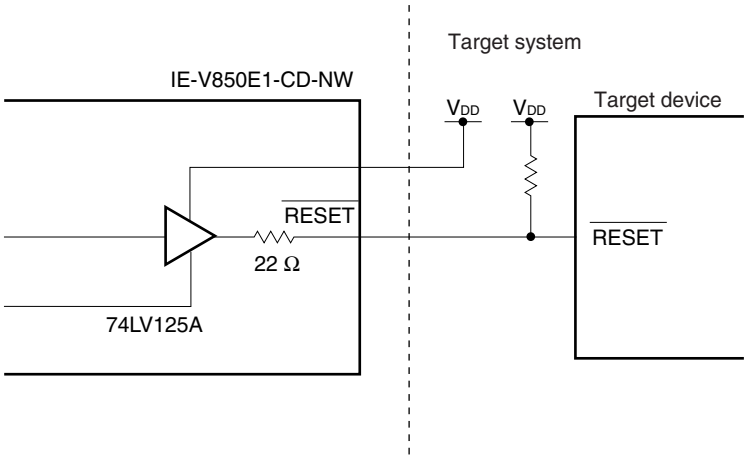


3.2.8 $\overline{\text{RESET}}$

This is the system reset input signal. If the $\overline{\text{DRST}}$ pin of target device is an alternate-function pin, $\overline{\text{DRST}}$ can be enabled/disabled by the value of the OCDM0 bit in the device. Some devices have specifications such that the initial status of the alternate-function pin varies according to the reset source, so that in the case of reset via the $\overline{\text{RESET}}$ pin, $\overline{\text{DRST}}$ is enabled when OCDM0 = 1, and in the case of reset via POC (Power-On Clear function), $\overline{\text{DRST}}$ is disabled when OCDM0 = 0.

In the case of a target system where only reset via POC is used in such a device, $\overline{\text{DRST}}$ cannot be enabled, and therefore on-chip debugging cannot be performed. In such a case, the $\overline{\text{DRST}}$ pin is enabled by performing the connection shown in Figure 3-8 and applying reset via the $\overline{\text{RESET}}$ pin from the IE-V850E1-CD-NW.

Figure 3-8. $\overline{\text{RESET}}$ Pin Connection Example



3.3 IE Connection Connector

For connection to the IE-V850E1-CD-NW, an IE connection connector must be mounted on the target system. The IE connection connector can be selected from among the following.

- KEL connector (recommended)
- MICTOR connector[Note 1]
- 2.54 mm pitch 20-pin general-purpose connector[Note 2]

Notes 1. The MICTOR connector is conventionally supported as an IE connection connector that supports the high-speed trace interface. As this product does not support the high-speed trace interface, the MICTOR connector cannot be selected for this product.
To connect this product using the MICTOR connector, a MICTOR adapter (sold separately), which is a connector conversion board, is required. Either the B-137 (right-angle version) or the B-137A (straight version), both made by Lightwell Co., Ltd., can be used as the MICTOR adapter.

2. If the 2.54 mm pitch 20-pin general-purpose connector (sold separately) is selected, note that connection to the on-chip debug emulators of some third-party manufacturers is not possible.

3.3.1 KEL connector

If using the KEL connector as the IE connection connector, mount one of the following connectors on the target system.

- 8830E-026-170S: 26-pin straight type (included)
- 8830E-026-170L: 26-pin right-angle type (sold separately)

Remark The 8830E-026-170S and 8830E-026-170L are products of KEL Corporation.

Figure 3-9 and Table 3-1 show the IE connection connector pin configuration and the pin functions, respectively. Input/output is indicated as seen from the target device.

Figure 3-9. KEL Connector Pin Configuration

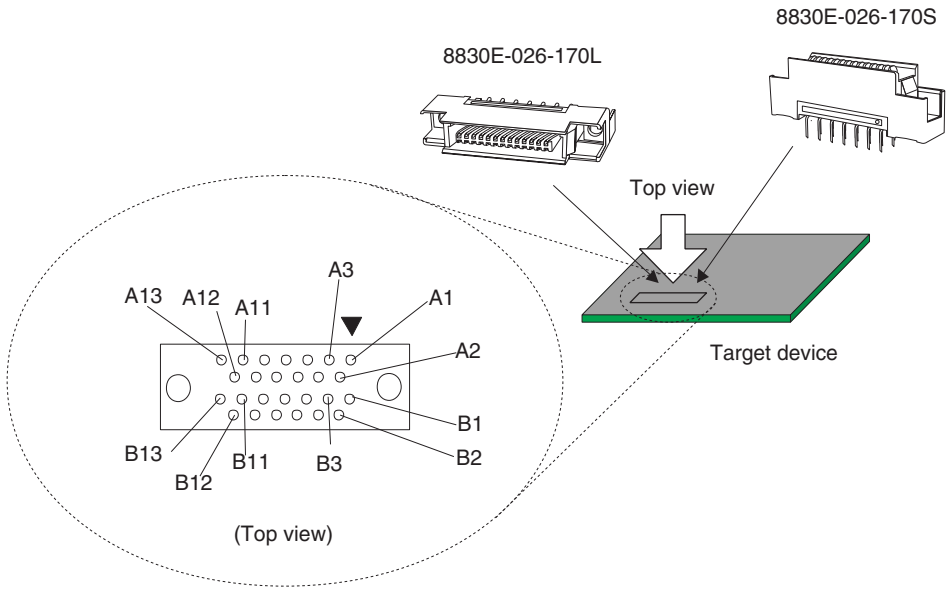


Table 3-1. KEL Connector Pin Functions

Pin No.	Signal Name	I/O	Description
A1 to A6	GND	–	Connect to GND
A7	DDI	IN	Data input
A8	DCK	IN	Clock input
A9	DMS	IN	Transfer mode selection input
A10	DDO	OUT	Data output
A11	$\overline{\text{DRST}}$	IN	Reset input to on-chip debug unit
A12	$\overline{\text{RESET}}$	IN	System reset input (leave open when not used)Note 1
A13	FLMD0	IN	Flash mode input (leave open when not used)Note 2
B1 to B10	GND	–	Connect to GND
B11	PORT0_IN	–	Connect to GND
B12	PORT1_IN	–	Connect to GND
B13	V_{DD}	–	Connect to V_{DD} for on-chip debugging (for target system power ON monitoring)

Notes 1. This may be required if $\overline{\text{DRST}}$ of the target device is an alternate-function pin and the initial value of the OCMD0 bit changes according to the reset source. (Refer to section **3.2.8 $\overline{\text{RESET}}$**.)

2. This is required when the target device incorporates flash memory.

3.3.2 MICTOR connector

When using the MICTOR connector as the IE connection connector, mount the following connector on the target system.

2-767004-2: 38-pin type (sold separately)

Remark The 2-767004-2 is a product of Tyco Electronics AMP K.K.

Figure 3-10 and Table 3-2 show the IE connector pin configuration and the pin functions, respectively. Input/output is indicated as seen from the target device.

Figure 3-10. MICTOR Connector Pin Configuration

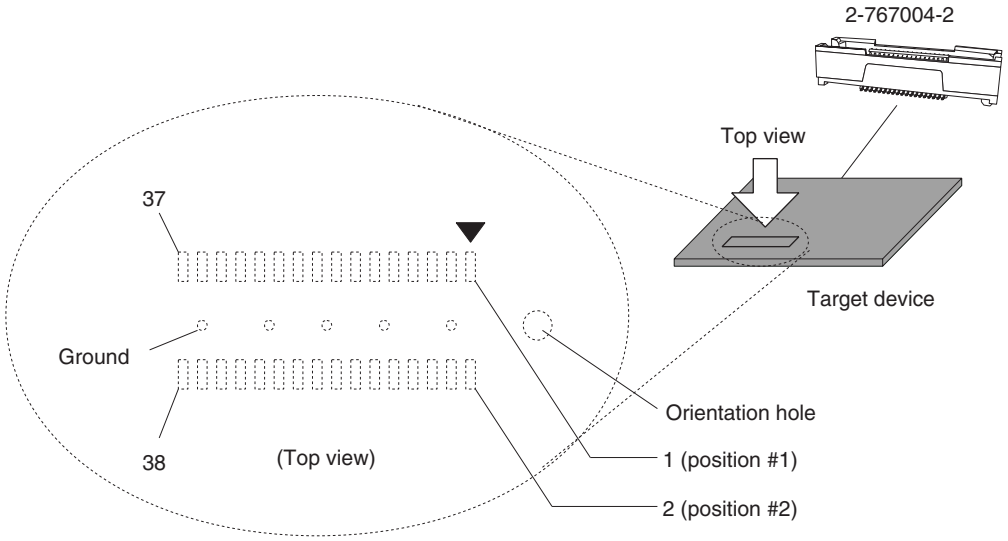


Table 3-2. MICTOR Connector Pin Functions

Pin No.	Signal Name	I/O	Description
1 and 2	GND	–	Connect to GND
3	DCK	IN	Clock input
4	V_{DD}	–	Connect to V_{DD} for on-chip debugging (for target system power ON monitoring)
5	DMS	IN	Transfer mode selection input
6	$\overline{\text{DRST}}$	IN	Reset input to on-chip debug unit
7	DDI	IN	Data input
8	$\overline{\text{RESET}}$	IN	System reset input (leave open when not used)[Note 1]
9	DDO	OUT	Data output
10	FLMD0	IN	Flash mode input (leave open when not used)[Note 2]
11	N.C	–	Open (not connected)
12	RESERVE	–	Open
13	N.C	–	Open (not connected)
14	PORT0_IN	–	Connect to GND
15	N.C	–	Open (not connected)
16	PORT1_IN	–	Connect to GND
17	GND	–	Connect to GND
18	PORT2_IN	–	Connect to GND
19	GND	–	Connect to GND
20	RESERVE	–	Open
21 to 38	GND	–	Connect to GND

Notes 1. This may be required if $\overline{\text{DRST}}$ of the target device is an alternate-function pin and the initial value of the OCMD0 bit changes according to the reset source. (Refer to section **3.2.8 $\overline{\text{RESET}}$**.)

2. This is required when the target device incorporates flash memory.

3.3.3 2.54 mm pitch 20-pin general-purpose connector

If using a 2.54 mm pitch general-purpose connector as the IE connector, mount a connector that can be connected to the IE connection cable on the target system.

Figure 3-11 and Table 3-3 show the IE connector pin configuration and the pin functions, respectively.

Figure 3-11. 2.54 mm Pitch Connector Pin Configuration

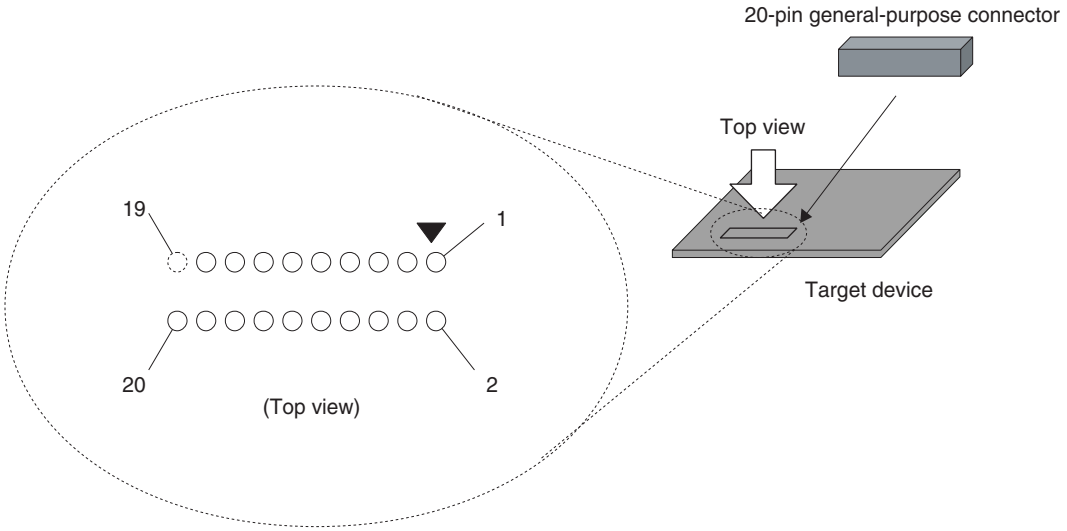


Table 3-3. 2.54 mm Pitch Connector Pin Functions

Pin No.	Signal Name	I/O	Description
1	GND	–	Connect to GND
2	DCK	IN	Clock input
3	GND	–	Connect to GND
4	DMS	IN	Transfer mode selection input
5	GND	–	GND
6	DDI	IN	Data input
7	GND	–	Connect to GND
8	$\overline{\text{DRST}}$	IN	Reset input to on-chip debug unit
9	GND	–	Connect to GND
10	RESERVE	–	Open
11	GND	–	Connect to GND
12	$\overline{\text{RESET}}$	IN	System reset input (leave open when not used)[Note 1]
13	GND	–	Connect to GND
14	FLMD0	IN	Flash mode input (leave open when not used)[Note 2]
15	GND	–	Connect to GND
16	RESERVE	–	Open
17	GND	–	Connect to GND
18	DDO	OUT	Data output
19	GND	–	Connect to GND
20	V_{DD}	–	Connect to V_{DD} for on-chip debugging (for target system power ON monitoring)

Notes 1. This may be required if $\overline{\text{DRST}}$ of the target device is an alternate-function pin and the initial value of the OCMD0 bit changes according to the reset source. (Refer to section **3.2.8 $\overline{\text{RESET}}$**.)

2. This is required when the target device incorporates flash memory.

CHAPTER 4 CAUTIONS ON USE

Observe the following cautions on use to avoid damaging the IE-V850E1-CD-NW.

- Do not place heavy objects on the IE-V850E1-CD-NW, or apply pressure to it.
- Do not drop the IE-V850E1-CD-NW, or subject it to physical shock or vibration.
- Do not use the IE-V850E1-CD-NW in a hot, humid or dusty environment. Avoid using or storing the IE-V850E1-CD-NW in a location where it is exposed to direct sunlight.
- Avoid subjecting the IE-V850E1-CD-NW to sudden environmental changes (in temperature or humidity).
- Do not spill liquids on the IE-V850E1-CD-NW.
- Do not use the connectors or cables of a different product.

APPENDIX A INSTALLATION OF DRIVER

The IE-V850E1-CD-NW is used inserted in the PC card slot on the host machine. The driver must be installed before using the IE-V850E1-CD-NW. The driver is included in the CD-ROM supplied with the IE-V850E1-CD-NW. It can also be downloaded from the website of NEC Electronics (http://www.necel.com/micro/).

The driver is common to the NEC Electronics PC interface card (IE-70000-CD-IF-A).

Refer to "\ID850NWC\DRIVER\README_E.TXT" on the CD-ROM for how to install the driver.

A.1 explains the procedure to install the IE-V850E1-CD-NW driver in Windows 98, and A.2 explains the procedure in Windows 2000.

Table A-1. Operating Environment

Target OS	Windows 98, Windows Me, Windows 2000, Windows NT 4.0, Windows XP
Target host machine	PC-9821 series, PC98-NX series, IBM PC/AT compatible machine with PCMCIA2.1/JEIDA standard Ver4.2-compliant PC card slot
Hardware resources used by the host machine	• I/O address: 100H to 3FFH (Only 20H bytes are available, specifying either 220H, 260H, 2E0H, 320H, or 3E0H as the base address.) • Interrupts: Not used

A.1 Installing in Windows 98

This section explains the procedure to install the driver when using Windows 98.

Installation method

The following describes the step-by-step installation procedure. The CD-ROM drive is assumed as E: in the explanation below.

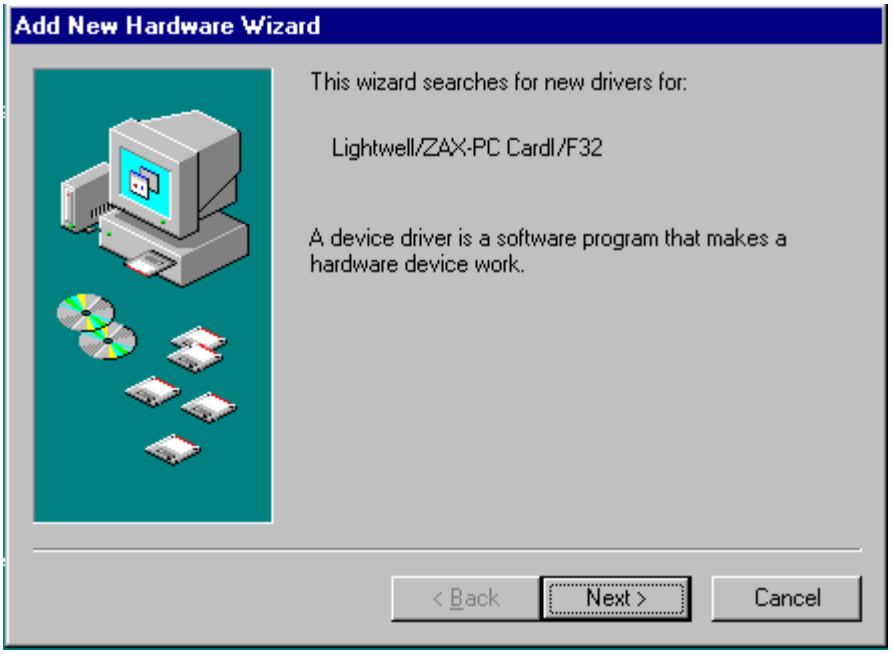
Step 1 Shutdown Windows 98 and turn off the power of the host machine.
Shutdown Windows 98 and turn off the power of the host machine.

Step 2 Insert the IE-V850E1-CD-NW in an open PC card slot.
Insert the IE-V850E1-CD-NW in the PC card slot on the host machine in the direction of the arrow on the surface (refer to **Figure 2-3 Installing IE-V850-CD-NW**).

Step 3 Turn on the power to the host machine and activate Windows 98.
Apply the power to the host machine and activate Windows 98.

Step 4 Install the driver by Plug&Play of Windows 98.

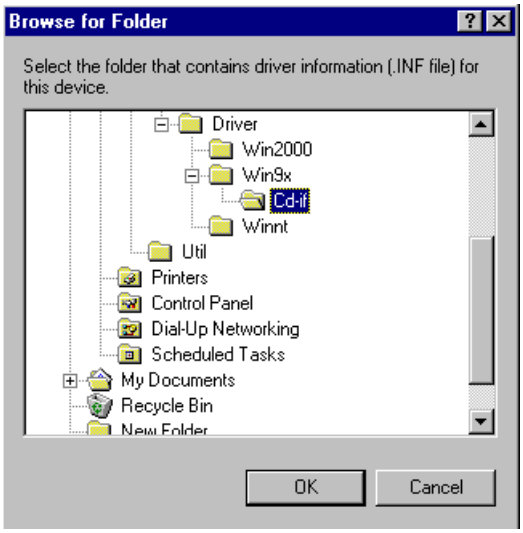
(1) While Windows 98 is being activated, the [Add New Hardware Wizard] window appears. Click [Next].



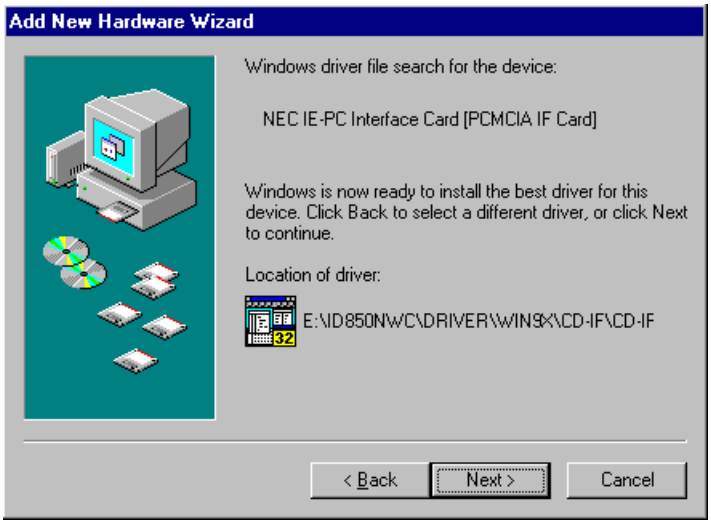
(2) Select “Search for the best driver for your device. (Recommended)” and click [Next].

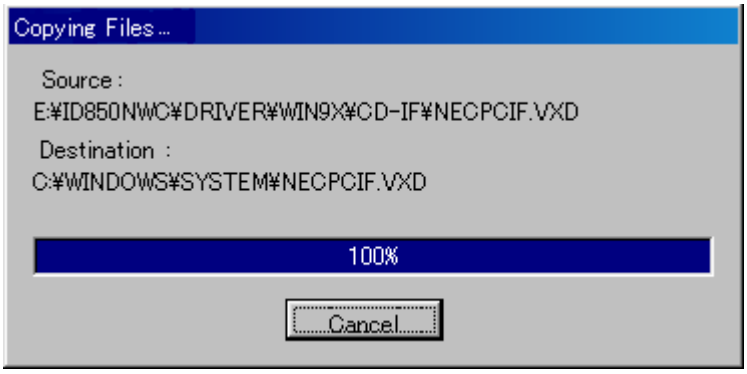
(3) Insert the attached CD-ROM in the CD-ROM drive.

(4) Select “Specify a location:”, input “E:\ID850NWC\DRIVER\WIN9X\CD-IF”, and then click [Next].
Alternately, click [Browse], select “E:\ID850NWC\DRIVER\WIN9X\CD-IF” from the drop-down list, click [OK], and then click [Next].

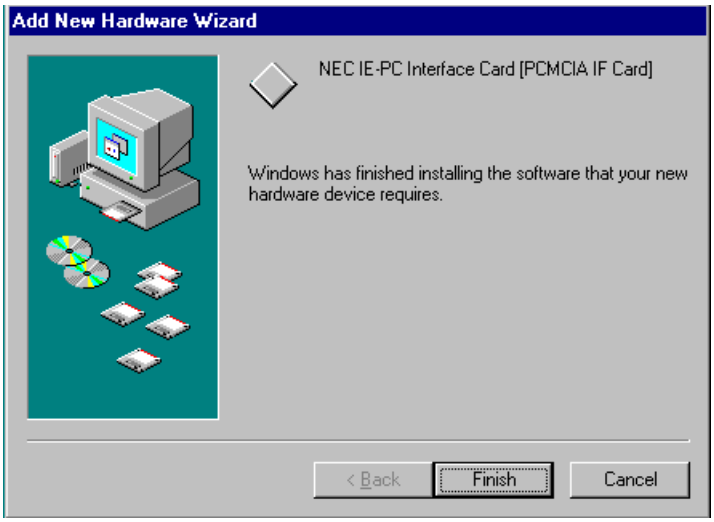


(5) “NEC IE-PC Interface Card [PCMCIA IF Card]” is displayed. Click [Next]. The necessary files are then automatically copied.





(6) Installation is complete. Click [Finish]. Activation of Windows 98 then continues.



A.2 Installing in Windows 2000

This section explains the procedure to install the driver when using Windows 2000.

Installation method

The following describes the step-by-step installation procedure. The CD-ROM drive is assumed as E: in the explanation below.

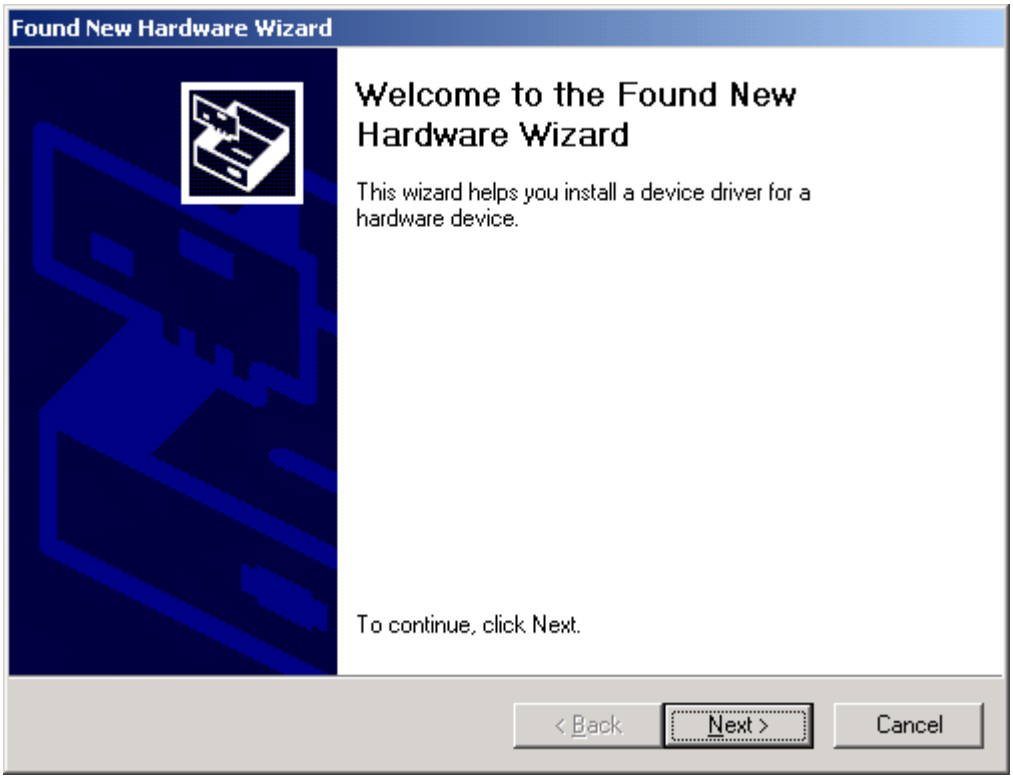
Step 1 Shutdown Windows 2000 and turn off the power of the host machine.
Shutdown Windows 2000 and turn off the power of the host machine.

Step 2 Insert the IE-V850E1-CD-NW in an open PC card slot.
Insert the IE-V850E1-CD-NW in the PC card slot on the host machine in the direction of the arrow on the surface (refer to **Figure 2-3 Installing IE-V850-CD-NW**).

Step 3 Turn on the power to the host machine and activate Windows 2000.
Apply the power to the host machine and activate Windows 2000.

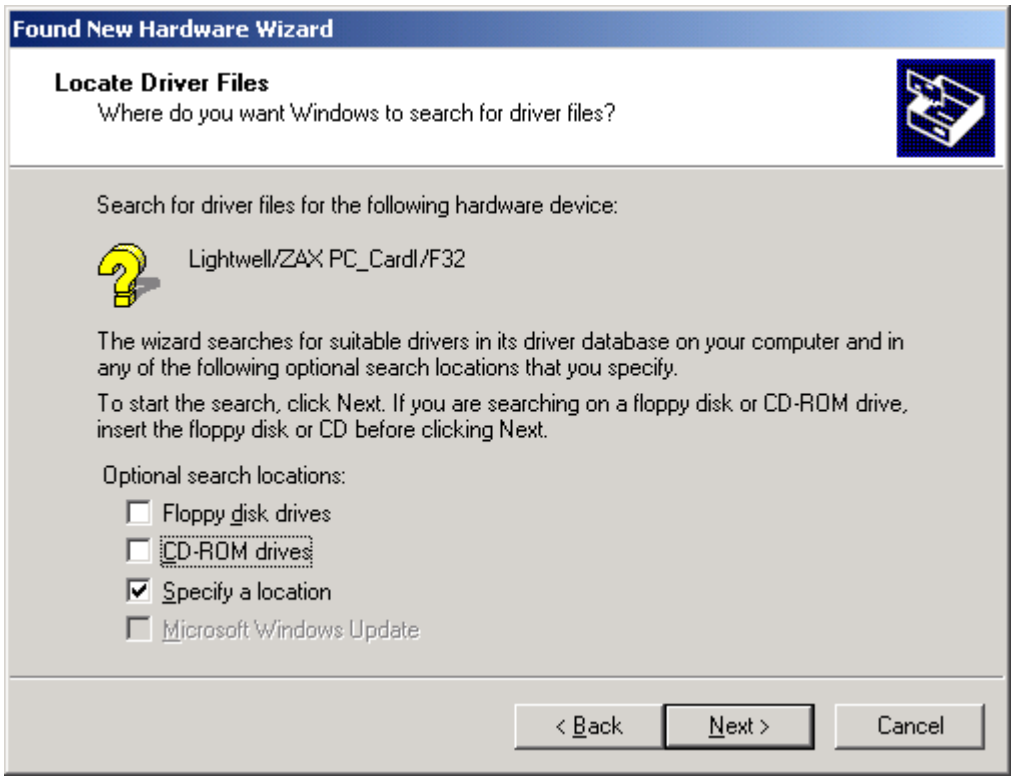
Step 4 Install the driver by Plug&Play of Windows 2000.

(1) While Windows 2000 is being activated, the [Found New Hardware Wizard] window appears. Click [Next].

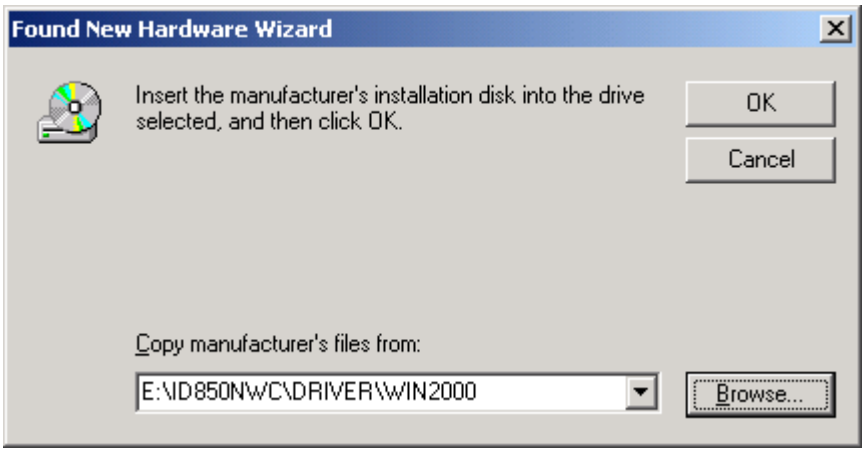


(2) Select “Search for a suitable driver for my device (recommended)” and click [Next].

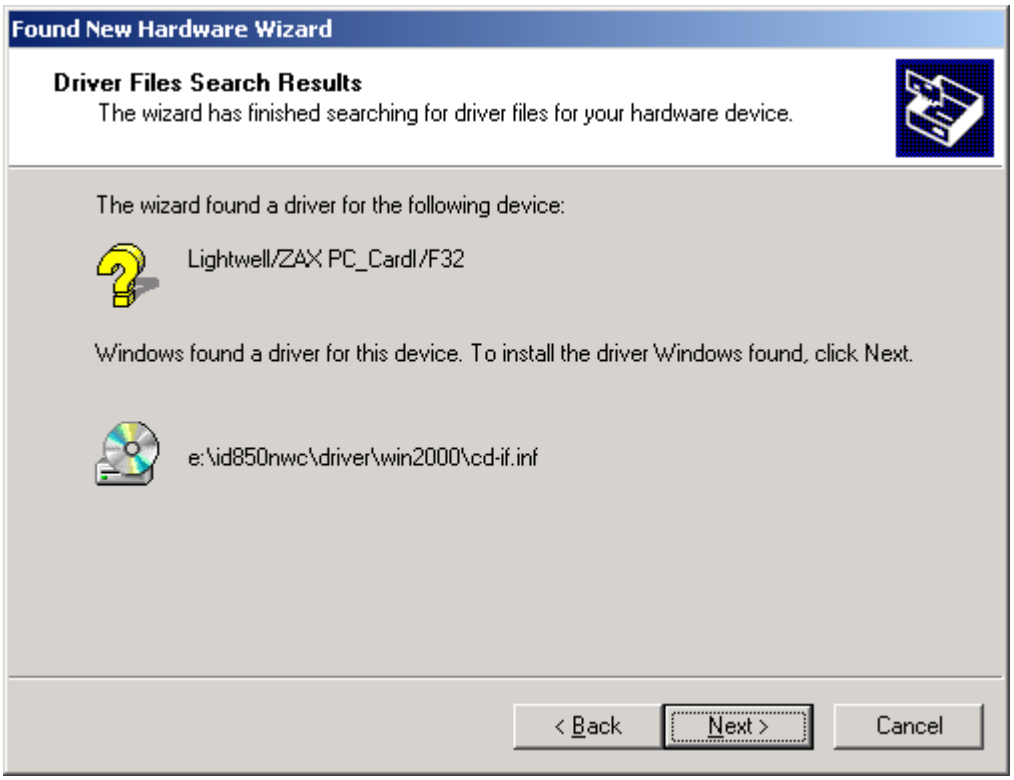
(3) Select “Specify a location” and click [Next].



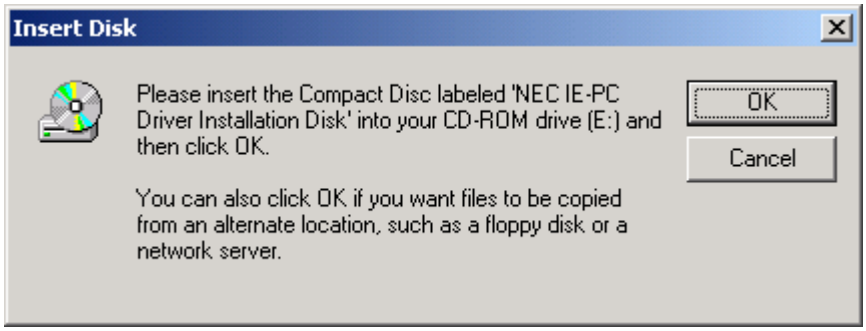
(4) Insert the attached CD-ROM in the CD-ROM drive and input “E:\ID850NWC\DRIVER\WIN2000” in the “Copy manufacturer’s files from:” field and click [OK].



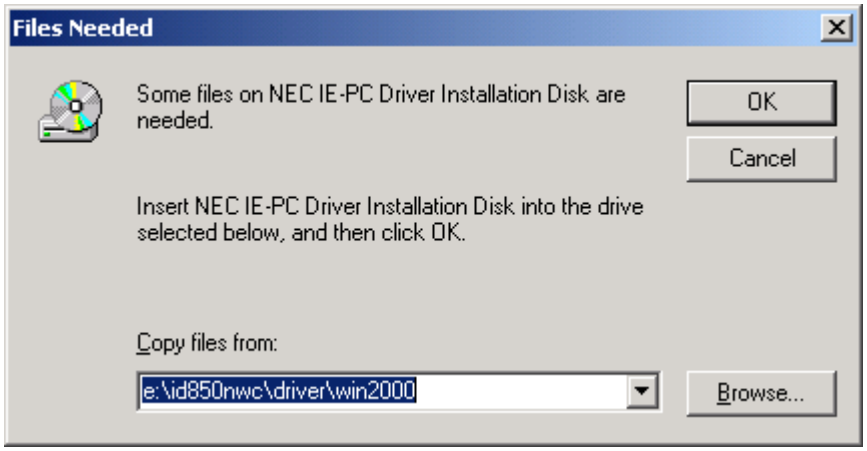
(5) Click [Next].

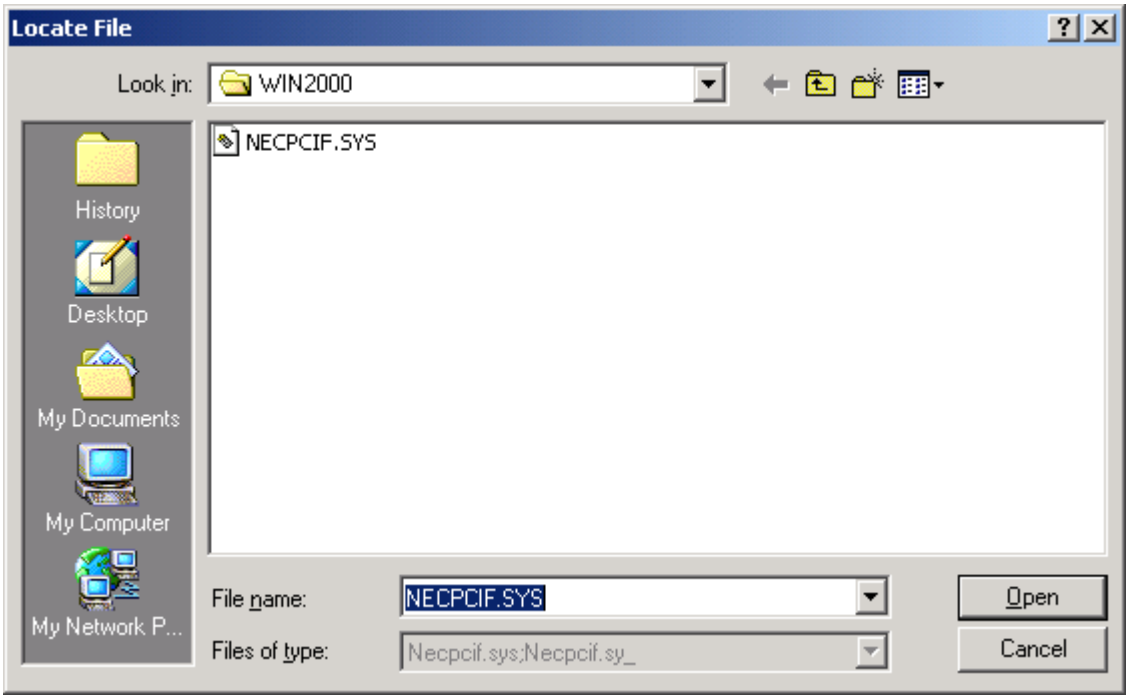


(6) The [Insert Disk] window is displayed. Click [OK].

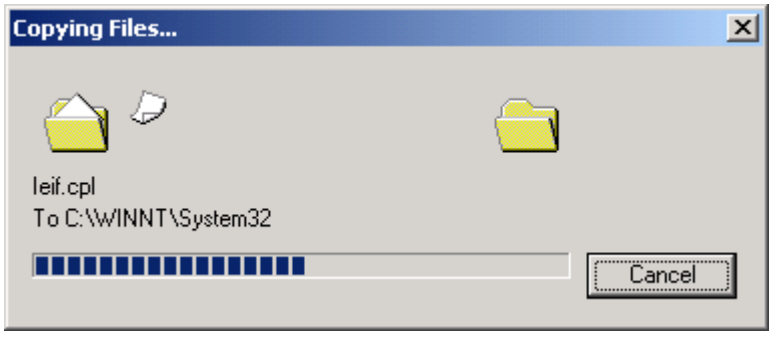


(7) The [Files Needed] window is displayed. Click [Browse] to open the [Locate File] window. Specify NECPCIF.SYS, click [Open], and then click [OK].

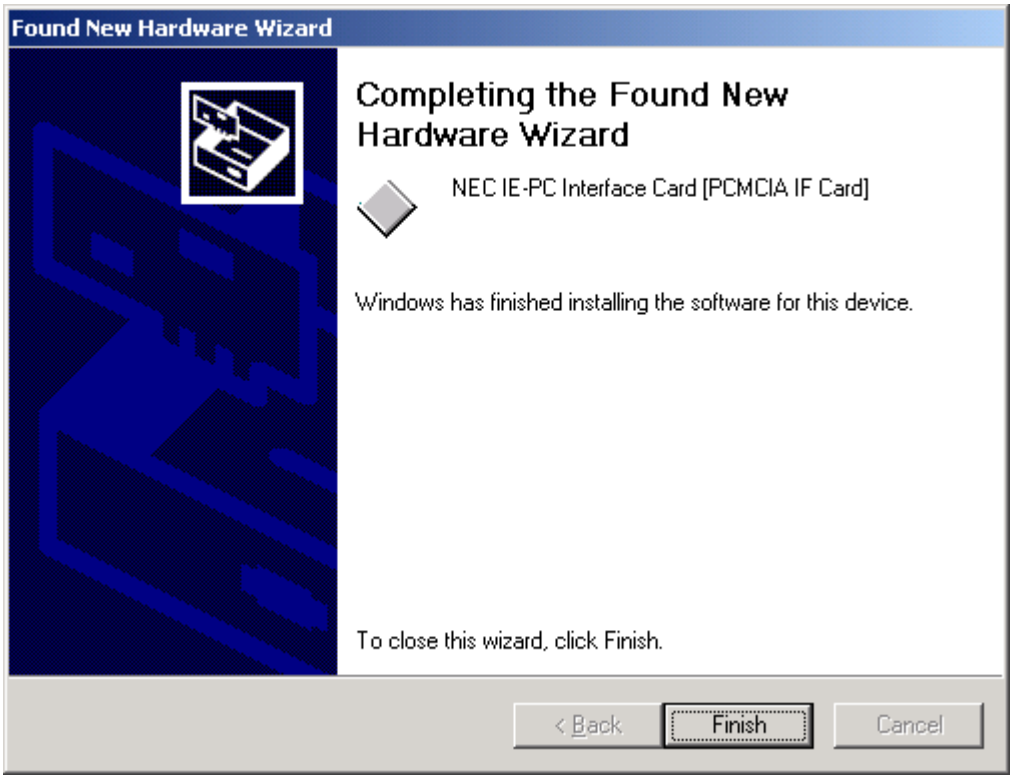




(8) The necessary files are automatically copied.

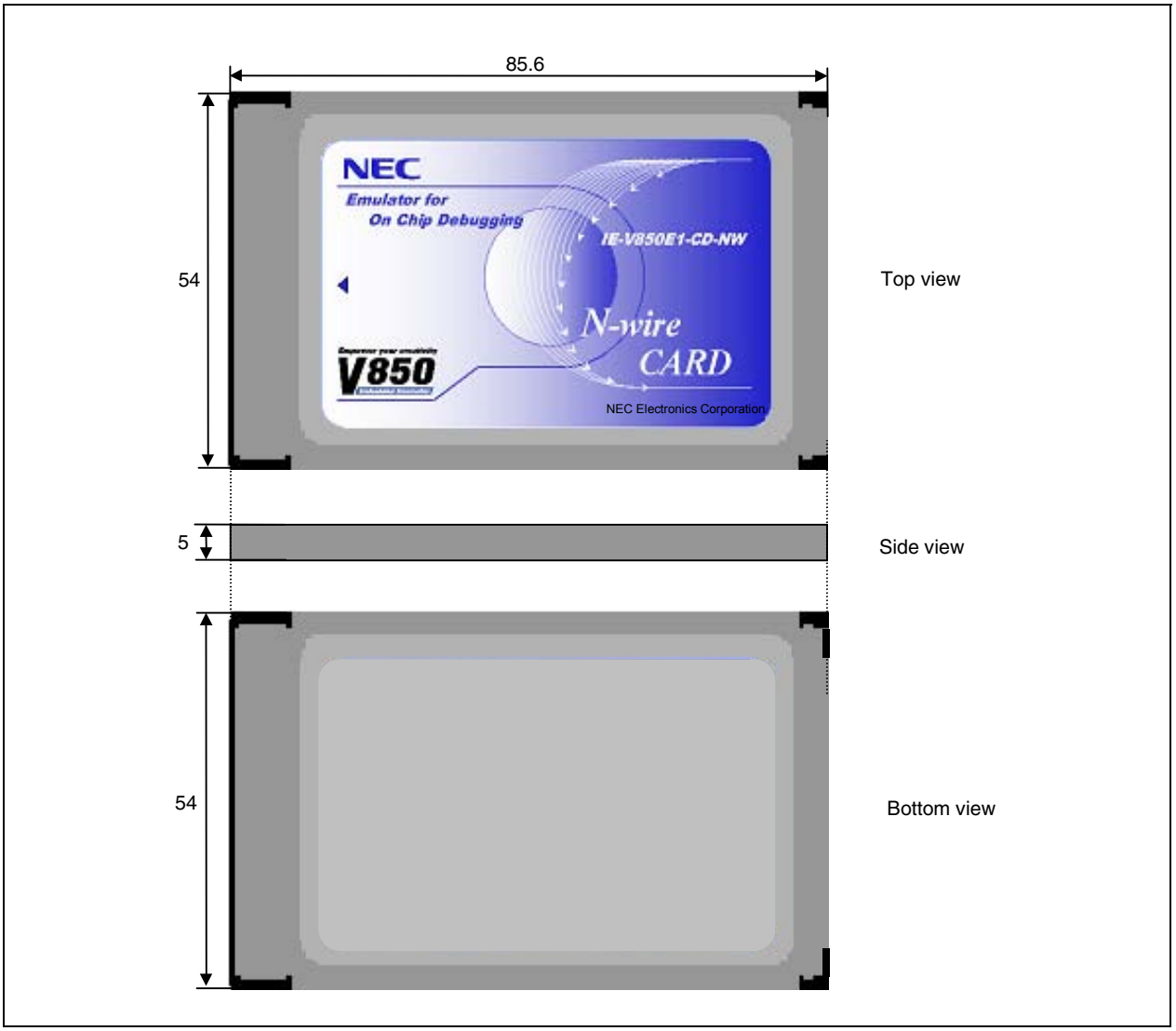


(9) The message “Completing the Found New Hardware Wizard” is displayed. Click [Finish]. Activation of Windows 2000 then continues.

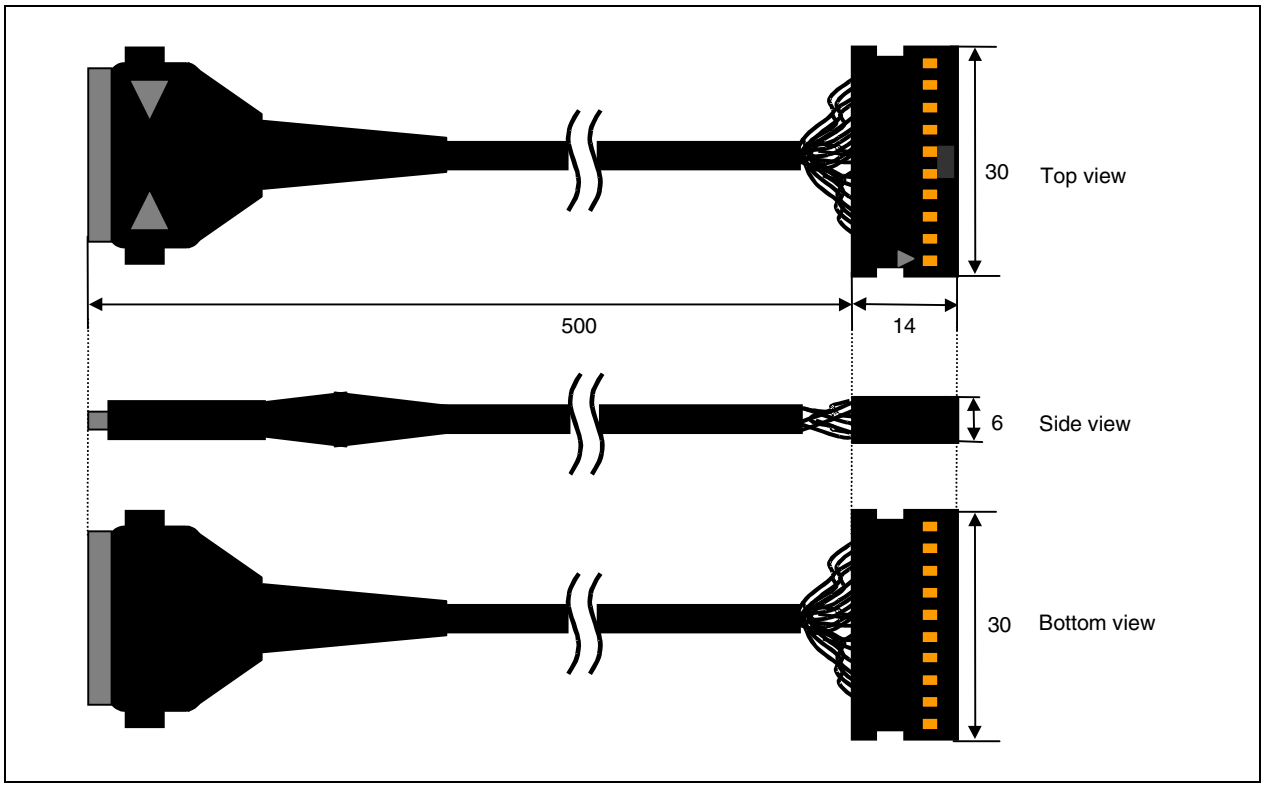


APPENDIX B PACKAGE DIMENSIONS

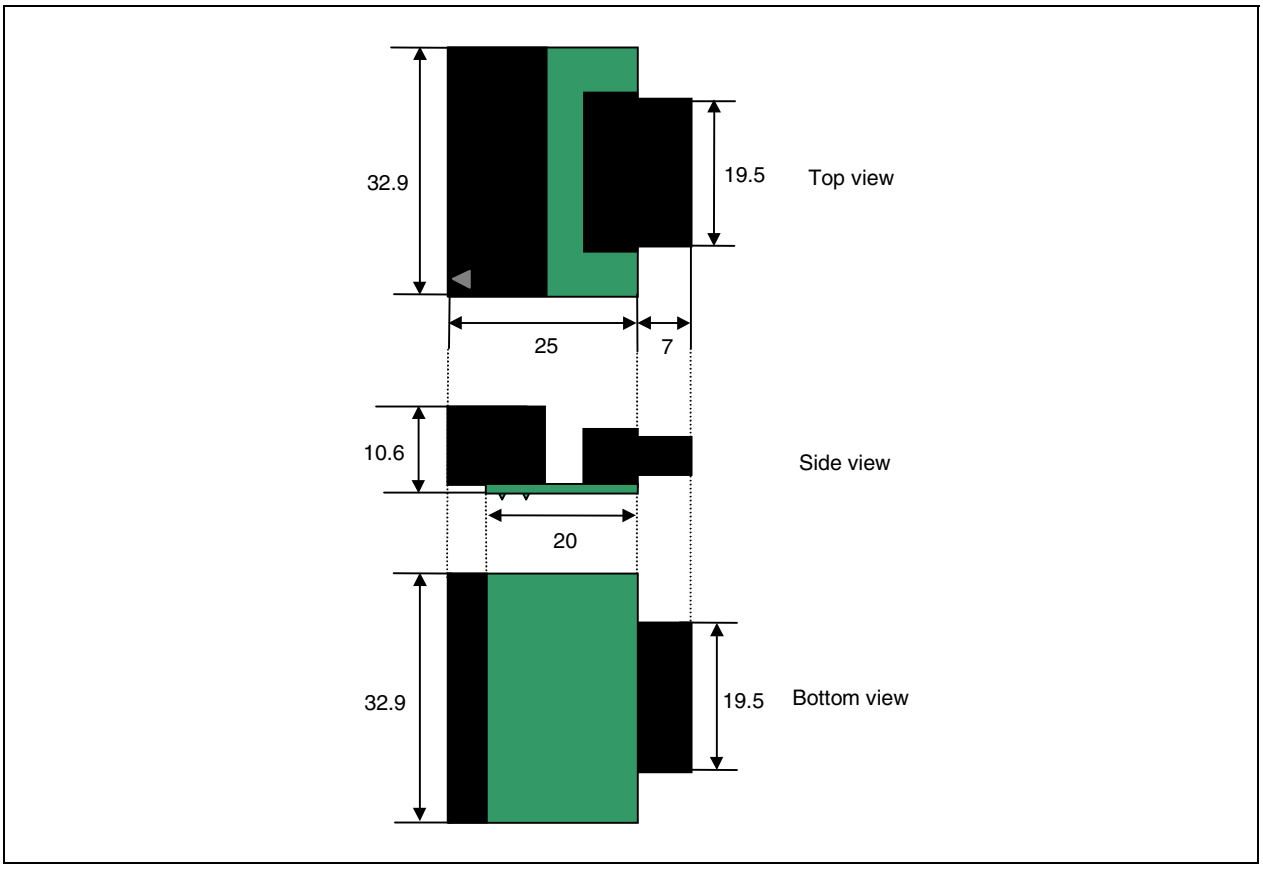
(1) IE-V850E1-CD-NW (unit: mm)



(2) IE connection cable (unit: mm)



(3) Connector conversion board (unit: mm)



APPENDIX C INTERNAL ROM/FLASH MEMORY SECURITY FUNCTION

A ten-byte ID code authentication function is provided in the microcontrollers with internal ROM/flash memory to prevent the memory contents from being read by an unauthorized person.

The ID code specifications are as follows. Embed the ID code in the internal ROM/flash memory in accordance with these specifications. Input the ID code in the Configuration dialog box of the integrated debugger to execute ID code authentication before starting debugging (reading the code of the internal ROM/flash memory of the target device) using the integrated debugger and the IE-V850E1-CD-NW.

[ID code specifications]

- Addresses 0x70 to 0x79 are used as the 10-byte ID code.
- Bit 7 at address 0x79 is used as the N-Wire emulator use enable flag (use disabled if “0”, and enabled if “1”).
- Debugging can be started if the ID code input in the integrated debugger and the ID code embedded in the internal ROM/flash memory match.
- Even if the ID code matches, debugging cannot be performed if the N-Wire emulator use enable flag is “0”.
- When the flash memory is in the erase status, the ID code is 0xFFFFFFFFFFFFFFFFFFFF.

An example of the ID code setting is shown below.

Example) When the following values are set to addresses 0x70 to 0x79

Address	Value [7:0]
0x70	0x12
0x71	0x34
0x72	0x56
0x73	0x78
0x74	0x9A
0x75	0xBC
0x76	0xDE
0x77	0xF1
0x78	0x23
0x79	0xD4

```
Example of assembler
.org 0x70
.byte 12
.byte 34
.byte 56
.byte 78
.byte 9a
.byte bc
.byte de
.byte f1
.byte 23
.byte d4
```

The ID code input in the Configuration dialog box of the integrated debugger ID850NWC is **123456789ABCDEF123D4** or **123456789abcdef123d4**.