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Renesas Electronics Corporation

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RENESAS

Customer Notification

IE-V850ES-G1

In-Circuit Emulator

Operating Precautions

Target device
V850ES

Global Document No. U18079EE6V0IF00 (6th edition)
Document No. TPS-HE-B-3105
Date Published October 2004

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(A) Product Version

1. Product Code: IE-V850ES-G1

Control Code[Note]	EVA Chip	Usable Exec Version
A	D703191AR DS4.5-3V or higher	EX85032.DLL version 5.41 or higher
B	D703191AR DS4.5-3V or higher	EX85032.DLL version 5.41 or higher
C	D703191AR DS4.5-3V or higher	EX85032.DLL version 5.41 or higher
D	D703191AR DS4.5-3V or higher	EX85032.DLL version 5.41 or higher
E	D703191AR DS4.5-3V or higher	EX85032.DLL version 5.41 or higher
F	D703191AR DS4.5-3V or higher	EX85032.DLL version 5.41 or higher

Note: The control code is the digit from the left od a 10-digit control code that starts from E, e.g. EA9040009L means control code A.
In case of an version update you may find an additional label on the bottom of the emulator case where you can take the control code (update level) from.

Caution: In conjunction with the usable exec version a qualified device file (Dxxxxx.800) is additionally necessary for the corresponding device, which has to be emulated. Make sure that you use the appropriated version of the device file. Please refer to the documentation of the dedicated EM1-board.

(B) Table of Operating Precautions

No.		Outline	Control code	IE-V850ES-G1 A	B	C	D/E	F
Restrictions dependent on CPU functions	a-1	Restriction on DMA transfer forcible termination		✗	✗	✗	✗	✗
	a-2	Restriction on program execution and DMA transfer in internal RAM		✗	✗	✗	✗	✗
Restrictions on debug functions	b-1	Restriction on operating frequency		✗	✗	✗	✗	✓
	b-2	Restrictions on break timing when guard area is fetched		✗	✗	✗	✗	✗
	b-3	ROM contents are rewritten if emulation ROM area is accessed for write		✗	✗	✗	✗	✗
	b-4	Restriction of SFR illegal break		✗	✗	✗	✗	✗
	b-5	Restriction on programmable I/O space		✗	✗	✗	✗	✗
	b-6	Break does not occur even if breakpoint is set		✗	✗	✗	✗	✗
	b-7	Restriction related to access address during DMA trace		✗	✗	✗	✗	✗
	b-8	Restriction on DBPC and DBPSW access during a break		✗	✗	✗	✗	✗
	b-9	Restriction on DBTRAP instruction		✗	✗	✗	✗	✗
	b-10	Restriction on access data		✗	✗	✗	✗	✗
	b-11	Restriction on SFR access during break		Supported by debugger				
	b-12	Restriction on target operating voltage		✗	✓	✓	✓	✓
	b-13	Restriction on accessinf emulation ROM area and emulation RAM area		✗	✗	✗	✗	✗

Remark: ✓ : Not applicable
✗ : Applicable

No.		Outline	Control code	IE-V850ES-G1 A	B	C	D/E	F
Restrictions on debug functions	b-14	Restriction that the debugger hangs up depending on the software break setting upon PSC register access		✗	✗	✗	✗	✗
	b-15	Restriction that the same branch instruction is traced twice		✗	✗	✗	✗	✗
	b-16	Restriction on 48-bit length mov instruction trace		✗	✗	✗	✗	✗
	b-17	Restriction on illegal trace of consecutive sld instructions		✗	✗	✗	✗	✗
	b-18	Restriction on pin mask function		✗	✗	✗	✗	✗
Directions of use	c-1	Use of emulation memory		✗	✗	✗	✗	✗
	c-2	Pin handling		✗	✗	✗	✗	✗
	c-3	Power saving		✗	✗	✗	✗	✗
	c-4	Pin control with target power OFF		✗	✗	✗	✗	✗
	c-5	Notes on trace data		✗	✗	✗	✗	✗
	c-6	Notes on instruction cache		✗	✗	✗	✗	✗

Remark: ✓ : Not applicable
✗ : Applicable

(C) Description of Operating Precautions

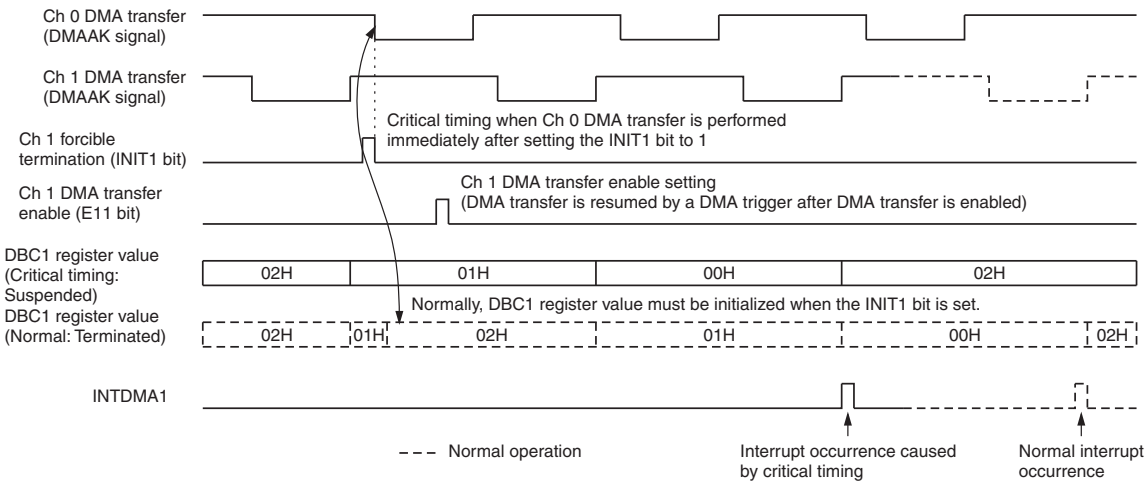
1. Restrictions Dependent on CPU Functions

No. a-1	Restriction on DMA transfer forcible termination (Specification change notice)

Details

When terminating a DMA transfer by setting the corresponding INITn bit of the DCHCn register, the transfer may not be terminated, but just suspended, even though the INITn bit is set (1). As a result, when the DMA transfer of a channel that should have been terminated is resumed, the DMA transfer will terminate after an unexpected number of transfers are completed and a DMA transfer completion interrupt may occur. In addition, a DMA transfer of a channel n for which the INITn bit is set after forcible termination may be performed once again with the initialized value (n= 0 to 3).
The critical situation occurs if a DMA transfer is executed immediately after a forcible termination is set (by setting the INITn bit), refer to figure below.
The critical timing does not depend on the number of transfer channels, transfer type, transfer target, transfer mode, or trigger, and can occur with any combination of the above elements that can be set under the specifications. In addition, another channel may affect the occurrence of this critical timing.

Operation example: Both DMA channels, ch 0 and ch 1, are in single transfer mode, and ch 1 DMA transfer count is 3 (DBC1 register value = 02H).



The following registers are buffer register with a 2-stage FIFO configuration of master and slave:

- DMA source address register (DSAnH, DSAnL)
- DMA destination address register (DDAnH, DDAnL)
- DMA transfer count register (DBCn)

If these registers are overwritten during a DMA transfer, or in the DMA suspended status, the value is written to the master register, and reflected in the slave register when the DMA transfer of the overwritten channel is terminated.
The “initialization” in the figure above means that the contents of the master register are reflected in the slave register.

No. a-1	Restriction on DMA transfer forcible termination (Specification change notice)

(cont.)

Workaround

The critical situation can be avoided by implementing any of the following procedures.

<1> Stop all transfers from DMA channels temporarily.

The following measure is effective if the program does not assume that the TCn bit of the DCHCn register is 1 except for the following workaround processing. (Since the TCn bit of the DCHCn register is cleared (0) when it is read, execution of the following procedure b) under <5> clears this bit.)

Procedure to avoid the critical timing:

<1> Disable interrupts (DI state)

<2> Read the DMA restart register (DRST) and transfer the ENn bit of each channel to a general purpose register (value A).

<3> Write 00H to the DMA restart register (DRST) twice**Note**.

By executing twice**Note**, the DMA transfer is definitely stopped before proceeding to <4>.

<4> Set (1) the INITn bit of the DCHCn register of the channel that should be terminated forcibly.

<5> Perform the following operations for value A read in (2) to obtain value B.

a) Clear (0) the bit of the channel that is not terminated forcibly.

b) If the TCn and ENn bits of the channel that is not terminated forcibly are 1, clear (0) the bit of the channel.

<6> Write value B in <5> to the DRST register.

<7> Enable interrupts (EI state)

Note: Execute three times if the transfer target (transfer source or transfer destination) is the internal RAM.

Remarks: 1. Be sure to execute <5> to prevent the ENn bit from being set illegally for channels that are terminated normally during the period of <2> and <3>

2. n = 0 to 3

<2> Repeat setting the INITn bit until the forcible DMA transfer termination is correctly performed (n = 0 to 3)

Procedure to avoid the critical timing:

<1> Copy the initial transfer count of the channel that should be terminated forcibly to a general-purpose register.

<2> Set (1) the INITn bit of the DCHCn register of the channel that should be terminated forcibly.

<3> Read the value of the DMA transfer count register (DBCn) of the channel that should be terminated forcibly and compare the value with the one copied in <1>. If the value do not match, repeat <2> and <3>.

Remarks: 1. When the DBCn register is read in procedure <3>, the remaining transfer count will be read if the DMA is stopped due to this bug. If the forcible DMA termination is performed correctly, the initial transfer count will be read.

2. Note that it may take some time for forcible termination to take effect if this workaround is implemented in an application in which DMA transfer other than for channels subject to forcible termination are frequently performed.

No. a-2	Restriction on program execution and DMA transfer in internal RAM (Specification change notice)

Details

When a DMA transfer for the internal RAM and a bit manipulation instruction (SET1, CLR1, or NOT1) allocated in the internal RAM or a data access instruction for a misaligned address are executed simultaneously, the CPU may deadlock due to conflict between the internal bus operations. At this time, only a reset can be acknowledged, an NMI or an maskable interrupt cannot be acknowledged any more.

Unaffected cases

The critical situation does not occur if no instruction is executed in the internal RAM, or no DMA transfer is performed on the internal RAM.

Workaround

Implement any of the following workarounds.

- Do not perform a DMA transfer for the internal RAM when an instruction allocated in the internal RAM is being executed.
- Do not execute an instruction allocated in the internal RAM when a DMA transfer for the internal RAM is being performed.

2. Restrictions on Debug Functions

No. b-1	Restrictions on operating frequency (Technical limitation)

Details

The maximum operating frequency is 20 MHz.

Workaround

None. Use a frequency of 20 MHz or lower.

No. b-2	Restrictions on break timing when guard area is fetched (Specification change notice)

Details

When program execution enters the guard area, one instruction in the guard area is executed and then a break occurs.

Workaround

None.

No. b-3	ROM contents are rewritten if emulation ROM area is accessed for write (Specification change notice)

Details

An illegal break occurs if the emulation ROM area is accessed for write, and the data of ROM is rewritten.

Workaround

None.

No. b-4	Restriction on SFR illegal break (Specification change notice)

Details

SFR illegal break is detected by “address condition + R/W attribute”. However, a break occurs if an 8-bit SFR is written in half-word units (break does not occur if an 8-bit SFR is read in half-word units).

Workaround

None.

No. b-5	Restriction on programmable I/O space (Specification change notice)

Details

a) If a programmable I/O space is mapped to the high-order 32 MB area, the programmable I/O space cannot be accessed during break.

b) If the programmable I/O space is access during program execution, an SFR illegal break occurs.

Workaround

a) Map the programmable I/O space to the low-order 32 MB area.

b) Map the area where the programmable I/O space exists to the emulation memory or target memory.

No. b-6	Break does not occur even if breakpoint is set (Specification change notice)

Details

- (Dis)assembly level:
  If breakpoints are set for two instructions in a row and a break occurs at the first instruction, a break may not occur at the second instruction in response to the subsequent request for resumption of execution.

```
0x80049c    mov    r9, r10      ← Setting of breakpoint
0x80049e    add    r7, r10      ← Setting of breakpoint
0x8004a0    addi   1, r10, r7
```

- Source level:
  If breakpoints are set for two execution statements in a row (of which each is expanded for a single instruction) and a break occurs at the first statement, a break may not occur at the second statement in response to the subsequent request for resumption of execution.

```
10   a = b;     (mov   r9, r10)     ← Setting of breakpoint
11   a += c;    (add   r7, r10)     ← Setting of breakpoint
```

Cause

If resumption of execution is requested at the position where program execution is stopped at a breakpoint, the instruction at the breakpoint is internally executed in one instruction step, and execution is resumed.
Some CPUs execute two instructions at a time, dependeing on the combination of instructions. In the above (dis)assembly level example, execution is resumed from address 0x8004a0. Therefore, the breakpoint set at address 0x80049e is not hit.

Workaround

- For software breakpoints preventive measures are implemented to the following debugger versions:
  - NEC debugger: ID850 E2.20f and later versions.
  - GHS Multi: Use EX85032.DLL version 5.40 or later.
  - IAR Embedded Workbench: Use EX85032.DLL version 5.40 or later.

- There is no preventive measure for hardware breaks.

No. b-7	Restrictions related to access address during DMA trace (Specification change notice)

Details

If DMA is started while internal RAM is accessed or the program in the internal RAM is executed, either the source address or destination address of DMA will become 3FFExxxh, indicating an internal RAM address for either of the above or for trace data.

Workaround

None.

No. b-8	Restriction on DBPC and DBPSW access during a break (Specification change notice)

Details

Although DBPC and DBPSW can be read during a break, they cannot be written to.

Workaround

None.

No. b-9	Restriction on DBTRAP instruction (Specification change notice)

Details

If a break occurs in the interrupt processing of a DBTRAP instruction that is executed while a user program is running, the DBPC and DBPSW will be read incorrectly by subsequent RUN instructions.

Workaround

None.

No. b-10	Restriction on access data traced by DMA (Specification change notice)

Details

When data in internal RAM is read by DMA, the read data value is not traced correctly. However, read address, write data, and write address are traced correctly.

Workaround

None.

No. b-11	Restriction on SFR read access during break (Specification change notice)

Details

The SFR bits that are normally cleared by a read access (e.g. TC bit of the DCHC register) are also cleared when displayed during a break by using the SFR display function in the debugger. (Even though these SFR bits are not read by the program they are cleared by displaying them.)

Workaround

None. However, the bit is not reset if the relevant SFR is not displayed by the debugger.
In addition, this restriction can be avoided by using the recent versions of device files and debuggers.

No. b-12	Restriction on target operating voltage (Technical limitation)

Details

Emulation cannot be performed when the target operating voltage is 3.5 V or higher.

Workaround

None.

No. b-13	Restriction on accessing emulation ROM area and emulation RAM area (Specification change notice)

Details

The emulation ROM area and emulation RAM area cannot be accessed via the 8-bit bus.

Workaround

Use the 16-bit bus for accessing the emulation ROM area and emulation RAM area.

No. b-14	Restriction that the debugger hangs up depending on the software break setting upon PSC register access (Specification change notice)

Details

The debugger hangs up if the STB bit of the PSC register is set (1) and a software break is set for the subsequent instruction.

Workaround

Do not set a software break for the subsequent instruction.

Example

```
mov 0x2, r1
st.b  r1, prcmd
st.b  r1,psc
nop       ← The debugger hangs up if a software break is set here.
nop       ← Setting a software break hereafter causes no problem.
```

No. b-15	Restriction that the same branch instruction is traced twice (Specification change notice)

Details

If interrupt generation and execution of a branch instruction (such as JMP, BR CALLT, or CTRET) conflict, the branch instruction is traced twice.
This restriction affects the trace display only. The actual instruction is executed only once.

Example

```
000   7 00000240 0000E007 BRM1  00      nop
001   1 00000242 E0074001 M1    00      reti
002   2 00000242 E0074001 M1    00      reti
003   2                          00
004   5 00000240 0000E007 M1    00      nop
005   1 00000242 E0074001 M1    00      reti
006   2 00000242 E0074001 M1    00      reti
007   2                          00
008   5 00000240 0000E007 M1    00      nop
009   1 00000242 E0074001 M1    00      reti
010   4 00001058 0000BF07 BRM1  00      nop
011   1 0000105A BF07FEFF M1    00      jr 0x1508
012   7 00000240 0000E007 BRM1  00      nop
013   1 00000242 E0074001 M1    00      reti
014   2 00000242 E0074001 M1    00      reti
015   2                          00
016   5 00000240 0000E007 M1    00      nop
017   1 00000242 E0074001 M1    00      reti
018   4 00001058 0000BF07 BRM1  00      nop
019   1 0000105A BF07FEFF M1    00      jr 0x1508
020   7 00000240 0000E007 BRM1  00      nop
```

reti is traced twice if **reti** conflicts with interrupt generation.

reti is traced once if **reti** does not conflict with interrupt generation.

Workaround

None.

No. b-16	Restriction on 48-bit length mov instruction trace (Specification change notice)

Details

If an interrupt occurs at the same time as a 48-bit length mov instruction is executed, the trace result is illegal. At this time, the trace result of the subsequent instruction may also be illegal.
This restriction affects the trace display only. The actual instruction is executed normally.

Example

- Trace result when instruction and interrupt do not conflict (the restriction does not apply).

```
00110  1 000010BE 2F061851 M1                      00  mov 0x205118,r15
00111  2 000010BE 2F062000                         00
00112  1 000010C4 6F070000 M1  0205118 xxxxxxx0 W  00  st.h r0,0x0[r15]
00113  1 000010C8 BF07EAFF M1                      00  jr 0x10b2
```

- Trace result when instruction and interrupt conflict (the restriction applies).

```
00110  1 000010BE 2F061851 M1                      00  ****
00111  2 000010BE 2F062000                         00  mov 0x20f146,r15
                                                       not r0, r0
00112  2                                           00
```

Workaround

None.

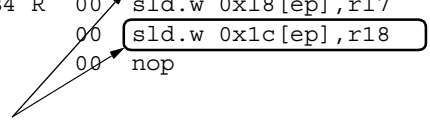
No. b-17	Restriction on illegal trace of consecutive sld instructions (Specification change notice)

Details

When the sld instruction is executed successively, the access data or access address in the trace data may not be displayed. The disassemble data is displayed normally.
This restriction affects the trace display only. The actual instruction is executed normally.

Example

```
021 1 0000002C 00000000 M1                      00  nop
022 1 0000002E 00000000 M1                      00  nop
023 1 00000030 0000005D M1  0FFFC000 A0077C96 R  00  nop
                                                    sld.w 0x0[ep],r11
024 1 00000034 0265046D M1                      00  sld.w 0x4[ep],r12
025 1 00000036 046D0675 M1  0FFFC004 5DD89D8B R  00  sld.w 0x8[ep],r13
026 1 00000038 0675087D M1                      00  sld.w 0xc[ep],r14
027 1 0000003A 087D0A85 M1                      00  sld.w 0x10[ep],r15
028 1 0000003C 0A850C8D M1                      00  sld.w 0x14[ep],r16
029 1 0000003E 0CD80E95 M1  0FFFC018 3FA7F8B4 R  00  sld.w 0x18[ep],r17
030 1 00000040 0E950000 M1                      00  sld.w 0x1c[ep],r18
031 1 00000042 00000000 M1                      00  nop
```



Instructions for which access address/access data is not displayed.

Workaround

None.

No. b-18	Restriction on pin mask function (Specification change notice)

Details

When using Green Hills MULTI, the $\overline{\text{WAIT}}$ and $\overline{\text{HLDRQ}}$ pins are not masked even if pin masking is set using the PINMASK command.
When using IAR Embedded Workbench, the $\overline{\text{WAIT}}$ and $\overline{\text{HLDRQ}}$ pins are not masked even if pin masking is set in the pin mask field of the Emulator→Hardware Setup dialog box.
The $\overline{\text{RESET}}$, STOP, and NMI pins can be masked normally.

Workaround

None.

3. Directions of Use

No. c-1	Use of emulation memory (Direction of use)

Details

- The emulation memory cannot be mapped to addresses higher that 4000000H in the 64 MB mode.
- The number of wait cycles for the emulation memory is not affected by the $\overline{\text{WAIT}}$ signal but is determined by the setting of the debugger or the setting of the wait control register (see table below).

		Emulation Memory Access	External Memory Access
$\overline{\text{WAIT}}$: Unmasked EMWAIT: Masked	Data wait	Fixed to 1 wait	Depends on the DWC0, DWC1 registers settings and $\overline{\text{WAIT}}$ signal status.
	Address wait	Fixed to 0 waits	Depends on the AWC register settings.
	Idle state	Fixed to 0 cycles	Depends on the BCC register settings
$\overline{\text{WAIT}}$: Unmasked EMWAIT: Unmasked	Data wait	Depends on the DWC0, DWC1 registers settings. 1 wait when set to 0 waits.	Depends on the DWC0, DWC1 registers settings and $\overline{\text{WAIT}}$ signal status.
	Address wait	Fixed to 0 waits	Depends on the AWC register settings.
	Idle state	Fixed to 0 cycles	Depends on the BCC register settings

When setting the number of waits for the emulation memory to the same number as for the actual external memory for the purpose of performance testing, select “Target Wait” using the debugger.

- Address waits cannot be inserted in the emulation memory.
  If it is necessary to insert an address wait, set as follows.

Number of data waits for CS space in emulation memory	=	Number of address waits for external memory or external I/O	+	Number of data waits for external memory or external I/O

This setting is effective to make the speed of access to the emulation memory equal to that to the external memory or external I/O when measuring the performance, etc.
Refer to the table above for how to insert waits in the emulation memory.

No. c-1	Use of emulation memory (Direction of use)

(cont)

Details

- The setting of the EXIMC register is not valid for the emulation memory; it is only valid for the memory and I/O that are mapped to the target. The emulation memory oprates via the separate bus regardless of the EXIMC settings.
  Since the difference between the cycle lengths of the multiplexed bus and separate bus is 1 clock, set the multiplexed bus as follows when it is used.
  This setting is effective to make the speed of access to the emulation memory equal to that to the external memory or external I/O when measuring the performance, etc.

Number of data waits for CS space in emulation memory	=	1	+	Number of data waits for external memory or external I/O

No. c-2	Pin handling (Direction of use)

Details

- The in-circuit emulator uses minimum pin handling, giving priority to compatibility with the device. Take adequate countermeasures against static electricity if the in-circuit emulator is used without the target connected.
- Inside the in-circuit emulator, pin handling is performed by the option board. For details, refer to the corresponding User's Manual of the option board.

No. c-3	Power saving (Direction of use)

Details

To save power, be sure to insert five NOP instructions after executing the HALT instruction and an instruction that sets the STB (or STP) bit of PSC register.

a) STB (or STP) bit (PSC register) setting instruction

```
mov     0x2, r11
movea   base_address, r0, r20    ; base_address = FFFF0000H
st.b    r11, PRCMD[r20]          ; PRCMD = 01FCH
st.b    r11, PSC[r20]            ; PSC = 01FEH
nop                              ; insert five nop's
nop
nop
nop
nop
```

b) HALT instruction

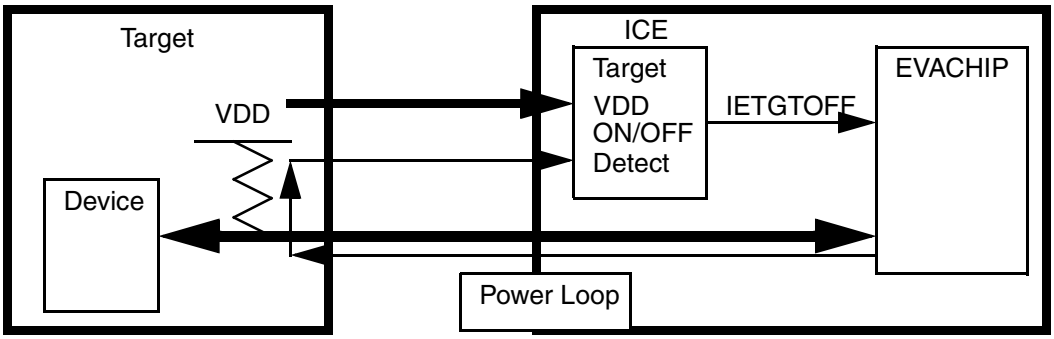
```
halt
nop                              ; insert five nop's
nop
nop
nop
nop
```

No. c-4	Pin control with target power OFF (Direction of use)

Details

When power to the emulator is ON and that to the target is OFF, leakage current may flow from the emulator to the target.
When the target is connected, the emulator always senses the target supply voltage by using a target supply voltage detector circuit, and the emulator is automatically reset when the target power is turned ON or OFF. In this reset status, the external bus signal go inter a high-impedance state.
Some external bus signals, however, drive a high level, and a current may leak into Vdd of the target via the pull-up resistor of the target.

The target supply voltage detector circuit of the emulator detects this VDD, and the emulator assumes that power is applied to the target. Consequently, reset is cleared and the external bus signals are driven. As a result, a leakage current flows.



No. c-5	Notes on trace data (Direction of use)

Details

- **Trace sequence of access data of LD and ST instructions**

If the LD and ST instructions are executed in that order, access of the ST instruction and access of the LD instruction are traced in this order for trace data.
If the LD instruction is the shortest (IRAM access), the read data is written to the same frame as the LD instruction. If the bus cycle is extended because of external memory access, the read data is written to trace after the ST instruction.
For instruction execution (fetch), the instruction that comes first is traced, and relation can be established based on the information on the access validity flag and direction of read/write.

Basically, because the data is known in the write cycle, preparation for writing the data to the tracer is made when the ST instruction is executed. In the read cycle, the data is written to the tracer when the read cycle is completed and the data is loaded. If the LD and ST instructions are arranged, therefore, the sequence of only the access data of the trace data may be reversed, like the data of the ST instruction → data of the LD instruction.

- **Trace timing of external logic data**

It takes the external logic data the number of clocks required for fetching 8 x 1 times to be output to the tracer.

The external logic data is sampled in synchronization with instruction execution and differs depending whether a program is stored in IROM or external memory, and on the number of wait cycles.
When a program is placed in the external memory, it also differs depending on whether a read/write cycle is inserted in the external memory.
The shortest time is 8 clocks when a program is placed in IROM.
The point to be noted is that the external logic data is not sampled every clock.
Because it is not sampled unless instruction execution is performed, a signal that changes after execution of on instruction and before execution of another cannot be detected.
If there is a possibility that an instruction is executed every clock as is the case with IROM, therefore the chance of missing the external logic data decreases. Conversely, if many wait cycles are inserted in the external memory, the chance of missing the external logic data increases.

No. c-6	Caution on fail-safe break in internal ROM/RAM area (Direction of use)

Details

The internal ROM/RAM of the in-circuit emulator is set as follows depending on the debugger setting.

Internal ROM	
Debugger Setting	Internal ROM space to Be Mapped (When Mapped from 00000000H Address)
0 KB	None
32 KB	00000000H to 00007FFFH
64 KB	00000000H to 0000FFFFH
128 KB	00000000H to 0001FFFFH
256 KB	00000000H to 0003FFFFH
512 KB	00000000H to 0007FFFFH
1024 KB	00000000H to 000FFFFFH
Other	Depends on the target device

Remark: No fail-safe occurs in any mapping case when an access (instruction fetch or data read access) to 00000000H to 000FFFFFH is performed. A write protect break occurs when a write access is performed.
To disable accessing to the space from 00080000H to 000FFFFFH, for example when 512 KB is set, implement a measure such as setting an event break.
In addition, no fail-safe break occurs when an access (instruction fetch or data read access) to 00100000H to 001FFFFFH is performed if internal ROM exists from address 00100000H.

(D) Valid Specification

Item	Date published	Document No.	Document Title
1	March 2003	U16313EJ1V0UM00	IE-V850ES-G1 In-Circuit Emulator (User's Manual)

(E) Revision History

Item	Date published	Document No.	Comment
1	June 2002	TPS-HE-B-3100	Initial release
2	June 2002	TPS-HE-B-3101	Revision of table of operating precautions
3	September 2002	TPS-HE-B-3102	Addition of control code C
4	October 2002	TPS-HE-B-3103	Addition of control code D
5	December 2003	TPS-HE-B-3104	Release in new format. Operating precautions are divided into “Restrictios dependent on CPU functions” (a), “Restrictions on debug functions” (b) and “Directions of use” (c) Former operating precaution no. 1 has been deleted. Former operating precautions no. 2 to 13 have got new no. b-1 to b-12. Additon of operating precautions no. a-1, a-2, b-13 to b-18. Former chapter of cautions adapted to the table format (c-1 to c-6).
6	October 2004	TPS-HE-B-3105	Addition of control F, for which restriction b-1 has been abolished.