

Nuvoton
Bus Termination Regulator
W83310DG

Data Sheet Revision History

NO	PAGES	DATES	VERSION	MAIN CONTENTS
1.	All	June, 2007	1.0	Remove non Pb-free part no: W83310DS
2	All	Dec., 2008	1.01	Change to Nuvoton document format
3				
4				
5				
6				

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LIFE SUPPORT APPLICATIONS

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1. GENERAL DESCRIPTION

The W83310DG is a linear regulator which provides power with the capability of continuous 2.0Amp bi-directional sinking and driving current for a high speed bus terminator application. The chip simply implements a stable power supply which tracks dynamically half of the input power. The output of the power supply follows the input of VREF1 and VREF2 pins. Setting the BOOT_SEL pin can decide to follow VREF1 or VREF2.. The W83310DG is promoted with small footprint 8-SOP 150mil power package. The design of the W83310DG provides a high integration, high performance, and cost-effective solution.

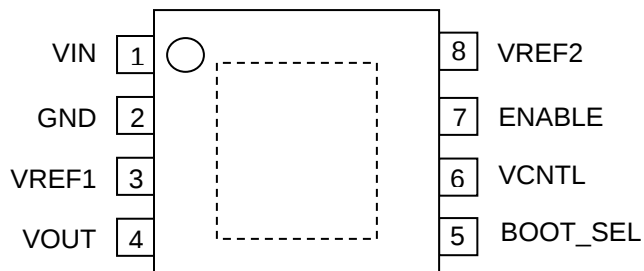
2. FEATURES

- Support DDRI (1.25VTT), DDRII (0.9VTT) and DDRIII (0.75VTT) Requirements
- Sink and Source 2A Continuous Current
- Integrated Power MOSFET
- Adjustable VOUT by External Resistors
- Low External Component Count
- Low Output Voltage Offset
- Short Circuit Protection
- 0°C to 70°C Ambient Operating Temperature Range
- SOP-8 (Exposed Pad) Package, Lead (Pb) Free

3. APPLICATIONS

- Desktop PCs, Notebooks, and Workstations
- Graphics Card Memory Termination
- DDRI, DDRII and DDRIII Memory Systems

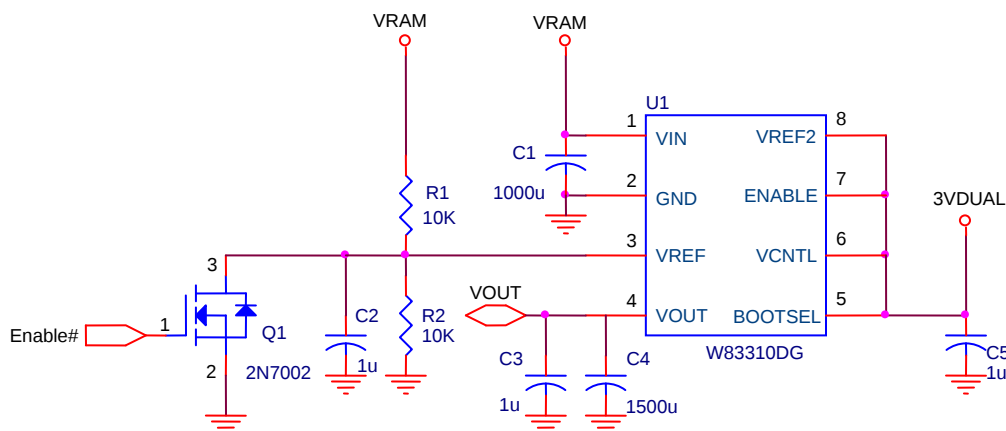
4. PIN CONFIGURATION AND DESCRIPTION



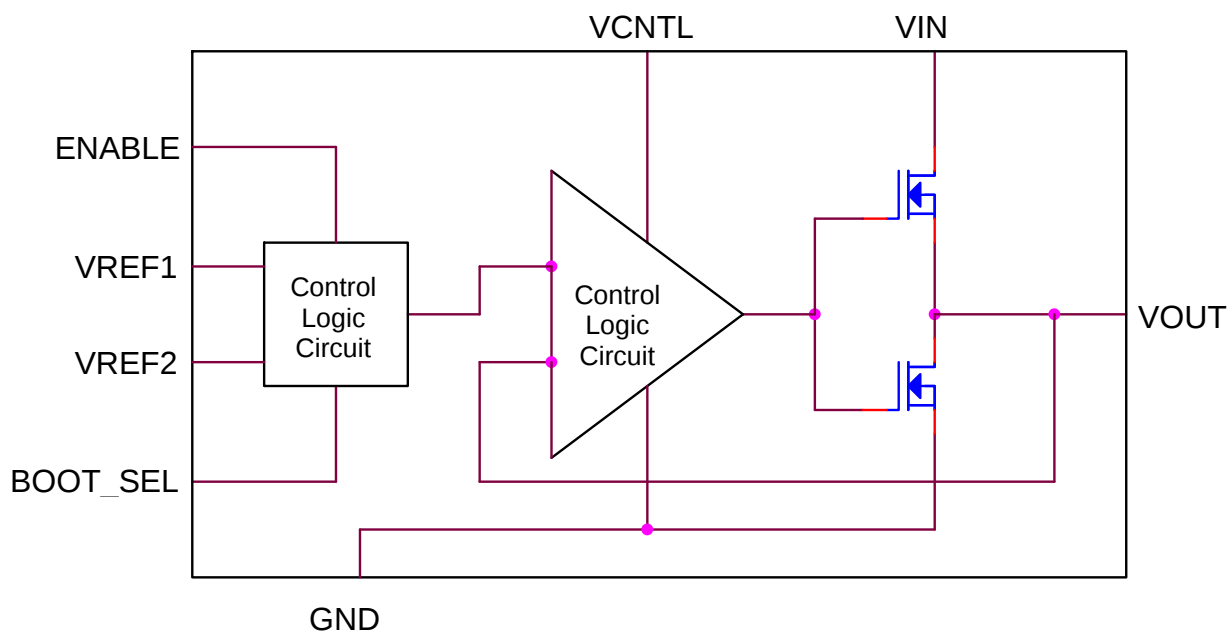
W83310DG
(Top View)

SYMBOL	PIN	I/O	FUNCTION
VIN	1	I	Main power input pin which supplies current to the output pin.
GND	2		Ground
VREF1	3	I	Internal reference voltage source1. Reference voltage on the pin will be referred with the pin value when BOOT_SEL pin is set High.
VOUT	4	O	Voltage output pin which is regulated to VREF voltage.
BOOT_SEL	5	I	The signal for the chip reference voltage source selection. The function is designed for Intel® Springdale chipset GMCH_V _{TT} application.
VCNTL	6	I	Power for internal control logic circuitry.
ENABLE	7	I	Chip function enable pin. 1: Enable; 0: Disable
VREF2	8	I	Internal reference voltage source2. Reference voltage on the pin will be referred with the pin value when BOOT_SEL pin is set Low.

5. APPLICATION CIRCUIT



6. INTERNAL BLOCK DIAGRAM



7. ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Input Voltage	VIN	-0.3 to 5	V
Control Logic Input Voltage	VCNTL	-0.3 to 5	V
Electrostatic discharge protection	Human Body Mode	±2	kV
	Machine Mode	±200	V
	Latch-Up	±100	mA
Package Thermal Resistance	θ_{JA}	75	°C/W
Storage Temperature Range		-65 to 150	°C

8. RECOMMENDED OPERATING CONDITIONS

ITEM	SYMBOL	MIN	MAX	UNIT
Input Voltage	VIN	1.5	3.6	V
	VCNTL	3	3.6	
Operating Temperature Range		0	70	°C
Junction Temperature Range		0	125	°C

9. ELECTRICAL CHARACTERISTICS

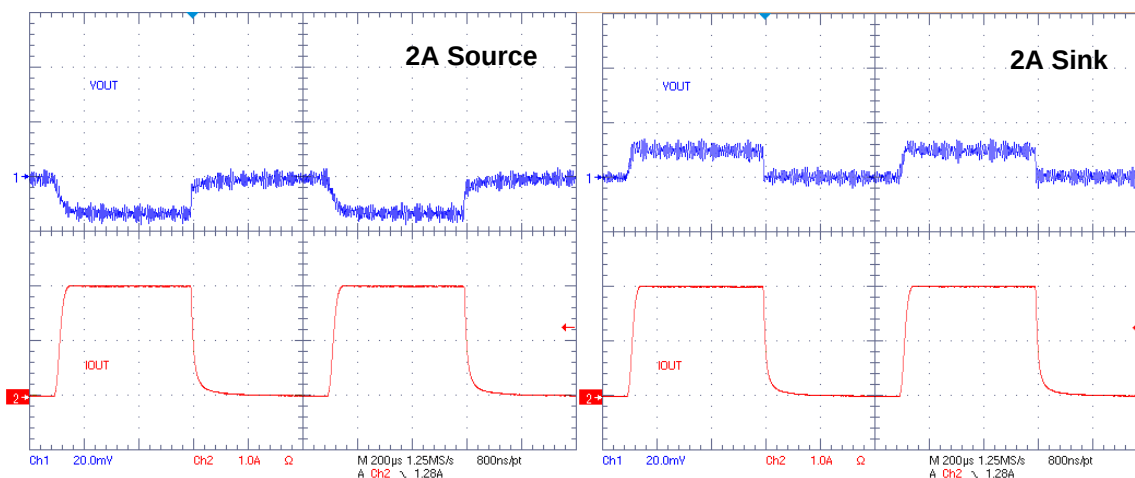
$T_A = 25^\circ\text{C}$, VCNTL= 3.3 V, VIN=2.5V/1.8V/1.5V, VREF=1.25V/0.9V/0.75V, C_{OUT}=1000uF, all voltage outputs unloaded (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
Input						
VCNTL Operating Current	I _{CNTL}	I _{OUT} =0A	--	0.5	1	mA
Output (DDRI / DDRII / DDRIII)						
Output Offset Voltage	V _{OS}	I _{OUT} =0A	-5	0	5	mV
Load Regulation	ΔV _L	I _{OUT} =0 → +2A	-40	--	40	mV
		I _{OUT} =-0 → 2A	-40	--	40	
Protection						
Short Current Limit	I _{LIM}	V _{OUT} short to ground	--	4	--	A
VREF1/2 Shutdown Mode						
Shutdown Threshold	V _{IH}	Enable	0.8	--	--	V

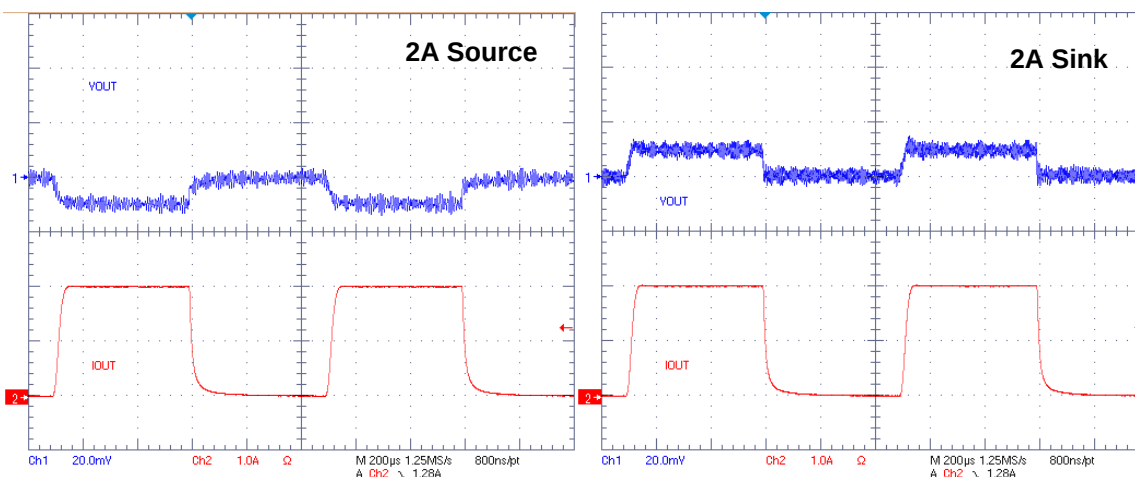
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
	V_{IL}	Disable	--	--	0.2	
Input Pins Trigger Level						
BOOT_SEL Pin	V_{IH}	High	1	--	--	V
	V_{IL}	Low	--	--	0.2	
ENABLE Pin	V_{IH}	Enable	1	--	--	V
	V_{IL}	Disable	--	--	0.2	

10. TYPICAL OPERATING WAVEFORMS

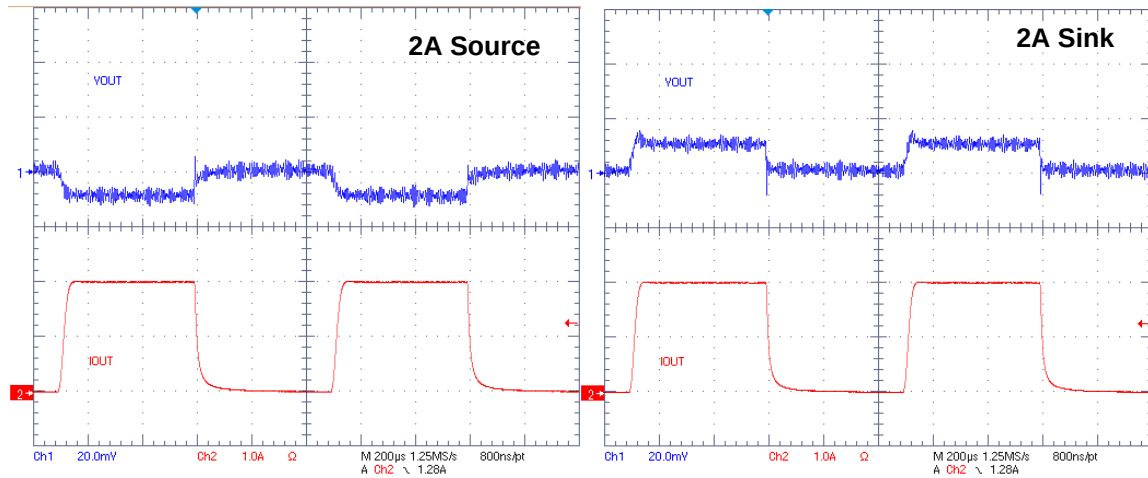
- Transient Response, $V_{CNTL}=3.3V$, $V_{IN}=2.5V$, $V_{REF}=1.25V$, $V_{OUT}=1.25V$



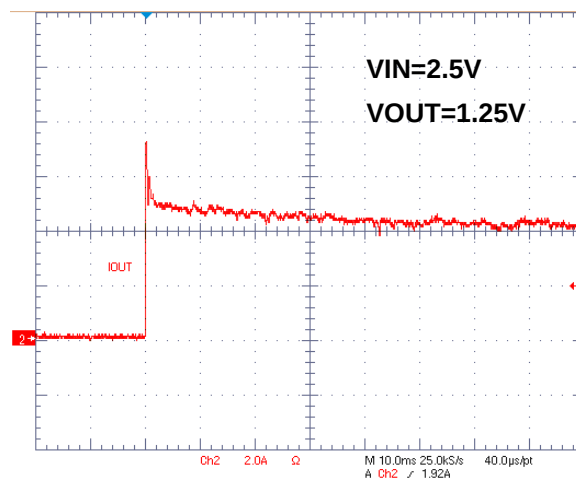
- Transient Response, $V_{CNTL}=3.3V$, $V_{IN}=1.8V$, $V_{REF}=0.9V$, $V_{OUT}=0.9V$

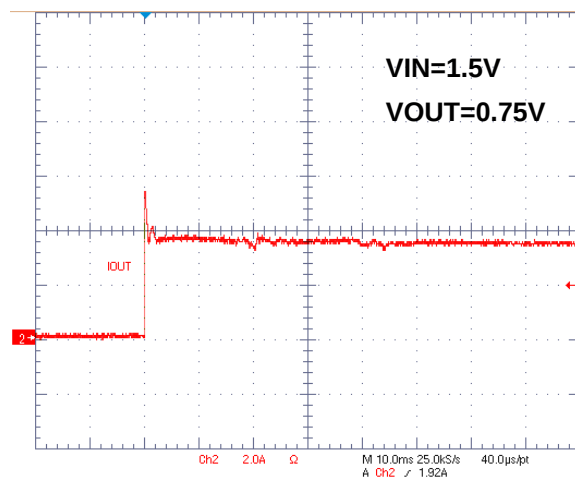
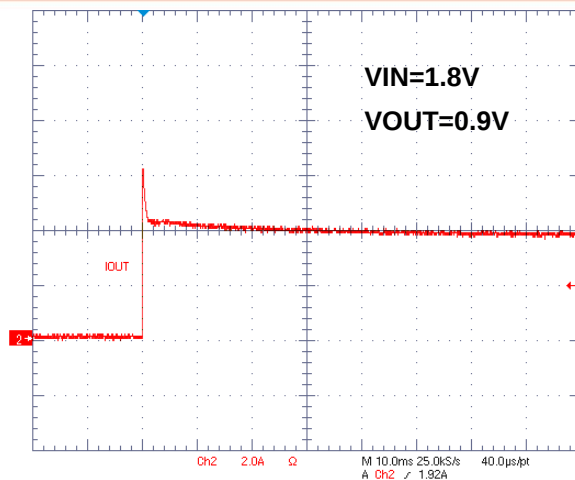


- Transient Response, $V_{CNTL}=3.3V$, $V_{IN}=1.5V$, $V_{REF}=0.75V$, $V_{OUT}=0.75V$

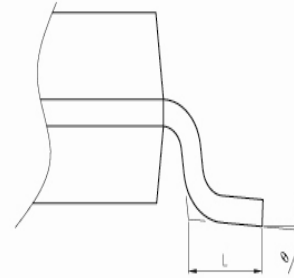
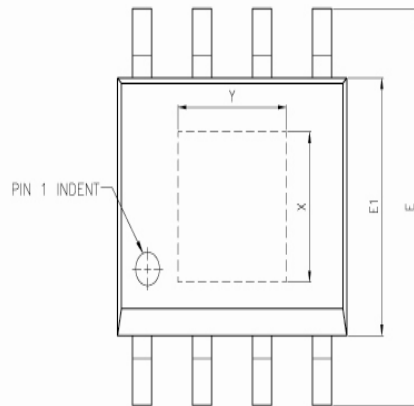


- Output Short Circuit Protection, $V_{CNTL}=3.3V$, V_{OUT} shorted to ground

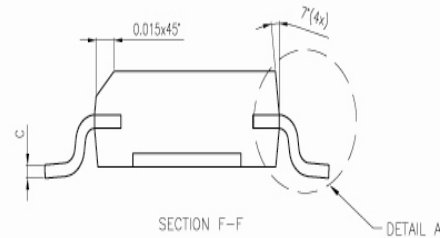
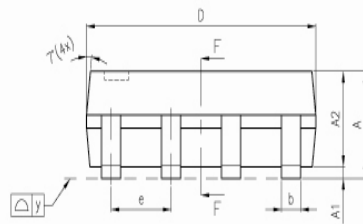




11. PACKAGE DIMENSION



DETAIL A



SECTION F-F

NOTE :

1. CONTROLLING DIMENSION : INCH
2. LEAD FRAME MATERIAL : COPPER 194
3. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS AND GATE BURRS. MOLD FLASH, TIE BAR BURRS AND GATE BURRS SHALL NOT EXCEED 0.006"[0.15mm] PER END. DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010"[0.25mm] PER SIDE.
4. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.003"[0.08mm] TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.0028"[0.07mm]
5. TOLERANCE : ± 0.010 "[0.25mm] UNLESS OTHERWISE SPECIFIED.
6. OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPEC.
7. REFERENCE DOCUMENT : JEDEC SPEC MS-012

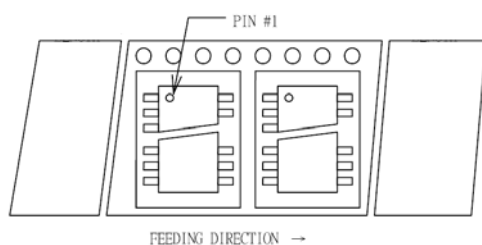
SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.05	—	0.15	0.002	—	0.006
A2	—	1.45	—	—	0.057	—
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.79	5.99	6.20	0.228	0.236	0.244
E1	3.81	3.91	3.99	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
L	0.38	0.71	1.27	0.015	0.028	0.050
y	—	—	0.076	—	—	0.003
θ	0°	—	8°	0°	—	8°

EXPOSED PAD DIMENSION : (MIL)

PAD SIZE: $\times$ $\times$

90°90

➤ TAPING SPECIFICATION



8 Pin ESOP Package

12. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	SUPPLIED AS	PRODUCTION FLOW
W83310DG	8PIN ESOP(Pb-free package)	E Shape: 100 units/Tube T Shape: 2,500 units/T&R	Commercial, 0°C to +70 °C

13. HOW TO READ THE TOP MARKING



Left line: Winbond logo (Nuvoton)

1st & 2nd line: W83310DG – the part number

3rd line: Tracking code 706 X Y

706: Packages assembled in Year 07', week 06

X: Assembly house ID Code

Y: The IC version Code

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