ADC12DL066 Dual 12-Bit, 66 Msps, 450 MHz Input Bandwidth A/D Converter w/Internal Reference

Check for Samples: ADC12DL066

FEATURES

- **Choice of Binary or 2's Complement Output Format**
- **Single +3.3V Supply Operation**
- **Outputs 2.4V to 3.3V Compatible**
- **Pin Compatible with ADC12D040**
- **Power Down Mode**
- **Internal/External Reference**

KEY SPECIFICATIONS

- **Resolution: 12 Bits**
- **DNL: ±0.5 LSB (typ)**
- **SNR (f_{IN} = 10 MHz): 66 dB (typ)**
- **SFDR (f_{IN} = 10 MHz): 81 dB (typ)**
- **Power Consumption**
  - **Operating: 686 mW (typ)**
  - **Power Down Mode: 75 mW (typ)**

APPLICATIONS

- **Ultrasound and Imaging**
- **Instrumentation**
- **Communications Receivers**
- **Sonar/Radar**
- **xDSL**
- **Cable Modems**
- **DSP Front Ends**

DESCRIPTION

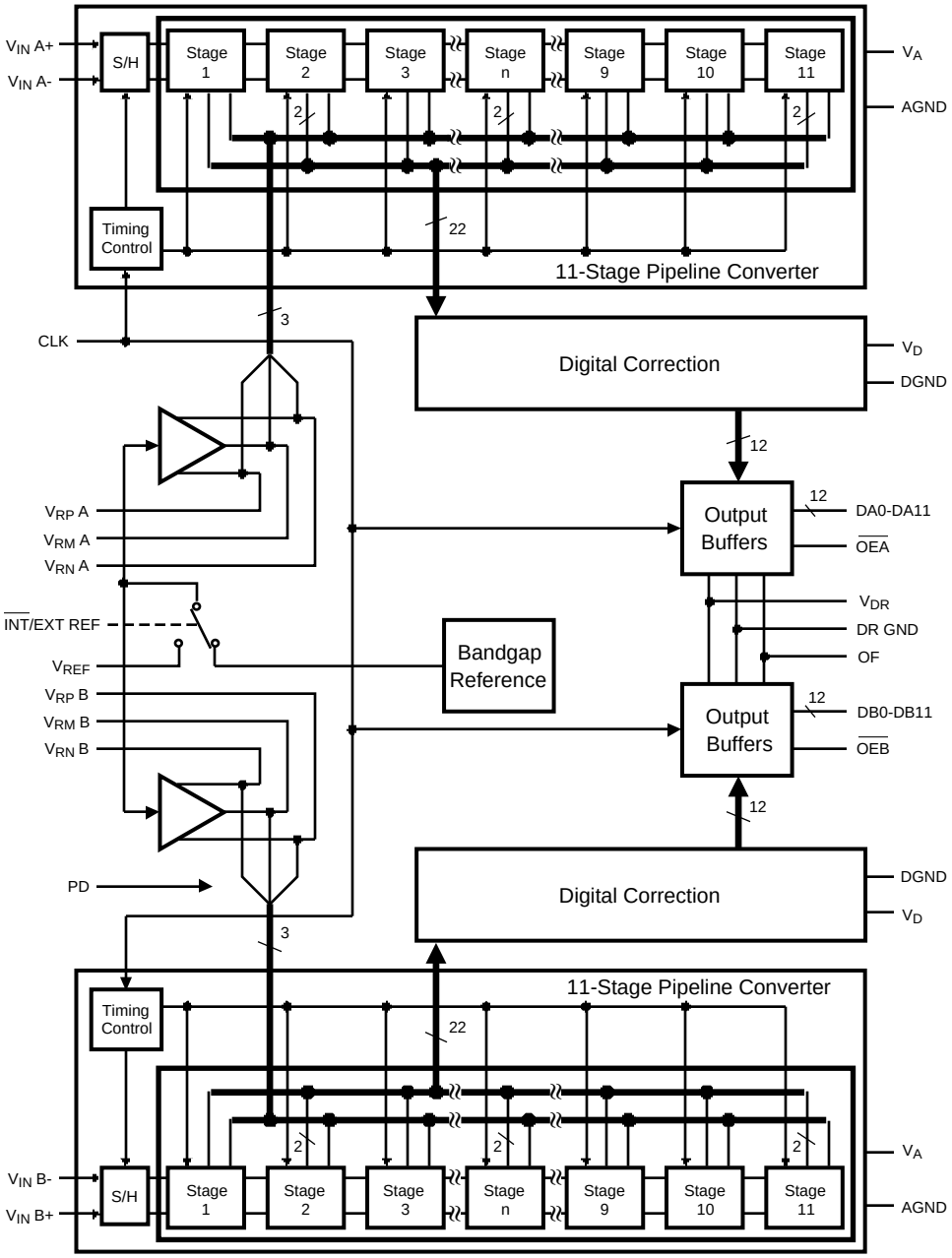
The ADC12DL066 is a dual, low power monolithic CMOS analog-to-digital converter capable of converting analog input signals into 12-bit digital words at 66 Megasamples per second (Msps), minimum. This converter uses a differential, pipeline architecture with digital error correction and an on-chip sample-and-hold circuit to minimize die size and power consumption while providing excellent dynamic performance and a 450 MHz Full Power Bandwidth. Operating on a single 3.3V power supply, the ADC12DL066 achieves 10.7 effective bits and consumes just 686 mW at 66 Msps, including the reference current. The Power Down feature reduces power consumption to 75 mW.

The differential inputs provide a full scale differential input swing equal to 2 times V_{REF} with the possibility of a single-ended input. Full use of the differential input is recommended for optimum performance. The digital outputs from the two ADCs are available on separate 12-bit buses with an output data format choice of offset binary or two's complement.

To ease interfacing to lower voltage systems, the digital output driver power pins of the ADC12DL066 can be connected to a separate supply voltage in the range of 2.4V to the digital supply voltage.

This device is available in the 64-lead TQFP package and will operate over the industrial temperature range of −40°C to +85°C. An evaluation board is available to ease the evaluation process.

Block Diagram



Connection Diagram

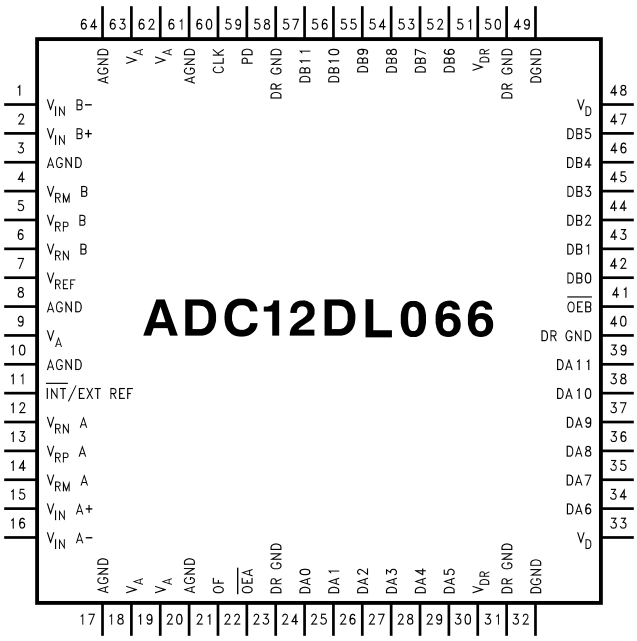
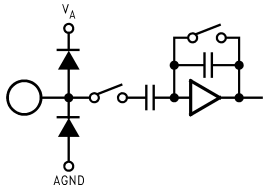
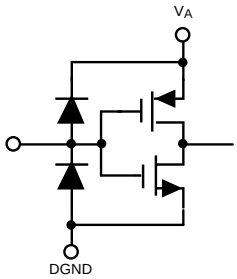
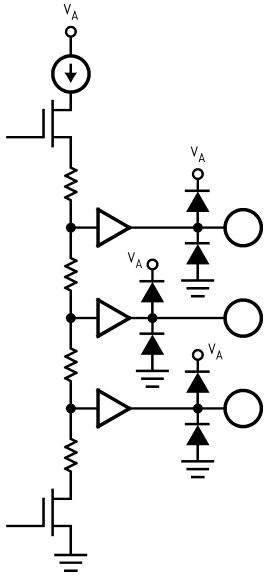
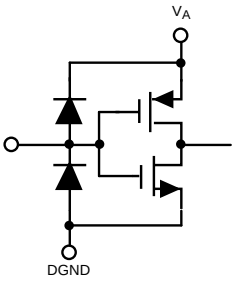
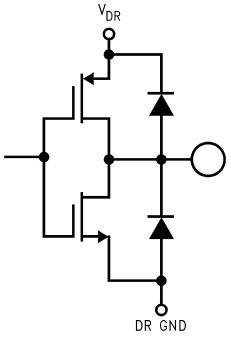


Figure 1. 64-Lead TQFP Package
Package Number PAG

PIN DESCRIPTIONS AND EQUIVALENT CIRCUITS

Pin No.	Symbol	Equivalent Circuit	Description
ANALOG I/O			
15 2	$V_{IN}A+$ $V_{IN}B+$		Differential analog input pins. With a 1.0V reference voltage the differential full-scale input signal level is 2.0 V_{P-P} with each input pin voltage centered on a common mode voltage, V_{CM}. The negative input pins may be connected to V_{CM} for single-ended operation, but a differential input signal is required for best performance.
16 1	$V_{IN}A-$ $V_{IN}B-$		
7	V_{REF}		Reference input. This pin should be bypassed to AGND with a 0.1 µF capacitor when an external reference is used. V_{REF} is 1.0V nominal and should be between 0.8V to 1.5V.
11	$\overline{INT}$/EXT REF		Reference source select pin. With a logic low at this pin the internal 1.0V reference is selected and the V_{REF} pin need not be driven. With a logic high on this pin an external reference voltage should be applied to V_{REF} input pin 7.
13 5	$V_{RP}A$ $V_{RP}B$		These pins are high impedance reference bypass pins only; they are not reference output pins. Bypass per Reference Pins. DO NOT LOAD these pins.
14 4	$V_{RM}A$ $V_{RM}B$		
12 6	$V_{RN}A$ $V_{RN}B$		

PIN DESCRIPTIONS AND EQUIVALENT CIRCUITS (continued)

Pin No.	Symbol	Equivalent Circuit	Description
DIGITAL I/O			
60	CLK		Digital clock input. The range of frequencies for this input is as specified in the electrical tables with guaranteed performance at 66 MHz. The input is sampled on the rising edge of this input.
22 41	$\overline{OEA}$ $\overline{OEB}$		$\overline{OEA}$ and $\overline{OEB}$ are the output enable pins that, when low, holds their respective data output pins in the active state. When either of these pins is high, the corresponding outputs are in a high impedance state.
59	PD		PD is the Power Down input pin. When high, this input puts the converter into the power down mode. When this pin is low, the converter is in the active mode.
21	OF		Output Format pin. A logic low on this pin causes output data to be in offset binary format. A logic high on this pin causes the output data to be in 2's complement format.
24–29 34–39	DA0–DA11		Digital data output pins that make up the 12-bit conversion results of their respective converters. DA0 and DB0 are the LSBs, while DA11 and DB11 are the MSBs of the output words. Output levels are TTL/CMOS compatible.
42–47 52–57	DB0–DB11		
ANALOG POWER			
9, 18, 19, 62, 63	V_A		Positive analog supply pins. These pins should be connected to a quiet +3.3V source and bypassed to AGND with 0.1 µF capacitors located within 1 cm of these power pins, and with a 10 µF capacitor.
3, 8, 10, 17, 20, 61, 64	AGND		The ground return for the analog supply.
DIGITAL POWER			
33, 48	V_D		Positive digital supply pin. This pin should be connected to the same quiet +3.3V source as is V_A and be bypassed to DGND with a 0.1 µF capacitor located within 1 cm of the power pin and with a 10 µF capacitor.
32, 49	DGND		The ground return for the digital supply.
30, 51	V_{DR}		Positive digital supply pin for the ADC12DL066's output drivers. This pin should be connected to a voltage source of +2.4V to V_D and be bypassed to DR GND with a 0.1 µF capacitor. If the supply for this pin is different from the supply used for V_A and V_D, it should also be bypassed with a 10 µF capacitor. V_{DR} should never exceed the voltage on V_D. All bypass capacitors should be located within 1 cm of the supply pin.
23, 31, 40, 50, 58	DR GND		The ground return for the digital supply for the ADC12DL066's output drivers. These pins should be connected to the system digital ground, but not be connected in close proximity to the ADC12DL066's DGND or AGND pins. See LAYOUT AND GROUNDING (Layout and Grounding) for more details.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2][3]

V_A, V_D, V_{DR}		4.2V
$\|V_A – V_D\|$		≤ 100 mV
Voltage on Any Input or Output Pin		−0.3V to (V_A or V_D +0.3V)
Input Current at Any Pin[4]		±25 mA
Package Input Current[4]		±50 mA
Package Dissipation at T_A = 25°C		See[5]
ESD Susceptibility[6]	Human Body Model	2500V
	Machine Model	250V
Soldering Temperature, Infrared, 10 sec.[7]		235°C
Storage Temperature		−65°C to +150°C

(1) All voltages are measured with respect to GND = AGND = DGND = 0V, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND, or V_{IN} > V_A), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.
(5) The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature, (T_A), and can be calculated using the formula $P_D MAX = (T_J max - T_A) / \theta_{JA}$. The values for maximum power dissipation will only be reached when the device is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.
(6) Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through 0Ω.
(7) The 235°C reflow temperature refers to infrared reflow. For Vapor Phase Reflow (VPR), the following Conditions apply: Maintain the temperature at the top of the package body above 183°C for a minimum 60 seconds. The temperature measured on the package body must not exceed 220°C. Only one excursion above 183°C is allowed per reflow cycle.

Operating Ratings[1][2]

Operating Temperature	−40°C ≤ T_A ≤ +85°C
Supply Voltage (V_A, V_D)	+3.0V to +3.6V
Output Driver Supply (V_{DR})	+2.4V to V_D
V_{REF} Input	0.8V to 1.5V
CLK, PD, $\overline{OE}$	−0.05V to (V_D + 0.05V)
Analog Input Pins	0V to (V_A − 0.5V)
Common Mode Input Voltage (V_{CM})	0.5V to 1.5V
|AGND–DGND|	≤100mV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND = AGND = DGND = 0V, unless otherwise specified.

Package Thermal Resistance

Package	θ_{J-A}
64-Lead TQFP	50°C / W

Converter Electrical Characteristics

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, V_A = V_D = +3.3V, V_{DR} = +2.5V, PD = 0V, $\overline{INT}$/EXT REF pin = +3.3V, V_{REF} = +1.0V, f_{CLK} = 66 MHz, f_{IN} = 10 MHz, t_r = t_f = 2 ns, C_L = 15 pF/pin.
Boldface limits apply for T_J = T_{MIN} to T_{MAX}: all other limits T_J = 25°C (1)(2)(3)

Symbol	Parameter	Conditions		Typical (4)	Limits (4)	Units (Limits)
STATIC CONVERTER CHARACTERISTICS						
	Resolution with No Missing Codes				**12**	Bits (min)
INL	Integral Non Linearity (5)			±1.2	**±3.0**	LSB (max)
DNL	Differential Non Linearity			±0.5	**±1.0**	LSB (max)
PGE	Positive Gain Error			±0.2	**±3.6**	%FS (max)
NGE	Negative gain Error			±0.2	**±3.6**	%FS (max)
TC GE	Gain Error Tempco	−40°C ≤ T_A ≤ +85°C		−60		ppm/°C
V_{OFF}	Offset Error (V_{IN}+ = V_{IN}−)			0.18	**+1.3** **-0.9**	%FS (max) %FS (min)
TC V_{OFF}	Offset Error Tempco	−40°C ≤ T_A ≤ +85°C		−2.4		ppm/°C
	Under Range Output Code			0	**0**	
	Over Range Output Code			4095	**4095**	
REFERENCE AND ANALOG INPUT CHARACTERISTICS						
V_{CM}	Common Mode Input Voltage			1.0	**0.5** **1.5**	V (min) V (max)
C_{IN}	V_{IN} Input Capacitance (each pin to GND)	V_{IN} = 2.5 Vdc + 0.7 V_{rms}	(CLK LOW)	8		pF
			(CLK HIGH)	7		pF
V_{REF}	External Reference Voltage (6)			1.00	**0.8** **1.5**	V (min) V (max)
R_{REF}	Reference Input Resistance			100		MΩ (min)

(1) The inputs are protected as shown below. Input voltage magnitudes above V_A or below GND will not damage this device, provided current is limited see Note 4 in the Absolute Maximum Ratings table. However, errors in the A/D conversion can occur if the input goes above V_A or below GND by more than 100 mV. As an example, if V_A is +3.3V, the full-scale input voltage must be ≤+3.4V to ensure accurate conversions (see Figure 2).
(2) To guarantee accuracy, it is required that $|V_A – V_D|$ ≤ 100 mV and separate bypass capacitors are used at each power supply pin.
(3) With the test condition for V_{REF} = +1.0V ($2V_{P-P}$ differential input), the 12-bit LSB is 488 µV.
(4) Typical figures are at T_J = 25°C, and represent most likely parametric norms. Test limits are guaranteed to AOQL (Average Outgoing Quality Level).
(5) Integral Non Linearity is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive and negative full-scale.
(6) Optimum performance will be obtained by keeping the reference input in the 0.8V to 1.5V range. The LM4051CIM3-ADJ (SOT-23 package) is recommended for external reference applications.

Converter Electrical Characteristics (continued)

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, V_A = V_D = +3.3V, V_{DR} = +2.5V, PD = 0V, $\overline{INT}$/EXT REF pin = +3.3V, V_{REF} = +1.0V, f_{CLK} = 66 MHz, f_{IN} = 10 MHz, t_r = t_f = 2 ns, C_L = 15 pF/pin.
Boldface limits apply for T_J = T_{MIN} to T_{MAX}: all other limits T_J = 25°C(1)(2)(3)

Symbol	Parameter	Conditions	Typical (4)	Limits (4)	Units (Limits)
DYNAMIC CONVERTER CHARACTERISTICS					
FPBW	Full Power Bandwidth	0 dBFS Input, Output at −3 dB	450		MHz
SNR	Signal-to-Noise Ratio	f_{IN} = 1 MHz, V_{IN} = −0.5 dBFS	66		dB
		f_{IN} = 10 MHz, V_{IN} = −0.5 dBFS	66	**64**	dB (min)
		f_{IN} = 33 MHz, V_{IN} = −0.5 dBFS	64		dB
		f_{IN} = 146 MHz, V_{IN} = −0.5 dBFS	55		dB
SINAD	Signal-to-Noise and Distortion	f_{IN} = 1 MHz, V_{IN} = −0.5 dBFS	66		dB
		f_{IN} = 10 MHz, V_{IN} = −0.5 dBFS	66	**63.3**	dB (min)
		f_{IN} = 33 MHz, V_{IN} = −0.5 dBFS	63		dB
		f_{IN} = 146MHz, V_{IN} = −0.5 dBFS	53		dB
ENOB	Effective Number of Bits	f_{IN} = 1 MHz, V_{IN} = −0.5 dBFS	10.7		Bits
		f_{IN} = 10 MHz, V_{IN} = −0,5 dBFS	10.7	**10.2**	Bits (min)
		f_{IN} = 33 MHz, V_{IN} = −0,5 dBFS	10.3		Bits
		f_{IN} = 146MHz, V_{IN} = −0,5 dBFS	8.7		Bits
THD	Total Harmonic Distortion	f_{IN} = 1 MHz, V_{IN} = −0.5 dBFS	−78		dB
		f_{IN} = 10 MHz, V_{IN} = −0.5 dBFS	−78	**−67.8**	dB (min)
		f_{IN} = 33 MHz, V_{IN} = −0.5 dBFS	−70		dB
		f_{IN} = 146MHz, V_{IN} = −0.5 dBFS	−59		dB
H2	Second Harmonic Distortion	f_{IN} = 1 MHz, V_{IN} = −0.5 dBFS	−90		dB
		f_{IN} = 10 MHz, V_{IN} = −0.5 dBFS	−85	**−70.4**	dB (min)
		f_{IN} = 33 MHz, V_{IN} = −0.5 dBFS	−72		dB
		f_{IN} = 146MHz, V_{IN} = −0.5 dBFS	−67		dB
H3	Third Harmonic Distortion	f_{IN} = 1 MHz, V_{IN} = −0.5 dBFS	−83		dB
		f_{IN} = 10 MHz, V_{IN} = −0.5 dBFS	−85	**−71.0**	dB (min)
		f_{IN} = 33 MHz, V_{IN} = −0.5 dBFS	−76		dB
		f_{IN} = 146MHz, V_{IN} = −0.5 dBFS	−66		dB
SFDR	Spurious Free Dynamic Range	f_{IN} = 1 MHz, V_{IN} = −0.5 dBFS	79		dB
		f_{IN} = 10 MHz, V_{IN} = −0.5 dBFS	81	**68.5**	dB (min)
		f_{IN} = 33 MHz, V_{IN} = −0.5 dBFS	72		dB
		f_{IN} = 146MHz, V_{IN} = −0.5 dBFS	63		dB
IMD	Intermodulation Distortion	f_{IN} = 9.6 MHz and 10.2 MHz, each = −6.0 dBFS	−64		dBFS
INTER-CHANNEL CHARACTERISTICS					
	Channel—Channel Offset Match		±0.03		%FS
	Channel—Channel Gain Match		±0.1		%FS
	Crosstalk	10 MHz Tested, Channel; 20 MHz Other Channel	80		dB
		10 MHz Tested, Channel; 195 MHz Other Channel	63		dB

DC and Logic Electrical Characteristics

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, V_A = V_D = +3.3V, V_{DR} = +2.5V, PD = 0V, $\overline{INT}$/EXT REF pin = +3.3V, V_{REF} = +1.0V, f_{CLK} = 66 MHz, f_{IN} = 10 MHz, t_r = t_f = 2 ns, C_L = 15 pF/pin. **Boldface limits apply for T_J = T_{MIN} to T_{MAX}:** all other limits T_J = 25°C (1)(2)(3)

Symbol	Parameter	Conditions		Typical (4)	Limits (4)	Units (Limits)
CLK, PD, $\overline{OE}$ DIGITAL INPUT CHARACTERISTICS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_D = 3.6V			**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	V_D = 3.0V			**1.0**	V (max)
$I_{IN(1)}$	Logical "1" Input Current	V_{IN} = 3.3V		10		µA
$I_{IN(0)}$	Logical "0" Input Current	V_{IN} = 0V		−10		µA
C_{IN}	Digital Input Capacitance			5		pF
D0–D11 DIGITAL OUTPUT CHARACTERISTICS						
$V_{OUT(1)}$	Logical "1" Output Voltage	I_{OUT} = −0.5 mA	V_{DR} = 2.5V		**2.3**	V (min)
			V_{DR} = 3V		**2.7**	V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	I_{OUT} = 1.6 mA, V_{DR} = 3V			**0.4**	V (max)
I_{OZ}	TRI-STATE Output Current	V_{OUT} = 2.5V or 3.3V		100		nA
		V_{OUT} = 0V		−100		nA
$+I_{SC}$	Output Short Circuit Source Current	V_{OUT} = 0V		−20		mA
$-I_{SC}$	Output Short Circuit Sink Current	V_{OUT} = V_{DR}		20		mA
C_{OUT}	Digital Output Capacitance			5		pF
POWER SUPPLY CHARACTERISTICS						
I_A	Analog Supply Current	PD Pin = DGND, V_{REF} = 1.0V PD Pin = V_D		177 14	**237**	mA (max) mA
I_D	Digital Supply Current	PD Pin = DGND PD Pin = V_D , f_{CLK} = 0		31 8.7	**34**	mA (max) mA
I_{DR}	Digital Output Supply Current	PD Pin = DGND, C_L = 0 pF (5) PD Pin = V_D, f_{CLK} = 0		<2 0		mA mA
	Total Power Consumption	PD Pin = DGND, C_L = 0 pF (6) PD Pin = V_D, f_{CLK} = 0		686 75	**895**	mW (max) mW
PSRR1	Power Supply Rejection Ratio	Rejection of Full-Scale Error with V_A = 3.0V vs. 3.6V		56		dB
PSRR2	Power Supply Rejection Ratio	Rejection of Power Supply Noise with 10 MHz, 500 mV riding on V_A		44		dB

(1) The inputs are protected as shown below. Input voltage magnitudes above V_A or below GND will not damage this device, provided current is limited see Note 4 in the Absolute Maximum Ratings table. However, errors in the A/D conversion can occur if the input goes above V_A or below GND by more than 100 mV. As an example, if V_A is +3.3V, the full-scale input voltage must be ≤+3.4V to ensure accurate conversions (see Figure 2).
(2) To guarantee accuracy, it is required that $|V_A–V_D|$ ≤ 100 mV and separate bypass capacitors are used at each power supply pin.
(3) With the test condition for V_{REF} = +1.0V ($2V_{P-P}$ differential input), the 12-bit LSB is 488 µV.
(4) Typical figures are at T_J = 25°C, and represent most likely parametric norms. Test limits are guaranteed to AOQL (Average Outgoing Quality Level).
(5) I_{DR} is the current consumed by the switching of the output drivers and is primarily determined by load capacitance on the output pins, the supply voltage, V_{DR}, and the rate at which the outputs are switching (which is signal dependent). I_{DR}=V_{DR}(C_0 x f_0 + C_1 x f_1 +....C_{11} x f_{11}) where V_{DR} is the output driver power supply voltage, C_n is total capacitance on the output pin, and f_n is the average frequency at which that pin is toggling.
(6) Excludes I_{DR}. See (6)

AC Electrical Characteristics

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, V_A = V_D = +3.3V, V_{DR} = +2.5V, PD = 0V, $\overline{INT}$/EXT REF pin = +3.3V, V_{REF} = +1.0V, f_{CLK} = 66 MHz, f_{IN} = 10 MHz, t_r = t_f = 2 ns, C_L = 15 pF/pin. **Boldface limits apply for T_J = T_{MIN} to T_{MAX}:** all other limits T_J = 25ºC (1)(2)(3)(4)

Symbol	Parameter	Conditions		Typical (5)	Limits (5)	Units (Limits)
f_{CLK}[1]	Maximum Clock Frequency				**66**	MHz (min)
f_{CLK}[2]	Minimum Clock Frequency			15		MHz
t_{CH}	Clock High Time				**6.6**	ns (min)
t_{CL}	Clock Low Time				**6.6**	ns (min)
t_{CONV}	Conversion Latency				**6**	Clock Cycles
t_{OD}	Data Output Delay after Rising CLK Edge	V_{DR} = 2.5V	rising	6.6	**9.0**	ns (max)
			falling	6.0	**8.5**	ns (max)
		V_{DR} = 3.3V	rising	6.4	**9.0**	ns (max)
			falling	6.5	**9.0**	ns (max)
t_{AD}	Aperture Delay			2		ns
t_{AJ}	Aperture Jitter			1.2		ps rms
t_{HOLD}	Clock Edge to Data Transition			8		ns
t_{DIS}	Data outputs into Hi-Z Mode			10		ns
t_{EN}	Data Outputs Active after Hi-Z Mode			10		ns
t_{PD}	Power Down Mode Exit Cycle	0.1 µF on pins 4, 14; series 1.5 Ω & 1 µF between pins 5, 6 and between pins 12, 13		500		µs

(1) The inputs are protected as shown below. Input voltage magnitudes above V_A or below GND will not damage this device, provided current is limited see Note 4 in the Absolute Maximum Ratings table. However, errors in the A/D conversion can occur if the input goes above V_A or below GND by more than 100 mV. As an example, if V_A is +3.3V, the full-scale input voltage must be ≤+3.4V to ensure accurate conversions (see Figure 2).
(2) To guarantee accuracy, it is required that $|V_A–V_D|$ ≤ 100 mV and separate bypass capacitors are used at each power supply pin.
(3) With the test condition for V_{REF} = +1.0V ($2V_{P-P}$ differential input), the 12-bit LSB is 488 µV.
(4) Timing specifications are tested at TTL logic levels, V_{IL} = 0.4V for a falling edge and V_{IH} = 2.4V for a rising edge.
(5) Typical figures are at T_J = 25°C, and represent most likely parametric norms. Test limits are guaranteed to AOQL (Average Outgoing Quality Level).

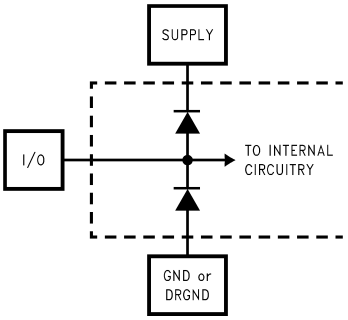


Figure 2.

Specification Definitions

APERTURE DELAY is the time after the rising edge of the clock to when the input signal is acquired or held for conversion.

APERTURE JITTER (APERTURE UNCERTAINTY) is the variation in aperture delay from sample to sample. Aperture jitter manifests itself as noise in the output.

CLOCK DUTY CYCLE is the ratio of the time during one cycle that a repetitive digital waveform is high to the total time of one period. The specification here refers to the ADC clock input signal.

COMMON MODE VOLTAGE (V_{CM}) is the common d.c. voltage applied to both input terminals of the ADC.

CONVERSION LATENCY is the number of clock cycles between initiation of conversion and when that data is presented to the output driver stage. Data for any given sample is available at the output pins the Pipeline Delay plus the Output Delay after the sample is taken. New data is available at every clock cycle, but the data lags the conversion by the pipeline delay.

CROSSTALK is coupling of energy from one channel into the other channel.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as (SINAD - 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR (G.E.) is the deviation from the ideal slope of the transfer function. It can be calculated as:

$$\text{G.E.} = \text{Pos. Full-Scale Error} - \text{Neg. Full-Scale Error} \quad (1)$$

Gain Error can also be separated into Positive Gain Error (PGE) and Negative Gain Error (NGE), which are.

$$\text{PGE} = \text{Pos. Full-Scale Error} - \text{Offset Error} \quad (2)$$

$$\text{NGE} = \text{Offset Error} - \text{Neg. Full-Scale Error} \quad (3)$$

GAIN ERROR MATCHING is the difference in gain errors between the two converters divided by the average gain of the converters.

INTEGRAL NON LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the intermodulation products to the total power in the original frequencies. IMD is usually expressed in dBFS.

LSB (LEAST SIGNIFICANT BIT) is the bit that has the smallest value or weight of all bits. This value is $V_{REF}/2^n$, where “n” is the ADC resolution in bits, which is 12 in the case of the ADC12DL066.

MISSING CODES are those output codes that will never appear at the ADC outputs. The ADC12DL066 is guaranteed not to have any missing codes.

MSB (MOST SIGNIFICANT BIT) is the bit that has the largest value or weight. Its value is one half of full scale.

NEGATIVE FULL SCALE ERROR is the difference between the actual first code transition and its ideal value of ½ LSB above negative full scale.

OFFSET ERROR is the difference between the two input voltages [(V_{IN}+) – (V_{IN}–)] required to cause a transition from code 2047 to 2048.

OUTPUT DELAY is the time delay after the rising edge of the clock before the data update is presented at the output pins.

OVER RANGE RECOVERY TIME is the time required after V_{IN} goes from a specified voltage out of the normal input range to a specified voltage within the normal input range and the converter makes a conversion with its rated accuracy.

PIPELINE DELAY (LATENCY) See CONVERSION LATENCY.

POSITIVE FULL SCALE ERROR is the difference between the actual last code transition and its ideal value of 1½ LSB below positive full scale.

POWER SUPPLY REJECTION RATIO (PSRR) is a measure of how well the ADC rejects a change in the power supply voltage. For the ADC12DL066, PSRR1 is the ratio of the change in Full-Scale Error that results from a change in the d.c. power supply voltage, expressed in dB. PSRR2 is a measure of how well an a.c. signal riding upon the power supply is rejected at the output.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or d.c.

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the irms values of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input and may or may not be a harmonic.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dB, of the rms total of the first nine harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

$$THD = 20 \times \log \sqrt{\frac{f_2^2 + \ldots + f_{10}^2}{f_1^2}} \quad (4)$$

where

- F_1 is the RMS power of the fundamental (output) frequency and f_2 through f_{10} are the RMS power of the first 9 harmonic frequencies in the output spectrum.

– Second Harmonic Distortion (2ND HARM) is the difference expressed in dB, between the RMS power in the input frequency at the output and the power in its 2nd harmonic level at the output.

– Third Harmonic Distortion (3RD HARM) is the difference, expressed in dB, between the RMS power in the input frequency at the output and the power in its 3rd harmonic level at the output.

Timing Diagram

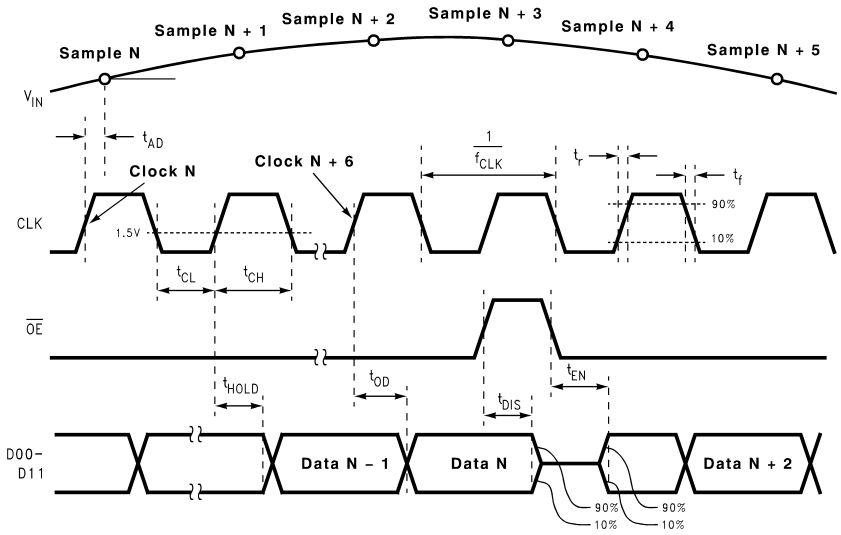


Figure 3. Output Timing

Transfer Characteristic

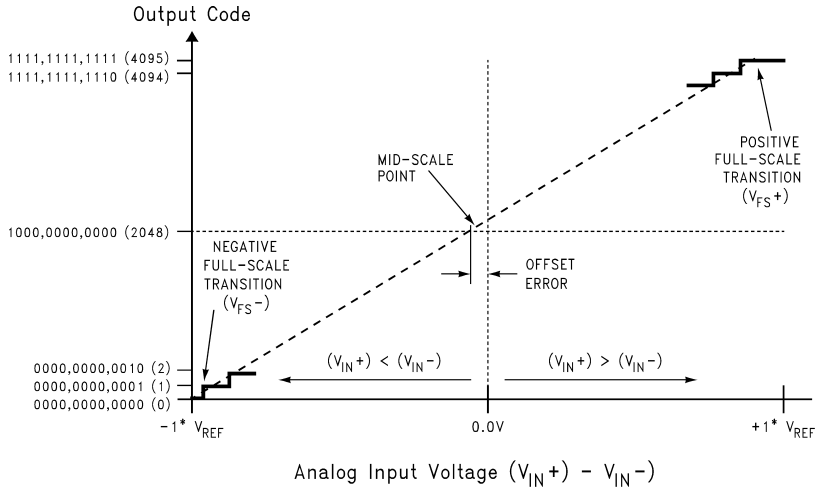


Figure 4. Transfer Characteristic

Typical Performance Characteristics

$V_A = V_D = +3.3V$, $V_{DR} = +2.5V$, $f_{CLK} = 66$ MHz, $f_{IN} = 10$ MHz unless otherwise stated

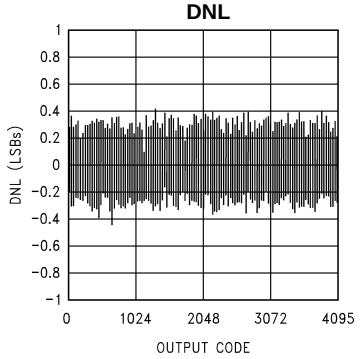


Figure 5.

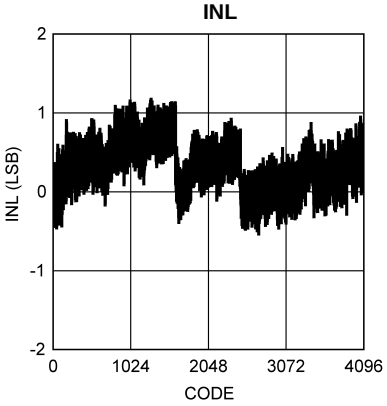


Figure 6.

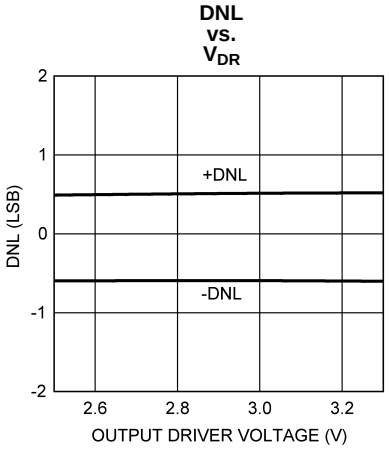


Figure 7.

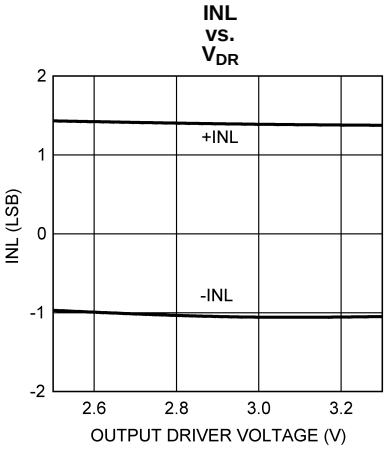


Figure 8.

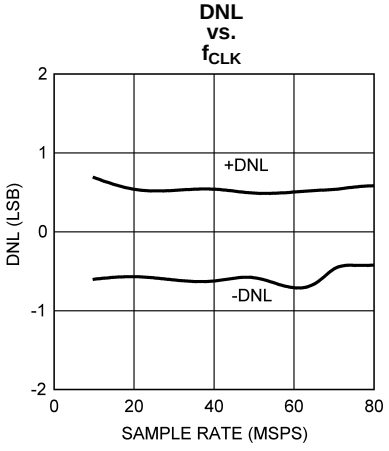


Figure 9.

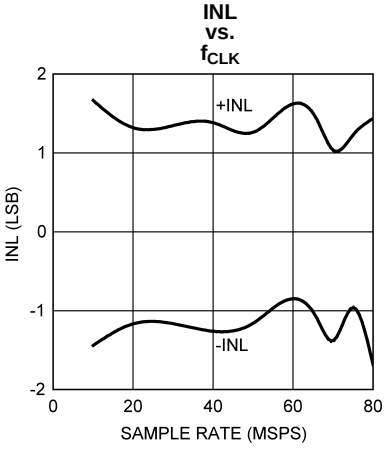


Figure 10.

Typical Performance Characteristics (continued)

V_A = V_D = +3.3V, V_{DR} = +2.5V, f_{CLK} = 66 MHz, f_{IN} = 10 MHz unless otherwise stated

DNL vs. Clock Duty Cycle

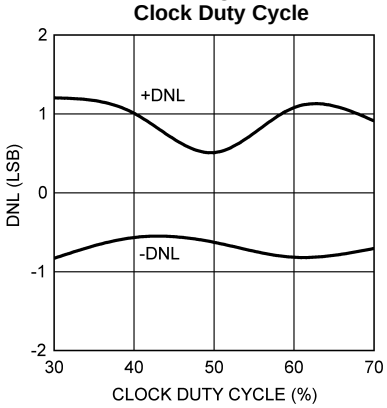


Figure 11.

INL vs. Clock Duty Cycle

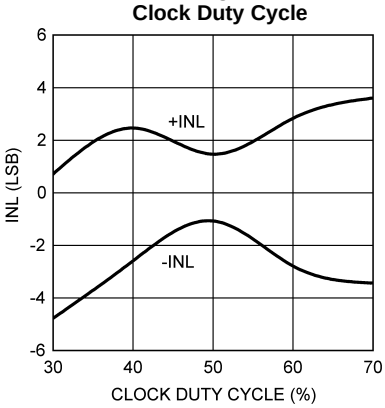


Figure 12.

DNL vs. Temperature

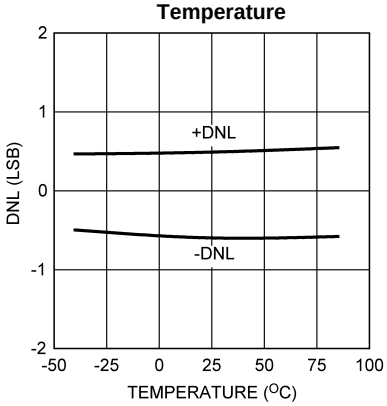


Figure 13.

INL vs. Temperature

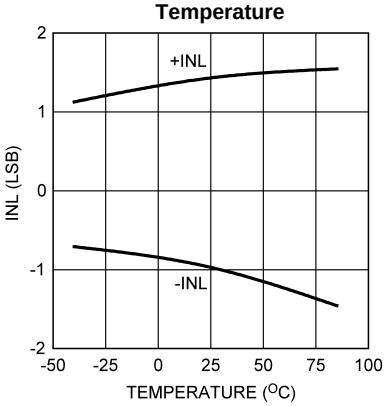


Figure 14.

SNR, SINAD, SFDR vs. V_{DR}

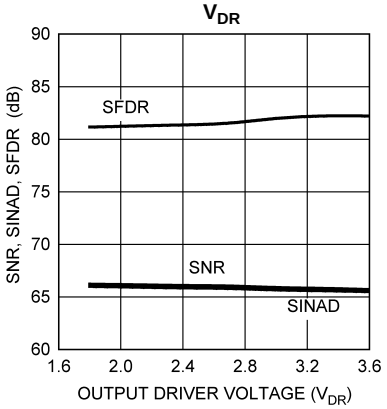


Figure 15.

SNR, SINAD, SFDR vs. f_{CLK}

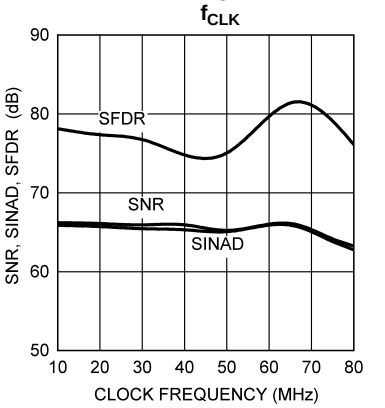


Figure 16.

Typical Performance Characteristics (continued)

$V_A = V_D = +3.3V$, $V_{DR} = +2.5V$, $f_{CLK} = 66$ MHz, $f_{IN} = 10$ MHz unless otherwise stated

SNR, SINAD, SFDR vs. CLOCK DUTY CYCLE

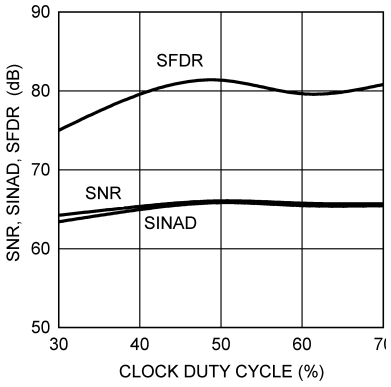


Figure 17.

SNR, SINAD, SFDR vs. V_{CM}

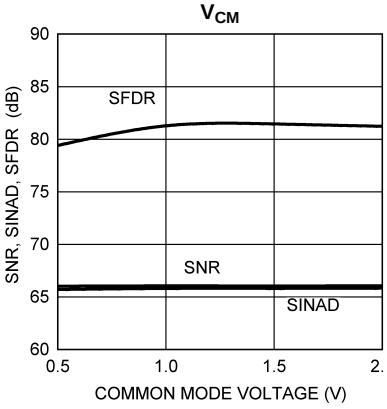


Figure 18.

SNR, SINAD, SFDR vs. V_{REF}

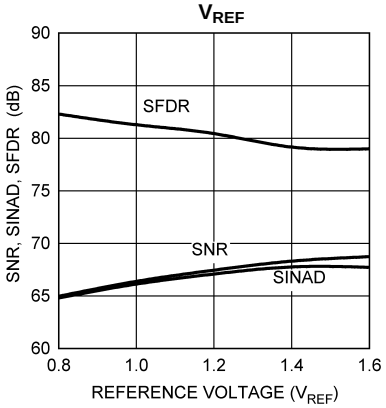


Figure 19.

SNR, SINAD, SFDR vs. Temperature

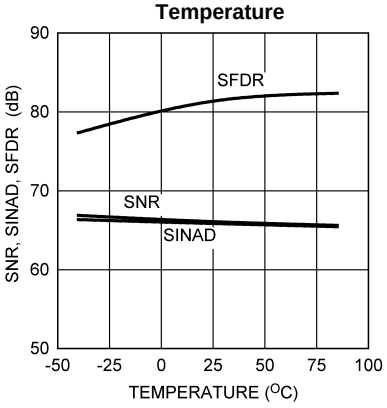


Figure 20.

Distortion vs. V_{DR}

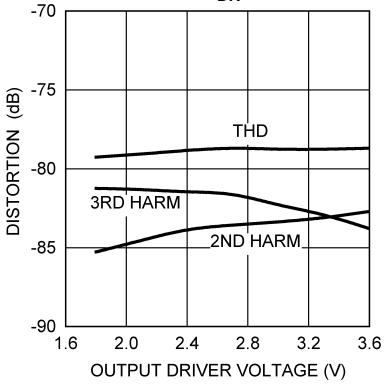


Figure 21.

Distortion vs. F_{CLK}

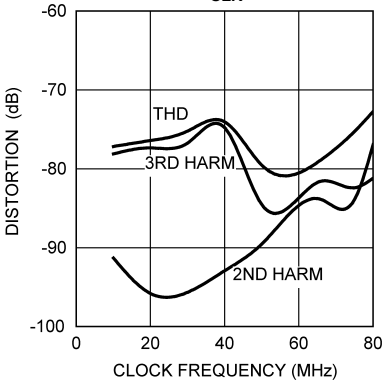


Figure 22.

Typical Performance Characteristics (continued)

V_A = V_D = +3.3V, V_{DR} = +2.5V, f_{CLK} = 66 MHz, f_{IN} = 10 MHz unless otherwise stated

Distortion vs. Clock Duty Cycle

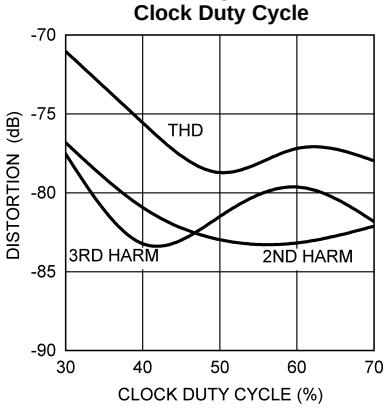


Figure 23.

Distortion vs. V_{CM}

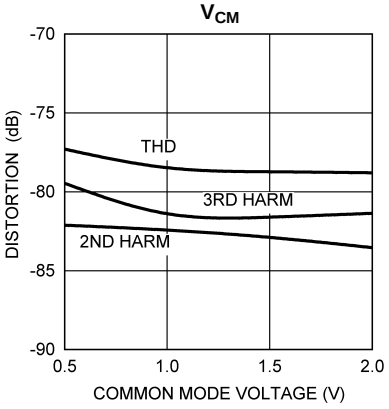


Figure 24.

Distortion vs. V_{REF}

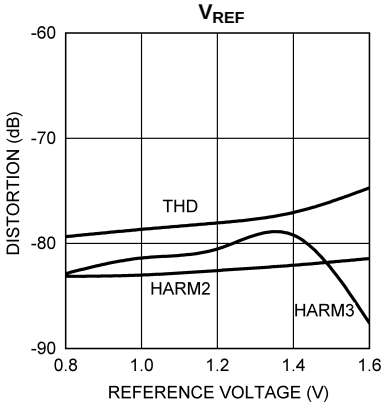


Figure 25.

Distortion vs. Temperature

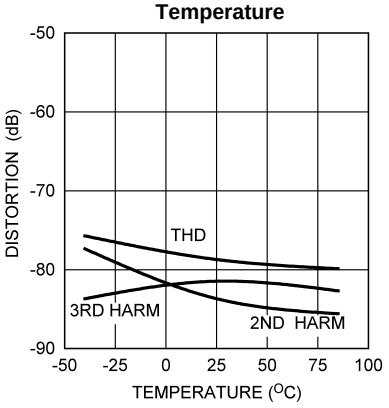


Figure 26.

t_{OD} vs. V_{DR}

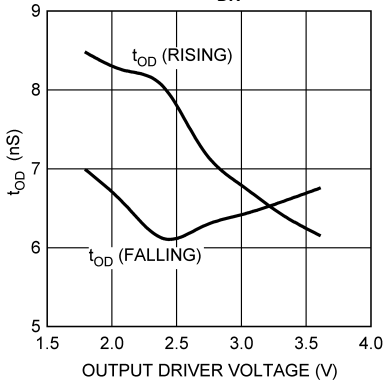


Figure 27.

SPECTRAL PLOT, F_{IN} = 10 MHz

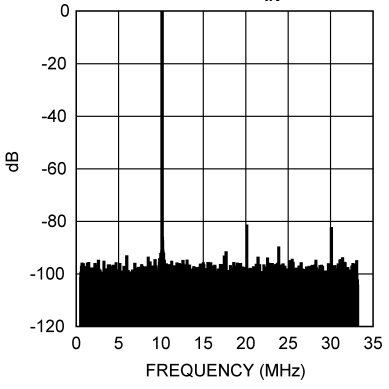


Figure 28.

Typical Performance Characteristics (continued)

$V_A = V_D = +3.3V$, $V_{DR} = +2.5V$, $f_{CLK} = 66$ MHz, $f_{IN} = 10$ MHz unless otherwise stated

SPECTRAL PLOT, F_{IN} = 33 MHz

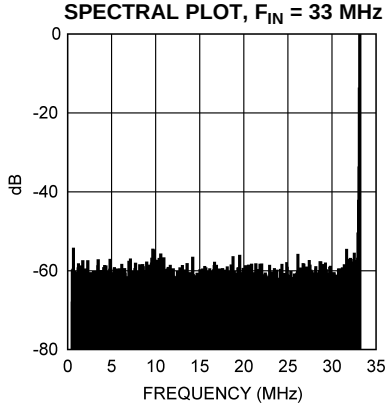


Figure 29.

IMD PERFORMANCE, $F_{IN}1$ = 9.6 MHz, $F_{IN}2$ = 10.2 MHz

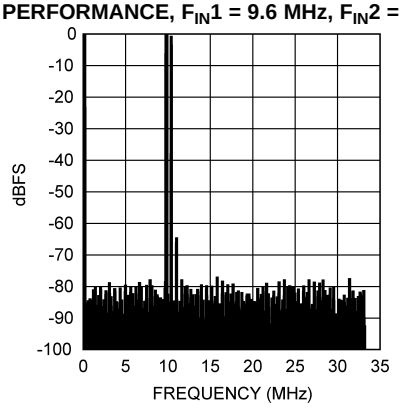


Figure 30.

FUNCTIONAL DESCRIPTION

Operating on a single +3.3V supply, the ADC12DL066 uses a pipeline architecture and has error correction circuitry to help ensure maximum performance. The differential analog input signal is digitized to 12 bits. The user has the choice of using an internal 1.0 Volt stable reference or using an external reference. Any external reference is buffered on-chip to ease the task of driving that pin.

The output word rate is the same as the clock frequency, which can be between 15 Msps (typical) and 66 Msps with fully specified performance at 66 Msps. The analog input voltage for both channels is acquired at the rising edge of the clock and the digital data for a given sample is delayed by the pipeline for 6 clock cycles. A choice of Offset Binary or Two's Complement output format is selected with the OF pin.

A logic high on the power down (PD) pin reduces the converter power consumption to 75 mW.

APPLICATION INFORMATION

OPERATING CONDITIONS

We recommend that the following conditions be observed for operation of the ADC12DL066:

$3.0V \le V_A \le 3.6V$

$V_D = V_A$

$2.4V \le V_{DR} \le V_D$

$15\ MHz \le f_{CLK} \le 66\ MHz$

$0.8V \le V_{REF} \le 1.5V$

$V_{REF}/2 \le V_{CM} \le 1.2V$

Analog Inputs

The ADC12DL066 has two analog signal input pairs, V_{IN} A+ and V_{IN} A- for one converter and V_{IN} B+ and V_{IN} B- for the other converter. Each pair of pins forms a differential input pair. There is one reference input pin, V_{REF}, for use of an optional external reference.

The analog input circuitry contains an input boost circuit that provides improved linearity over a wide range of analog input voltages. To prevent an on-chip over voltage condition that could impair device reliability, the input signal should never exceed the voltage described as

$$\text{Peak } V_{IN} \le V_A - 1.0V. \quad (5)$$

Reference Pins

The ADC12DL066 is designed to operate with a 1.0V reference, but performs well with reference voltages in the range of 0.8V to 1.5V. Lower reference voltages will decrease the signal-to-noise ratio (SNR) of the ADC12DL066. Increasing the reference voltage (and the input signal swing) beyond 1.5V may degrade THD and SFDR for a full-scale input, especially at higher input frequencies.

It is important that all grounds associated with the reference voltage and the analog input signal make connection to the ground plane at a single, quiet point to minimize the effects of noise currents in the ground path.

The ADC12DL066 will perform well with reference voltages up to 1.5V for full-scale input frequencies up to 10 MHz. However, more headroom is needed as the input frequency increases, so the maximum reference voltage (and input swing) will decrease for higher full-scale input frequencies.

The six Reference Bypass Pins (V_{RP}A, V_{RM}A, V_{RN}A, V_{RP}B, V_{RM}B and V_{RN}B) are made available for bypass purposes. The V_{RM}A and V_{RM}B pins should each be bypassed to ground with a 0.1 µF capacitor. A series 1.5Ω resistor (5%) and 1.0 µF capacitor (±20%) should be placed between the V_{RP}A and V_{RN}A pins and between the V_{RP}B and V_{RN}B pins, as shown in Figure 33. This configuration is necessary to avoid reference oscillation, which could result in reduced SFDR and/or SNR.

Smaller capacitor values than those specified will allow faster recovery from the power down mode, but may result in degraded noise performance. DO NOT LOAD these pins. Loading any of these pins may result in performance degradation. The ADC12DL066 does not have a reference output pin.

The nominal voltages for the reference bypass pins are as follows:

$V_{RM}A = V_{RM}B = V_A / 2$

$V_{RP}A = V_{RP}B = V_{RM} + V_{REF} / 2$

$V_{RN}A = V_{RN}B = V_{RM} - V_{REF} / 2$

The V_{RM} pins may be used as common mode voltage (V_{CM}) sources for the analog input pins as long as no d.c. current is drawn from them. However, because the voltages at the V_{RM} pins are half that of the V_A supply pin, using these pins for common mode voltage sources will result in reduced input headroom (the difference between the V_A supply voltage and the peak signal voltage at either analog input) and the possibility of reduced THD and SFDR performance. For this reason, it is recommended that V_A always exceed V_{REF} by at least 2 Volts when using the V_{RM} pins as V_{CM} sources. For high input frequencies it may be necessary to increase this headroom to maintain THD and SFDR performance.

User choice of an on-chip or external reference voltage is provided. The internal 1.0 Volt reference is in use when the the $\overline{\text{INT}}$/EXT REF pin is at a logic low, regardless of any voltage applied to the V_{REF} pin. When the $\overline{\text{INT}}$/EXT REF pin is at a logic high, the voltage at the V_{REF} pin is used for the voltage reference. Optimum ADC dynamic performance is obtained when the reference voltage is in the range of 0.8V to 1.5V. When an external reference is used, the V_{REF} pin should be bypassed to ground with a 0.1 µF capacitor close to the reference input pin. There is no need to bypass the V_{REF} pin when the internal reference is used.

There is no direct access to the internal reference voltage. However the nominal value of the reference voltage, whether the internal or an external reference is used, is approximately equal to $V_{RP} - V_{RN}$.

Signal Inputs

The signal inputs are V_{IN} A+ and V_{IN}A− for one ADC and V_{IN}B+ and V_{IN}B− for the other ADC. The input signal, V_{IN}, is defined as

$$V_{IN}\ A = (V_{IN}A+) - (V_{IN}A-) \quad (6)$$

for the "A" converter and

$$V_{IN}\ B = (V_{IN}B+) - (V_{IN}B-) \quad (7)$$

for the "B" converter. Figure 31 shows the expected input signal range. Note that the common mode input voltage, V_{CM}, should be in the range of 0.5V to 1.5V with a nominal value of 1.0V.

The ADC12DL066 performs best with a differential input signal with each input centered around a common mode voltage, V_{CM}. The peak-to-peak voltage swing at each analog input pin should not exceed the value of the reference voltage or the output data will be clipped.

The two input signals should be exactly 180° out of phase from each other and of the same amplitude. For single frequency inputs, angular errors result in a reduction of the effective full scale input. For complex waveforms, however, angular errors will result in distortion.

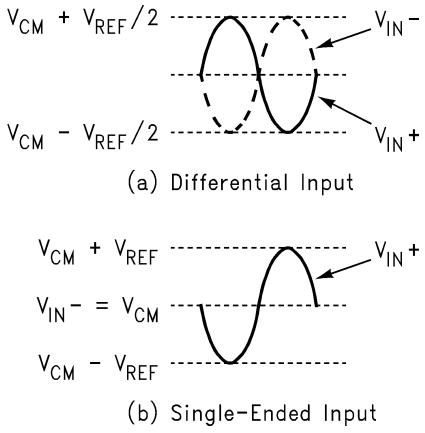


Figure 31. Expected Input Signal Range

For single frequency sine waves with angular errors of less than 45° (π/4) between the two inputs, the full scale error in LSB can be described as approximately

$$E_{FS} = 2^{(n-1)} * (1 - \cos (dev)) = 2048 * (1 - \cos (dev))$$ (8)

where

- dev is the angular difference in degrees between the two signals having a 180° relative phase relationship to each other (see Figure 32). Drive the analog inputs with a source impedance less than 100Ω.

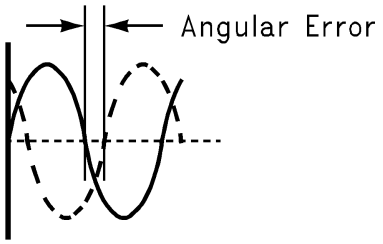


Figure 32. Angular Errors Between the Two Input Signals Will Reduce the Output Level or Cause Distortion

Single-Ended Operation

Single-ended performance is inferior to performance obtained when differential input signals are used. For this reason, single-ended operation is not recommended. However, if single ended-operation is required and the resulting performance degradation is acceptable, one of the analog inputs should be connected to the d.c. mid point voltage of the driven input. The peak-to-peak differential input signal at the driven input pin should be twice the reference voltage to maximize SNR and SINAD performance (Figure 31*b*). For example, set V_{REF} to 0.5V, bias V_{IN}− to 1.0V and drive V_{IN}+ with a signal range of 0.5V to 1.5V.

Because very large input signal swings can degrade distortion performance, better performance with a single-ended input can be obtained by reducing the reference voltage when maintaining a full-range output. Table 1 and Table 2 indicate the input to output relationship of the ADC12DL066. Note again that single-ended operation of the ADC12D040 is not recommended because of the degraded performance that results. A single-ended to differential conversion circuit is shown in Figure 34.

Table 1. Input to Output Relationship – Differential Input

V_{IN}^+	V_{IN}^-	Binary Output	2's Complement Output
$V_{CM} - V_{REF} / 2$	$V_{CM} + V_{REF / 2}$	0000 0000 0000	1000 0000 0000
$V_{CM} - V_{REF / 4}$	$V_{CM} + V_{REF} / 4$	0100 0000 0000	1100 0000 0000
V_{CM}	V_{CM}	1000 0000 0000	0000 0000 0000
$V_{CM} + V_{REF} / 4$	$V_{CM} - V_{REF} / 4$	1100 0000 0000	0100 0000 0000
$V_{CM} + V_{REF} / 2$	$V_{CM} - V_{REF} / 2$	1111 1111 1111	0111 1111 1111

Table 2. Input to Output Relationship – Single-Ended Input

V_{IN}^+	V_{IN}^-	Binary Output	2's Complement Output
$V_{CM} - V_{REF}$	V_{CM}	0000 0000 0000	1000 0000 0000
$V_{CM} - V_{REF} / 2$	V_{CM}	0100 0000 0000	1100 0000 0000
V_{CM}	V_{CM}	1000 0000 0000	0000 0000 0000
$V_{CM} + V_{REF} / 2$	V_{CM}	1100 0000 0000	0100 0000 0000
$V_{CM} + V_{REF}$	V_{CM}	1111 1111 1111	0111 1111 1111

Driving the Analog Inputs

The V_{IN}+ and the V_{IN}− inputs of the ADC12DL066 consist of an analog switch followed by a switched-capacitor amplifier. The capacitance seen at the analog input pins changes with the clock level, appearing as 8 pF when the clock is low, and 7 pF when the clock is high.

As the internal sampling switch opens and closes, current pulses occur at the analog input pins, resulting in voltage spikes at these pins. As a driving amplifier attempts to counteract these voltage spikes, a damped oscillation may appear at the ADC analog inputs. Do not attempt to filter out these pulses. Rather, use amplifiers to drive the ADC12DL066 input pins that are able to react to these pulses and settle before the switch opens and another sample is taken. The LMH6550, LMH6702, LMH6628, LMH6622 and the LMH6655 are good amplifiers for driving the ADC12DL066.

To help isolate the pulses at the ADC input from the amplifier output, use RCs at the inputs, as can be seen in Figure 33 and Figure 34. These components should be placed close to the ADC inputs because the input pins of the ADC is the most sensitive part of the system and this is the last opportunity to filter that input.

For Nyquist applications the RC pole should be at the ADC sample rate. The ADC input capacitance in the sample mode should be considered when setting the RC pole. Setting the pole in this manner will provide best SNR performance.

To obtain best SINAD and ENOB performance, reduce the RC time constant until SNR and THD are numerically equal to each other. To obtain best distortion and SFDR performance, eliminate the RC altogether.

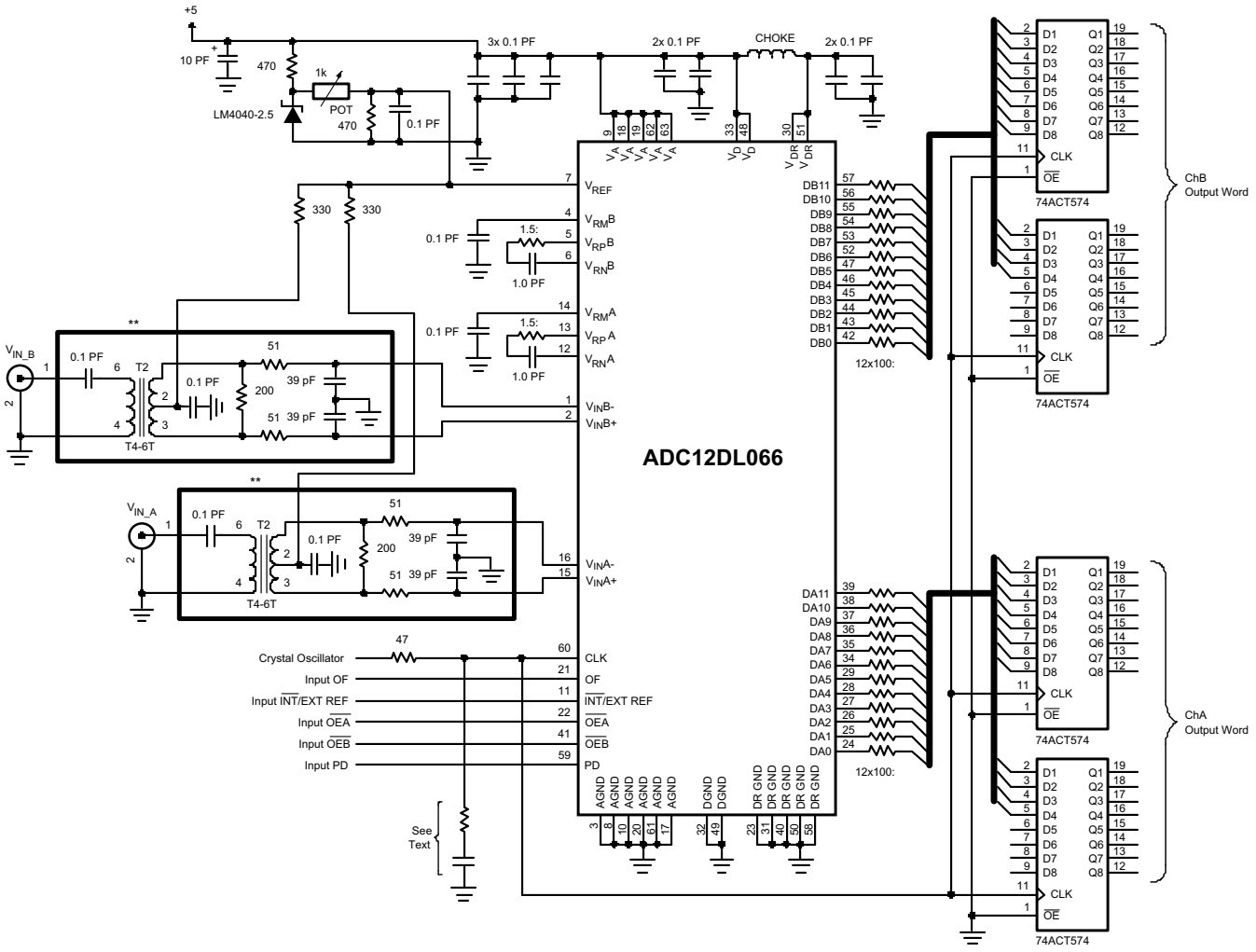


Figure 33. Application Circuit using Transformer or Differential Op-Amp Drive Circuit

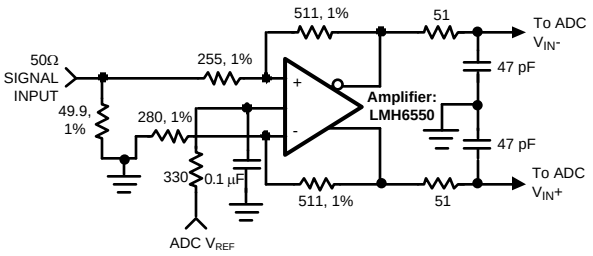


Figure 34. Differential Drive Circuit using a fully differential amplifier.

For undersampling applications, the RC pole should be set at about 1.5 to 2 times the maximum input frequency to maintain a linear delay response.

Note that the ADC12DL066 is not designed to operate with single-ended inputs. However, doing so is possible if the degraded performance is acceptable. See Single-Ended Operation.

Figure 33 shows a narrow band application with a transformer used to convert single-ended input signals to differential. Figure 34 shows the use of a fully differential amplifier for single-ended to differential conversion. The LMH6550 is recommended for single-ended to differential conversion when d.c. or very low frequencies must be accommodated. Of course, the LMH6550 may also be used to amplify differential signals.

Input Common Mode Voltage

The input common mode voltage, V_{CM}, should be of a value such that the peak excursions of the analog signal does not go more negative than ground or more positive than 1.0 Volt below the V_A supply voltage. The nominal V_{CM} should generally be about $V_{REF}/2$, but $V_{RB}A$ and $V_{RB}B$ can be used as a V_{CM} source as long as no d.c. current is drawn from either of these pins.

DIGITAL INPUTS

Digital TTL/CMOS compatible inputs consist of CLK, $\overline{OEA}$, $\overline{OEB}$, OF, $\overline{INT}$/EXT REF and PD.

The CLK Pin

The **CLK** signal controls the timing of the sampling process. Drive the clock input with a stable, low jitter clock signal in the range of 15 MHz to 75 MHz with rise and fall times of 2 ns or less. The trace carrying the clock signal should be as short as possible and should not cross any other signal line, analog or digital, not even at 90°.

If the **CLK** is interrupted, or its frequency too low, the charge on internal capacitors can dissipate to the point where the accuracy of the output data will degrade. This is what limits the lowest sample.

The ADC clock line should be considered to be a transmission line and be series terminated at the source end to match the source impedance with the characteristic impedance of the clock line. It generally is not necessary to terminate the far (ADC) end of the clock line, but if a single clock source is driving more than one device (a condition that is generally not recommended), far end termination may be needed. The far end termination should be near but beyond the ADC clock pin as seen from the clock source.

It is highly desirable that the the source driving the ADC **CLK** pin only drive that pin. However, if that source is used to drive other things, each driven pin should be a.c. terminated with a series RC to ground, as shown in Figure 33, such that the resistor value is equal to the characteristic impedance of the clock line and the capacitor value is

$$C \geq \frac{4 \times t_{PD} \times L}{Z_o} \quad (9)$$

where

- t_{PD} is the signal propagation time in ns/unit length, "L" is the line length and Z_O is the characteristic impedance of the clock line. This termination should be as close as possible to the ADC clock pin but beyond it as seen from the clock source. Typical t_{PD} is about 150 ps/inch (60 ps/cm) on FR-4 board material. The units of "L" and t_{PD} should be the same (inches or centimeters).

The duty cycle of the clock signal can affect the performance of the A/D Converter. Because achieving a precise duty cycle is difficult, the ADC12DL066 is designed to maintain performance over a range of duty cycles. While it is specified and performance is guaranteed with a 50% clock duty cycle, performance is typically maintained over a clock duty cycle range of 43% to 57% at 66 Msps.

Take care to maintain a constant clock line impedance throughout the length of the line. Refer to Application Note AN-905 for information on setting characteristic impedance.

The $\overline{\text{OEA}}$, $\overline{\text{OEB}}$ Pins

The $\overline{\text{OEA}}$ and $\overline{\text{OEB}}$ pins, when high, put the output pins of their respective converters into a high impedance state. When either of these pins is low, the corresponding outputs are in the active state. The ADC12DL066 will continue to convert whether these pins are high or low, but the output can not be read while the pin is high.

Since ADC noise increases with increased output capacitance at the digital output pins, do not use the TRI-STATE outputs of the ADC12DL066 to drive a bus. Rather, each output pin should be located close to and drive a single digital input pin. To further reduce ADC noise, a 100 Ω resistor in series with each ADC digital output pin, located close to their respective pins, should be added to the circuit.

The PD Pin

The PD pin, when high, holds the ADC12DL066 in a power-down mode to conserve power when the converter is not being used. The power consumption in this state is 75 mW with a 66 MHz clock and 40mW if the clock is stopped when PD is high. The output data pins are undefined and the data in the pipeline is corrupted while in the power down mode.

The Power Down Mode Exit Cycle time is determined by the value of the components on pins 4, 5, 6, 12, 13 and 14 and is about 500 µs with the recommended components on the V_{RP}, V_{RM} and V_{RN} reference bypass pins. These capacitors loose their charge in the Power Down mode and must be recharged by on-chip circuitry before conversions can be accurate. Smaller capacitor values allow slightly faster recovery from the power down mode, but can result in a reduction in SNR, SINAD and ENOB performance.

The OF Pin

The output data format is offset binary when the OF pin is at a logic low or 2's complement when the OF pin is at a logic high. While the sense of this pin may be changed "on the fly," doing this is not recommended as the output data could be erroneous for a few clock cycles after this change is made.

The $\overline{\text{INT}}$/EXT REF Pin

The $\overline{\text{INT}}$/EXT REF pin determines whether the internal reference or an external reference voltage is used. With this pin at a logic low, the internal 1.0V reference is in use. With this pin at a logic high an external reference must be applied to the V_{REF} pin, which should then be bypassed to ground. There is no need to bypass the V_{REF} pin when the internal reference is used. There is no access to the internal reference voltage, but its value is approximately equal to $V_{RP} - V_{RN}$.

DATA OUTPUT PINS

The ADC12DL066 has 24 TTL/CMOS compatible Data Output pins. Valid data is present at these outputs while the $\overline{\text{OE}}$ and PD pins are low. While the t_{OD} time provides information about output timing, t_{OD} will change with a change of clock frequency. At the rated 66 MHz clock rate, the data transition can be coincident with the rise of the clock and about 7 ns before the fall of the clock (depending upon V_{DR}), so the *falling edge* of the clock should be used to capture the output data. At lower clock frequencies the data transition occurs a little after the rising edge of the clock, but the fall of the clock still appears to be the best edge for data capture. However, circuit board layout will affect relative delays of the clock and data, so it is important to consider these relative delays when designing the digital interface.

Be very careful when driving a high capacitance bus. The more capacitance the output drivers must charge for each conversion, the more instantaneous digital current flows through V_{DR} and DR GND. These large charging current spikes can cause on-chip ground noise and couple into the analog circuitry, degrading dynamic performance. Adequate bypassing, limiting output capacitance and careful attention to the ground plane will reduce this problem. Additionally, bus capacitance beyond the specified 15 pF/pin will cause t_{OD} to increase, making it difficult to properly latch the ADC output data. The result could be an apparent reduction in dynamic performance.

To minimize noise due to output switching, minimize the load currents at the digital outputs. This can be done by connecting buffers (74AC541, for example) between the ADC outputs and any other circuitry. Only one driven input should be connected to each output pin. Additionally, inserting series resistors of about 100Ω at the digital outputs, close to the ADC pins, will isolate the outputs from trace and other circuit capacitances and limit the output currents, which could otherwise result in performance degradation. See Figure 33.

Note that, although the ADC12DL066 has Tri-State outputs, these outputs should not be used to drive a bus and the charging and discharging of large capacitances can degrade SNR performance. Each output pin should drive only one pin of a receiving device and the interconnecting lines should be as short as practical.

POWER SUPPLY CONSIDERATIONS

The power supply pins should be bypassed with a 10 µF capacitor and with a 0.1 µF ceramic chip capacitor within a centimeter of each power pin. Leadless chip capacitors are preferred because they have low series inductance.

As is the case with all high-speed converters, the ADC12DL066 is sensitive to power supply noise. Accordingly, the noise on the analog supply pin should be kept below 100 mV_{P-P}.

No pin should ever have a voltage on it that is in excess of the supply voltages, not even on a transient basis. Be especially careful of this during power turn on and turn off.

The V_{DR} pin provides power for the output drivers and may be operated from a supply in the range of 2.4V to V_D (nominal 5V). This can simplify interfacing to lower voltage devices and systems. Note, however, that t_{OD} increases with reduced V_{DR}. **DO NOT operate the V_{DR} pin at a voltage higher than V_D.**

LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals are essential to ensure accurate conversion. Maintaining separate analog and digital areas of the board, with the ADC12DL066 between these areas, is required to achieve specified performance.

The ground return for the data outputs (DR GND) carries the ground current for the output drivers. The output current can exhibit high transients that could add noise to the conversion process. To prevent this from happening, the DR GND pins should NOT be connected to system ground in close proximity to any of the ADC12DL066's other ground pins.

Capacitive coupling between the typically noisy digital circuitry and the sensitive analog circuitry can lead to poor performance. The solution is to keep the analog circuitry separated from the digital circuitry, and to keep the clock line as short as possible.

The effects of the noise generated from the ADC output switching can be minimized through the use of 100Ω resistors in series with each data output line. Locate these resistors as close to the ADC output pins as possible.

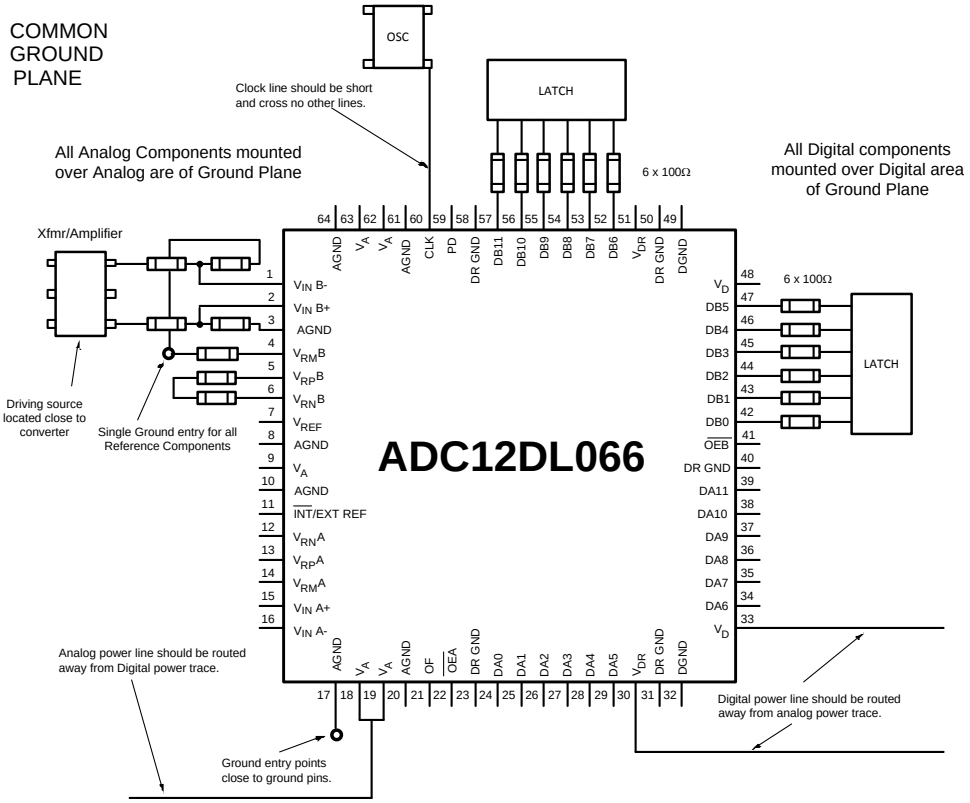


Figure 35. Example of a Suitable Layout

Since digital switching transients are composed largely of high frequency components, total ground plane copper weight will have little effect upon the logic-generated noise. This is because of the skin effect. Total surface area is more important than is total ground plane volume.

Generally, analog and digital lines should cross each other at 90° to avoid crosstalk. To maximize accuracy in high speed, high resolution systems, however, avoid crossing analog and digital lines altogether. It is important to keep clock lines as short as possible and isolated from ALL other lines, including other digital lines. Even the generally accepted 90° crossing should be avoided with the clock line as even a little coupling can cause problems at high frequencies. This is because other lines can introduce jitter into the clock line, which can lead to degradation of SNR. Also, the high speed clock can introduce noise into the analog chain.

Best performance at high frequencies and at high resolution is obtained with a straight signal path. That is, the signal path through all components should form a straight line wherever possible.

Be especially careful with the layout of inductors. Mutual inductance can change the characteristics of the circuit in which they are used. Inductors should *not* be placed side by side, even with just a small part of their bodies beside each other.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input pins and ground or to the reference input pin and ground should be connected to a very clean point in the ground plane.

Figure 35 gives an example of a suitable layout. All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed in the analog area of the board. All digital circuitry and I/O lines should be placed in the digital area of the board. The ADC12DL066 should be between these two areas. Furthermore, all components in the reference circuitry and the input signal chain that are connected to ground should be connected together with short traces and enter the ground plane at a single, quiet point. All ground connections should have a low inductance path to ground.

DYNAMIC PERFORMANCE

To achieve the best dynamic performance, the clock source driving the CLK input must be free of jitter. Isolate the ADC clock from any digital circuitry with buffers, as with the clock tree shown in Figure 36. The gates used in the clock tree must be capable of operating at frequencies much higher than those used if added jitter is to be prevented.

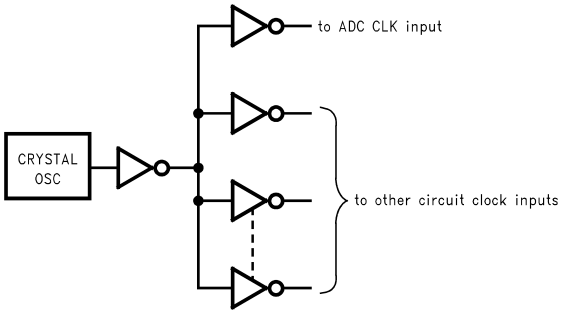


Figure 36. Isolating the ADC Clock from other Circuitry with a Clock Tree

Best performance will be obtained with a differential input drive, compared with a single-ended drive, as discussed in Single-Ended Operation and Driving the Analog Inputs.

As mentioned in LAYOUT AND GROUNDING, it is good practice to keep the ADC clock line as short as possible and to keep it well away from any other signals. Other signals can introduce jitter into the clock signal, which can lead to reduced SNR performance, and the clock can introduce noise into other lines. Even lines with 90° crossings have capacitive coupling, so try to avoid even these 90° crossings of the clock line.

COMMON APPLICATION PITFALLS

Driving the inputs (analog or digital) beyond the power supply rails. For proper operation, all inputs should not go more than 100 mV beyond the supply rails (more than 100 mV below the ground pins or 100 mV above the supply pins). Exceeding these limits on even a transient basis may cause faulty or erratic operation. It is not uncommon for high speed digital components (e.g., 74F devices) to exhibit overshoot or undershoot that goes above the power supply or below ground. A resistor of about 47Ω to 100Ω in series with any offending digital input, close to the signal source, will eliminate the problem.

Do not allow input voltages to exceed the supply voltage, even on a transient basis. Not even during power up or power down.

Be careful not to overdrive the inputs of the ADC12DL066 with a device that is powered from supplies outside the range of the ADC12DL066 supply. Such practice may lead to conversion inaccuracies and even to device damage.

Attempting to drive a high capacitance digital data bus. The more capacitance the output drivers must charge for each conversion, the more instantaneous digital current flows through V_{DR} and DR GND. These large charging current spikes can couple into the analog circuitry, degrading dynamic performance. Adequate bypassing and maintaining separate analog and digital areas on the pc board will reduce this problem.

Additionally, bus capacitance beyond the specified 15 pF/pin will cause t_{OD} to increase, making it difficult to properly latch the ADC output data. The result could, again, be an apparent reduction in dynamic performance.

The digital data outputs should be buffered (with 74AC541, for example). Dynamic performance can also be improved by adding series resistors at each digital output, close to the ADC12DL066, which reduces the energy coupled back into the converter output pins by limiting the output current. A reasonable value for these resistors is 100Ω.

Using an inadequate amplifier to drive the analog input. As explained in Signal Inputs, the capacitance seen at the input alternates between 8 pF and 7 pF, depending upon the phase of the clock. This dynamic load is more difficult to drive than is a fixed capacitance.

If the amplifier exhibits overshoot, ringing, or any evidence of instability, even at a very low level, it will degrade performance. A small series resistor at each amplifier output and a capacitor at the analog inputs (as shown in Figure 32 and Figure 34) will improve performance. The LMH6702 and the LMH6628 have been successfully used to drive the analog inputs of the ADC12DL066.

Also, it is important that the signals at the two inputs have exactly the same amplitude and be exactly 180º out of phase with each other. Board layout, especially equality of the length of the two traces to the input pins, will affect the effective phase between these two signals. Remember that an operational amplifier operated in the non-inverting configuration will exhibit more time delay than will the same device operating in the inverting configuration.

Operating with the reference pins outside of the specified range. As mentioned in Reference Pins, V_{REF} should be in the range of

$$0.8V \le V_{REF} \le 1.5V \quad (10)$$

Operating outside of these limits could lead to performance degradation.

Inadequate network on Reference Bypass pins ($V_{RP}A$, $V_{RN}A$, $V_{RM}A$, $V_{RP}B$, $V_{RN}B$ and $V_{RM}B$). As mentioned in Reference Pins, these pins should be bypassed with 0.1 µF capacitors to ground at $V_{RM}A$ and $V_{RM}B$ and with a series RC of 1.5 Ω and 1.0 µF between pins $V_{RP}A$ and $V_{RN}A$ and between $V_{RP}B$ and $V_{RN}B$ for best performance.

Using a clock source with excessive jitter, using excessively long clock signal trace, or having other signals coupled to the clock signal trace. This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR and SINAD performance.

REVISION HISTORY

Changes from Revision F (February 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	28

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC12DL066CIVS/NOPB	ACTIVE	TQFP	PAG	64	160	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	ADC12DL066 CIVS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

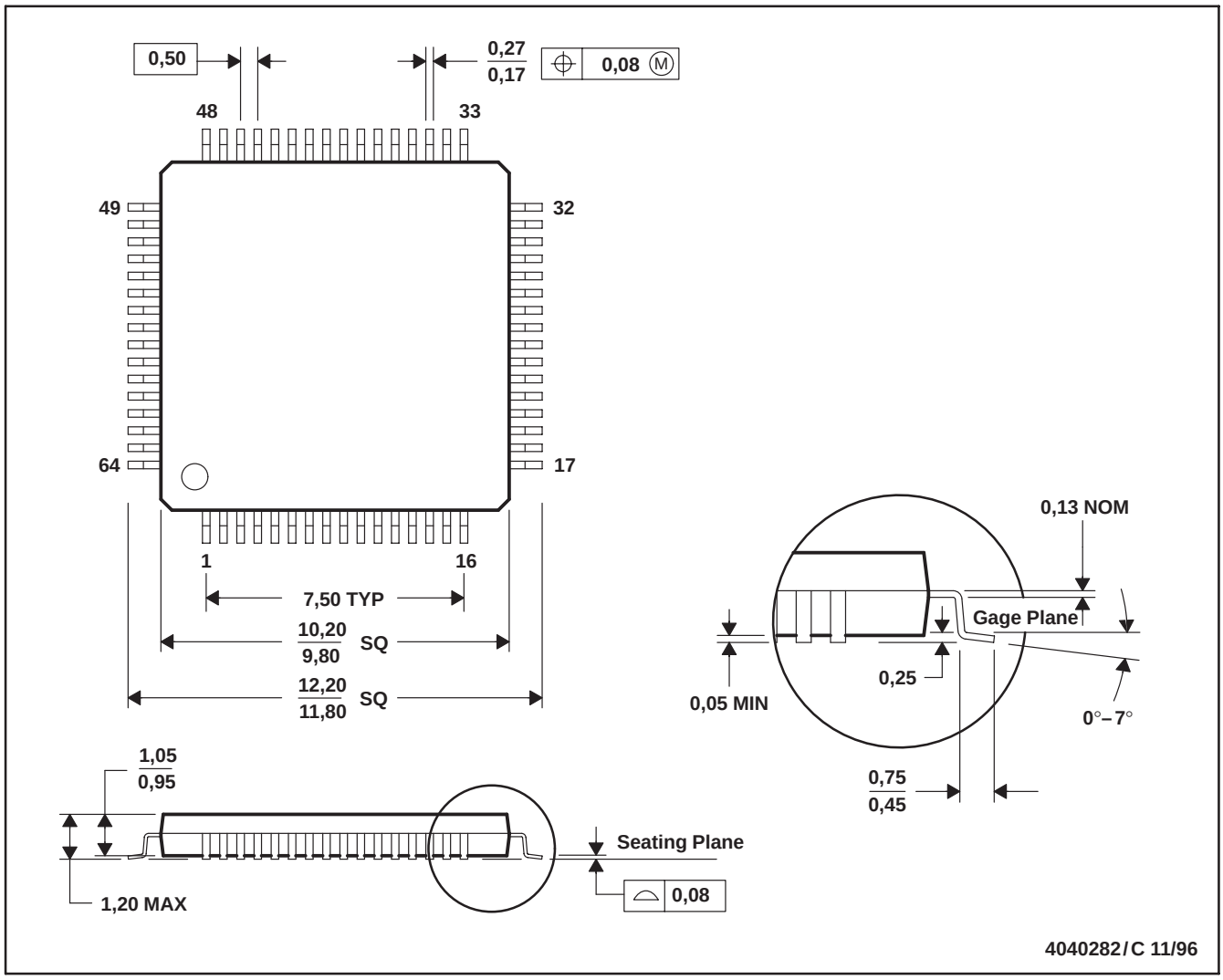
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

PAG (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265