Dual-Channel, 14- and 16-Bit, 250-MSPS Analog-to-Digital Converters

Check for Samples: ADS42JB49, ADS42JB69

FEATURES

- **Dual-Channel ADCs**
- **14- and 16-Bit Resolution**
- **Maximum Clock Rate: 250 MSPS**
- **JESD204B Serial Interface**
  - **Subclass 0, 1, 2 Compliant**
  - **Up to 3.125 Gbps**
  - **Two and Four Lanes Support**
- **Analog Input Buffer with High-Impedance Input**
- **Flexible Input Clock Buffer: Divide-by-1, -2, and -4**
- **Differential Full-Scale Input: 2 V_{PP} and 2.5 V_{PP} (Register Programmable)**
- **Package: 9-mm × 9-mm QFN-64**
- **Power Dissipation: 850 mW/Ch**
- **Aperture Jitter: 85 f_S rms**
- **Internal Dither**
- **Channel Isolation: 100 dB**
- **Performance:**
  - **f_{IN} = 170 MHz at 2 V_{PP}, –1 dBFS**
    - **SNR: 73.3 dBFS**
    - **SFDR: 93 dBc for HD2, HD3**
    - **SFDR: 100 dBc for Non HD2, HD3**
  - **f_{IN} = 170 MHz at 2.5 V_{PP}, –1 dBFS**
    - **SNR: 74.7 dBFS**
    - **SFDR: 89 dBc for HD2, HD3 and 95 dBc for Non HD2, HD3**

APPLICATIONS

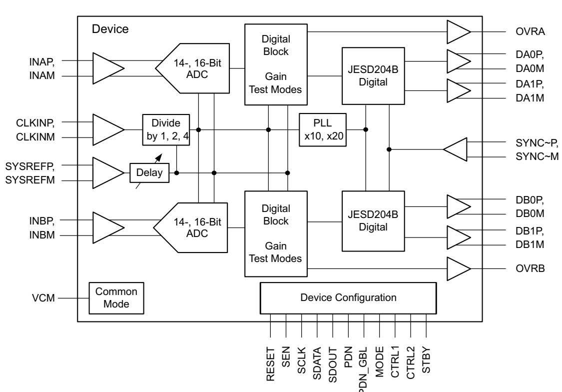
- **Communication and Cable Infrastructure**
- **Multi-Carrier, Multimode Cellular Receivers**
- **Radar and Smart Antenna Arrays**
- **Broadband Wireless**
- **Test and Measurement Systems**
- **Software-Defined and Diversity Radios**
- **Microwave and Dual-Channel I/Q Receivers**
- **Repeaters**
- **Power Amplifier Linearization**

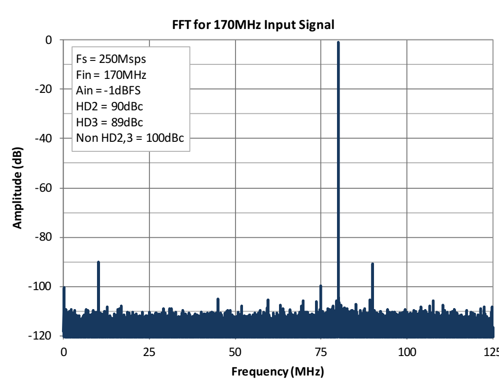
DESCRIPTION

The ADS42JB69 and ADS42JB49 are high-linearity, dual-channel, 16- and 14-bit, 250-MSPS, analog-to-digital converters (ADCs). These devices support the JESD204B serial interface with data rates up to 3.125 Gbps. The buffered analog input provides uniform input impedance across a wide frequency range while minimizing sample-and-hold glitch energy making it easy to drive analog inputs up to very high input frequencies. A sampling clock divider allows more flexibility for system clock architecture design. The devices employ internal dither algorithms to provide excellent spurious-free dynamic range (SFDR) over a large input frequency range.

RELATED PRODUCTS

INTERFACE OPTION	14-BIT, 160 MSPS	14-BIT, 250 MSPS	16-BIT, 250 MSPS
DDR, QDR LVDS	—	ADS42LB49	ADS42LB69
JESD204B	ADS42JB46	ADS42JB49	ADS42JB69





This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE
ADS42JB49	QFN-64	RGC	–40°C to +85°C
ADS42JB69	QFN-64	RGC	–40°C to +85°C

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range, unless otherwise noted.

		VALUE	UNIT
Supply voltage range	AVDD3V	–0.3 to 3.6	V
	AVDD	–0.3 to 2.1	V
	DRVDD	–0.3 to 2.1	V
	IOVDD	–0.3 to 2.1	V
Voltage between AGND and DGND		–0.3 to 0.3	V
Voltage applied to input pins	INAP, INBP, INAM, INBM	–0.3 to 3	V
	CLKINP, CLKINM	–0.3 to minimum (2.1, AVDD + 0.3)	V
	SYNC~P, SYNC~M	–0.3 to minimum (2.1, AVDD + 0.3)	V
	SYSREFP, SYSREFM	–0.3 to minimum (2.1, AVDD + 0.3)	V
	SCLK, SEN, SDATA, RESET, PDN_GBL, CTRL1, CTRL2, STBY, MODE	–0.3 to 3.9	V
Temperature range	Operating free-air, T_A	–40 to +85	°C
	Operating junction, T_J	+125	°C
	Storage, T_{stg}	–65 to +150	°C
Electrostatic discharge (ESD) rating	Human body model (HBM)	2	kV

THERMAL INFORMATION

THERMAL METRIC(1)		ADS42JB49, ADS42JB69	UNITS
		RGC (QFN)	
		64 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	22.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	7.1	
θ_{JB}	Junction-to-board thermal resistance	2.5	
ψ_{JT}	Junction-to-top characterization parameter	0.1	
ψ_{JB}	Junction-to-board characterization parameter	2.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS(1)

Over operating free-air temperature range, unless otherwise noted.

PARAMETER			MIN	NOM	MAX	UNIT
SUPPLIES						
AVDD	Analog supply voltage		1.7	1.8	1.9	V
AVDD3V	Analog buffer supply voltage		3.15	3.3	3.45	V
DRVDD	Digital supply voltage		1.7	1.8	1.9	V
IOVDD	Output buffer supply voltage		1.7	1.8	1.9	V
ANALOG INPUTS						
V_{ID}	Differential input voltage range	Default after reset		2		V_{PP}
		Register programmable(2)		2.5		V_{PP}
V_{ICR}	Input common-mode voltage			VCM ± 0.025		V
	Maximum analog input frequency with 2.5-V_{PP} input amplitude			250		MHz
	Maximum analog input frequency with 2-V_{PP} input amplitude			400		MHz
CLOCK INPUT						
	Input clock sample rate	10x mode	60		250	MSPS
		20x mode	40		156.25	MSPS
	Input clock amplitude differential (V_{CLKP} – V_{CLKM})	Sine wave, ac-coupled	0.3(3)	1.5		V_{PP}
		LVPECL, ac-coupled		1.6		V_{PP}
		LVDS, ac-coupled		0.7		V_{PP}
		LVCMOS, single-ended, ac-coupled		1.5		V
	Input clock duty cycle		35%	50%	65%	
DIGITAL OUTPUTS						
C_{LOAD}	Maximum external load capacitance from each output pin to DRGND			3.3		pF
R_{LOAD}	Single-ended load resistance			+50		Ω
T_A	Operating free-air temperature		–40		+85	°C

(1) After power-up, to reset the device for the first time, use the RESET pin only. Refer to the *Register Initialization* section.
(2) For details, refer to the *Digital Gain* section.
(3) Refer to the *Performance vs Clock Amplitude* curves, Figure 32 and Figure 33.

Table 1. High-Frequency Modes Summary

REGISTER ADDRESS	VALUE	DESCRIPTION
Dh	90h	High-frequency modes should be enabled for input frequencies greater than 250 MHz.
Eh	90h	High-frequency modes should be enabled for input frequencies greater than 250 MHz.

ELECTRICAL CHARACTERISTICS: ADS42JB69 (16-Bit)

Typical values are at T_A = +25°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, and sampling rate = 250 MSPS, unless otherwise noted. Minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, and IOVDD = 1.8 V.

PARAMETER		TEST CONDITIONS	2-V_{PP} FULL-SCALE			2.5-V_{PP} FULL-SCALE			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz		74			75.9		dBFS
		f_{IN} = 70 MHz		73.8			75.6		dBFS
		f_{IN} = 170 MHz	70.8	73.3			74.7		dBFS
		f_{IN} = 230 MHz		72.6			74		dBFS
SINAD	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz		73.9			75.7		dBFS
		f_{IN} = 70 MHz		73.7			75.3		dBFS
		f_{IN} = 170 MHz	69.6	73.2			74.5		dBFS
		f_{IN} = 230 MHz		72.2			73.1		dBFS
SFDR	Spurious-free dynamic range (including second and third harmonic distortion)	f_{IN} = 10 MHz		95			90		dBc
		f_{IN} = 70 MHz		91			88		dBc
		f_{IN} = 170 MHz	81	93			89		dBc
		f_{IN} = 230 MHz		84			82		dBc
THD	Total harmonic distortion	f_{IN} = 10 MHz		92			88		dBc
		f_{IN} = 70 MHz		89			86		dBc
		f_{IN} = 170 MHz	78	91			86		dBc
		f_{IN} = 230 MHz		82			80		dBc
HD2	2nd-order harmonic distortion	f_{IN} = 10 MHz		95			95		dBc
		f_{IN} = 70 MHz		91			88		dBc
		f_{IN} = 170 MHz	81	93			94		dBc
		f_{IN} = 230 MHz		84			82		dBc
HD3	3rd-order harmonic distortion	f_{IN} = 10 MHz		95			90		dBc
		f_{IN} = 70 MHz		96			93		dBc
		f_{IN} = 170 MHz	81	94			89		dBc
		f_{IN} = 230 MHz		86			84		dBc
	Worst spur (other than second and third harmonics)	f_{IN} = 10 MHz		102			102		dBc
		f_{IN} = 70 MHz		103			103		dBc
		f_{IN} = 170 MHz	87	100			95		dBc
		f_{IN} = 230 MHz		99			93		dBc
IMD	Two-tone intermodulation distortion	f_1 = 46 MHz, f_2 = 50 MHz, each tone at –7 dBFS		97			95		dBFS
		f_1 = 185 MHz, f_2 = 190 MHz, each tone at –7 dBFS		90			89		dBFS
	Crosstalk	20-MHz, full-scale signal on channel under observation; 170-MHz, full-scale signal on other channel		100			100		dB
	Input overload recovery	Recovery to within 1% (of full-scale) for 6-dB overload with sine-wave input		1			1		Clock cycle
PSRR	AC power-supply rejection ratio	For 50-mV_{PP} signal on AVDD supply, up to 10 MHz		> 40			> 40		dB
ENOB	Effective number of bits	f_{IN} = 170 MHz		11.9			12.1		LSBs
DNL	Differential nonlinearity	f_{IN} = 170 MHz		±0.6			±0.6		LSBs
INL	Integrated nonlinearity	f_{IN} = 170 MHz		±3	±8		±3.5		LSBs

ELECTRICAL CHARACTERISTICS: ADS42JB49 (14-Bit)

Typical values are at T_A = +25°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, and sampling rate = 250 MSPS, unless otherwise noted. Minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, and IOVDD = 1.8 V.

PARAMETER		TEST CONDITIONS	2-V_{PP} FULL-SCALE			2.5-V_{PP} FULL-SCALE			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz		73.4			75		dBFS
		f_{IN} = 70 MHz		73.2			74.7		dBFS
		f_{IN} = 170 MHz	69.5	72.7			74		dBFS
		f_{IN} = 230 MHz		72.2			73.4		dBFS
SINAD	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz		73.3			74.8		dBFS
		f_{IN} = 70 MHz		73.1			74.5		dBFS
		f_{IN} = 170 MHz	68.5	72.7			73.8		dBFS
		f_{IN} = 230 MHz		71.8			72.6		dBFS
SFDR	Spurious-free dynamic range (including second and third harmonic distortion)	f_{IN} = 10 MHz		95			90		dBc
		f_{IN} = 70 MHz		91			88		dBc
		f_{IN} = 170 MHz	79	93			89		dBc
		f_{IN} = 230 MHz		84			82		dBc
THD	Total harmonic distortion	f_{IN} = 10 MHz		92			88		dBc
		f_{IN} = 70 MHz		89			86		dBc
		f_{IN} = 170 MHz	76	90			86		dBc
		f_{IN} = 230 MHz		82			80		dBc
HD2	2nd-order harmonic distortion	f_{IN} = 10 MHz		95			95		dBc
		f_{IN} = 70 MHz		91			88		dBc
		f_{IN} = 170 MHz	79	93			94		dBc
		f_{IN} = 230 MHz		84			82		dBc
HD3	3rd-order harmonic distortion	f_{IN} = 10 MHz		95			90		dBc
		f_{IN} = 70 MHz		96			93		dBc
		f_{IN} = 170 MHz	79	94			89		dBc
		f_{IN} = 230 MHz		86			84		dBc
	Worst spur (other than second and third harmonics)	f_{IN} = 10 MHz		102			102		dBc
		f_{IN} = 70 MHz		103			103		dBc
		f_{IN} = 170 MHz	87	101			95		dBc
		f_{IN} = 230 MHz		99			93		dBc
IMD	Two-tone intermodulation distortion	f_1 = 46 MHz, f_2 = 50 MHz, each tone at –7 dBFS		97			95		dBFS
		f_1 = 185 MHz, f_2 = 190 MHz, each tone at –7 dBFS		90			89		dBFS
	Crosstalk	20-MHz, full-scale signal on channel under observation; 170-MHz, full-scale signal on other channel		100			100		dB
	Input overload recovery	Recovery to within 1% (of full-scale) for 6-dB overload with sine-wave input		1			1		Clock cycle
PSRR	AC power-supply rejection ratio	For a 50-mV_{PP} signal on AVDD supply, up to 10 MHz		> 40			> 40		dB
ENOB	Effective number of bits	f_{IN} = 170 MHz		11.8			12		LSBs
DNL	Differential nonlinearity	f_{IN} = 170 MHz		±0.15			±0.15		LSBs
INL	Integrated nonlinearity	f_{IN} = 170 MHz		±0.75	±3		±0.9		LSBs

ELECTRICAL CHARACTERISTICS: GENERAL

Typical values are at +25°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, and sampling rate = 250 MSPS, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, and IOVDD = 1.8 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
V_{ID}	Differential input voltage range	Default (after reset)		2		V_{PP}
		Register programmed(1)		2.5		V_{PP}
		Differential input resistance (at 170 MHz)		1.2		kΩ
		Differential input capacitance (at 170 MHz)		4		pF
	Analog input bandwidth	With 50-Ω source impedance, and 50-Ω termination		900		MHz
VCM	Common-mode output voltage			1.9		V
	VCM output current capability			10		mA
DC ACCURACY						
	Offset error		–20		20	mV
E_{GREF}	Gain error as a result of internal reference inaccuracy alone			±2		%FS
E_{GCHAN}	Gain error of channel alone			–5		%FS
	Temperature coefficient of E_{GCHAN}			0.01		Δ%/°C
POWER SUPPLY						
IAVDD	Analog supply current			128	160	mA
IAVDD3V	Analog buffer supply current			290	330	mA
IDRVDD	Digital supply current			228	252	mA
IOVDD	Output buffer supply current	50-Ω external termination from pin to IOVDD, f_{IN} = 2.5 MHz		60	100	mA
	Analog power			231		mW
	Analog buffer power			957		mW
	Digital power			410		mW
	Power consumption by output buffer	50-Ω external termination from pin to IOVDD, f_{IN} = 2.5 MHz		109		mW
	Total power			1.7	1.96	W
	Global power-down				160	mW

(1) Refer to the *Serial Interface* section.

TIMING CHARACTERISTICS

Typical values are at +25°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, and sampling rate = 250 MSPS, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, and IOVDD = 1.8 V. See Figure 1.

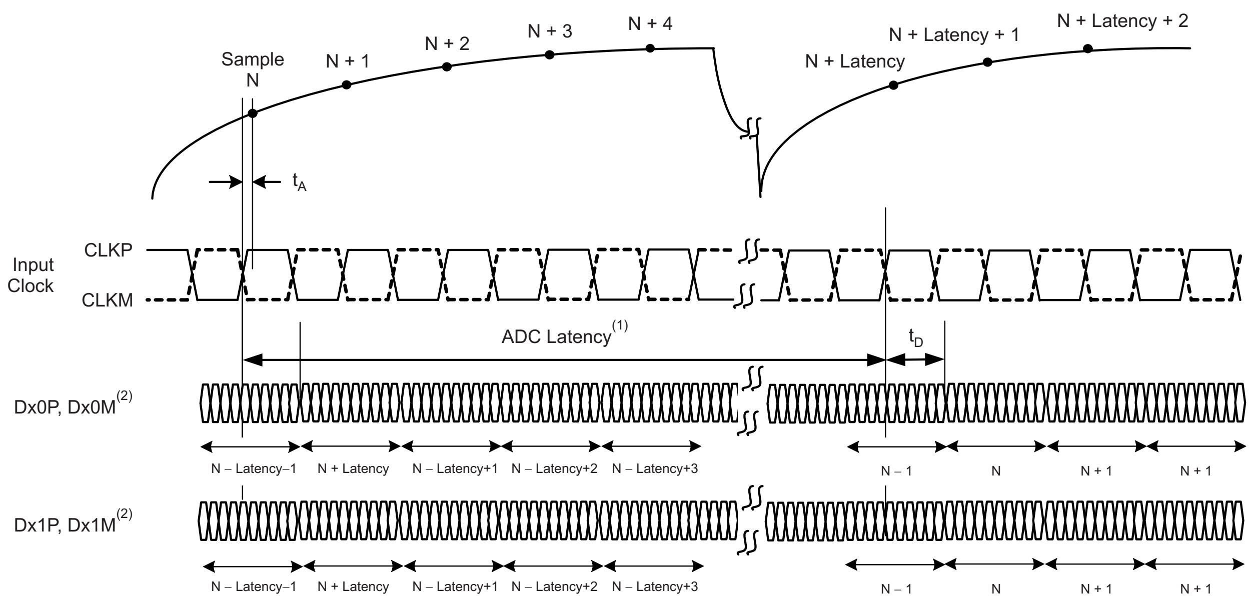
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
SAMPLE TIMING CHARACTERISTICS						
	Aperture delay		0.4	0.7	1.1	ns
	Aperture delay matching	Between two channels on the same device		±70		ps
		Between two devices at the same temperature and supply voltage		±150		ps
	Aperture jitter			85		f_S rms
	Wake-up time	Time to valid data after coming out of STANDBY mode		50	200	µs
		Time to valid data after coming out of global power-down		250	1000	µs
$t_{SU\_SYNC\sim}$	Setup time for SYNC~	Referenced to input clock rising edge	400			ps
$t_{H\_SYNC\sim}$	Hold time for SYNC~	Referenced to input clock rising edge	100			ps
t_{SU_SYSREF}	Setup time for SYSREF	Referenced to input clock rising edge	400			ps
t_{H_SYSREF}	Hold time for SYSREF	Referenced to input clock rising edge	100			ps
CML OUTPUT TIMING CHARACTERISTICS						
	Unit interval		320		1667	ps
	Serial output data rate				3.125	Gbps
	Total jitter	2.5 Gbps (10x mode, f_S = 250 MSPS)		0.28		$_{P-P}$UI
		3.125 Gbps (20x mode, f_S = 156.25 MSPS)		0.3		$_{P-P}$UI
t_R, t_F	Data rise time, data fall time	Rise and fall times measured from 20% to 80%, differential output waveform, 600 Mbps ≤ bit rate ≤ 3.125 Gbps		105		ps

Table 2. Latency in Different Modes(1)(2)

MODE	PARAMETER	LATENCY (N Cycles)	TYPICAL DATA DELAY (t_D, ns)
10x	ADC latency	23	0.65 × t_S + 3
	Normal OVR latency	14	6.7
	Fast OVR latency	9	6.7
	from SYNC~ falling edge to CGS phase(3)	16	0.65 × t_S + 3
	from SYNC~ rising edge to ILA sequence(4)	25	0.65 × t_S + 3
20x	ADC latency	22	0.85 × t_S + 3
	Normal OVR latency	14	6.7
	Fast OVR latency	9	6.7
	from SYNC~ falling edge to CGS phase(3)	15	0.85 × t_S + 3
	from SYNC~ rising edge to ILA sequence(4)	16	0.85 × t_S + 3

(1) Overall latency = latency + t_D.
(2) t_S is the time period of the ADC conversion clock.
(3) Latency is specified for subclass 2. In subclass 0, the SYNC~ falling edge to CGS phase latency is 16 clock cycles in 10x mode and 15 clock cycles in 20x mode.
(4) Latency is specified for subclass 2. In subclass 0, the SYNC~ rising edge to ILA sequence latency is 11 clock cycles in 10x mode and 11 clock cycles in 20x mode.

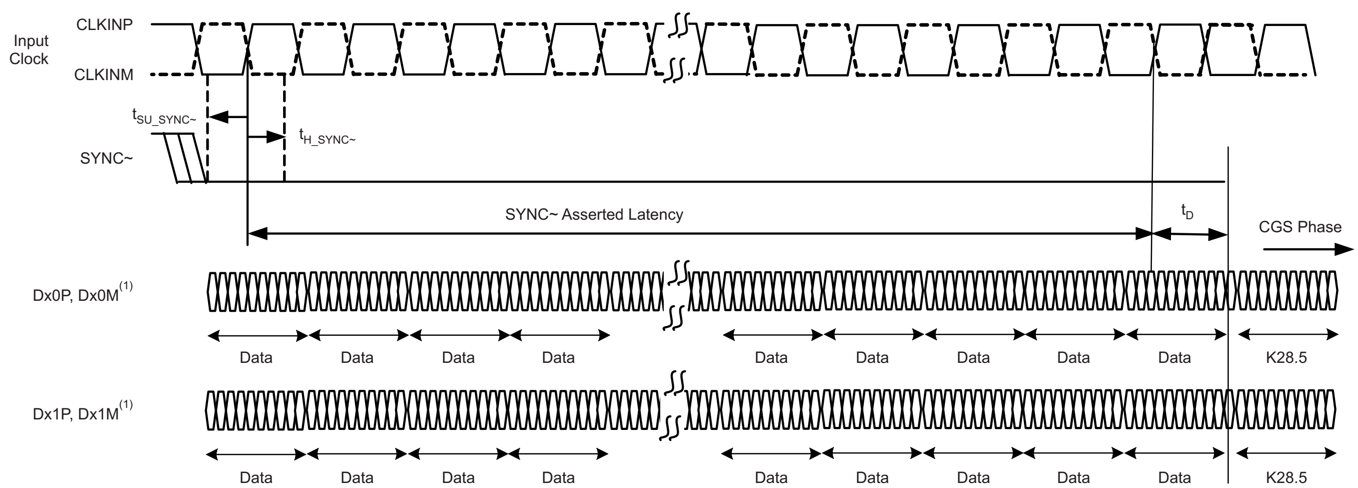
TIMING DIAGRAMS



(1) Overall latency = ADC latency + t_D.

(2) x = A for channel A and B for channel B.

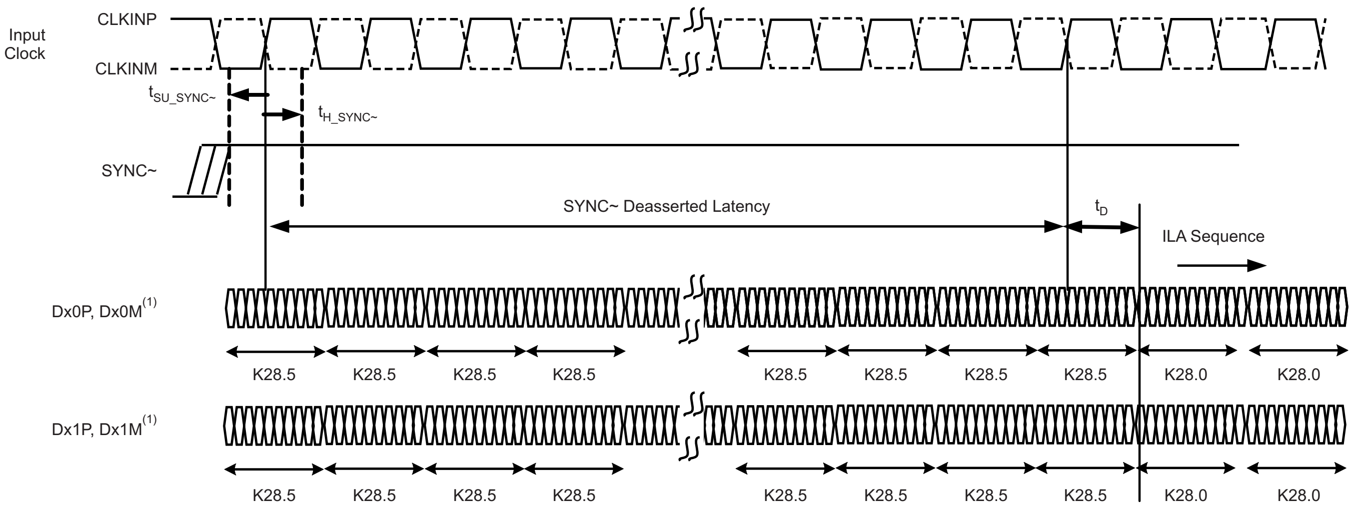
Figure 1. ADC Latency



(1) x = A for channel A and B for channel B.

Figure 2. SYNC~ Latency in CGS Phase (Two-Lane Mode)

TIMING DIAGRAMS (continued)



(1) x = A for channel A and B for channel B.

Figure 3. SYNC~ Latency in ILAS Phase (Two-Lane Mode)

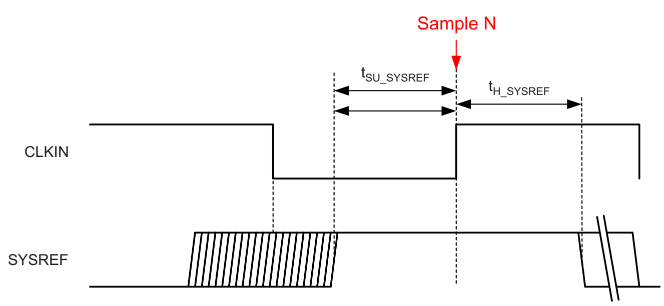


Figure 4. SYSREF Timing (Subclass 1)

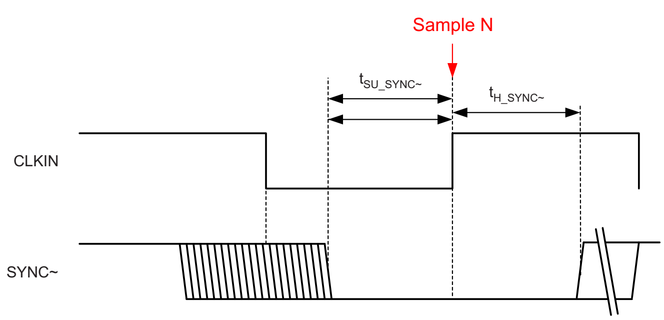


Figure 5. SYNC~ Timing (Subclass 2)

DIGITAL CHARACTERISTICS

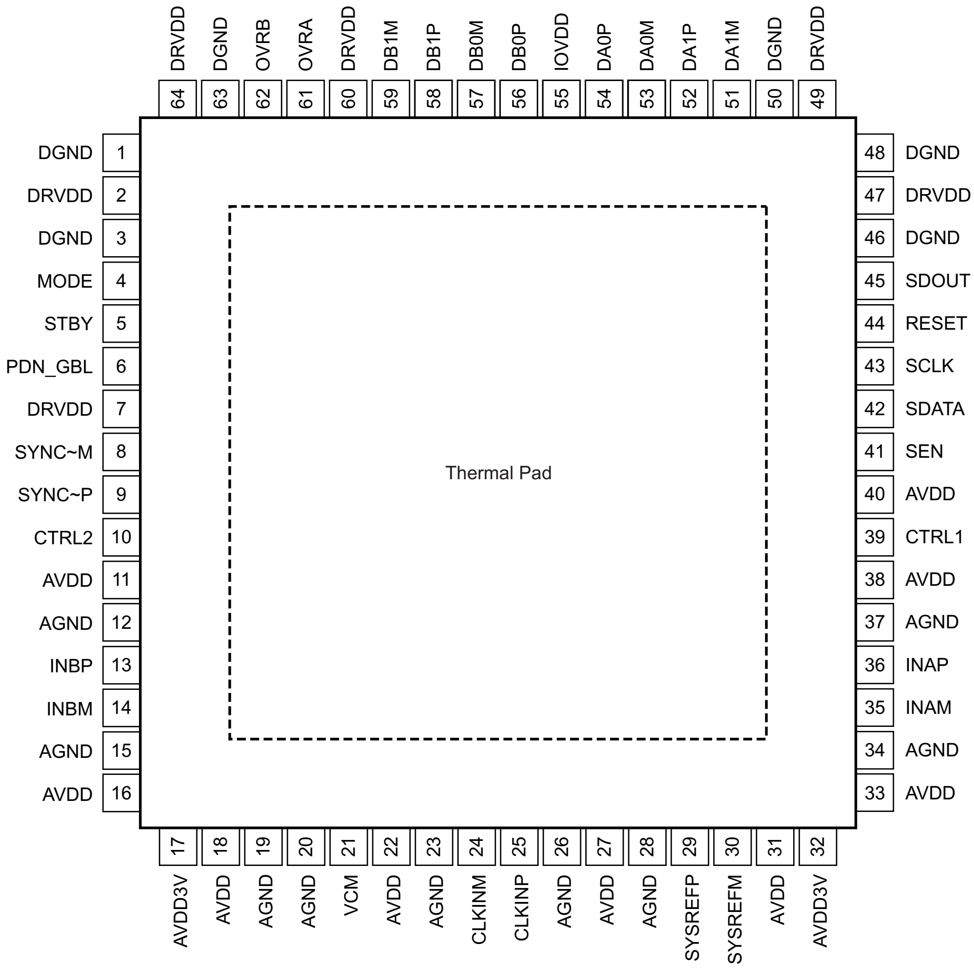
The dc specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level '0' or '1'. AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, and IOVDD = 1.8 V, unless otherwise noted.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (RESET, SCLK, SEN, SDATA, PDN_GBL, STBY, CTRL1, CTRL2, MODE)(1)						
	High-level input voltage	All digital inputs support 1.8-V and 3.3-V logic levels	1.2			V
	Low-level input voltage	All digital inputs support 1.8-V and 3.3-V logic levels			0.4	V
	High-level input current	SEN		0		µA
		RESET, SCLK, SDATA, PDN_GBL, STBY, CTRL1, CTRL2, MODE		10		µA
	Low-level input current	SEN		10		µA
		RESET, SCLK, SDATA, PDN_GBL, STBY, CTRL1, CTRL2, MODE		0		µA
DIGITAL INPUTS (SYNC~P, SYNC~M, SYSREFP, SYSREFM)						
	High-level input voltage			1.3		V
	Low-level input voltage			0.5		V
V_{CM_DIG}	Input common-mode voltage			0.9		V
DIGITAL OUTPUTS (SDOUT, OVRA, OVRB)						
	High-level output voltage		DRVDD – 0.1	DRVDD		V
	Low-level output voltage				0.1	V
DIGITAL OUTPUTS (JESD204B Interface: DA[0,1], DB[0,1])(2)						
	High-level output voltage			IOVDD		V
	Low-level output voltage			IOVDD – 0.4		V
$\|V_{OD}\|$	Output differential voltage			0.4		V
V_{OCM}	Output common-mode voltage			IOVDD – 0.2		V
	Transmitter short-circuit current	Transmitter terminals shorted to any voltage between –0.25 V and 1.45 V	–100		100	mA
	Single-ended output impedance			50		Ω
	Output capacitance	Output capacitance inside the device, from either output to ground		2		pF

(1) RESET, SCLK, SDATA, PDN_GBL, STBY, CTRL1, CTRL2 and MODE pins have 150-kΩ (typical) internal pull-down resistor to ground, while SEN pin has 150-kΩ (typical) pull-up resistor to AVDD.
(2) 50-Ω, single-ended external termination to IOVDD.

PINOUT INFORMATION

RGC PACKAGE
QFN-64
(Top View)



PIN ASSIGNMENTS: JESD204B Output Interface

NAME	PIN NO.	I/O	FUNCTION	DESCRIPTION
AGND	12, 15, 19, 20, 23, 26, 28, 34, 37	I	Supply	Analog ground
AVDD	11, 16, 18, 22, 27, 31, 33, 38, 40	I	Supply	1.8-V analog power supply
AVDD3V	17, 32	I	Supply	3.3-V analog supply for analog buffer
CLKINM	24	I	Clock	Differential ADC clock input
CLKINP	25	I	Clock	Differential ADC clock input
CTRL1	39	I	Control	Power-down control with an internal 150-kΩ pull-down resistor
CTRL2	10	I	Control	Power-down control with an internal 150-kΩ pull-down resistor
DA0P/M	54, 53	O	Interface	JESD204B serial data output for channel A, lane 0
DA1P/M	52,51	O	Interface	JESD204B serial data output for channel A, lane 1
DB0P/M	56,57	O	Interface	JESD204B serial data output for channel B, lane 0
DB1P/M	58,59	O	Interface	JESD204B serial data output for channel B, lane 1
DGND	1, 3, 46, 48, 50, 63	I	Supply	Digital ground
DRVDD	2, 7, 47, 49, 60, 64	I	Supply	Digital 1.8-V power supply
INAM	35	I	Input	Differential analog input for channel A
INAP	36	I	Input	Differential analog input for channel A
INBM	14	I	Input	Differential analog input for channel B
INBP	13	I	Input	Differential analog input for channel B
IOVDD	55	I	Supply	Digital 1.8-V power supply for the JESD204B transmitter
MODE	4	I	Control	Connect to GND
OVRA	61	O	Interface	Overrange indication channel A in CMOS output format.
OVRB	62	O	Interface	Overrange indication channel B in CMOS output format.
PDN_GBL	6	I	Control	Global power down. Active high with an internal 150-kΩ pull-down resistor.
RESET	44	I	Control	Hardware reset; active high. This pin has an internal 150-kΩ pull-down resistor.
SCLK	43	I	Control	Serial interface clock input. This pin has an internal 150-kΩ pull-down resistor.
SDATA	42	I	Control	Serial interface data input. This pin has an internal 150-kΩ pull-down resistor.
SDOUT	45	O	Control	Serial interface data output
SEN	41	I	Control	Serial interface enable. This pin has an internal 150-kΩ pull-up resistor.
STBY	5	I	Control	Standby. Active high with an internal 150-kΩ pull-down resistor.
SYNC~P	9	I	Interface	Synchronization input for JESD204B port
SYNC~M	8	I	Interface	Synchronization input for JESD204B port
SYSREFM	30	I	Clock	External SYSREF input (subclass 1)
SYSREFP	29	I	Clock	External SYSREF input (subclass 1)
VCM	21	O	Output	1.9-V common-mode output voltage for analog inputs
Thermal Pad	65	GND	Ground	Connect to ground plane

TYPICAL CHARACTERISTICS: ADS42JB69

Typical values are at T_A = +25°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

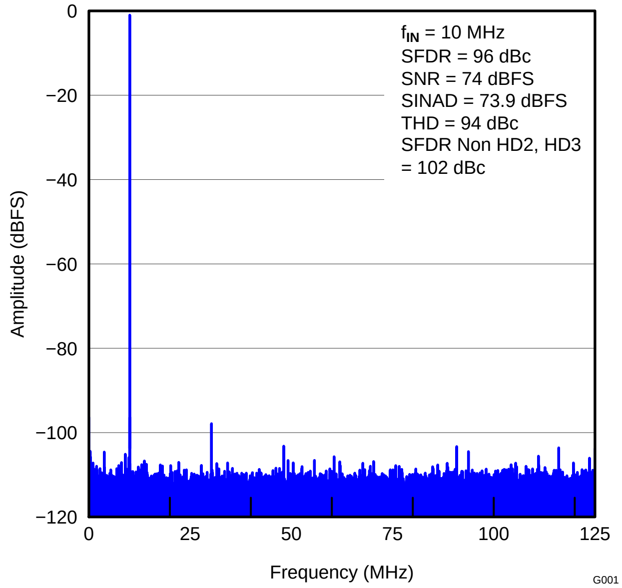


Figure 6. FFT FOR 10-MHz INPUT SIGNAL

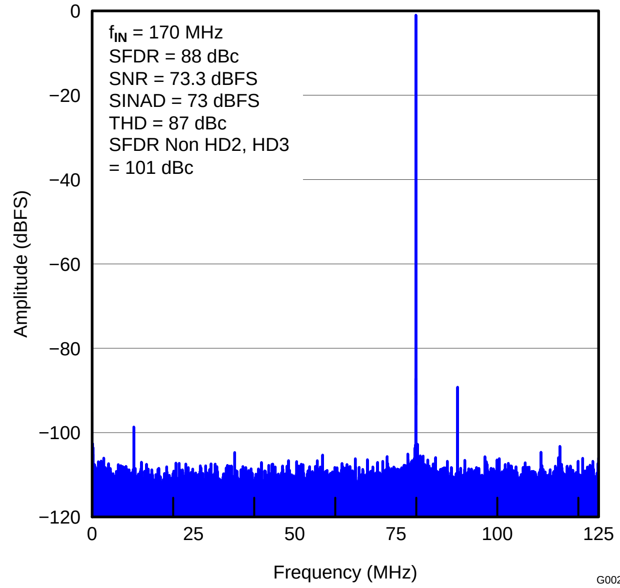


Figure 7. FFT FOR 170-MHz INPUT SIGNAL

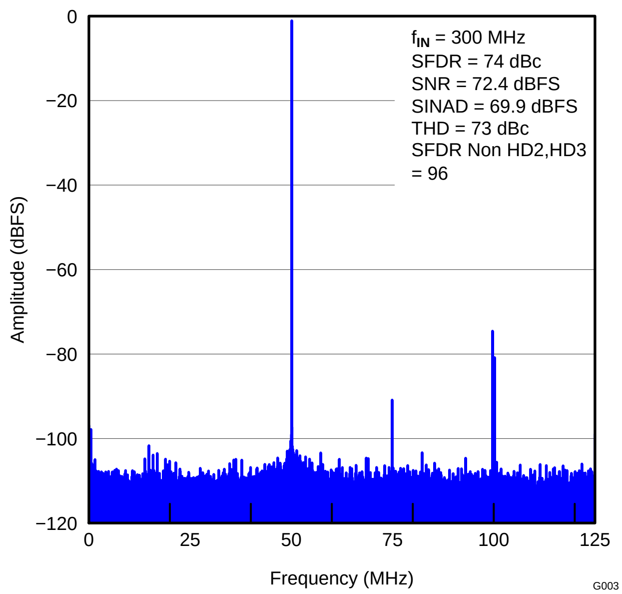


Figure 8. FFT FOR 300-MHz INPUT SIGNAL

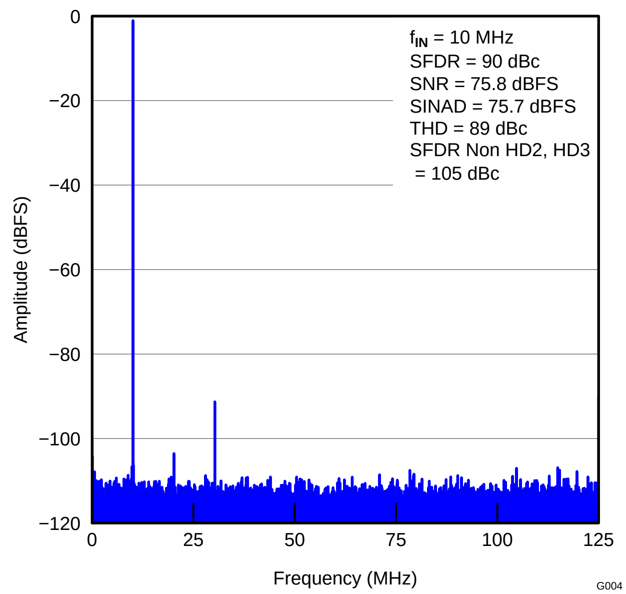


Figure 9. FFT FOR 10-MHz INPUT SIGNAL (2.5-V_{PP} Full-Scale)

TYPICAL CHARACTERISTICS: ADS42JB69 (continued)

Typical values are at T_A = +25°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

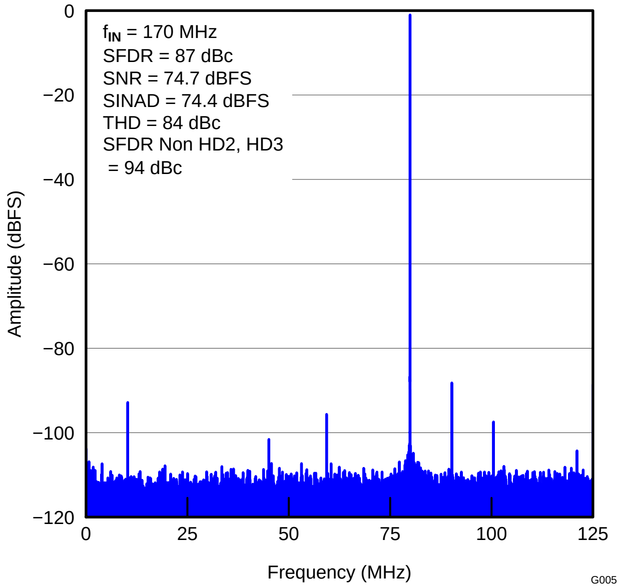


Figure 10. FFT FOR 170-MHz INPUT SIGNAL (2.5-V_{PP} Full-Scale)

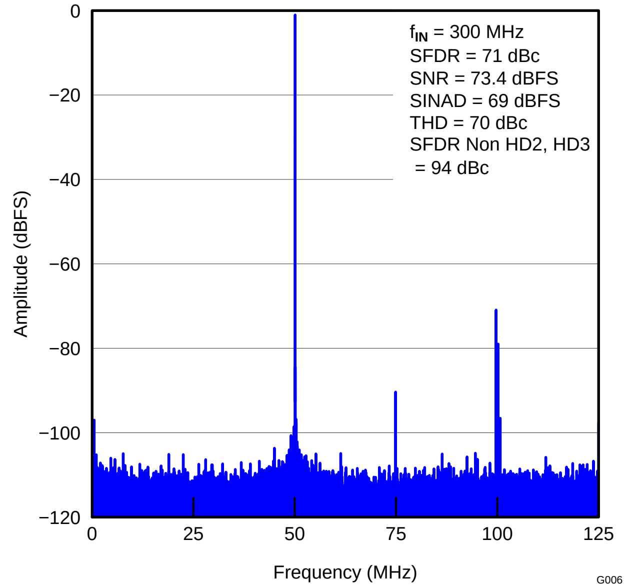


Figure 11. FFT FOR 300-MHz INPUT SIGNAL (2.5-V_{PP} Full-Scale)

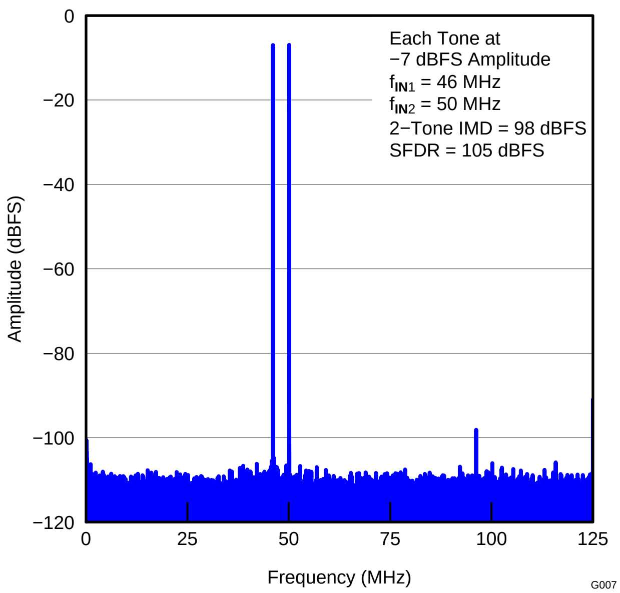


Figure 12. FFT FOR TWO-TONE INPUT SIGNAL (–7 dBFS at 46 MHz and 50 MHz)

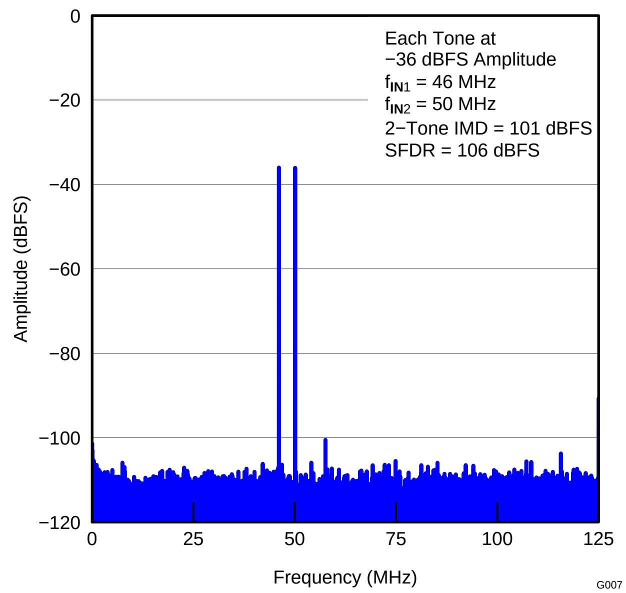


Figure 13. FFT FOR TWO-TONE INPUT SIGNAL (–36 dBFS at 46 MHz and 50 MHz)

TYPICAL CHARACTERISTICS: ADS42JB69 (continued)

Typical values are at T_A = +25°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

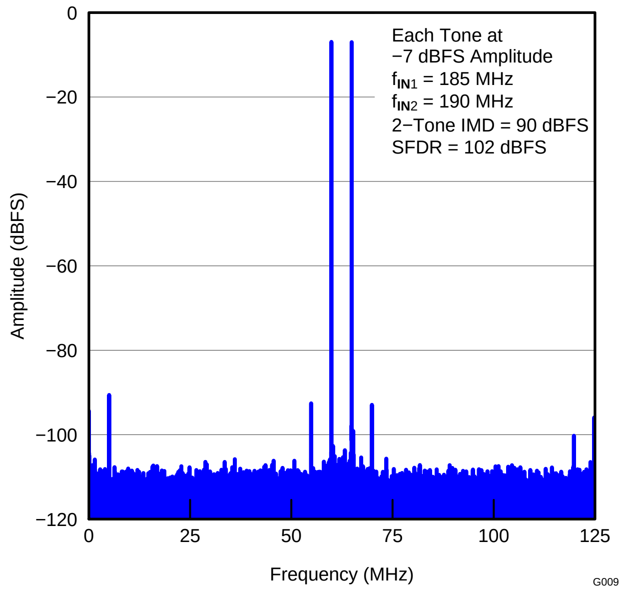


Figure 14. FFT FOR TWO-TONE INPUT SIGNAL (–7 dBFS at 185 MHz and 190 MHz)

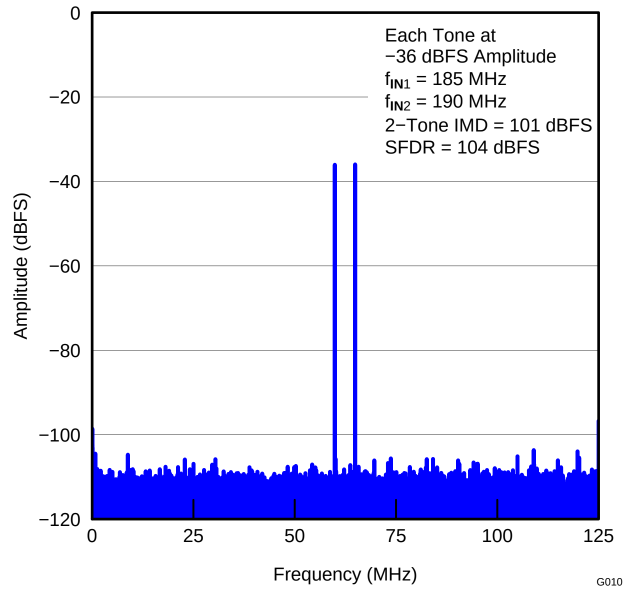


Figure 15. FFT FOR TWO-TONE INPUT SIGNAL (–36 dBFS at 185 MHz and 190 MHz)

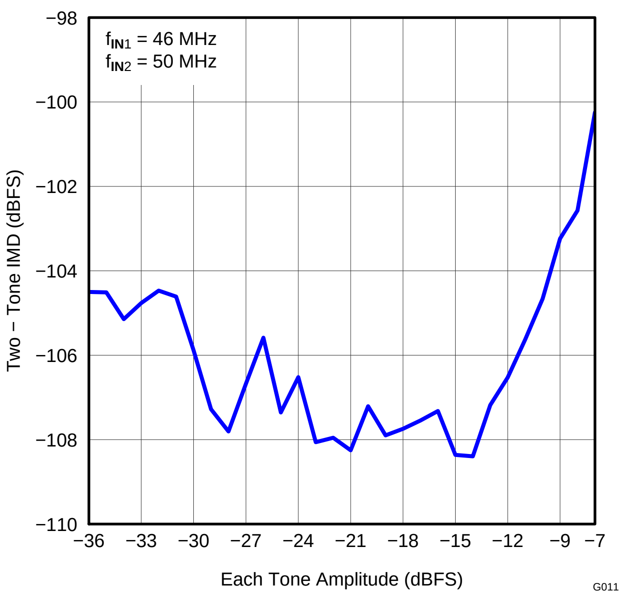


Figure 16. INTERMODULATION DISTORTION vs INPUT AMPLITUDE (46 MHz and 50 MHz)

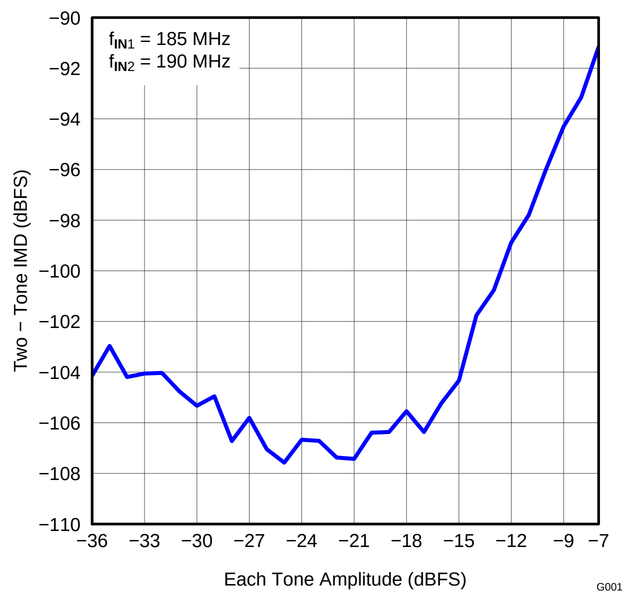


Figure 17. INTERMODULATION DISTORTION vs INPUT AMPLITUDE (185 MHz and 190 MHz)

TYPICAL CHARACTERISTICS: ADS42JB69 (continued)

Typical values are at T_A = +25°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

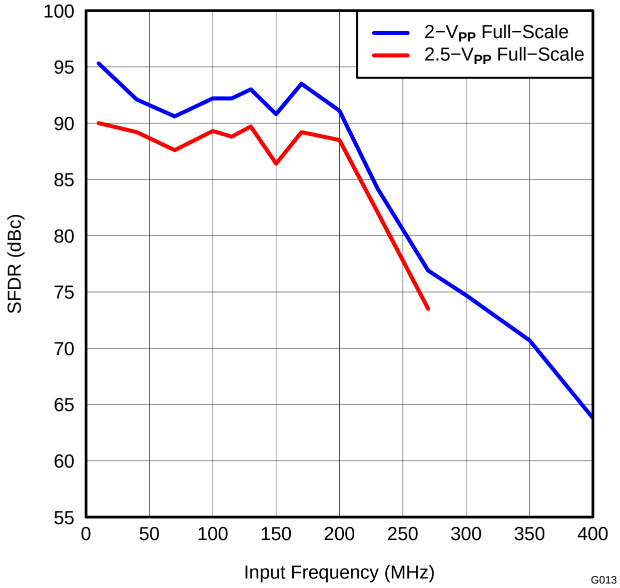


Figure 18. SPURIOUS-FREE DYNAMIC RANGE vs INPUT FREQUENCY

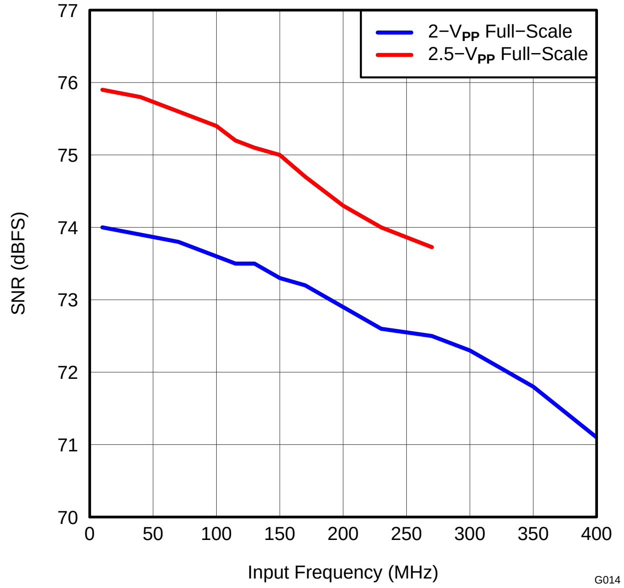


Figure 19. SIGNAL-TO-NOISE RATIO vs INPUT FREQUENCY

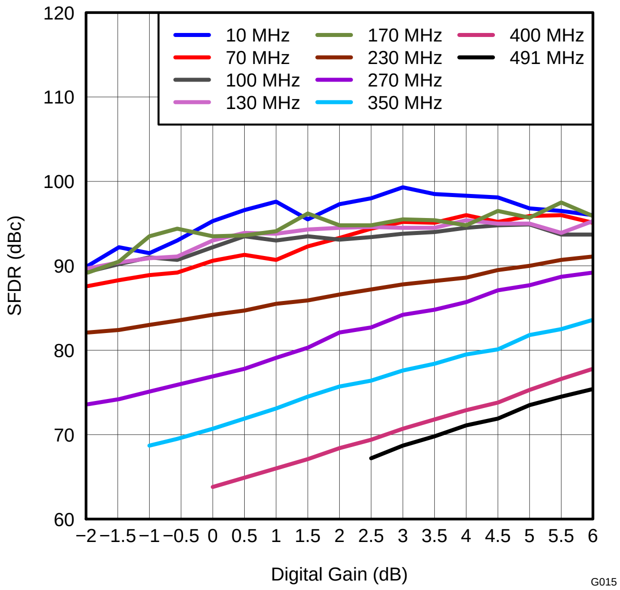


Figure 20. SPURIOUS-FREE DYNAMIC RANGE vs DIGITAL GAIN

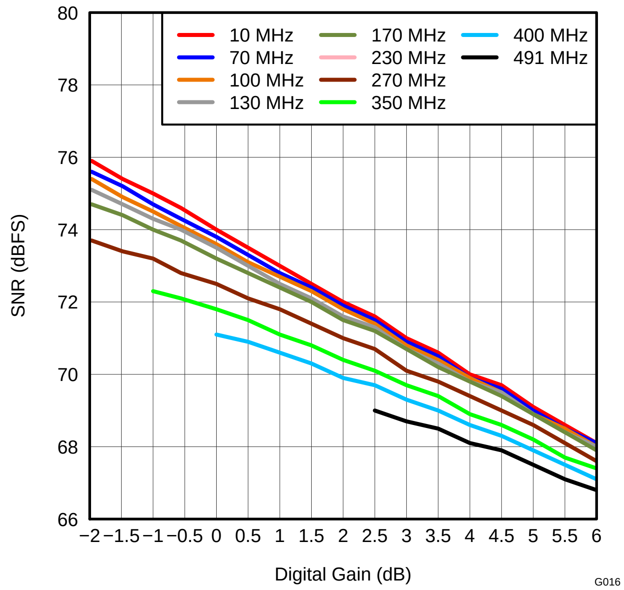


Figure 21. SIGNAL-TO-NOISE RATIO vs DIGITAL GAIN

TYPICAL CHARACTERISTICS: ADS42JB69 (continued)

Typical values are at T_A = +25°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

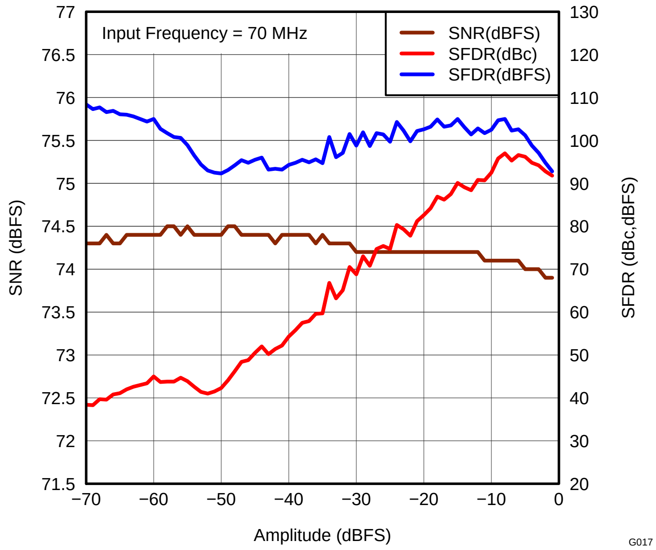


Figure 22. PERFORMANCE vs INPUT AMPLITUDE (70 MHz)

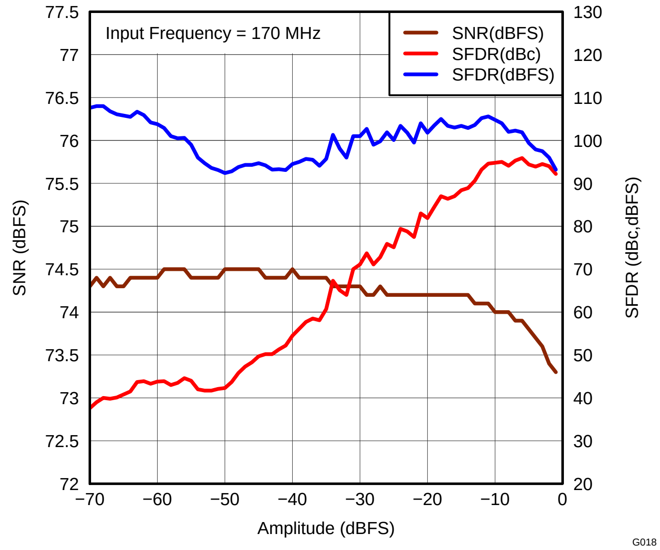


Figure 23. PERFORMANCE vs INPUT AMPLITUDE (170 MHz)

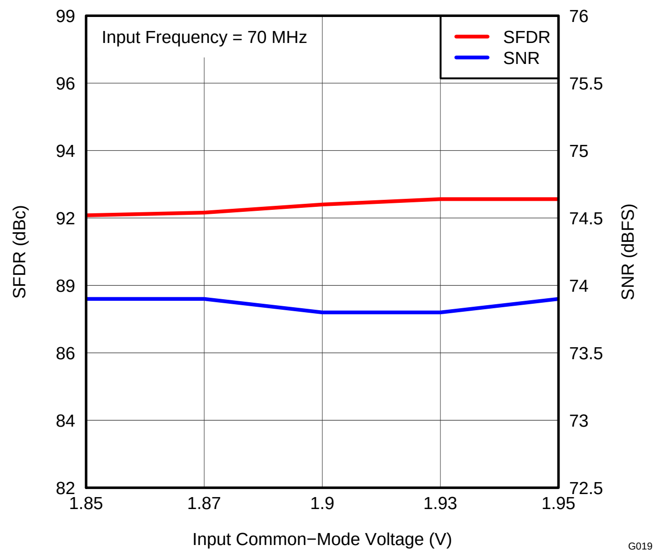


Figure 24. PERFORMANCE vs INPUT COMMON-MODE VOLTAGE (70 MHz)

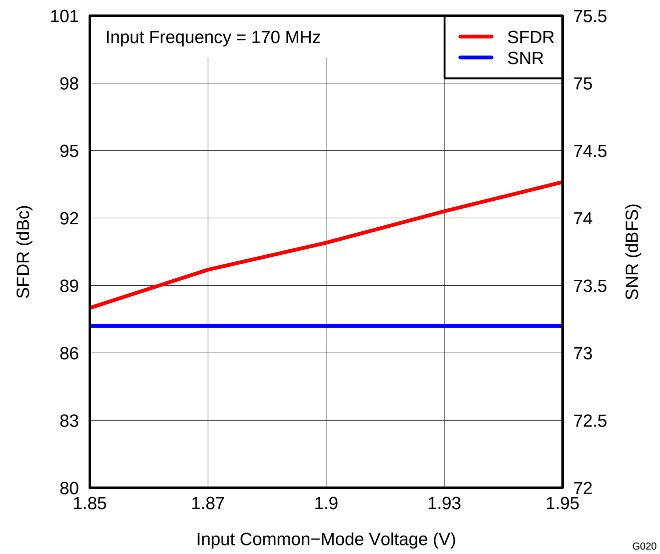


Figure 25. PERFORMANCE vs INPUT COMMON-MODE VOLTAGE (170 MHz)

TYPICAL CHARACTERISTICS: ADS42JB69 (continued)

Typical values are at T_A = +25°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

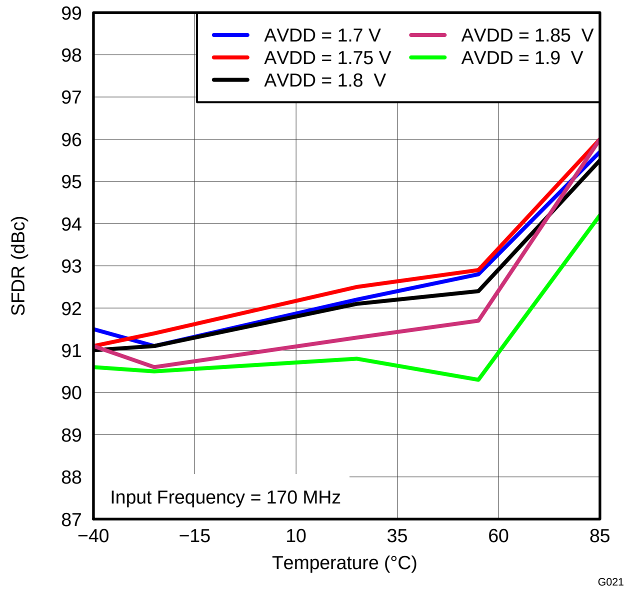


Figure 26. SPURIOUS-FREE DYNAMIC RANGE vs AVDD SUPPLY AND TEMPERATURE (170 MHz)

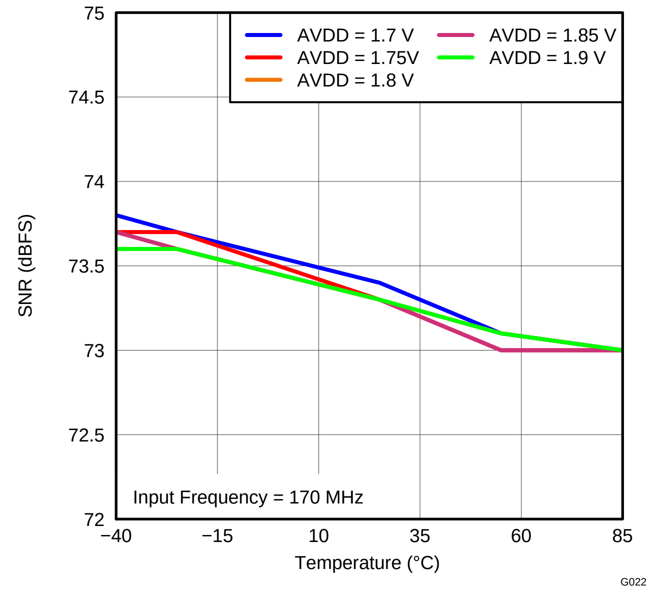


Figure 27. SIGNAL-TO-NOISE RATIO vs AVDD SUPPLY AND TEMPERATURE (170 MHz)

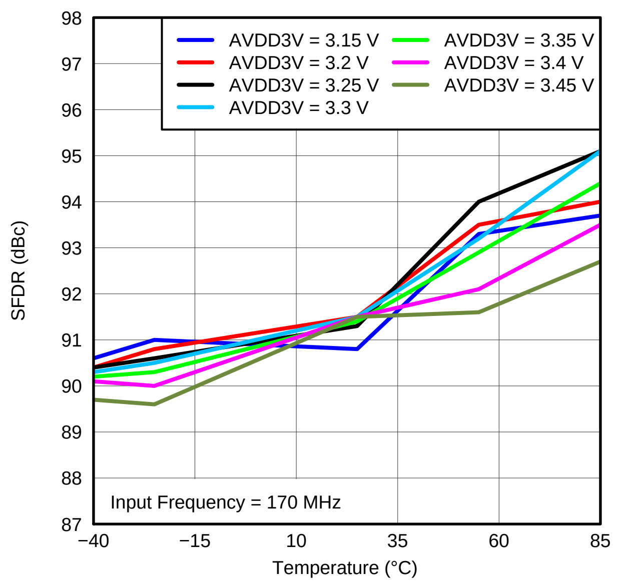


Figure 28. SPURIOUS-FREE DYNAMIC RANGE vs AVDD_BUF SUPPLY AND TEMPERATURE (170 MHz)

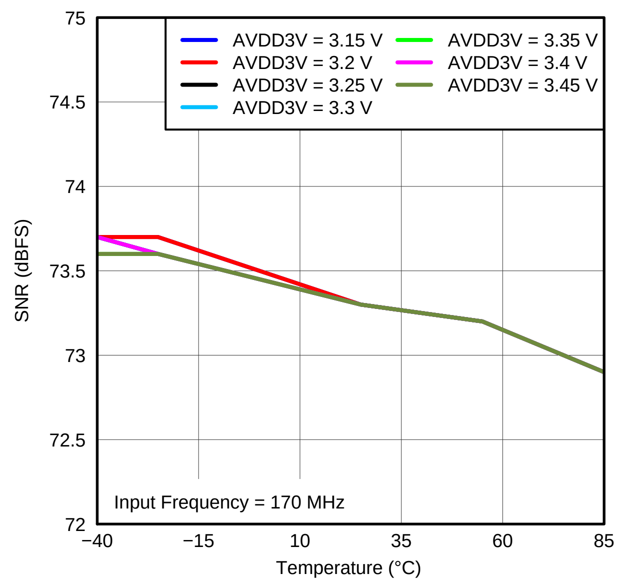


Figure 29. SIGNAL-TO-NOISE RATIO vs AVDD_BUF SUPPLY AND TEMPERATURE (170 MHz)

TYPICAL CHARACTERISTICS: ADS42JB69 (continued)

Typical values are at T_A = +25°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

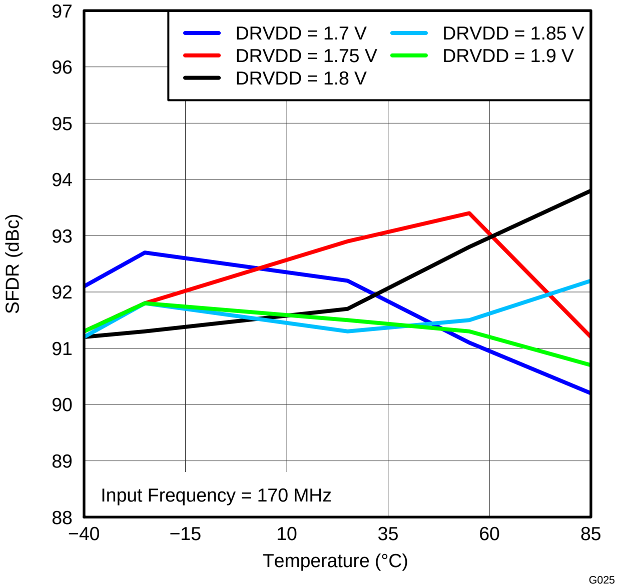


Figure 30. SPURIOUS-FREE DYNAMIC RANGE vs DRVDD SUPPLY AND TEMPERATURE (170 MHz)

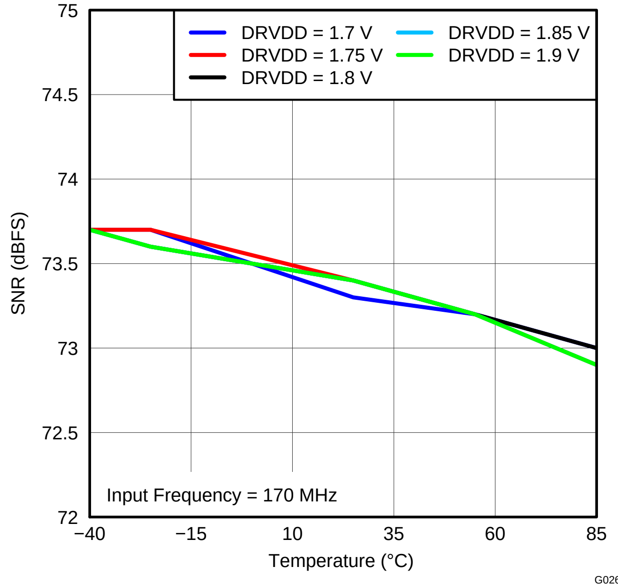


Figure 31. SIGNAL-TO-NOISE RATIO vs DRVDD SUPPLY AND TEMPERATURE (170 MHz)

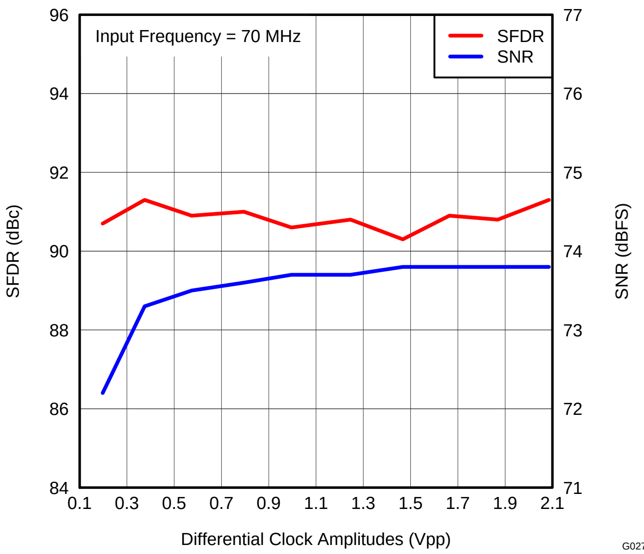


Figure 32. PERFORMANCE vs CLOCK AMPLITUDE (70 MHz)

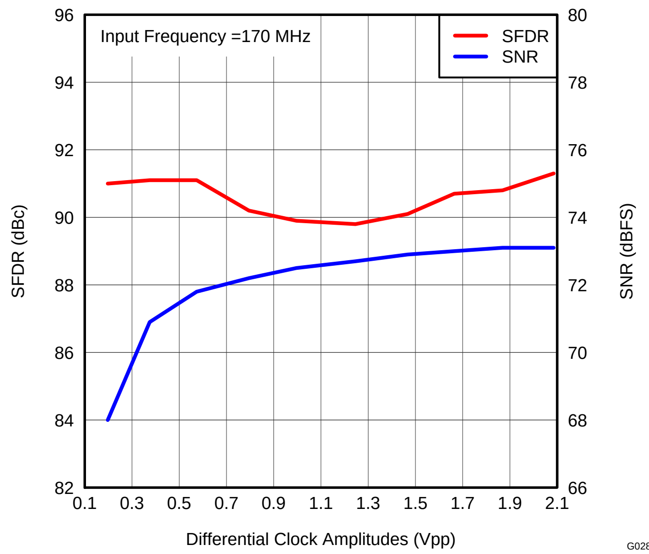


Figure 33. PERFORMANCE vs CLOCK AMPLITUDE (170 MHz)

TYPICAL CHARACTERISTICS: ADS42JB69 (continued)

Typical values are at T_A = +25°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

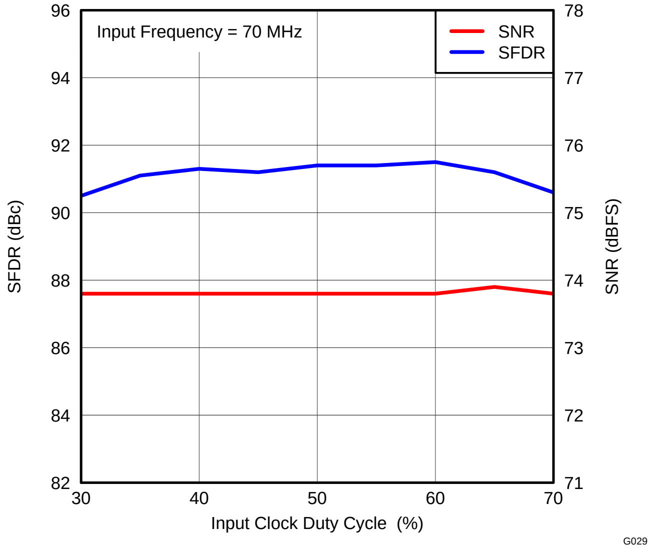


Figure 34. PERFORMANCE vs CLOCK DUTY CYCLE (70 MHz)

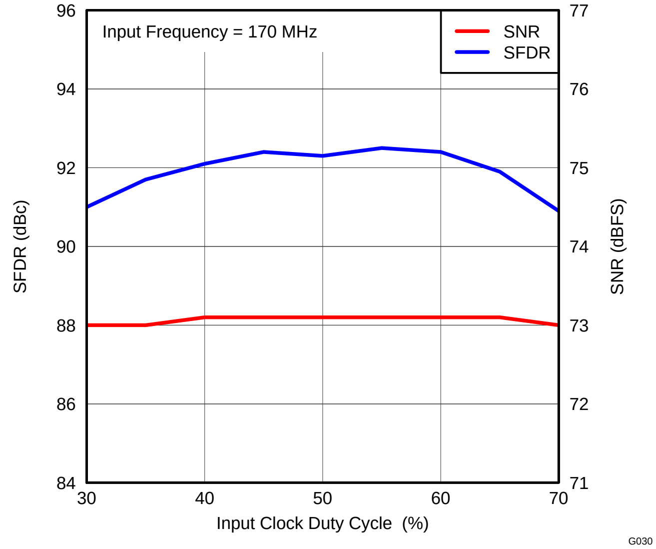


Figure 35. PERFORMANCE vs CLOCK DUTY CYCLE (170 MHz)

TYPICAL CHARACTERISTICS: ADS42JB49

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

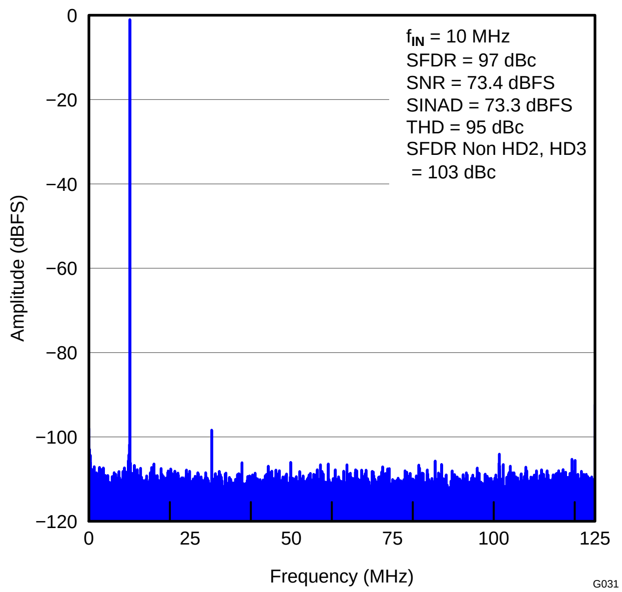


Figure 36. FFT FOR 10-MHz INPUT SIGNAL

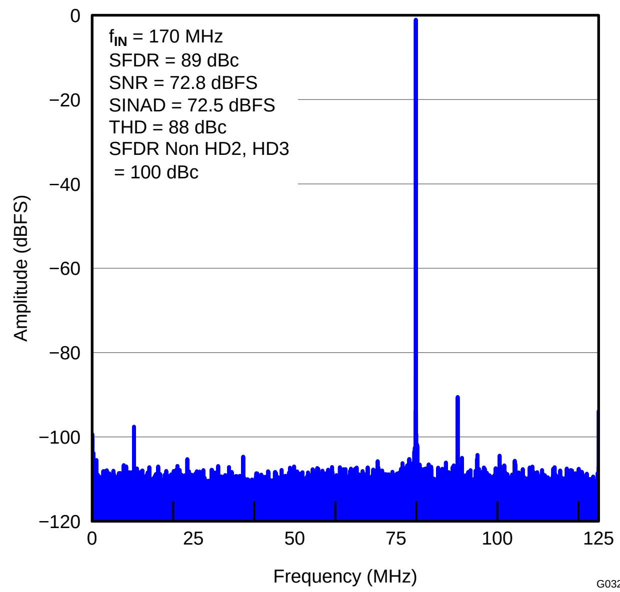


Figure 37. FFT FOR 170-MHz INPUT SIGNAL

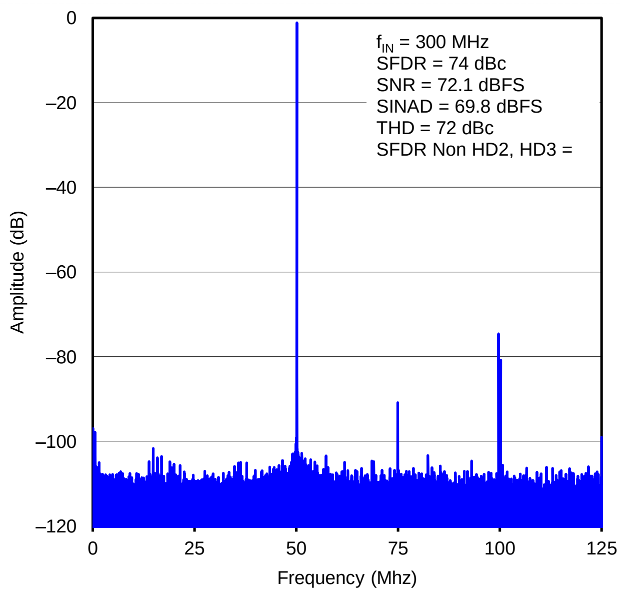


Figure 38. FFT FOR 300-MHz INPUT SIGNAL

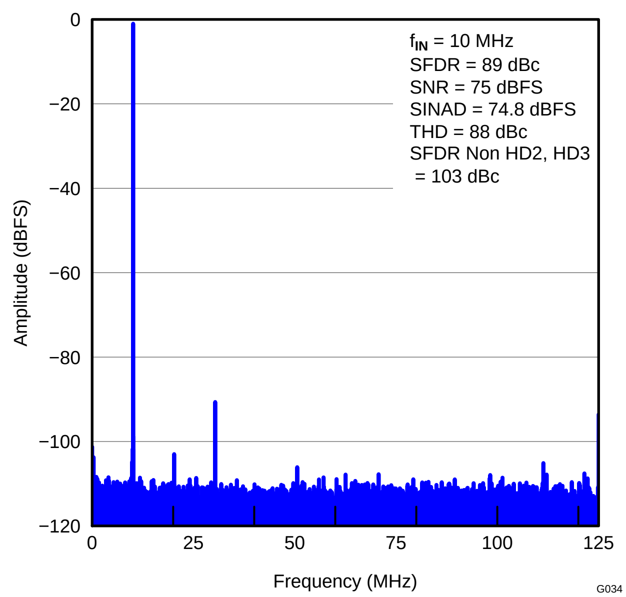


Figure 39. FFT FOR 10-MHz INPUT SIGNAL (2.5-V_{PP} Full-Scale)

TYPICAL CHARACTERISTICS: ADS42JB49 (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

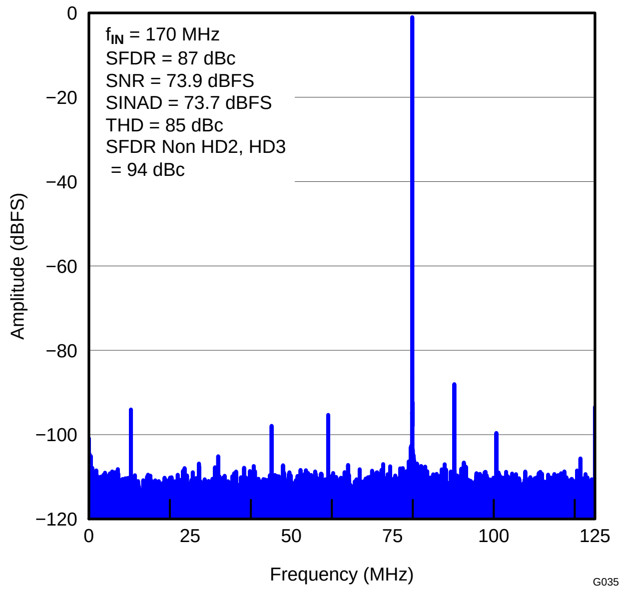


Figure 40. FFT FOR 170-MHz INPUT SIGNAL (2.5-V_{PP} Full-Scale)

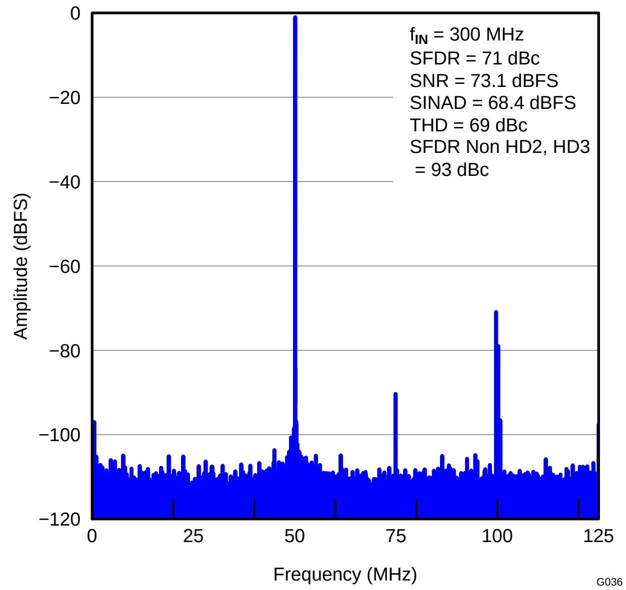


Figure 41. FFT FOR 300-MHz INPUT SIGNAL (2.5-V_{PP} Full-Scale)

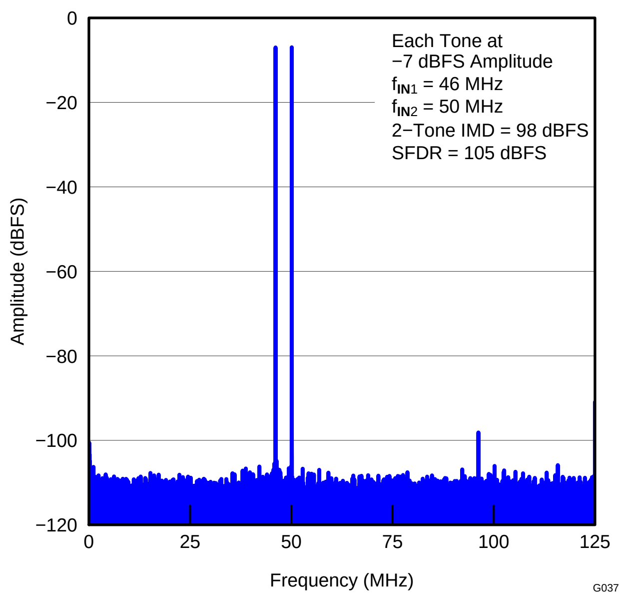


Figure 42. FFT FOR TWO-TONE INPUT SIGNAL (–7 dBFS at 46 MHz and 50 MHz)

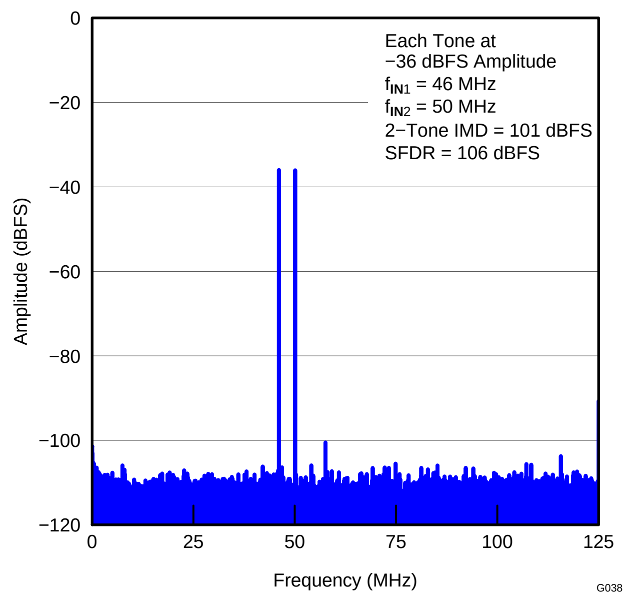


Figure 43. FFT FOR TWO-TONE INPUT SIGNAL (–36 dBFS at 46 MHz and 50 MHz)

TYPICAL CHARACTERISTICS: ADS42JB49 (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

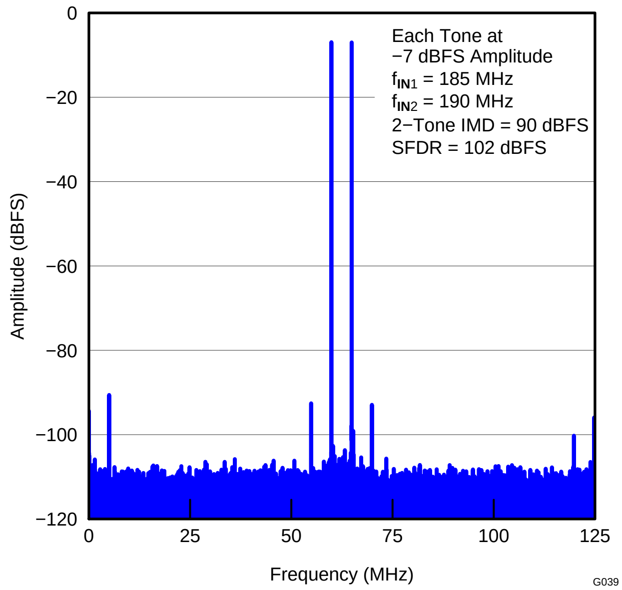


Figure 44. FFT FOR TWO-TONE INPUT SIGNAL (–7 dBFS at 185 MHz and 190 MHz)

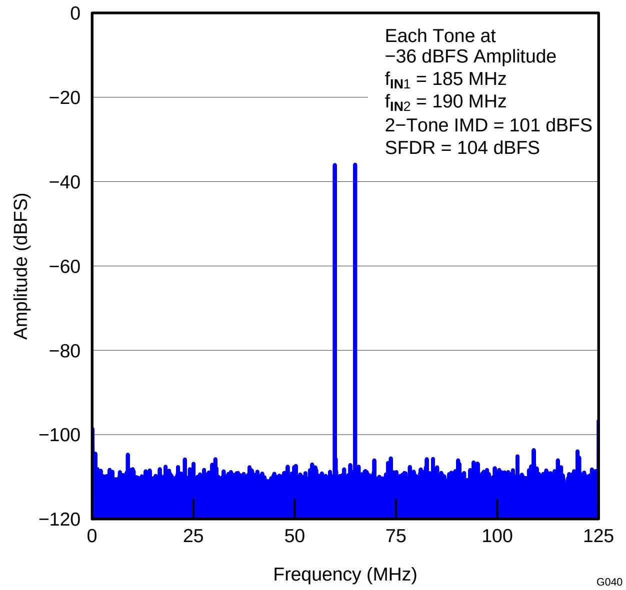


Figure 45. FFT FOR TWO-TONE INPUT SIGNAL (–36 dBFS at 185 MHz and 190 MHz)

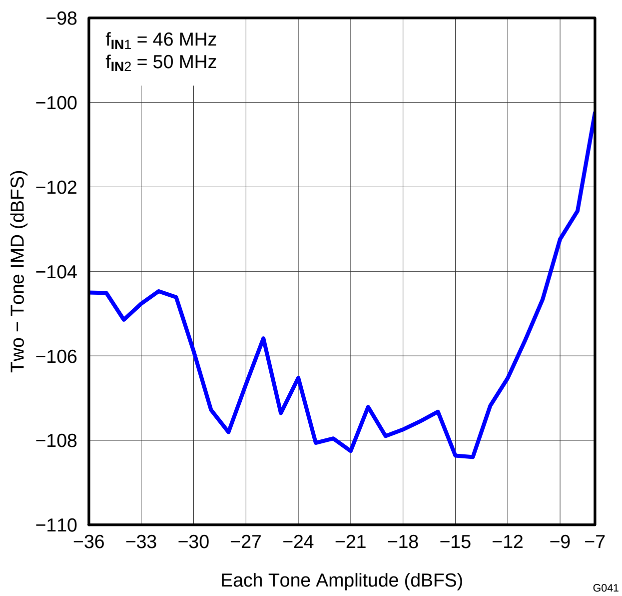


Figure 46. INTERMODULATION DISTORTION vs INPUT AMPLITUDE (46 MHz and 50 MHz)

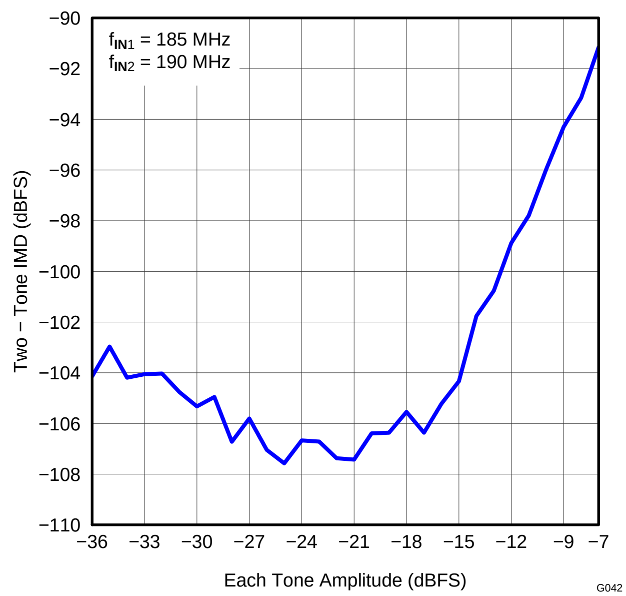


Figure 47. INTERMODULATION DISTORTION vs INPUT AMPLITUDE (185 MHz and 190 MHz)

TYPICAL CHARACTERISTICS: ADS42JB49 (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

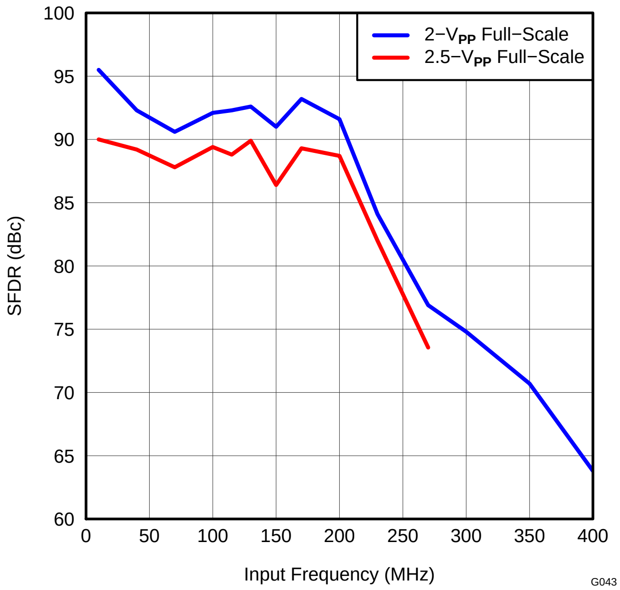


Figure 48. SPURIOUS-FREE DYNAMIC RANGE vs INPUT FREQUENCY

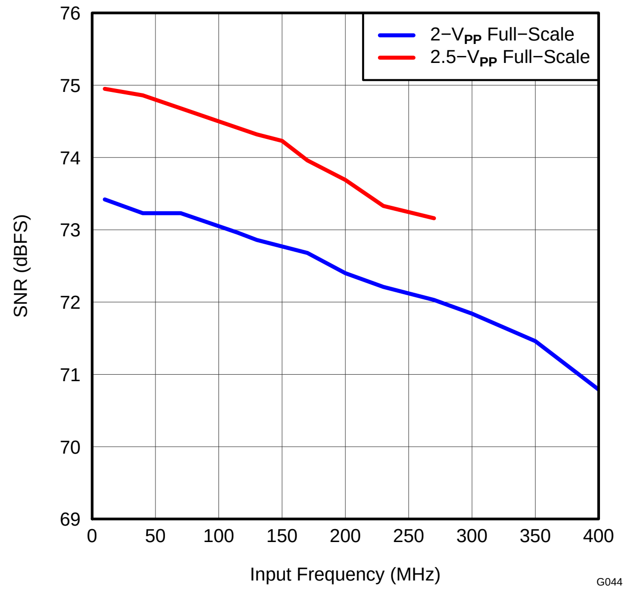


Figure 49. SIGNAL-TO-NOISE RATIO vs INPUT FREQUENCY

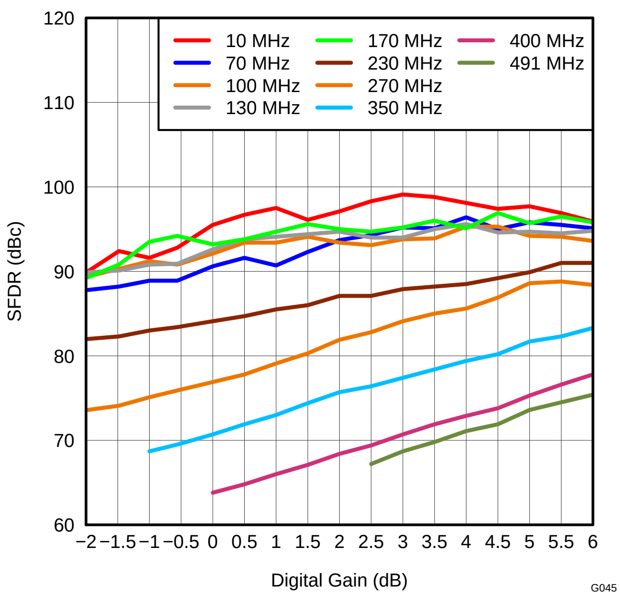


Figure 50. SPURIOUS-FREE DYNAMIC RANGE vs DIGITAL GAIN

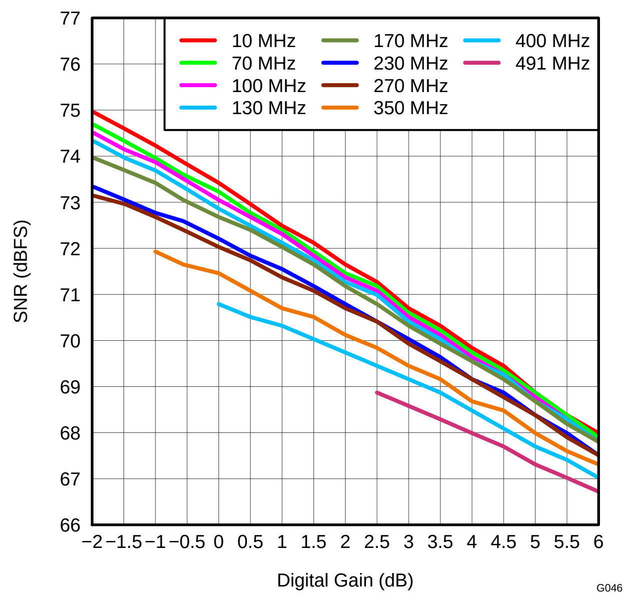


Figure 51. SIGNAL-TO-NOISE RATIO vs DIGITAL GAIN

TYPICAL CHARACTERISTICS: ADS42JB49 (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

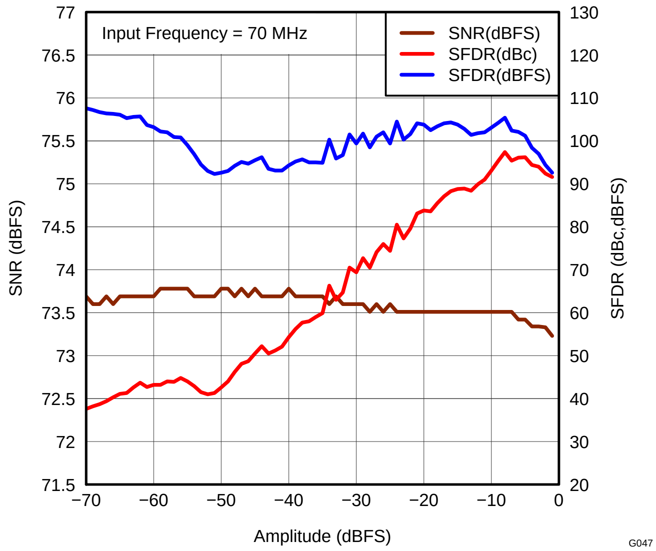


Figure 52. PERFORMANCE vs INPUT AMPLITUDE (70 MHz)

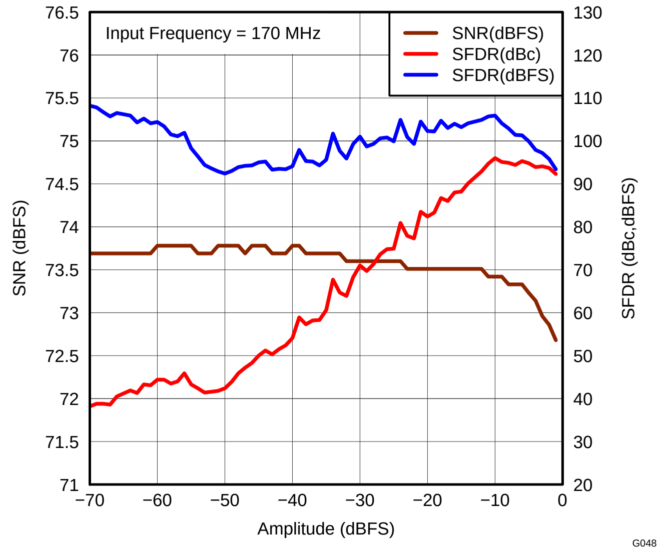


Figure 53. PERFORMANCE vs INPUT AMPLITUDE (170 MHz)

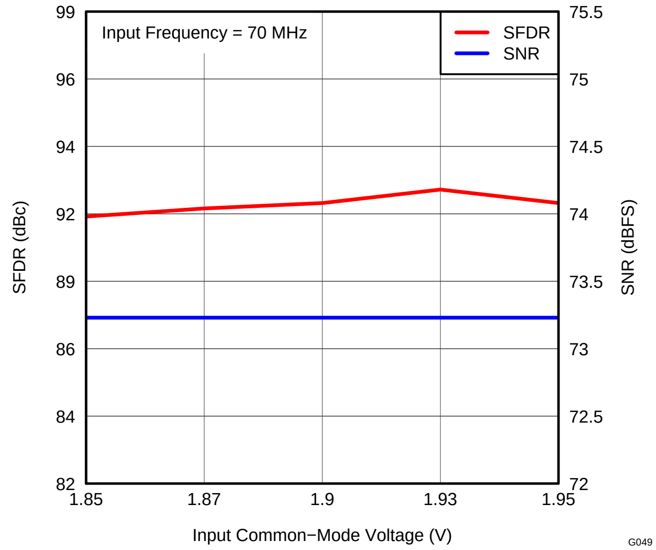


Figure 54. PERFORMANCE vs INPUT COMMON-MODE VOLTAGE (70 MHz)

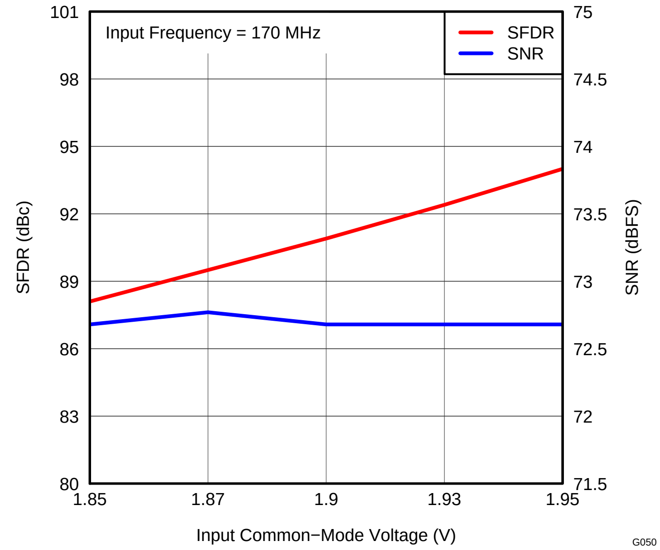


Figure 55. PERFORMANCE vs INPUT COMMON-MODE VOLTAGE (170 MHz)

TYPICAL CHARACTERISTICS: ADS42JB49 (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

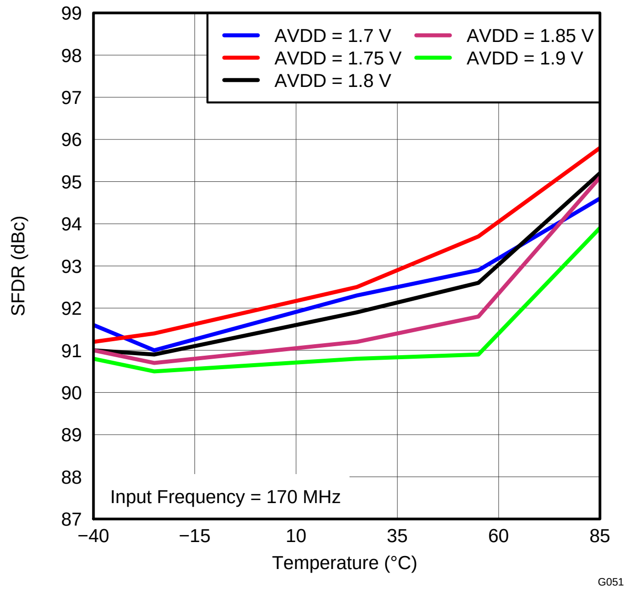


Figure 56. SPURIOUS-FREE DYNAMIC RANGE vs AVDD SUPPLY AND TEMPERATURE (170 MHz)

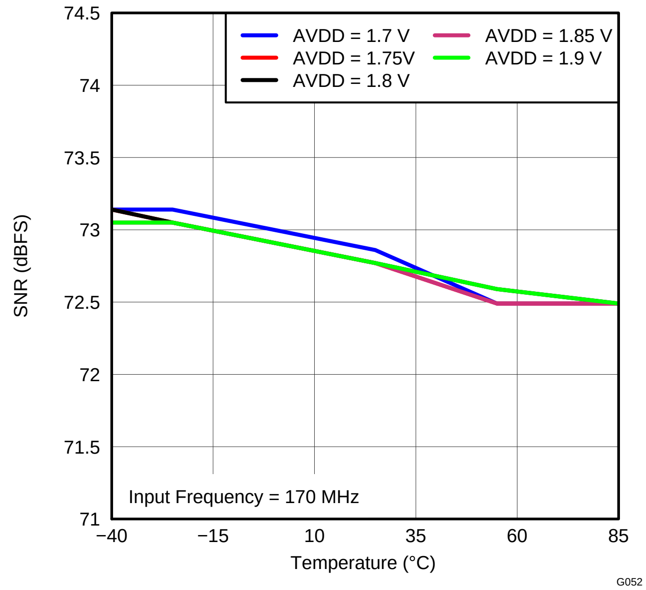


Figure 57. SIGNAL-TO-NOISE RATIO vs AVDD SUPPLY AND TEMPERATURE (170 MHz)

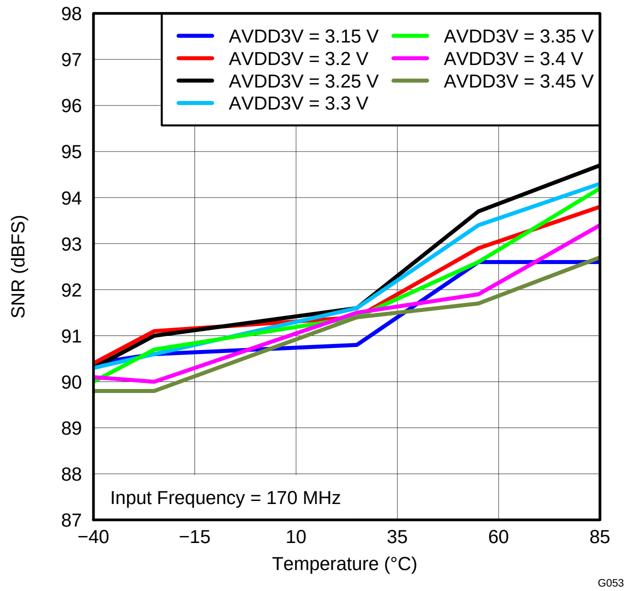


Figure 58. SPURIOUS-FREE DYNAMIC RANGE vs AVDD_BUF SUPPLY AND TEMPERATURE (170 MHz)

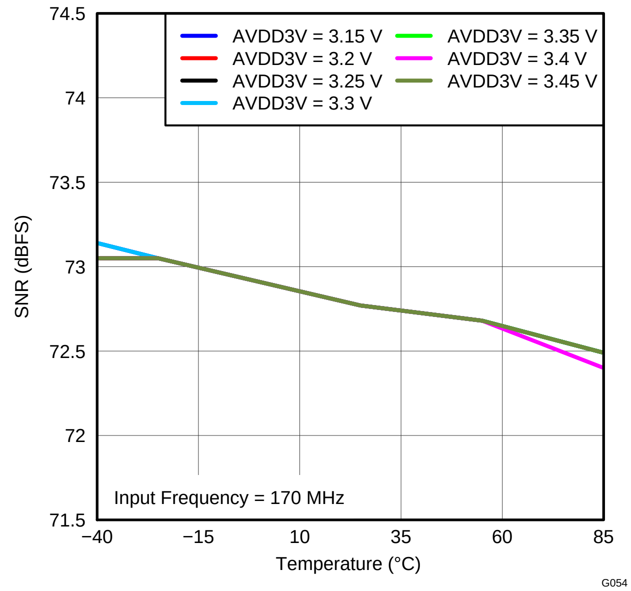


Figure 59. SIGNAL-TO-NOISE RATIO vs AVDD_BUF SUPPLY AND TEMPERATURE (170 MHz)

TYPICAL CHARACTERISTICS: ADS42JB49 (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

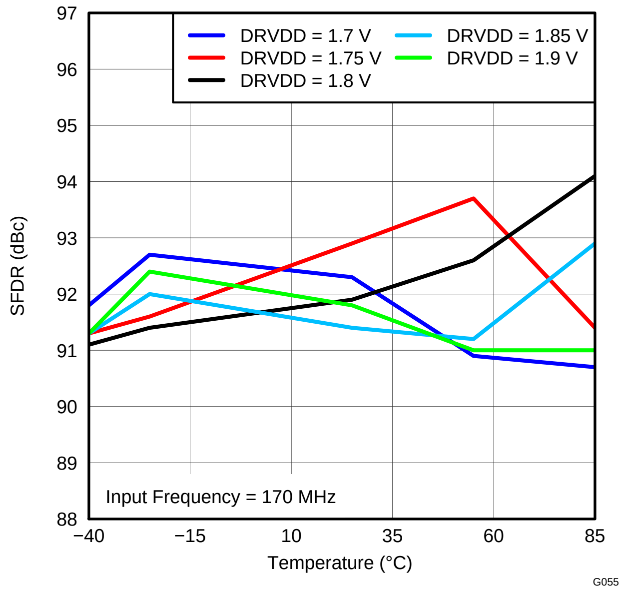


Figure 60. SPURIOUS-FREE DYNAMIC RANGE vs DRVDD SUPPLY AND TEMPERATURE (170 MHz)

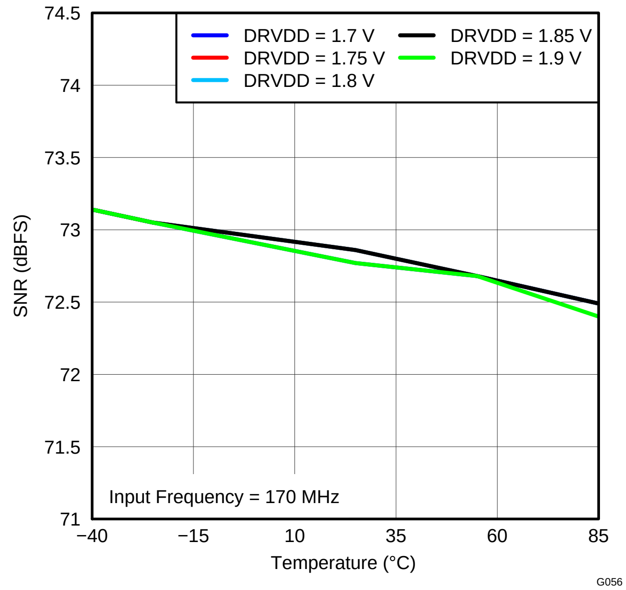


Figure 61. SIGNAL-TO-NOISE RATIO vs DRVDD SUPPLY AND TEMPERATURE (170 MHz)

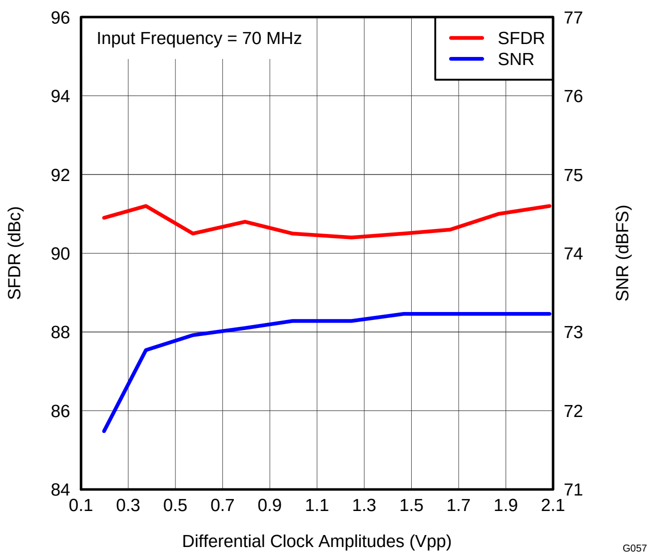


Figure 62. PERFORMANCE vs CLOCK AMPLITUDE (70 MHz)

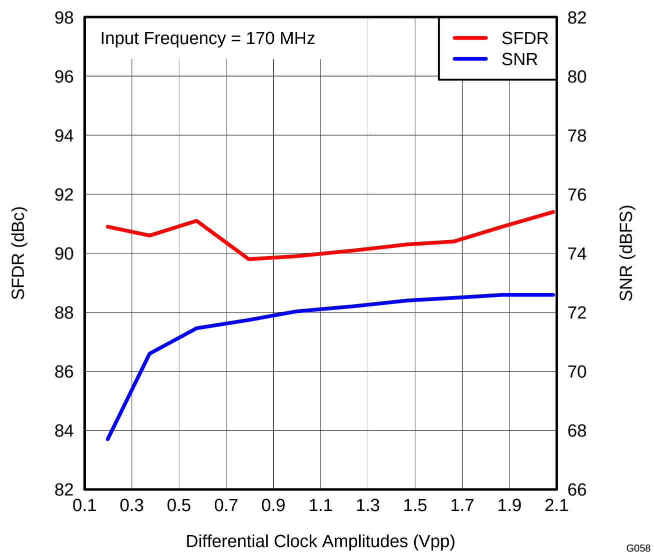


Figure 63. PERFORMANCE vs CLOCK AMPLITUDE (170 MHz)

TYPICAL CHARACTERISTICS: ADS42JB49 (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

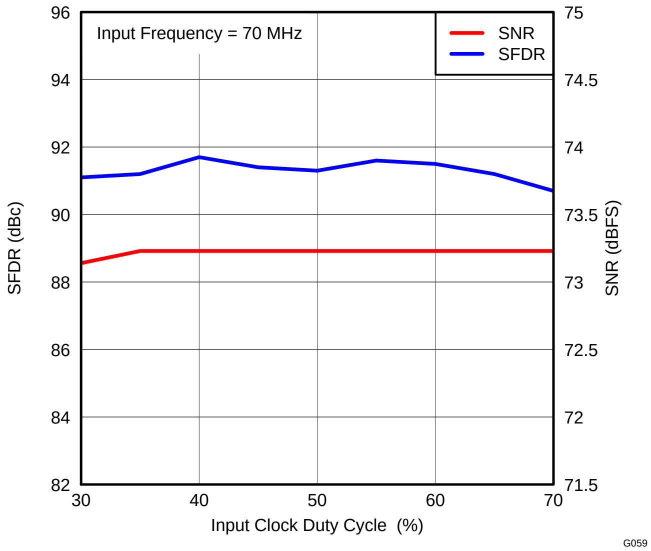


Figure 64. PERFORMANCE vs CLOCK DUTY CYCLE (70 MHz)

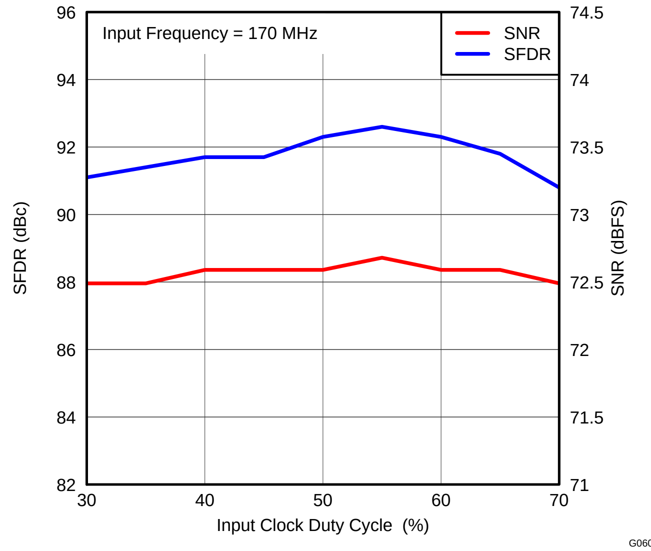


Figure 65. PERFORMANCE vs CLOCK DUTY CYCLE (170 MHz)

TYPICAL CHARACTERISTICS: COMMON

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 64k-point FFT, unless otherwise noted.

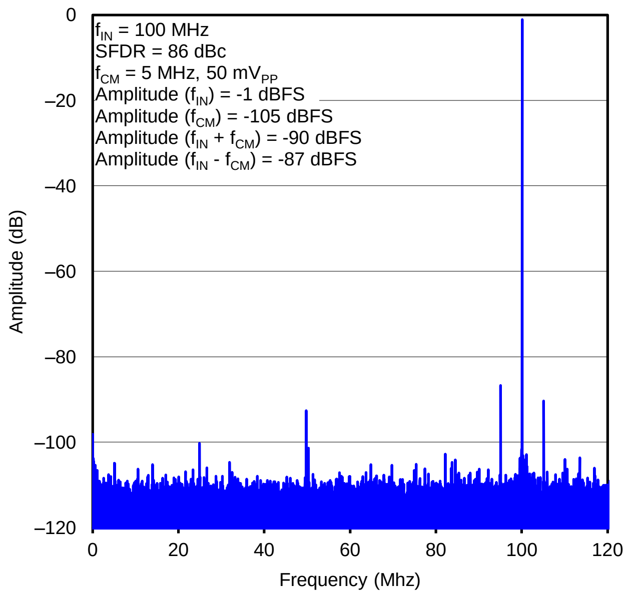


Figure 66. COMMON-MODE REJECTION RATIO FFT

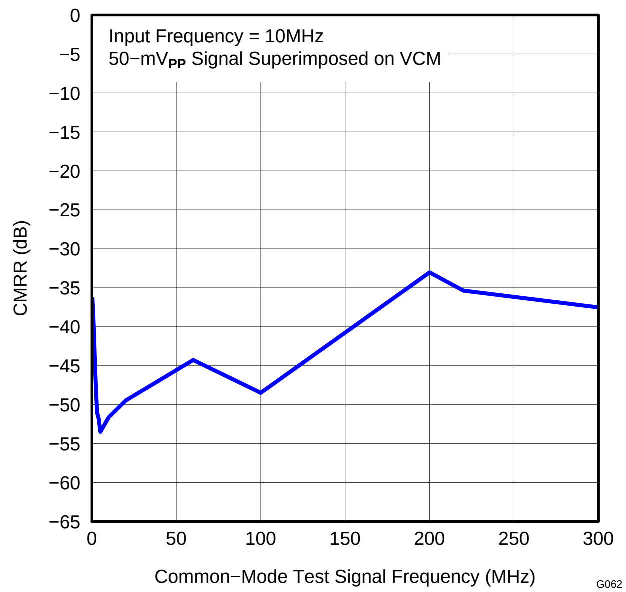


Figure 67. COMMON-MODE REJECTION RATIO vs TEST SIGNAL FREQUENCY

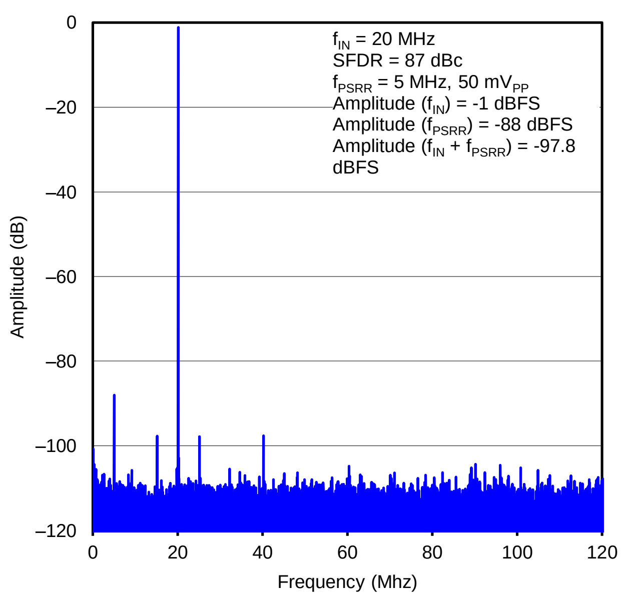


Figure 68. POWER-SUPPLY REJECTION RATIO FFT FOR AVDD SUPPLY

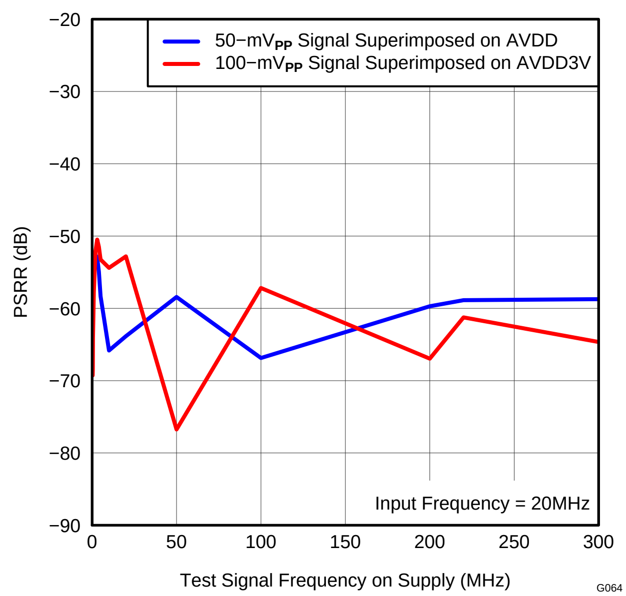


Figure 69. POWER-SUPPLY REJECTION RATIO vs TEST SIGNAL FREQUENCY

TYPICAL CHARACTERISTICS: COMMON (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 64k-point FFT, unless otherwise noted.

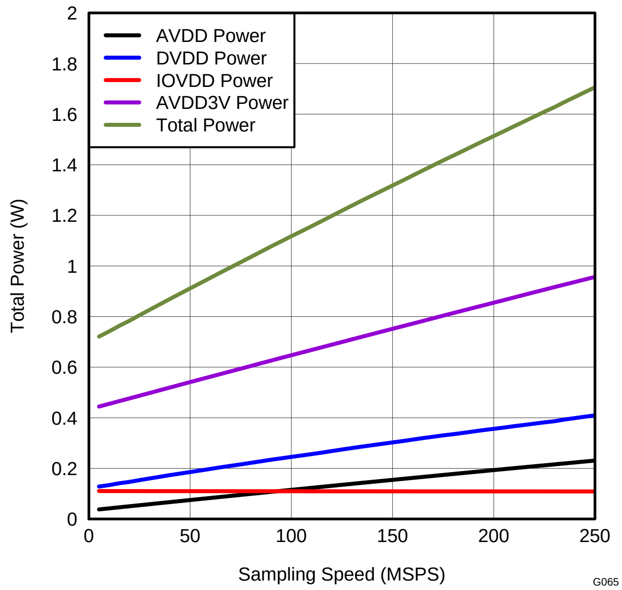


Figure 70. TOTAL POWER vs SAMPLING FREQUENCY

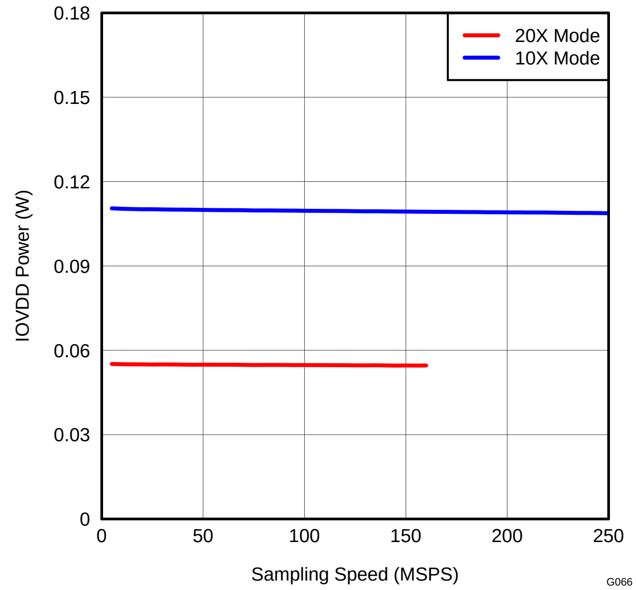


Figure 71. IOVDD POWER vs SAMPLING FREQUENCY

TYPICAL CHARACTERISTICS: CONTOUR

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 64k-point FFT, unless otherwise noted.

Spurious-Free Dynamic Range (SFDR): General

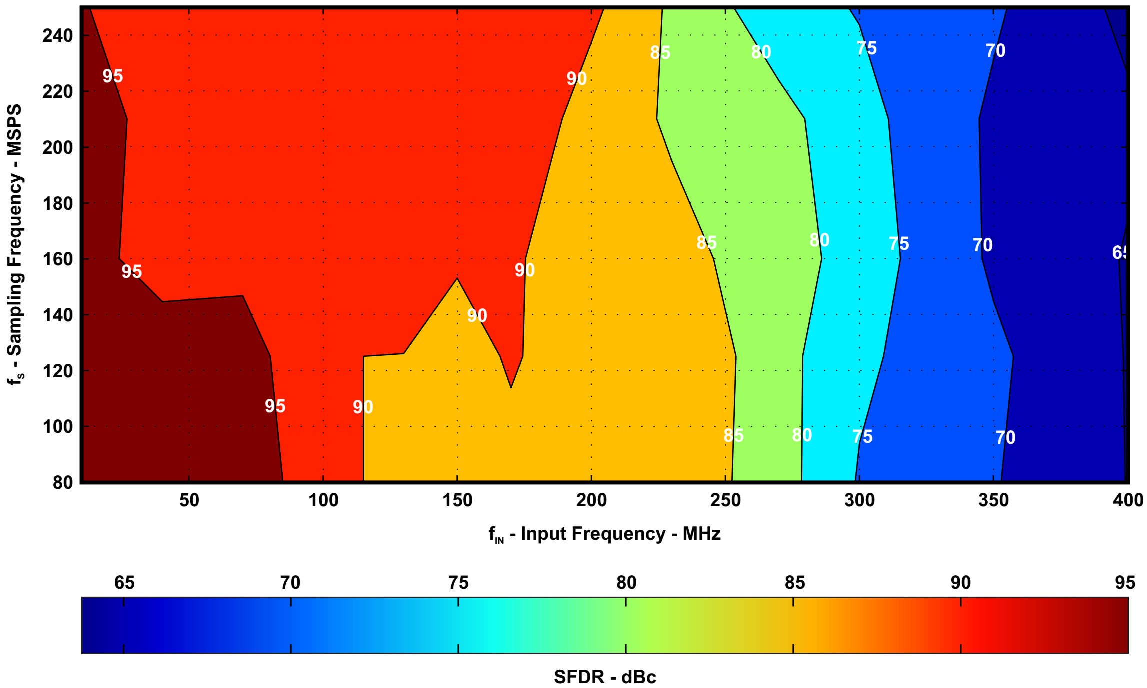


Figure 72. 0-dB GAIN (SFDR)

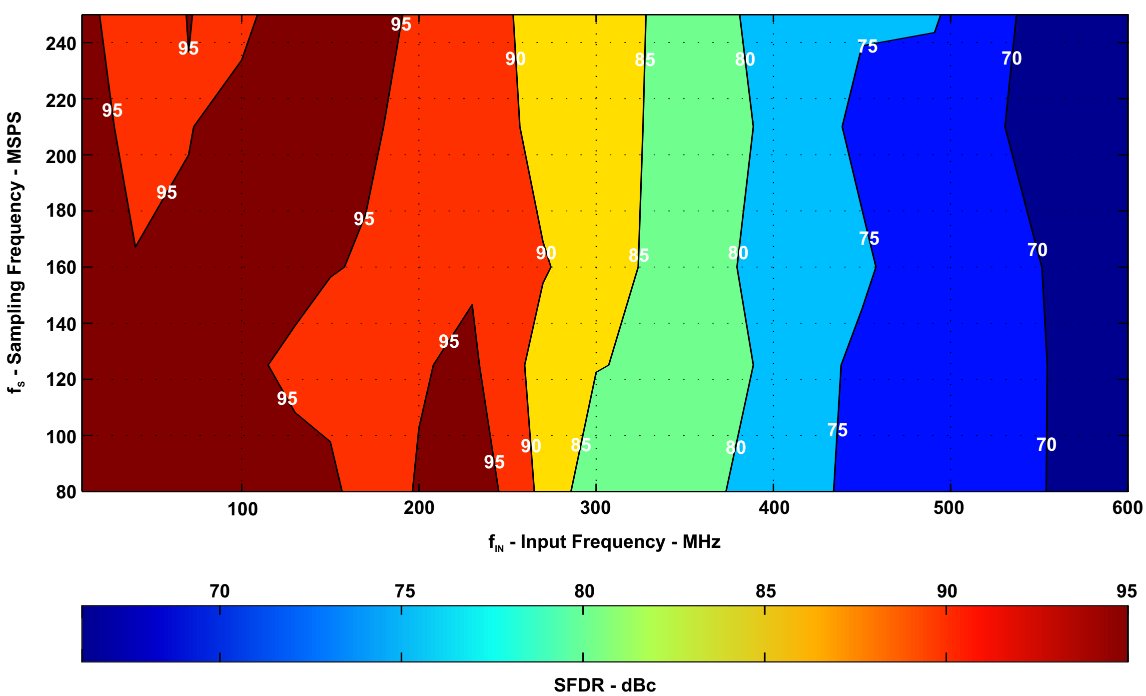


Figure 73. 6-dB GAIN (SFDR)

TYPICAL CHARACTERISTICS: CONTOUR (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 64k-point FFT, unless otherwise noted.

Signal-to-Noise Ratio (SNR): ADS42JB69

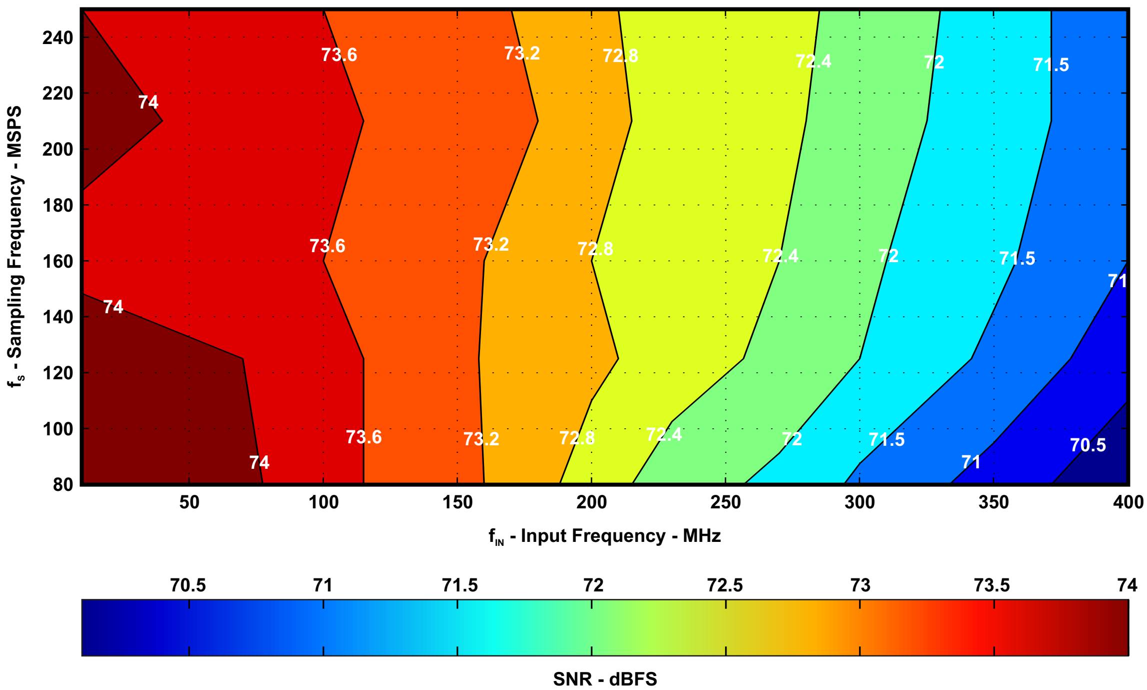


Figure 74. 0-dB GAIN (SNR, ADS42JB69)

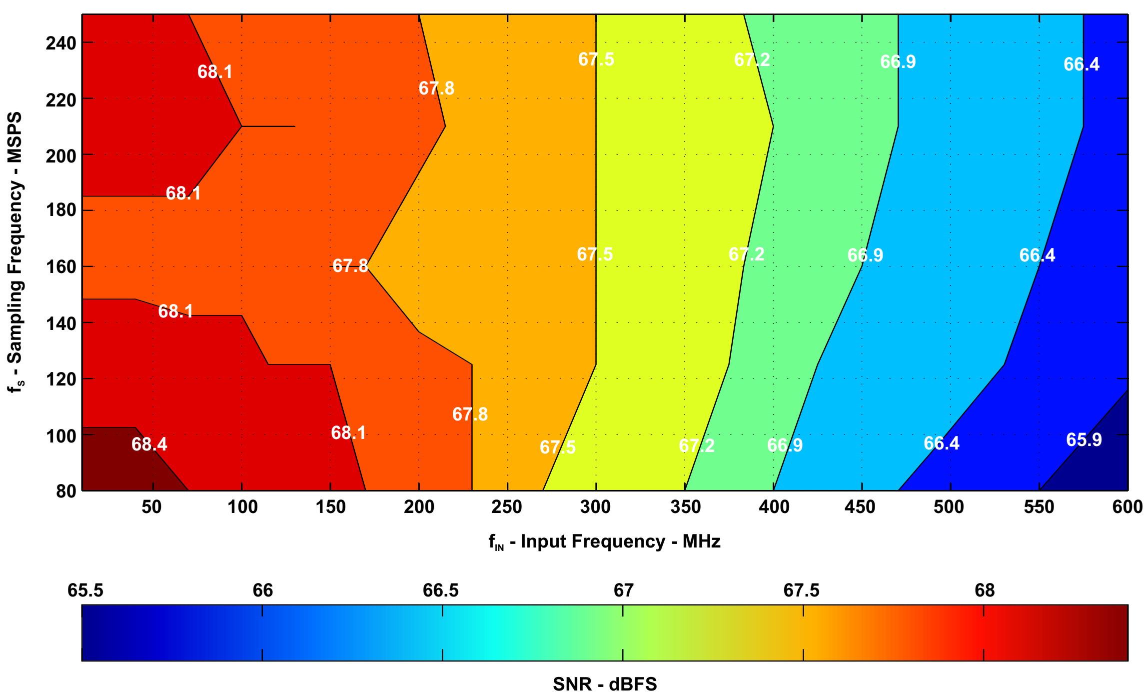


Figure 75. 6-dB GAIN (SNR, ADS42JB69)

TYPICAL CHARACTERISTICS: CONTOUR (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 64k-point FFT, unless otherwise noted.

Signal-to-Noise Ratio (SNR): ADS42JB49

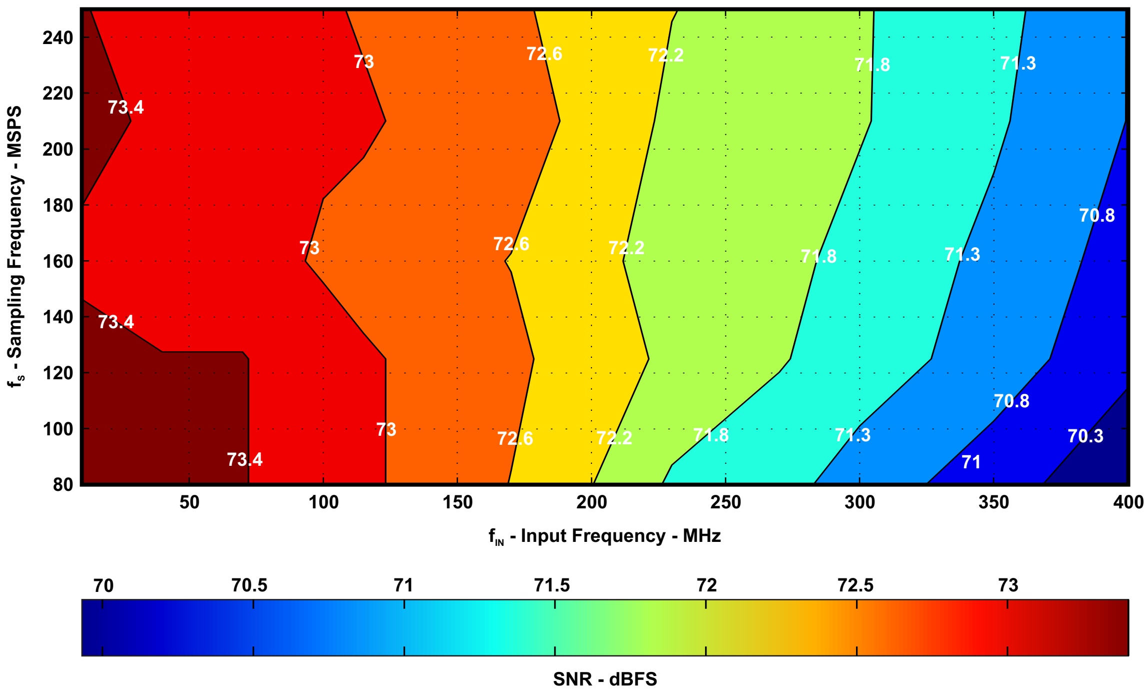


Figure 76. 0-dB GAIN (SNR, ADS42JB49)

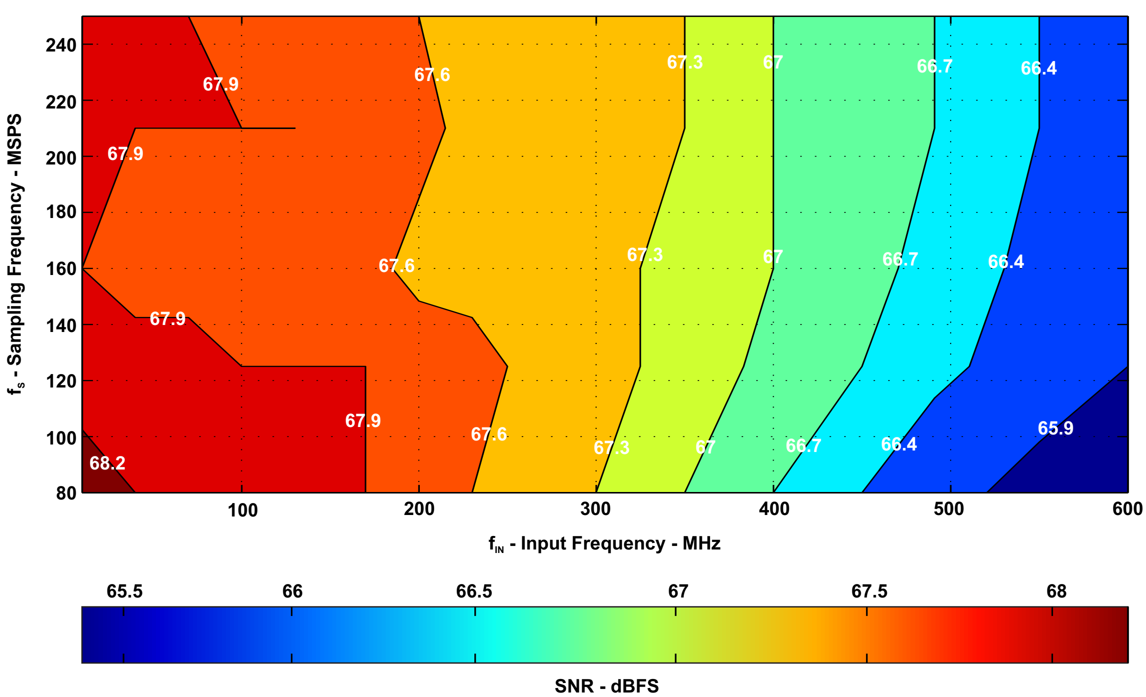


Figure 77. 6-dB GAIN (SNR, ADS42JB49)

DEVICE CONFIGURATION

The ADS42JB49 and ADS42JB69 can be configured using a serial programming interface, as described in the *Serial Interface* section. In addition, the device has four dedicated parallel pins (PDN_GBL, STBY, CTRL1, and CTRL2) for controlling the power-down modes.

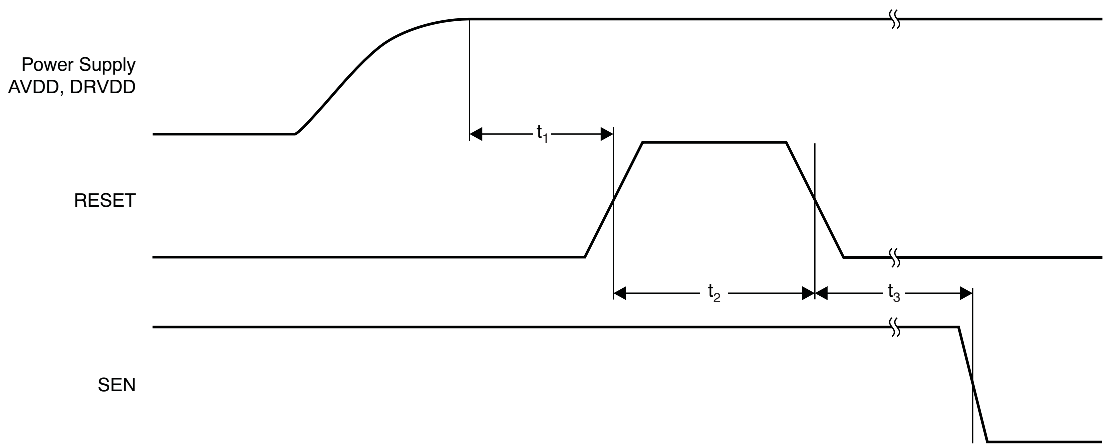
SERIAL INTERFACE

The ADC has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), SDATA (serial interface data), and SDOUT (serial interface data output) pins. Serially shifting bits into the device is enabled when SEN is low. SDATA serial data are latched at every SCLK rising edge when SEN is active (low). The serial data are loaded into the register at every 16th SCLK rising edge when SEN is low. When the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiples of 16-bit words within a single active SEN pulse. The interface functions with SCLK frequencies from 20 MHz down to very low speeds (of a few hertz) and also with non-50% SCLK duty cycle.

Register Initialization

After power-up, the internal registers must be initialized to their default values through a **hardware reset** by applying a high pulse on the RESET pin (of widths greater than 10 ns), as shown in Figure 78. Later during operation, if required serial interface registers can be cleared by:

1. Either through a hardware reset or
2. By applying a software reset. When using the serial interface, set the RESET bit (D0 in register address 08h) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.



NOTE: After power-up, the internal registers must be initialized to their default values through a hardware reset by applying a high pulse on the RESET pin.

Figure 78. Reset Timing Diagram

Table 3. Reset Timing (1)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Power-on delay	Delay from AVDD and DRVDD power-up to active RESET pulse	1			ms
t_2	Reset pulse width	Active RESET signal pulse width	10			ns
					1	µs
t_3	Register write delay	Delay from RESET disable to SEN active	100			ns

(1) Typical values at +25°C; minimum and maximum values across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, unless otherwise noted.

Serial Register Write

The internal device register can be programmed following these steps:

1. Drive the SEN pin low.
2. Set the R/W bit to '0' (bit A7 of the 8-bit address).
3. Set bit A6 in the address field to '0'.
4. Initiate a serial interface cycle specifying the address of the register (A5 to A0) whose content must be written (as shown in Figure 79 and Table 4).
5. Write the 8-bit data that is latched on the SCLK rising edge.

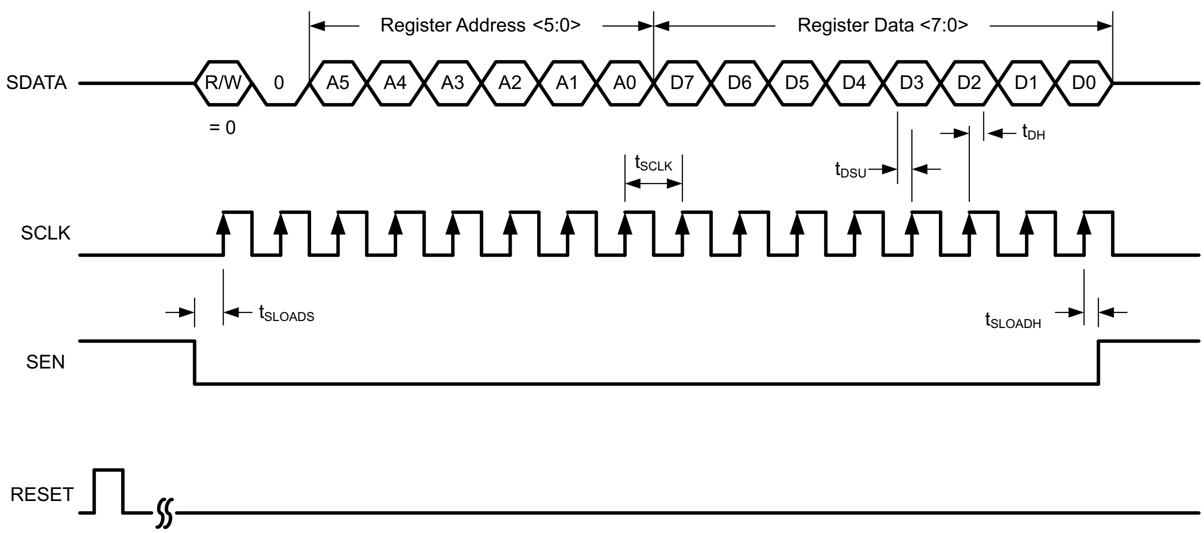


Figure 79. Serial Register Write Timing Diagram

Table 4. Serial Interface Timing(1)

PARAMETER		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (equal to 1 / t_{SCLK})	> dc		20	MHz
t_{SLOADS}	SEN to SCLK setup time	25			ns
t_{SLOADH}	SCLK to SEN hold time	25			ns
t_{DSU}	SDIO setup time	25			ns
t_{DH}	SDIO hold time	25			ns

(1) Typical values are at +25°C, minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD3V = 3.3 V, and AVDD = DRVDD = IOVDD = 1.8 V, unless otherwise noted.

Serial Register Readout

The device includes a mode where the contents of the internal registers can be read back. This readback mode may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC.

1. Set bit A7 (MSB) of 8 bit address to '1'.
2. Write the address of register on bits A5 through A0 whose contents must be read. See Figure 80
3. The device outputs the contents (D7 to D0) of the selected register on the SDOUT pin (pin 45).
4. The external controller can latch the contents at the SCLK rising edge.

When serial registers are enabled for writing (bit A7 of 8-bit address bus is 0), the SDOUT pin is in a high-impedance mode. If serial readout is not used, the SDOUT pin must float. Figure 80 shows a timing diagram of this readout mode. SDOUT comes out at the SCLK falling edge with an approximate delay (t_{SD_DELAY}) of 20 ns, as shown in Figure 81.

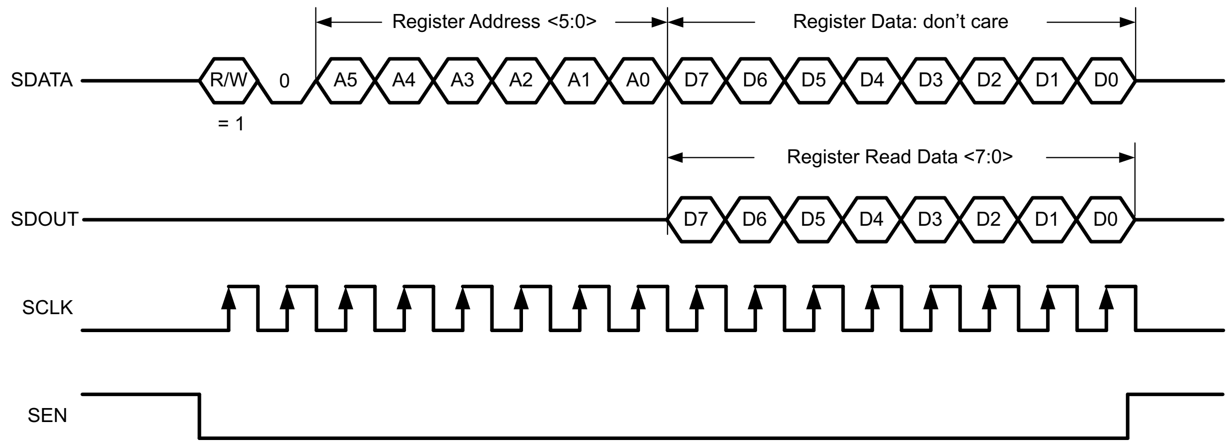


Figure 80. Serial Register Readout Timing Diagram

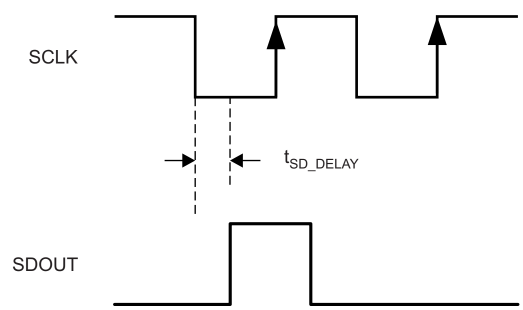


Figure 81. SDOUT Timing Diagram

PIN CONTROLS

The device power-down functions can be controlled either through the parallel control pins (STBY, PDN_GBL, CTRL1, and CTRL2) or through an SPI register setting.

STBY places the device in a standby power-down mode. PDN_GBL places the device in global power-down mode.

Table 5. CTRL1, CTRL2 Pin Functions

CTRL1	CTRL2	DESCRIPTION
Low	Low	Normal operation
High	Low	Channel A powered down
Low	High	Channel B powered down
High	High	Global power-down

Table 6. PDN_GBL Pin Function

PDN_GBL	DESCRIPTION
Low	Normal operation
High	Global power-down. Wake-up from this mode is slow.

Table 7. STBY Pin Function

STBY	DESCRIPTION
Low	Normal operation
High	ADCs are powered down while the input clock buffer and output CML buffers are alive. Wake-up from this mode is fast.

SUMMARY OF SERIAL INTERFACE REGISTERS

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
06	0	0	0	0	0	0	CLK DIV	
07	0	0	0	0	0	SYSREF DELAY		
08	PDN CHA	PDN CHB	STDBY	DATA FORMAT	Always write 1	0	0	RESET
0B	CHA GAIN					CHA GAIN EN	0	0
0C	CHBGAIN					CHB GAIN EN	0	0
0D	HIGH FREQ 1	0	0	HIGH FREQ 1	0	0	0	FAST OVR EN
0E	HIGH FREQ 2	0	0	HIGH FREQ 2	0	0	0	0
0F	CHA TEST PATTERNS				CHB TEST PATTERNS			
10	CUSTOM PATTERN (15:8)							
11	CUSTOM PATTERN (15:8)							
12	CUSTOM PATTERN (15:8)							
13	CUSTOM PATTERN (15:8)							
1F	Always write 0	FAST OVR THRESHOLD						
26	SERDES TEST PATTERN		IDLE SYNC	TESTMODE EN	FLIP ADC DATA	LAN ALIGN	FRAME ALIGN	TX LINK CONFIG DATA0
27	0	0	0	0	0	0	CTRLK	CTRLF
2B	SCRAMBLE EN	0	0	0	0	0	0	0
2C	0	0	0	0	0	0	0	OCTETS PER FRAME
2D	0	0	0	FRAMES PER MULTIFRAME				
30	SUBCLASS			0	0	0	0	0
36	SYNC REQ	LMFC RESET MASK	0	0	OUTPUT CURRENT SEL			
37	LINK LAYER TESTMODE			LINK LAYER RPAT	0	PULSE DET MODES		
38	FORCE LMFC COUNT	LMFC COUNT INIT					RELEASE ILANE SEQ	

DESCRIPTION OF SERIAL INTERFACE REGISTERS

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
6	0	0	0	0	0	0	CLK DIV	

Default: 00h

D[1:0] **CLK DIV** Internal clock divider for input sample clock

00 Divide-by-1 (clock divider bypassed)

01 Divide-by-2

10 Divide-by-1

11 Divide-by-4

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
7	0	0	0	0	0	0	SYSREF DELAY	

Default: 00h

D[2:0] **SYSREF DELAY** Controls the delay of the SYSREF input with respect to the input clock. Typical values for the expected delay of different settings are:

000 0-ps delay

001 60-ps delay

010 120-ps delay

011 180-ps delay

100 240-ps delay

101 300-ps delay

110 360-ps delay

111 420-ps delay

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
8	PDN CHA	PDN CHB	STDBY	DATA FORMAT	Always write 1	0	0	RESET

Default: 00h

D7	**PDN CHA**	Power-down channel A
0	Normal operation	
1	Channel A power down	
D6	**PDN CHB**	Power-down channel B
0	Normal operation	
1	Channel B power down	
D5	**STBY**	Dual ADC is placed into standby mode
0	Normal operation	
1	Both ADCs are powered down (input clock buffer and CML output buffers are alive)	
D4	**DATA FORMAT**	Digital output data format
0	Twos complement	
1	Offset binary	
D3	**Always write 1**	
	Default value of this bit is 0. It must always be set to 1	
D0	**RESET**	Software reset applied
	This bit resets all internal registers to the default values and self-clears to ‘0’.	

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
B	CHA GAIN					CHA GAIN EN	0	0

Default: 00h

D[7:3] **CHA GAIN** Digital gain for channel A (must set the CHA GAIN EN bit first, bit D2)

Table 8. Digital Gain for Channel A

REGISTER VALUE	DIGITAL GAIN	FULL-SCALE INPUT VOLTAGE		REGISTER VALUE	DIGITAL GAIN	FULL-SCALE INPUT VOLTAGE
00000	0 dB	**2.0 V_{PP}**		01010	1.5 dB	1.7 V_{PP}
00001	Do not use	—		01011	2 dB	1.6 V_{PP}
00010	Do not use	—		01100	2.5 dB	1.5 V_{PP}
00011	–2.0 dB	**2.5 V_{PP}**		01101	3 dB	1.4 V_{PP}
00100	–1.5 dB	2.4 V_{PP}		01110	3.5 dB	1.3 V_{PP}
00101	–1.0 dB	2.2 V_{PP}		01111	4 dB	1.25 V_{PP}
00110	–0.5 dB	2.1 V_{PP}		10000	4.5 dB	1.2 V_{PP}
00111	0 dB	**2.0 V_{PP}**		10001	5 dB	1.1 V_{PP}
01000	0.5 dB	1.9 V_{PP}		10010	5.5 dB	1.05 V_{PP}
01001	1 dB	1.8 V_{PP}		10011	6 dB	1.0 V_{PP}

D2 **CHA GAIN EN** Digital gain enable bit for channel A

0 Digital gain disabled

1 Digital gain enabled

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
C	CHB GAIN					CHB GAIN EN	0	0

Default: 00h

D[7:3] **CHB GAIN** Digital gain for channel B (must set the CHA GAIN EN bit first, bit D2)

Table 9. Digital Gain for Channel B

REGISTER VALUE	DIGITAL GAIN	FULL-SCALE INPUT VOLTAGE		REGISTER VALUE	DIGITAL GAIN	FULL-SCALE INPUT VOLTAGE
00000	0 dB	**2.0 V_{PP}**		01010	1.5 dB	1.7 V_{PP}
00001	Do not use	—		01011	2 dB	1.6 V_{PP}
00010	Do not use	—		01100	2.5 dB	1.5 V_{PP}
00011	–2.0 dB	**2.5 V_{PP}**		01101	3 dB	1.4 V_{PP}
00100	–1.5 dB	2.4 V_{PP}		01110	3.5 dB	1.3 V_{PP}
00101	–1.0 dB	2.2 V_{PP}		01111	4 dB	1.25 V_{PP}
00110	–0.5 dB	2.1 V_{PP}		10000	4.5 dB	1.2 V_{PP}
00111	0 dB	**2.0 V_{PP}**		10001	5 dB	1.1 V_{PP}
01000	0.5 dB	1.9 V_{PP}		10010	5.5 dB	1.05 V_{PP}
01001	1 dB	1.8 V_{PP}		10011	6 dB	1.0 V_{PP}

D2 **CHB GAIN EN** Digital gain enable bit for channel B

0 Digital gain disabled

1 Digital gain enabled

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
D	HIGH FREQ 1	0	0	HIGH FREQ 1	0	0	0	FAST OVR EN

D7, D4 HIGH FREQ 1 High frequency mode 1

00 Default

11 Use for input frequencies > 250 MHz along with HIGH FREQ 2

D0 **FAST OVR EN** Selects if normal or fast OVR signal is presented on OVRA, OVRB pins

0 Normal OVR on OVRA, OVRB pins

1 Fast OVR on OVRA, OVRB pins

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
E	HIGH FREQ 2	0	0	HIGH FREQ 2	0	0	0	0

D7, D4 HIGH FREQ 2 High frequency mode 2

00 Default

11 Use for input frequencies > 250 MHz along with HIGH FREQ 1

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
F	CHA TEST PATTERNS				CHB TEST PATTERNS			

Default: 00h

D[7:4]	**CHA TEST PATTERNS**	Channel A test pattern programmability
	16-bit test pattern data is selected as input to JESD block (in ADS42JB49, last two LSBs of 16-bit data are replaced by 00)	
0000	Normal operation	
0001	All '0's	
0010	All '1's	
0011	Toggle pattern:	In ADS42JB69, data is an alternating sequence of 1010101010101010 and 0101010101010101. In ADS42JB49, data alternates between 10101010101010 and 01010101010101.
0100	Digital ramp:	In ADS42JB69, data increments by 1 LSB every clock cycle from code 0 to 65535. In ADS42JB49 data increments by 1 LSB every 4th clock cycle from code 0 to 16383.
0101	Do not use	
0110	Single pattern:	In ADS42JB69, data is same as programmed by registers bits CUSTOM PATTERN 1 [15:0]. In ADS42JB49, data is same as programmed by register bits CUSTOM PATTERN 1 [15:2].
0111	Double pattern:	In ADS42JB69, data alternates between CUSTOM PATTERN 1[15:0] and CUSTOM PATTERN 2[15:0] .In ADS42JB49 data alternates between CUSTOM PATTERN 1[15:2] and CUSTOM PATTERN 2[15:2].
1000	Deskew pattern:	In ADS42JB69, data is AAAAh. In ADS42JB49, data is 3AAAh.
1001	Do not use	
1010	PRBS pattern:	Data is a sequence of pseudo random numbers.
1011	8-Point sine wave:	In ADS42JB69, data is a repetitive sequence of following 8 numbers forming a sine-wave in 2s complement format: 1, 9598, 32768, 55938, 65535, 55938, 32768, 9598. In ADS42JB49, data is a repetitive sequence of following 8 numbers forming a sine-wave in 2s complement format: 0, 2399, 8192, 13984, 16383, 13984, 8192, 2399.
D3-D0	**CHB TEST PATTERNS**	Channel B test pattern programmability
	16-bit test pattern data is selected as input to JESD block (in ADS42JB49, last two LSBs of 16-bit data are replaced by 00)	
0000	Normal operation	
0001	All '0's	
0010	All '1's	
0011	Toggle pattern:	In ADS42JB69, data is an alternating sequence of 1010101010101010 and 0101010101010101. In ADS42JB49, data alternates between 10101010101010 and 01010101010101.
0100	Digital ramp:	In ADS42JB69, data increments by 1 LSB every clock cycle from code 0 to 65535. In ADS42JB49 data increments by 1 LSB every 4th clock cycle from code 0 to 16383.
0101	Do not use	
0110	Single pattern:	In ADS42JB69, data is same as programmed by registers bits CUSTOM PATTERN 1 [15:0]. In ADS42JB49, data is same as programmed by register bits CUSTOM PATTERN 1 [15:2].
0111	Double pattern:	In ADS42JB69, data alternates between CUSTOM PATTERN 1[15:0] and CUSTOM PATTERN 2[15:0] .In ADS42JB49 data alternates between CUSTOM PATTERN 1[15:2] and CUSTOM PATTERN 2[15:2].
1000	Deskew pattern:	In ADS42JB69, data is AAAAh. In ADS42JB49, data is 3AAAh.
1001	Do not use	
1010	PRBS pattern:	Data is a sequence of pseudo random numbers.
1011	8-Point sine wave:	In ADS42JB69, data is a repetitive sequence of following 8 numbers forming a sine-wave in 2s complement format: 1, 9598, 32768, 55938, 65535, 55938, 32768, 9598. In ADS42JB49, data is a repetitive sequence of following 8 numbers forming a sine-wave in 2s complement format: 0, 2399, 8192, 13984, 16383, 13984, 8192, 2399.

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
10	CUSTOM PATTERN 1 (15:8)							

Default: 00h

D[7:0]	**CUSTOM PATTERN 1 (15:8)**	Sets custom pattern 1 (15:8) using these bits for both channels

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
11	CUSTOM PATTERN 1 (7:0)							

Default: 00h

D[7:0] **CUSTOM PATTERN 1 (7:0)** Sets custom pattern 1 (7:0) using these bits for both channels

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
12	CUSTOM PATTERN 2 (15:8)							

Default: 00h

D[7:0] **CUSTOM PATTERN 2 (15:8)** Sets custom pattern 2 (15:8) using these bits for both channels

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
13	CUSTOM PATTERN 2 (7:0)							

Default: 00h

D[7:0] **CUSTOM PATTERN 2 (7:0)** Sets custom pattern 2 (7:0) using these bits for both channels

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
1F	Always write 0	FAST OVR THRESHOLD						

Default: FFh

D7 **Always write 0**

Default value of this bit is '1'. Always write this bit to '0' when fast OVR thresholds are programmed.

D[6:0] **FAST OVR THRESHOLD**

The device has a fast OVR mode that indicates an overload condition at the ADC input. The input voltage level at which the overload is detected is referred to as the threshold and is programmable using the FAST OVR THRESHOLD bits. FAST OVR is triggered nine output clock cycles after the overload condition occurs. The threshold at which fast OVR is triggered is (full-scale × [the decimal value of the FAST OVR THRESHOLD bits] / 127). See section OVERRANGE INDICATION for details.

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
26	SERDES TEST PATTERN		IDLE SYNC	TESTMODE EN	FLIP ADC DATA	LANE ALIGN	FRANE ALIGN	TX LINK CONFIG DATA

Default: 00h

D[7:6] **SERDES TEST PATTERN** Sets test patterns in the transport layer of the JESD204B interface

00 Normal operation

01 Outputs clock pattern: Output is 10101010 pattern

10 Encoded pattern: Output is 1111111100000000

11 PRBS sequence: Output is $2^{15} – 1$

D5 **IDLE SYNC** Sets output pattern when SYNC~ is asserted

0 Sync code is k28.5 (0xBCBC)

1 Sync code is 0xBC50

D4 **TESTMODE EN** Generates long transport layer test pattern mode according to 5.1.63 clause of JESD204B specification

0 Test mode disabled

1 Test mode enabled

D3 **FLIP ADC DATA**

0 Normal operation

1 Output data order is reversed: MSB – LSB

D2 **LANE ALIGN** Inserts lane alignment character (K28.3) for the receiver to align to lane boundary per section 5.3.3.5 of the JESD204B specification.

0 Lane Alignment characters are not inserted.

1 Inserts lane alignment characters

D1 **FRAME ALIGN** Inserts frame alignment character (K28.7) for the receiver to align to frame boundary per section 5.3.3.4 of the JESD204B specification.

0 Frame Alignment characters are not inserted.

1 Inserts frame alignment characters

D0 **TX LINK CONFIG DATA** Disables sending initial link alignment (ILA) sequence when SYNC~ is de-asserted, '0'

0 ILA Enabled

1 ILA disabled

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
27	0	0	0	0	0	0	CTRL K	CTRL F

Default: 00h

D1 **CTRL K** Enables bit for number of frames per multiframe

0 Default

1 Frames per multiframe can be set in register 2Dh

D0 **CTRL F** Enables bit for number of octets per frame

0 Default

1 Octets per frame can be specified in register 2Ch

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
2B	SCRAMBLE EN	0	0	0	0	0	0	0

Default: 00h

D7 **SCRAMBLE EN** Scramble enable bit in the JESD204B interface

0 Scrambling disabled

1 Scrambling enabled

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
2C	0	0	0	0	0	0	0	OCTETS PER FRAME

Default: 00h

D[7:0] **OCTETS PER FRAME** Sets number of octets per frame (F)

0 10x mode using two lanes per ADC

1 20x mode using one lane per ADC

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
2D	0	0	0	FRAMES PER MULTIFRAME				

Default: 00h

D[4:0] **FRAMES PER MULTIFRAME** Sets number of frames per multiframe

After reset, the default settings for frames per multiframe are:

10x K = 16

20x K = 8

For each mode, K should not be set to a lower value.

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
30	SUBCLASS			0	0	0	0	0

Default: 40h

D[7:5] **SUBCLASS** Sets JESD204B subclass. Note that the default value of these bits after reset is '010', which makes subclass 2 the default class.

000 Subclass 0 Backward compatibility with JESD204A

001 Subclass 1 Deterministic latency using SYSREF signal

010 Subclass 2 Deterministic latency using SYNC~ detection (default subclass after reset)

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
36	SYNC REQ	LMFC RESET MASK	0	0	OUTPUT CURRENT SEL			

Default: 00h

D7	**SYNC REQ**	Generates synchronization request	
0	Normal operation		
1	Generates sync request		
D6	**LMFC RESET MASK**	Mask LMFC reset coming to digital	
0	LMFC reset is not masked		
1	Ignores LMFC reset		
D3-D0	**OUTPUT CURRENT SEL**	Changes JESD output buffer current	
0000	16 mA	1000	8 mA
0001	15 mA	1001	7 mA
0010	14 mA	1010	6 mA
0011	13 mA	1011	5 mA
0100	20 mA	1100	12 mA
0101	19 mA	1101	11 mA
0110	18 mA	1110	10 mA
0111	17 mA	1111	9 mA

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
37	LINK LAYER TESTMODE			LINK LAYER RPAT	0	PULSE DET MODES		

Default: 00h

D[7:5]	**LINK LAYER TESTMODE**	Generates pattern according to clause 5.3.3.8.2 of the JESD204B document
000	Normal ADC data	
001	D21.5 (high-frequency jitter pattern)	
010	K28.5 (mixed-frequency jitter pattern)	
011	Repeats initial lane alignment (generates K28.5 character and repeats lane alignment sequences continuously)	
100	12-octet RPAT jitter pattern	
D4	**LINK LAYER RPAT**	Changes the running disparity in modified RPAT pattern test mode (only when link layer test mode = 100)
0	Normal operation	
1	Changes disparity	
D[2:0]	**PULSE DET MODES**	Selects different detection modes for SYSREF (subclass 1) and SYNC (subclass 2)

D2	D1	D0	FUNCTIONALITY
0	Don't care	0	Allows all pulses to reset input clock dividers
1	Don't care	0	Do not allow reset of analog clock dividers
Don't care	0 -> 1 transition	1	Allows one pulse immediately after the 0 -> 1 transition to reset the divider

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
38	FORCE LMFC COUNT	LMFC COUNT INIT					RELEASE ILANE SEQ	

Default: 00h

D7 **FORCE LMFC COUNT** Forces LMFC count

0 Normal operation

1 Enables using a different starting value for the LMFC counter

D[6:2] **LMFC COUNT INIT** SYSREF receives the digital block and resets the LMFC count to '0'. K28.5 stops transmitting when the LMFC count reaches 31. The initial value that the LMFC count resets to can be set using LMFC COUNT INIT. In this manner, the Rx can be synchronized early because the Rx gets the LANE ALIGNMENT SEQUENCE early. The FORCE LMFC COUNT register bit must be enabled.

D[1:0] **RELEASE ILANE SEQ** Delays the generation of lane alignment sequence by 0, 1, 2, or 3 multiframes after the code group synchronization.

00 0

01 1

10 2

11 3

APPLICATION INFORMATION

THEORY OF OPERATION

The ADS42JB69 and ADS42JB49 is a family of high linearity, buffered analog input, dual-channel ADCs with maximum sampling rates up to 250 MSPS employing JESD204B interface. The conversion process is initiated by a rising edge of the external input clock and the analog input signal is sampled. The sampled signal is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. At every clock edge the sample propagates through the pipeline, resulting in a data latency of 23 clock cycles. The output is available in CML logic levels following JESD204B standard.

ANALOG INPUT

The analog input pins have analog buffers (running from the AVDD3V supply) that internally drive the differential sampling circuit. As a result of the analog buffer, the input pins present high input impedance to the external driving source (10-kΩ dc resistance and 4-pF input capacitance). The buffer helps isolate the external driving source from the switching currents of the sampling circuit. This buffering makes driving the buffered inputs easier than when compared to an ADC without the buffer.

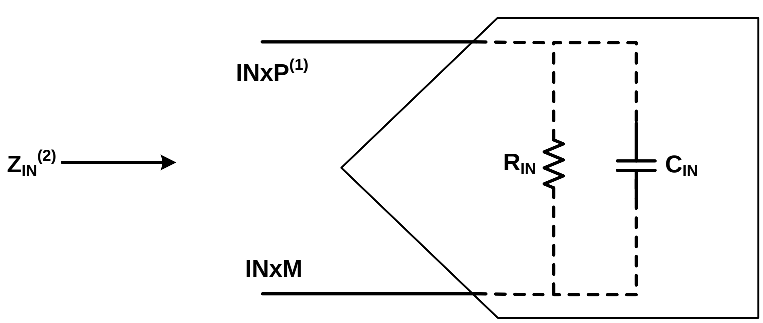
The input common-mode is set internally using a 5-kΩ resistor from each input pin to VCM so the input signal can be ac-coupled to the pins. Each input pin (INP, INM) must swing symmetrically between VCM + 0.5 V and VCM – 0.5 V, resulting in a 2-V_{PP} differential input swing. When programmed for 2.5-V_{PP} full-scale, each input pin must swing symmetrically between VCM + 0.625 V and VCM – 0.625 V.

The input sampling circuit has a high 3-dB bandwidth that extends up to 900 MHz (measured with a 50-Ω source driving a 50-Ω termination between INP and INM). The dynamic offset of the first-stage sub-ADC limits the maximum analog input frequency to approximately 250 MHz (with a 2.5-V_{PP} full-scale amplitude) and to approximately 400 MHz (with a 2-V_{PP} full-scale amplitude). This 3-dB bandwidth is different than the analog bandwidth of 900 MHz, which is only an indicator of signal amplitude versus frequency.

Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This technique improves the common-mode noise immunity and even-order harmonic rejection. A small resistor (5 Ω to 10 Ω) in series with each input pin is recommended to damp out ringing caused by package parasitics.

Figure 82, Figure 83, and Figure 84 show the differential impedance ($Z_{IN} = R_{IN} \parallel C_{IN}$) at the ADC input pins. The presence of the analog input buffer results in an almost constant input capacitance up to 1 GHz.



(1) X = A or B.

(2) $Z_{IN} = R_{IN} \parallel (1 / j\omega C_{IN})$.

Figure 82. ADC Equivalent Input Impedance

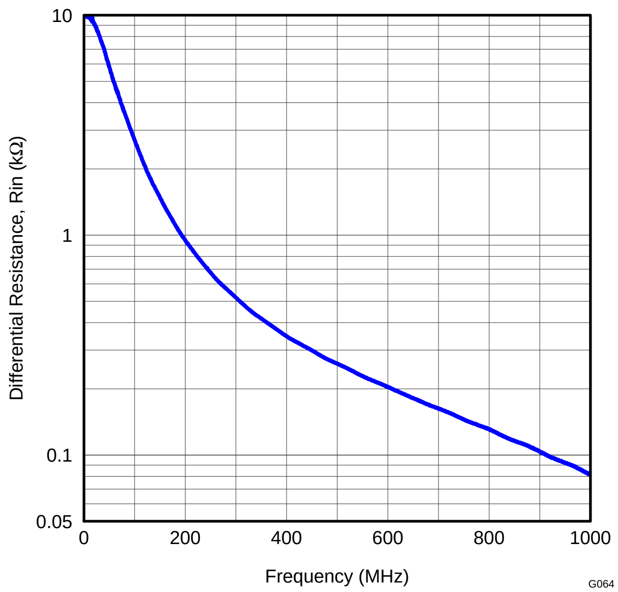


Figure 83. ADC Analog Input Resistance (R_{IN}) Across Frequency

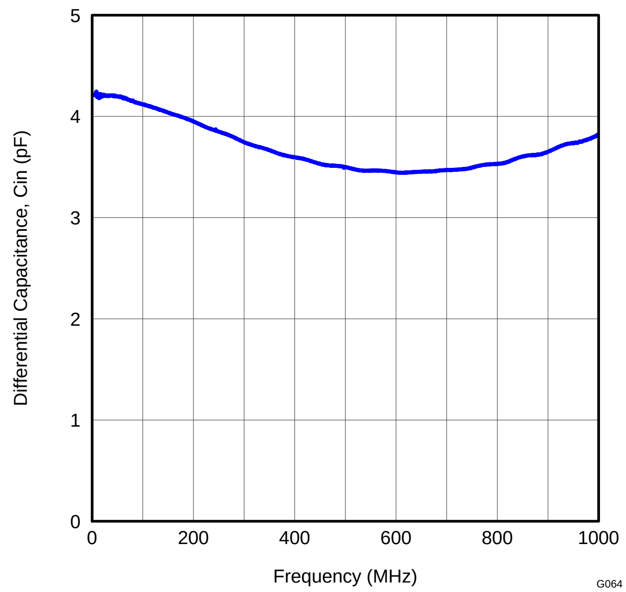


Figure 84. ADC Analog Input Capacitance (C_{IN}) Across Frequency

Driving Circuit

An example driving circuit configuration is shown in Figure 85. To optimize even-harmonic performance at high input frequencies (greater than the first Nyquist), the use of back-to-back transformers is recommended, as shown in Figure 85. Note that the drive circuit is terminated by 50 Ω near the ADC side. The ac-coupling capacitors allow the analog inputs to self-bias around the required common-mode voltage. An additional R-C-R (39 Ω - 6.8 pF - 39 Ω) circuit placed near device pins helps further improve HD3.

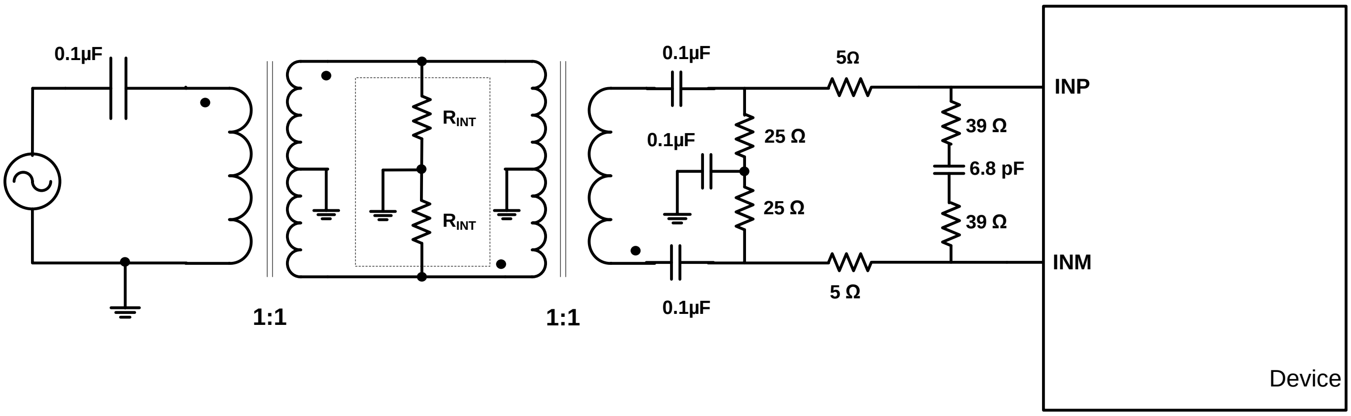


Figure 85. Drive Circuit for Input Frequencies upto 250MHz

The mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps minimize this mismatch and good performance is obtained for high-frequency input signals. An additional termination resistor pair may be required between the two transformers, as shown in Figure 85. The center point of this termination is connected to ground to improve the balance between the P (positive) and M (negative) sides. The values of the terminations between the transformers and on the secondary side must be chosen to obtain an effective 50 Ω (for a 50-Ω source impedance). For high input frequencies (>250MHz), the R-C-R circuit can be removed as indicated in Figure 86.

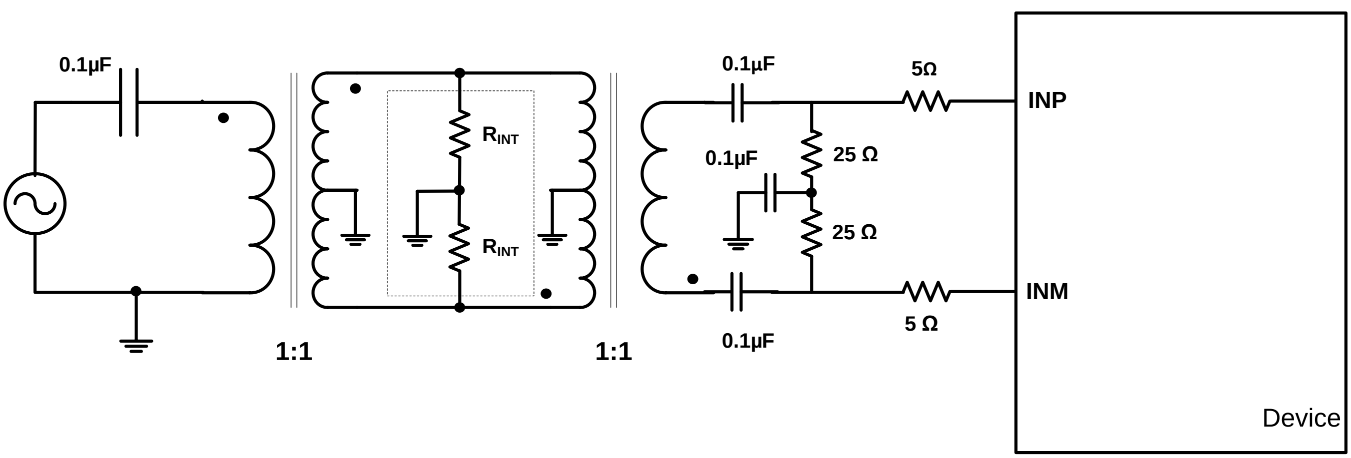
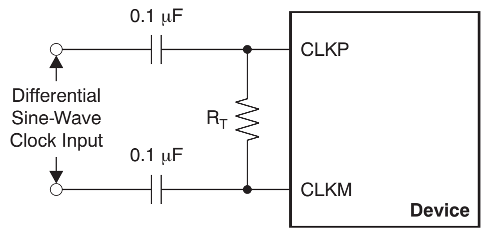


Figure 86. Drive Circuit for Input Frequencies > 250MHz

CLOCK INPUT

The device clock inputs can be driven differentially (sine, LVPECL, or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to 1.4 V using internal 5-kΩ resistors. The self-bias clock inputs of the ADS42JB69 and ADS42JB49 can be driven by the transformer-coupled, sine-wave clock source or by the ac-coupled, LVPECL and LVDS clock sources, as shown in Figure 87, Figure 88, and Figure 89. See Figure 90 for details regarding the internal clock buffer.



NOTE: R_T = termination resistor, if necessary.

Figure 87. Differential Sine-Wave Clock Driving Circuit

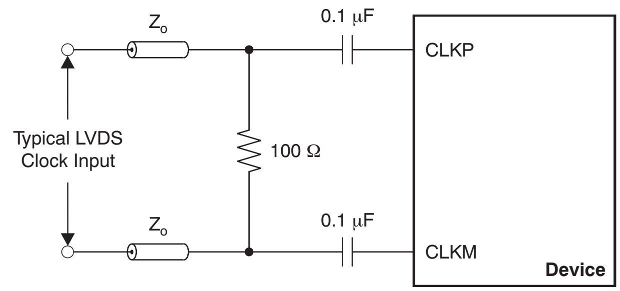


Figure 88. LVDS Clock Driving Circuit

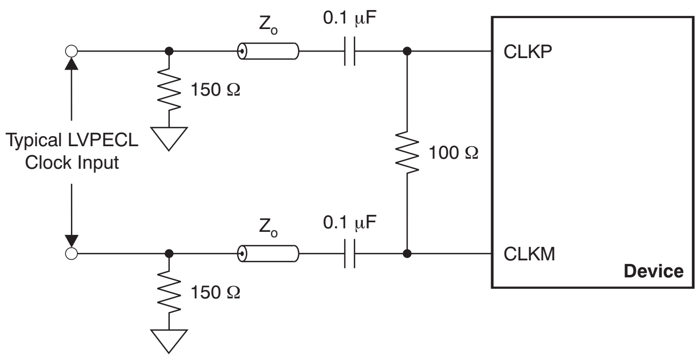
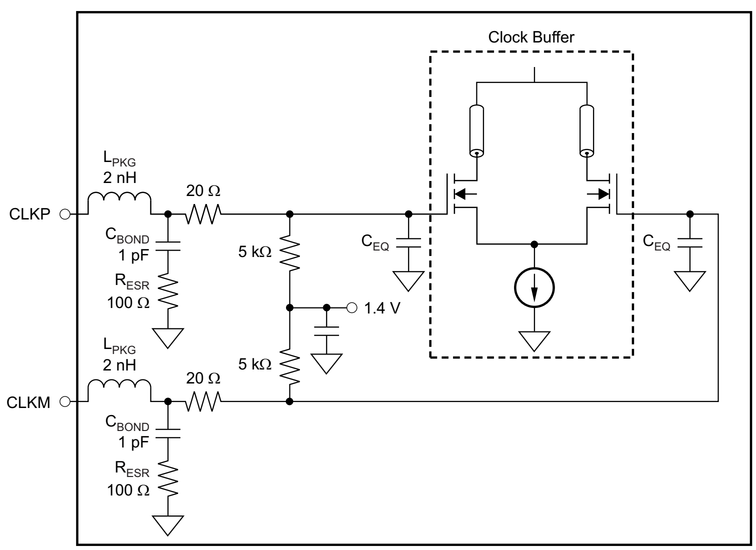


Figure 89. LVPECL Clock Driving Circuit



NOTE: C_{EQ} is 1 pF to 3 pF and is the equivalent input capacitance of the clock buffer.

Figure 90. Internal Clock Buffer

A single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1-µF capacitor, as shown in Figure 91. However, for best performance the clock inputs must be driven differentially, thereby reducing susceptibility to common-mode noise. For high input frequency sampling, TI recommends using a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effects of jitter. There is no change in performance with a non-50% duty cycle clock input.

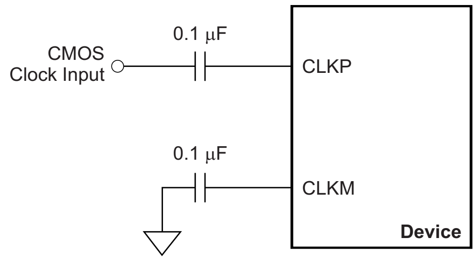


Figure 91. Single-Ended Clock Driving Circuit

DIGITAL GAIN

The device includes gain settings that can be used to obtain improved SFDR performance (compared to no gain). Gain is programmable from –2 dB to 6 dB (in 0.5-dB steps). For each gain setting, the analog input full-scale range scales proportionally. Table 10 shows how full-scale input voltage changes when digital gain are programmed in 1-dB steps. Refer to Table 8 to set digital gain using a serial interface register.

SFDR improvement is achieved at the expense of SNR; for 1 dB increase in digital gain, SNR degrades approximately between 0.5 dB and 1 dB. Therefore, gain can be used as a trade-off between SFDR and SNR. Note that the default gain after reset is 0 dB with a 2.0-V_{PP} full-scale voltage.

Table 10. Full-Scale Range Across Gains

DIGITAL GAIN	FULL-SCALE INPUT VOLTAGE
–2 dB	2.5 V_{PP} (1)
–1 dB	2.2 V_{PP}
0 dB (default)	2.0 V_{PP}
1 dB	1.8 V_{PP}
2 dB	1.6 V_{PP}
3 dB	1.4 V_{PP}
4 dB	1.25 V_{PP}
5 dB	1.1 V_{PP}
6 dB	1.0 V_{PP}

(1) Shaded cells indicate performance settings used in the Electrical Characteristics and Typical Characteristics.

OVERRANGE INDICATION

The device provides two different overrange indications. Normal OVR (default) is triggered if the final 16-bit data output exceeds the maximum code value. Fast OVR is triggered if the input voltage exceeds the programmable overrange threshold and is presented after only nine clock cycles, thus enabling a quicker reaction to an overrange event. By default, the normal overrange indication is output on the OVRA and OVRB pins. Using the register bit FAST OVR EN, the fast OVR indication can be presented on the overrange pins instead.

The input voltage level at which the overload is detected is referred to as the threshold and is programmable using the FAST OVR THRESHOLD bits. FAST OVR is triggered nine output clock cycles after the overload condition occurs. The threshold voltage amplitude at which fast OVR is triggered is: 1 × [the decimal value of the FAST OVR THRESH bits] / 127

When digital is programmed (for gain values > 0-dB), the threshold voltage amplitude is: $10^{-Gain/20}$ x [the decimal value of the FAST OVR THRESH bits] / 127

SNR AND CLOCK JITTER

The signal-to-noise ratio (SNR) of the ADC is limited by three different factors, as shown in Equation 1. Quantization noise is typically not noticeable in pipeline converters and is 96 dBFS for a 16-bit ADC. Thermal noise limits SNR at low input frequencies and clock jitter sets SNR for higher input frequencies.

$$SNR_{ADC}[dBc] = -20 \times \log \sqrt{\left(10 - \frac{SNR_{Quantization\_Noise}}{20}\right)^2 + \left(10 - \frac{SNR_{ThermalNoise}}{20}\right)^2 + \left(10 - \frac{SNR_{Jitter}}{20}\right)^2} \quad (1)$$

SNR limitation is a result of sample clock jitter and can be calculated by Equation 2:

$$SNR_{Jitter}\ [dBc] = -20 \times \log(2\pi \times f_{IN} \times t_{Jitter}) \quad (2)$$

The total clock jitter (T_{Jitter}) has three components: the internal aperture jitter (85 f_S for the device) is set by the noise of the clock input buffer, the external clock jitter, and the jitter from the analog input signal. T_{Jitter} can be calculated by Equation 3:

$$T_{Jitter} = \sqrt{(T_{Jitter,Ext.Clock\_Input})^2 + (T_{Aperture\_ADC})^2} \quad (3)$$

External clock jitter can be minimized by using high-quality clock sources and jitter cleaners as well as band-pass filters at the clock input while a faster clock slew rate improves ADC aperture jitter. The device has a 74.1-dBFS thermal noise and an 85-f_S internal aperture jitter. The SNR value depends on the amount of external jitter for different input frequencies, as shown in Figure 92.

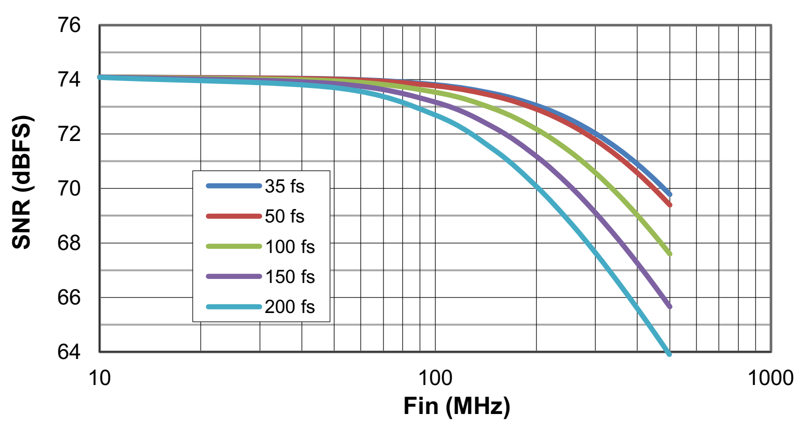


Figure 92. SNR versus Input Frequency and External Clock Jitter

INPUT CLOCK DIVIDER

The device is equipped with an internal divider on the clock input. This divider allows operation with a faster input clock, simplifying the system clock distribution design. The clock divider can be bypassed (divide-by-1) for operation with a 250-MHz clock. The divide-by-2 option supports a maximum 500-MHz input clock and the divide-by-4 option supports a maximum 1-GHz input clock frequency.

JESD204B INTERFACE

The JESD interface of ADS42JB49 and ADS42JB69, as shown in Figure 93 , supports device subclasses 0, 1, and 2 with a maximum output data rate (per lane) of 3.125 Gbps.

An external SYSREF (subclass 1) or SYNC~ (subclass 2) signal is used to align all internal clock phases and the local multiframe clock to a specific sampling clock edge. This alignment allows synchronization of multiple devices in a system and minimizes timing and alignment uncertainty.

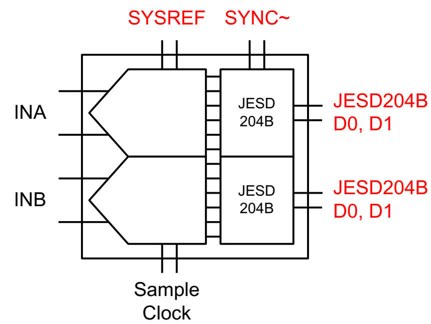


Figure 93. JESD204B Interface

Depending on the ADC sampling rate, the JESD204B output interface can be operated with either one or two lanes per ADC. The JESD204B interface can be configured using serial registers.

The JESD204B transmitter block (Figure 94) consists of the transport layer, the data scrambler, and the link layer. The transport layer maps the ADC output data into the selected JESD204B frame data format and manages if the ADC output data or test patterns are transmittied. The link layer performs the 8b and 10b data encoding as well as the synchronization and initial lane alignment using the SYNC~ input signal. Optionally, data from the transport layer can be scrambled.

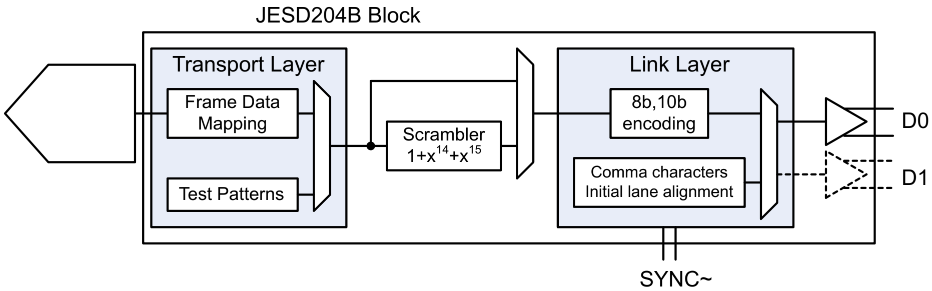


Figure 94. JESD204B Block

JESD204B Initial Lane Alignment (ILA)

When receiving device asserts the SYNC~ signal (i.e a logic low signal is applied on SYNC~P - SYNC~M), the device begins transmitting comma (K28.5) characters to establish code group synchronization (CGS).

When synchronization is complete, the receiving device de-asserts the SYNC~ signal and the ADS42JB49 and ADS42JB69 begin the initial lane alignment (ILA) sequence with the next local multiframe clock boundary. The device transmits four multiframes, each containing K frames (where K is SPI programmable). Each multiframe contains the frame start and end symbols; the second multiframe also contains the JESD204 link configuration data.

JESD204B Test Patterns

There are three different test patterns available in the transport layer of the JESD204B interface. The device supports a clock output, an encoded, and a PRBS (2^{15} – 1) pattern. These patterns can be enabled by serial register write in address 26h, bits D[7:6].

JESD204B Frame Assembly

The JESD204B standard defines the following parameters:

- L is the number of lanes per Lane.
- M is the number of converters per device.
- F is the number of octets per frame clock period.
- S is the number of samples per frame.

Table 11 lists the available JESD204B formats and valid device ranges. Ranges are limited by the maximum ADC sample frequency and the SERDES line rate.

Table 11. JESD240B Ranges

L	M	F	S	MAX ADC SAMPLING RATE (MSPS)	MAX f_{SERDES} (Gbps)
4	2	1	1	250	2.5
2	2	2	1	156.25	3.125

The detailed frame assembly in 10x and 20x modes for dual-channel operation is shown in Table 12. Note that unused lanes in 10x mode become 3-stated.

Table 12. Frame Assembly for Dual-Channel Mode(1)

LANE	LMF = 421				LMF = 222					
DA0	A_0[15:8]	A_1[15:8]	A_2[15:8]		A_0[15:8]	A_0[7:0]	A_1[15:8]	A_1[7:0]	A_2[15:8]	A_2[7:0]
DA1	A_0[7:0]	A_1[7:0]	A_2[7:0]		—	—	—	—	—	—
DB0	B_0[15:8]	B_1[15:8]	B_2[15:8]		B_0[15:8]	B_0[7:0]	B_1[15:8]	B_1[7:0]	B_2[15:8]	B_2[7:0]
DB1	B_0[7:0]	B_1[7:0]	B_2[7:0]		—	—	—	—	—	—

(1) In ADS42JB49 two LSBs of 16-bit data are padded with 00.

JESD LINK CONFIGURATION

During the lane alignment sequence, the ADS42JB69 and ADS42JB49 transmit JESD204B configuration parameters in the second multi-frame of the ILA sequence. Configuration bits are mapped in octets, as per the JESD204B standard described in Figure 95 and Table 13.

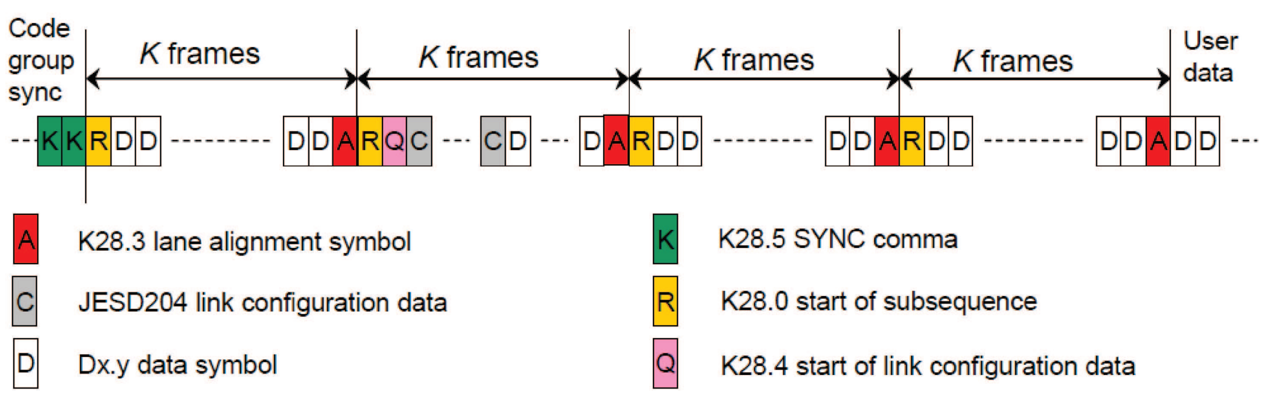


Figure 95. Initial Lane Alignment Sequence

Table 13. Mapping of Configuration Bits to Octets

Octet No	MSB	D6	D5	D4	D3	D2	D1	LSB
0	DID [7:0]							
1	ADJCNT[3:0]				BID[3:0]			
2	X	ADJDIR[0]	PHADJ[0]	LID[4:0]				
3	SCR[0]			L[4:0]				
4	F[7:0]							
5				K[4:0]				
6	M[7:0]							
7	CS[1:0]		X	N[4:0]				
8	SUBCLASSV[2:0]			N'[4:0]				
9	JESDV[2:0]			S[4:0]				
10	HD[0]	X	X	CF[4:0]				
11	RES1[7:0]							
12	RES2[7:0]							
13	FCHK[7:0]							

Configuration for 2-Lane (20x) SERDES Mode

Table 14 lists the values of the JESD204B configuration bits applicable for the 2-lane SERDES Mode. The default value of these bits after reset is also specified in the table.

Table 14. Configuration for 2-Lane SERDES Mode

PARAMETER	DESCRIPTION	PARAMETER RANGE	FIELD	ENCODING	DEFAULT VALUE AFTER RESET
ADJCNT	Number of adjustment resolution steps to adjust DAC LMFC. Applies to subclass 2 operation only.	0 ... 15	ADJCNT[3:0]	Binary value	0
ADJDIR	Direction to adjust DAC LMFC 0 – Advance 1 – Delay applies to subclass 2 operation only	0 … 1	ADJDIR[0]	Binary value	0
BID	Bank ID – extension to DID	0 ... 15	BID[3:0]	Binary value	0
CF	No. of control words per frame clock period per link	0 ... 32	CF[4:0]	Binary value	0
CS	No. of control bits per sample	0 ... 3	CS[1:0]	Binary value	0
DID	Device (= link) identification no.	0 ... 255	DID[7:0]	Binary value	0
F	No. of octets per frame	1 ... 256	F[7:0]	Binary value minus 1	1
HD	High-density format	0 ... 1	HD[0]	Binary value	0
JESDV	JESD204 version 000 – JESD204A 001 – JESD204B	0 … 7	JESDV[2:0]	Binary value	1
K	No. of frames per multi-frame	1 ... 32	K[4:0]	Binary value minus 1	8

Table 14. Configuration for 2-Lane SERDES Mode (continued)

PARAMETER	DESCRIPTION	PARAMETER RANGE	FIELD	ENCODING	DEFAULT VALUE AFTER RESET
L	No. of lanes per converter device (link)	1 ... 32	L[4:0]	Binary value minus 1	0
LID	Lane identification no. (within link)	0 ... 31	LID[4:0]	Binary value	LID[0] = 0, LID[1] = 1
M	No. of converters per device	1 ... 256	M[7:0]	Binary value minus 1	1
N	Converter resolution	1 ... 32	N[4:0]	Binary value minus 1	15
N’	Total no. of bits per sample	1 ... 32	N'[4:0]	Binary value minus 1	15
PHADJ	Phase adjustment request to DAC subclass 2 only.	0 ... 1	PHADJ[0]	Binary value	0
S	No. of samples per converter per frame cycle	1 ... 32	S[4:0]	Binary value minus 1	0
SCR	Scrambling enabled	0 ... 1	SCR[0]	Binary value	0
SUBCLASSV	Device subclass version 000 – Subclass 0 001 – Subclass 1 010 – Subclass 2	0 … 7	SUBCLASSV[2:0]	Binary value	2
RES1	Device subclass version 000 – Subclass 0 001 – Subclass 1 010 – Subclass 2	0 ... 255	RES1[7:0]	Binary value	0
RES2	Reserved field 2	0 ... 255	RES2[7:0]	Binary value	0
CHKSUM	Checksum Σ (all above fields) mod 256	0 ... 255	FCHK[7:0]	Binary value	44, 45

Configuration for 4-Lane (10x) SERDES Mode

Table 15 lists the values of the JESD204 configuration bits applicable for the 4-lane SERDES Mode. The default value of these bits after reset is also specified in the table.

Table 15. Configuration for 4-Lane SERDES Mode

PARAMETER	DESCRIPTION	PARAMETER RANGE	FIELD	ENCODING	DEFAULT VALUE AFTER RESET
ADJCNT	Number of adjustment resolution steps to adjust DAC LMFC. Applies to subclass 2 operation only.	0 ... 15	ADJCNT[3:0]	Binary value	0
ADJDIR	Direction to adjust DAC LMFC 0 – Advance 1 – Delay applies to subclass 2 operation only	0 … 1	ADJDIR[0]	Binary value	0
BID	Bank ID – extension to DID	0 ... 15	BID[3:0]	Binary value	0
CF	No. of control words per frame clock period per link	0 ... 32	CF[4:0]	Binary value	0
CS	No. of control bits per sample	0 ... 3	CS[1:0]	Binary value	0
DID	Device (= link) identification no.	0 ... 255	DID[7:0]	Binary value	0
F	No. of octets per frame	1 ... 256	F[7:0]	Binary value minus 1	0
HD	High-density format	0 ... 1	HD[0]	Binary value	1
JESDV	JESD204 version 000 – JESD204A 001 – JESD204B	0 … 7	JESDV[2:0]	Binary value	1
K	No. of frames per multi-frame	1 ... 32	K[4:0]	Binary value minus 1	16
L	No. of lanes per converter device (link)	1 ... 32	L[4:0]	Binary value minus 1	3
LID	Lane identification no (within link)	0 ... 31	LID[4:0]	Binary value	LID[0] = 0, LID[1] = 1, LID[2] = 2, LID[3] = 3
M	No. of converters per device	1 ... 256	M[7:0]	Binary value minus 1	1
N	Converter resolution	1 ... 32	N[4:0]	Binary value minus 1	15
N’	Total no. of bits per sample	1 ... 32	N'[4:0]	Binary value minus 1	15
PHADJ	Phase adjustment request to DAC subclass 2 only.	0 ... 1	PHADJ[0]	Binary value	0
S	No. of samples per converter per frame cycle	1 ... 32	S[4:0]	Binary value minus 1	0
SCR	Scrambling enabled	0 ... 1	SCR[0]	Binary value	0
SUBCLASSV	Device subclass version 000 – Subclass 0 001 – Subclass 1 010 – Subclass 2	0 … 7	SUBCLASSV[2:0]	Binary value	2

Table 15. Configuration for 4-Lane SERDES Mode (continued)

PARAMETER	DESCRIPTION	PARAMETER RANGE	FIELD	ENCODING	DEFAULT VALUE AFTER RESET
RES1	Device subclass version 000 – Subclass 0 001 – Subclass 1 010 – Subclass 2	0 ... 255	RES1[7:0]	Binary value	0
RES2	Reserved field 2	0 ... 255	RES2[7:0]	Binary value	0
CHKSUM	Checksum Σ(all above fields)mod 256	0 ... 255	FCHK[7:0]	Binary value	54, 55, 56, 57

CML Outputs

The device JESD204B transmitter uses differential CML output drivers. The CML output current is programmable from 5 mA to 20 mA using register settings.

The output driver includes an internal 50-Ω termination to IOVDD supply. External 50-Ω termination resistors connected to receiver common-mode voltage should be placed close to receiver pins. AC coupling can be used to avoid the common-mode mismatch between transmitter and receiver, as shown in Figure 96.

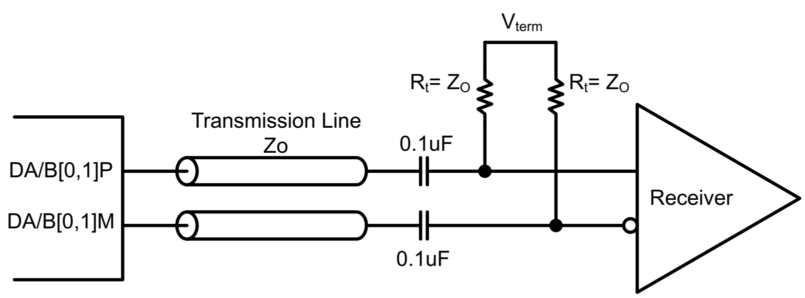


Figure 96. CML Output Connections

Figure 97 and Figure 98 show the data eye measurements of the device JESD204B transmitter against the JESD204B transmitter mask at 2.5 GBPS (10x mode) and 3.125 GBPS (20x mode), respectively.

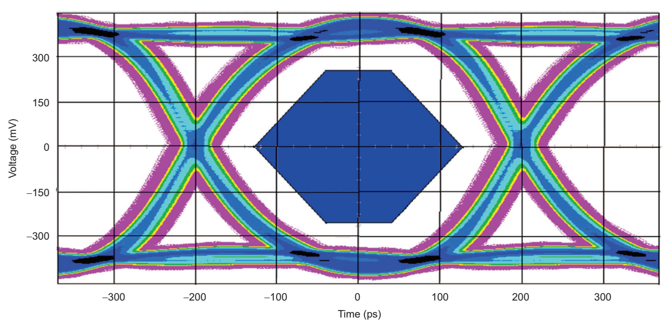


Figure 97. Eye Diagram: 2.5 Gbps

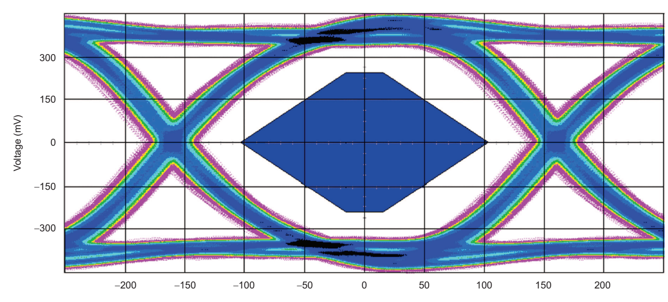


Figure 98. Eye Diagram: 3.125 Gbps

DEFINITION OF SPECIFICATIONS

Analog Bandwidth: The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low-frequency value.

Aperture Delay: The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs. This delay is different across channels. The maximum variation is specified as aperture delay variation (channel-to-channel).

Aperture Uncertainty (Jitter): The sample-to-sample variation in aperture delay.

Clock Pulse Width and Duty Cycle: The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

Maximum Conversion Rate: The maximum sampling rate at which specified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate: The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL): An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

Integral Nonlinearity (INL): The INL is the deviation of the ADC transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Gain Error: Gain error is the deviation of the ADC actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range. Gain error has two components: error as a result of reference inaccuracy (E_{GREF}) and error as a result of the channel (E_{GCHAN}). Both errors are specified independently as E_{GREF} and E_{GCHAN}.

To a first-order approximation, the total gain error is $E_{TOTAL} \sim E_{GREF} + E_{GCHAN}$.

For example, if $E_{TOTAL} = \pm0.5\%$, the full-scale input varies from $(1 – 0.5 / 100) \times FS_{ideal}$ to $(1 + 0.5 / 100) \times FS_{ideal}$.

Offset Error: The offset error is the difference, given in number of LSBs, between the ADC actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into millivolts.

Temperature Drift: The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX}. Temperature drift is calculated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference $T_{MAX} – T_{MIN}$.

Signal-to-Noise Ratio (SNR): SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and the first nine harmonics.

$$SNR = 10Log^{10} \frac{P_S}{P_N} \tag{4}$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Signal-to-Noise and Distortion (SINAD): SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10Log^{10} \frac{P_S}{P_N + P_D} \tag{5}$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Effective Number of Bits (ENOB): ENOB is a measure of the converter performance as compared to the theoretical limit based on quantization noise.

$$ENOB = \frac{SINAD - 1.76}{6.02} \quad (6)$$

Total Harmonic Distortion (THD): THD is the ratio of the power of the fundamental (P_S) to the power of the first nine harmonics (P_D).

$$THD = 10Log^{10} \frac{P_S}{P_N} \quad (7)$$

THD is typically given in units of dBc (dB to carrier).

Spurious-Free Dynamic Range (SFDR): The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion (IMD3): IMD3 is the ratio of the power of the fundamental (at frequencies f_1 and f_2) to the power of the worst spectral component at either frequency $2f_1 – f_2$ or $2f_2 – f_1$. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

DC Power-Supply Rejection Ratio (DC PSRR): DC PSSR is the ratio of the change in offset error to a change in analog supply voltage. The dc PSRR is typically given in units of mV/V.

AC Power-Supply Rejection Ratio (AC PSRR): AC PSRR is the measure of rejection of variations in the supply voltage by the ADC. If ΔV_{SUP} is the change in supply voltage and ΔV_{OUT} is the resultant change of the ADC output code (referred to the input), then:

$$PSRR = 20Log^{10} \frac{\Delta V_{OUT}}{\Delta V_{SUP}} \text{ (Expressed in dBc)} \quad (8)$$

Voltage Overload Recovery: The number of clock cycles taken to recover to less than 1% error after an overload on the analog inputs. This is tested by separately applying a sine wave signal with 6 dB positive and negative overload. The deviation of the first few samples after the overload (from the expected values) is noted.

Common-Mode Rejection Ratio (CMRR): CMRR is the measure of rejection of variation in the analog input common-mode by the ADC. If ΔV_{CM_IN} is the change in the common-mode voltage of the input pins and ΔV_{OUT} is the resulting change of the ADC output code (referred to the input), then:

$$CMRR = 20Log^{10} \frac{\Delta V_{OUT}}{\Delta V_{CM}} \text{ (Expressed in dBc)} \quad (9)$$

Crosstalk (only for multichannel ADCs): Crosstalk is a measure of the internal coupling of a signal from an adjacent channel into the channel of interest. Crosstalk is specified separately for coupling from the immediate neighboring channel (near-channel) and for coupling from channel across the package (far-channel). Crosstalk is usually measured by applying a full-scale signal in the adjacent channel. Crosstalk is the ratio of the power of the coupling signal (as measured at the output of the channel of interest) to the power of the signal applied at the adjacent channel input. Crosstalk is typically expressed in dBc.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (August 2013) to Revision E	Page
• Changed document status to Production Data	1
• Deleted second footnote from Ordering Information table	2

Changes from Revision C (July 2013) to Revision D	Page
• Updated front page block diagram	1
• Changed 2-V_{PP} Full-Scale *INL* maximum specification in ADS42JB49 Electrical Characteristics table	5

Changes from Revision B (July 2013) to Revision C	Page
• Added Internal Dither in Features Section	1
• Changed From "The devices provide excellent" to "The devices employ internal dither algorithms to provide"	1
• Changed 2-V_{PP} Full-Scale *INL* maximum specification in ADS42JB69 Electrical Characteristics table	4
• Deleted 2.5-V_{PP} Full-Scale *INL* maximum specification in ADS42JB69 Electrical Characteristics table	4
• Changed 2-V_{PP} Full-Scale *INL* maximum specification in ADS42JB49 Electrical Characteristics table	5
• Deleted 2.5-V_{PP} Full-Scale *INL* maximum specification in ADS42JB49 Electrical Characteristics table	5
• Changed E_{GREF} specifications in General Electrical Characteristics table	6

Changes from Revision A (November 2012) to Revision B	Page
• Changed document status to Mixed Status	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS42JB49IRGC25	ACTIVE	VQFN	RGC	64	25	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 85	AZ42JB49	Samples
ADS42JB49IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 85	AZ42JB49	Samples
ADS42JB49IRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 85	AZ42JB49	Samples
ADS42JB69IRGC25	ACTIVE	VQFN	RGC	64	25	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 85	AZ42JB69	Samples
ADS42JB69IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 85	AZ42JB69	Samples
ADS42JB69IRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 85	AZ42JB69	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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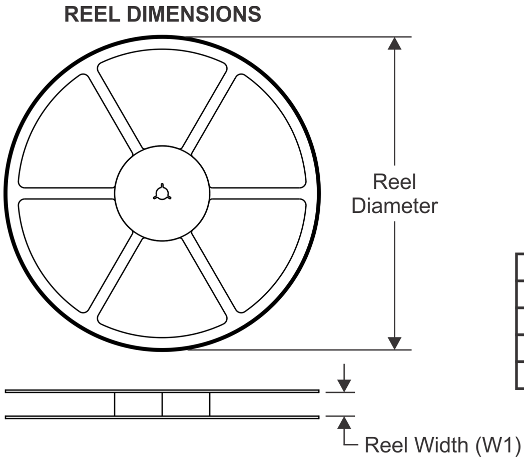
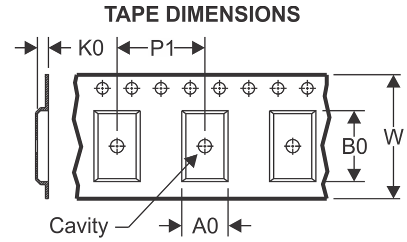
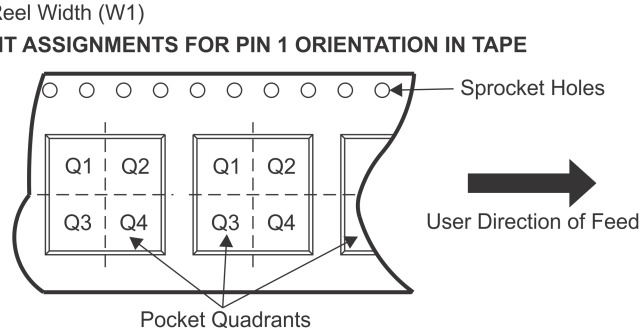
TAPE AND REEL INFORMATION





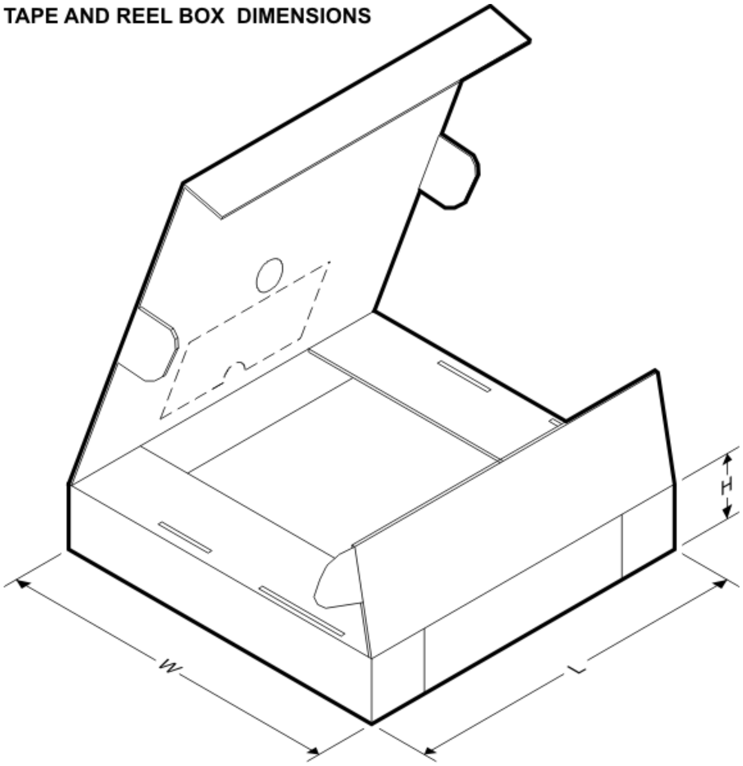
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS42JB49IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS42JB49IRGCT	VQFN	RGC	64	250	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS42JB69IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS42JB69IRGCT	VQFN	RGC	64	250	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

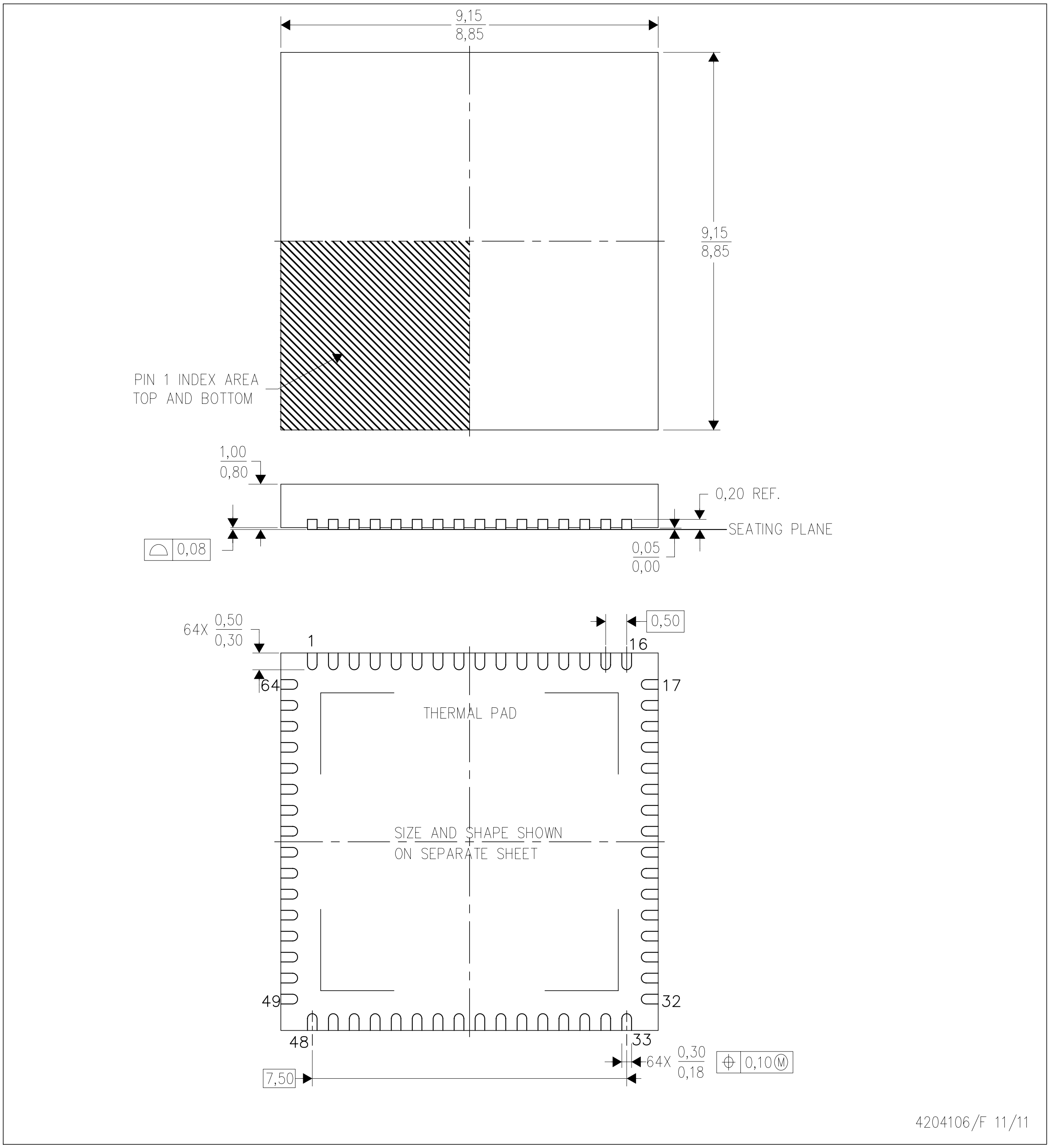
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS42JB49IRGCR	VQFN	RGC	64	2000	336.6	336.6	28.6
ADS42JB49IRGCT	VQFN	RGC	64	250	336.6	336.6	28.6
ADS42JB69IRGCR	VQFN	RGC	64	2000	336.6	336.6	28.6
ADS42JB69IRGCT	VQFN	RGC	64	250	336.6	336.6	28.6

RGC(S-PVQFN-N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No-leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

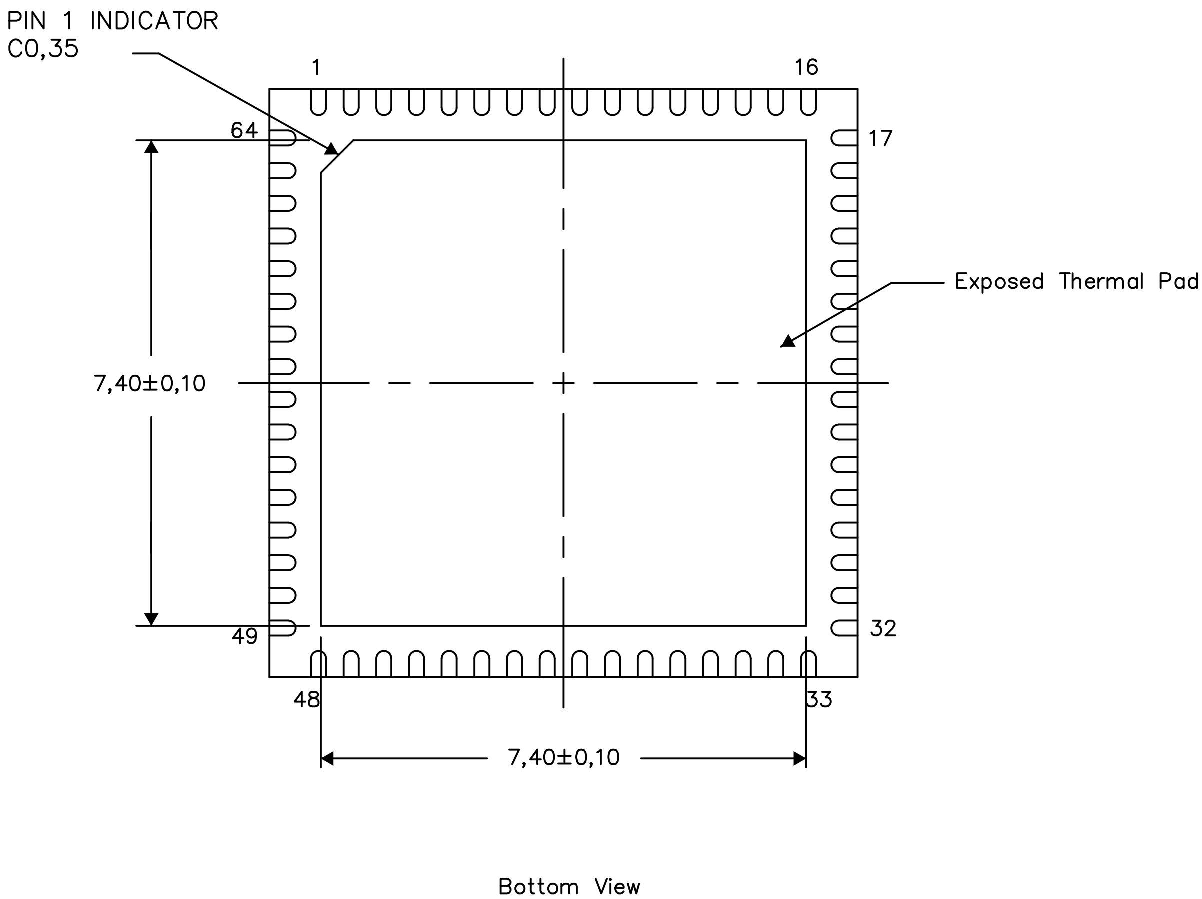
RGC (S-PVQFN-N64) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

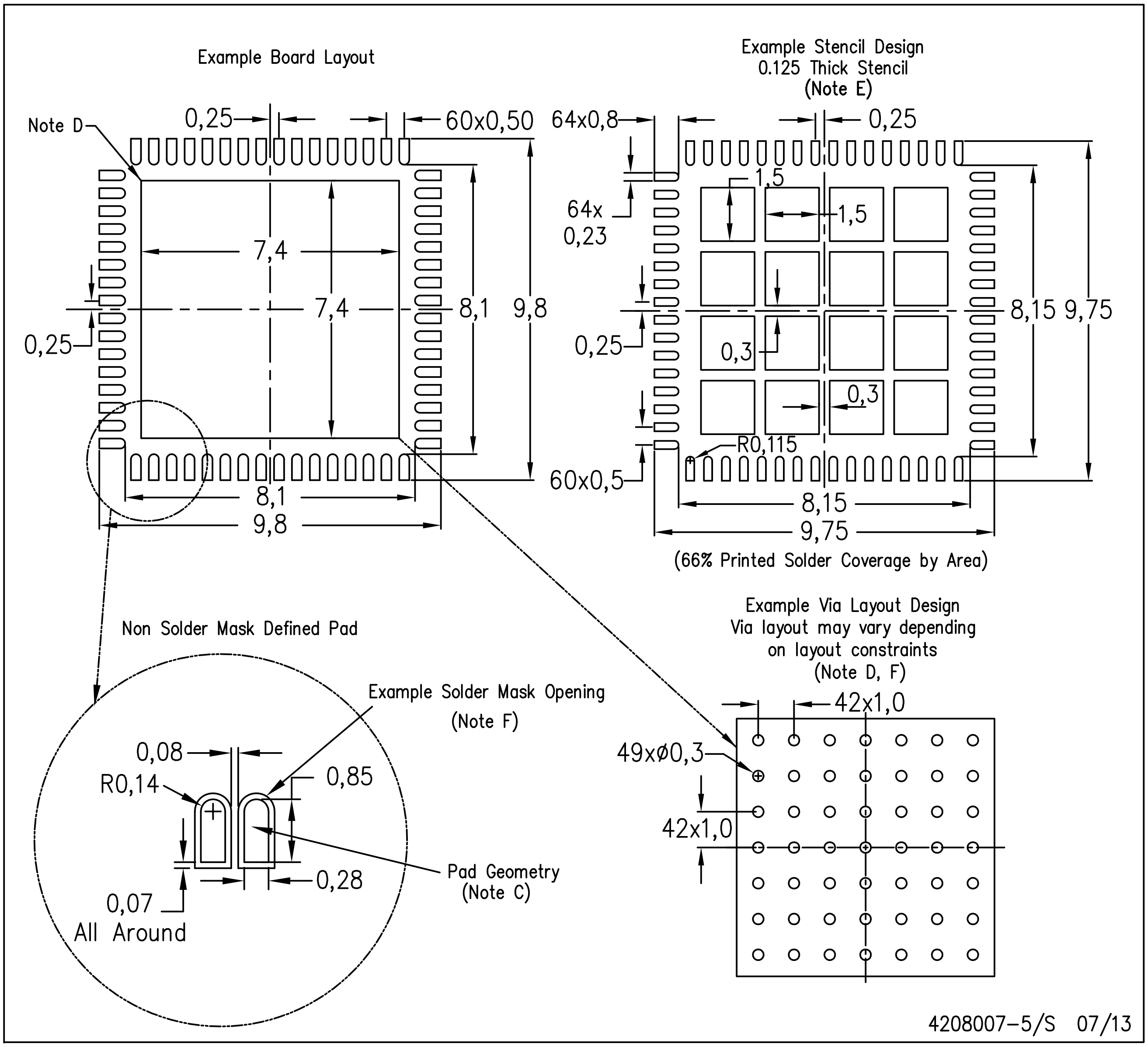


Exposed Thermal Pad Dimensions

4206192-4/AB 10/13

NOTE: A. All linear dimensions are in millimeters

RGC (S-PVQFN-N64) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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