Integrated Analog Front-End for Heart Rate Monitors and Low-Cost Pulse Oximeters

Check for Samples: AFE4400

FEATURES

- **Fully-Integrated Analog Front-End for Pulse Oximeter Applications:**
  - **Flexible Pulse Sequencing and Timing Control**
- **Transmit:**
  - **Integrated LED Driver (H-Bridge or Push/Pull)**
  - **95-dB Dynamic Range**
  - **LED Current:**
    - **Programmable to 50 mA with 8-Bit Current Resolution**
  - **Low Power:**
    - **100 µA + Average LED Current**
  - **Programmable LED On-Time**
  - **Independent LED2 and LED1 Current Reference**
- **Receive Channel with High Dynamic Range:**
  - **13 Noise-Free Bits**
  - **Low Power: < 670 µA at 3.3-V Supply**
  - **Flexible Receive Sample Time**
  - **Flexible Transimpedance Amplifier with Programmable LED Settings**
  - **Integrated Digital Ambient Estimation and Subtraction**
- **Integrated Fault Diagnostics:**
  - **Photodiode and LED Open and Short Detection**
  - **Cable On/Off Detection**
- **Supplies:**
  - **Rx = 2.0 V to 3.6 V**
  - **Tx = 3.0 V to 5.25 V**
- **Package: Compact QFN-40 (6 mm × 6 mm)**
- **Specified Temperature Range: 0°C to +70°C**

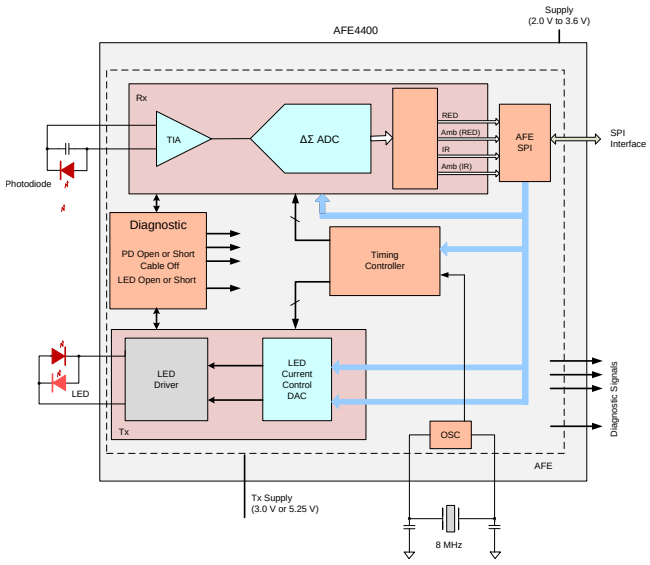
APPLICATIONS

- **Low-Cost Medical Pulse Oximeter Applications**
- **Optical HRM**
- **Industrial Photometry Applications**

DESCRIPTION

The AFE4400 is a fully-integrated analog front-end (AFE) that is ideally suited for pulse oximeter applications. The device consists of a low-noise receiver channel with an integrated analog-to-digital converter (ADC), an LED transmit section, and diagnostics for sensor and LED fault detection. The AFE4400 is a very configurable timing controller. This flexibility enables the user to have complete control of the device timing characteristics. To ease clocking requirements and provide a low-jitter clock to the AFE4400, an oscillator is also integrated that functions from an external crystal. The device communicates to an external microcontroller or host processor using an SPI™ interface.

The AFE4400 is a complete AFE solution packaged in a single, compact QFN-40 package (6 mm × 6 mm) and is specified over the operating temperature range of 0°C to +70°C.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FAMILY AND ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	LED DRIVE CONFIGURATION	LED DRIVE CURRENT (mA, max)	Tx POWER SUPPLY (V)	OPERATING TEMPERATURE RANGE
AFE4400	QFN-40	Bridge, push-pull	50	3 to 5.25	0°C to +70°C
AFE4490	QFN-40	Bridge, push-pull	50, 75, 100, 150, and 200	3 to 5.25	–40°C to +85°C

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		VALUE	UNIT
AVDD to AVSS		–0.3 to +7	V
DVDD to DGND		–0.3 to +7	V
AGND to DGND		–0.3 to +0.3	V
Analog input to AVSS		AVSS – 0.3 to AVDD + 0.3	V
Digital input to DVDD		DVSS – 0.3 to DVDD + 0.3	V
Input current to any pin except supply pins(2)		±7	mA
Input current	Momentary	±50	mA
	Continuous	±7	mA
Operating temperature range		0 to +70	°C
Storage temperature range, T_{stg}		–60 to +150	°C
Maximum junction temperature, T_J		+125	°C
Electrostatic discharge (ESD) ratings	Human body model (HBM) JEDEC standard 22, test method A114-C.01, all pins	±4000	V
	Charged device model (CDM) JEDEC standard 22, test method C101, all pins	±1500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing beyond the supply rails must be current-limited to 10 mA or less.

THERMAL INFORMATION

THERMAL METRIC(1)		AFE4400 RHA (QFN) 40 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	35	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	31	
θ_{JB}	Junction-to-board thermal resistance	26	
ψ_{JT}	Junction-to-top characterization parameter	0.1	
ψ_{JB}	Junction-to-board characterization parameter	n/a	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range, unless otherwise noted.

PARAMETER			VALUE	UNIT
SUPPLIES				
RX_ANA_SUP	AFE analog supply		2.0 to 3.6	V
RX_DIG_SUP	AFE digital supply		2.0 to 3.6	V
TX_CTRL_SUP	Transmit controller supply		3.0 to 5.25	V
LED_DRV_SUP	Transmit LED driver supply	H-bridge or common anode configuration	[3.0 or (1.0 + V_{LED} + V_{CABLE})(1)(2), whichever is greater] to 5.25	V
	Difference between LED_DRV_SUP and TX_CTRL_SUP		–0.3 to +0.3	V
TEMPERATURE				
	Specified temperature range		0 to +70	°C
	Storage temperature range		–60 to +150	°C

(1) V_{LED} refers to the maximum voltage drop across the external LED (at maximum LED current) connected between the TXP and TXN pins (in H-bridge mode) and from the TXP and TXN pins to LED_DRV_SUP (in the common anode configuration).
(2) V_{CABLE} refers to voltage drop across any cable, connector, or any other component in series with the LED.

ELECTRICAL CHARACTERISTICS

Minimum and maximum specifications are at T_A = –20°C to +85°C. Typical specifications are at +25°C.
All specifications are at RX_ANA_SUP = RX_DIG_SUP = 3 V, TX_CTRL_SUP = LED_DRV_SUP = 3.3 V, stage 2 amplifier disabled, and f_{CLK} = 8 MHz, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PERFORMANCE (Full-Signal Chain)						
I_{IN_FS}	Full-scale input current	R_F = 10 kΩ		50		µA
		R_F = 25 kΩ		20		µA
		R_F = 50 kΩ		10		µA
		R_F = 100 kΩ		5		µA
		R_F = 250 kΩ		2		µA
		R_F = 500 kΩ		1		µA
		R_F = 1 MΩ		0.5		µA
PRF	Pulse repetition frequency		62.5		5000	SPS
DC_{PRF}	PRF duty cycle				25%	
CMRR	Common-mode rejection ratio	f_{CM} = 50 Hz and 60 Hz, LED1 and LED2 with R_{SERIES} = 500 kΩ, R_F = 500 kΩ		75		dB
		f_{CM} = 50 Hz and 60 Hz, LED1-AMB and LED2-AMB with R_{SERIES} = 500 kΩ, R_F = 500 kΩ		95		dB
PSRR	Power-supply rejection ratio	f_{PS} = 50 Hz, 60 Hz at PRF = 200 Hz		100		dB
		f_{PS} = 50 Hz, 60 Hz at PRF = 600 Hz		106		dB
$PSRR_{LED}$	PSRR, transmit LED driver	With respect to ripple on LED_DRV_SUP		75		dB
$PSRR_{Tx}$	PSRR, transmit control	With respect to ripple on TX_CTRL_SUP		60		dB
$PSRR_{Rx}$	PSRR, receiver	With respect to ripple on RX_ANA_SUP and RX_DIG_SUP		60		dB
	Total integrated noise current, input-referred (receiver with transmitter loop back, 0.1-Hz to 5-Hz bandwidth)	R_F = 100 kΩ, PRF = 600 Hz, duty cycle = 5%		36		pA_{RMS}
		R_F = 500 kΩ, PRF = 600 Hz, duty cycle = 5%		13		pA_{RMS}
N_{FB}	Noise-free bits (receiver with transmitter loop back, 0.1-Hz to 5-Hz bandwidth)	R_F = 100 kΩ, PRF = 600 Hz, duty cycle = 5%		14.3		Bits
		R_F = 500 kΩ, PRF = 600 Hz, duty cycle = 5%		13.5		Bits
RECEIVER FUNCTIONAL BLOCK LEVEL SPECIFICATION						
	Total integrated noise current, input referred (receiver alone) over 0.1-Hz to 5-Hz bandwidth	R_F = 500 kΩ, ambient cancellation enabled, stage 2 gain = 4, PRF = 1200 Hz, LED duty cycle = 25%		1.4		pA_{RMS}
		R_F = 500 kΩ, ambient cancellation enabled, stage 2 gain = 4, PRF = 1200 Hz, LED duty cycle = 5%		5		pA_{RMS}
I-V TRANSIMPEDANCE AMPLIFIER						
G	Gain	R_F = 10 kΩ to 1 MΩ	See the *Receiver Channel* section for details			V/µA
	Gain accuracy			±7%		
	Feedback resistance	R_F	10k, 25k, 50k, 100k, 250k, 500k, and 1M			Ω
	Feedback resistor tolerance	R_F		±20%		
	Feedback capacitance	C_F	5, 10, 25, 50, 100, and 250			pF
	Feedback capacitor tolerance	C_F		±20%		
	Full-scale differential output voltage			1		V
	Common-mode voltage on input pins	Set internally		0.9		V
	External differential input capacitance	Includes equivalent capacitance of photodiode, cables, EMI filter, and so forth	10		1000	pF
	Shield output voltage, V_{CM}	With a 1-kΩ series resistor and a 10-nF decoupling capacitor to ground		0.9		V

ELECTRICAL CHARACTERISTICS (continued)

Minimum and maximum specifications are at T_A = –20°C to +85°C. Typical specifications are at +25°C.
All specifications are at RX_ANA_SUP = RX_DIG_SUP = 3 V, TX_CTRL_SUP = LED_DRV_SUP = 3.3 V, stage 2 amplifier disabled, and f_{CLK} = 8 MHz, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AMBIENT CANCELLATION STAGE						
	Gain			0, 3.5, 6, 9.5, and 12		dB
	Current DAC range		0		10	µA
	Current DAC step size			1		µA
LOW-PASS FILTER						
	Low-pass corner frequency	3-dB attenuation		500		Hz
	Pass-band attenuation, 2 Hz to 10 Hz	Duty cycle = 25%		0.004		dB
		Duty cycle = 10%		0.041		dB
	Filter settling time	After diagnostics mode		28		ms
ANALOG-TO-DIGITAL CONVERTER						
	Resolution				22	Bits
	Sample rate	See the *ADC Operation and Averaging Module* section		4 × PRF		SPS
	ADC full-scale voltage			±1.2		V
	ADC conversion time	See the *ADC Operation and Averaging Module* section	50		PRF / 4	µs
	ADC reset time		2			t_{CLK}
TRANSMITTER						
	Output current range			Selectable, 0 to 50 (see the LEDCNTRL: LED Control Register for details)		mA
	LED current DAC error			±10%		
	Output current resolution			8		Bits
	Transmitter noise dynamic range, over 0.1-Hz to 5-Hz bandwidth	At 5-mA output current		95		dB
		At 25-mA output current		95		dB
		At 50-mA output current		95		dB
	Voltage on TXP (or TXN) pin when low-side switch connected to TXP (or TXN) turns on	At 50-mA output current		1.0 + (voltage drop across LED, cable, and so forth) to 5.25		V
	Minimum sample time of LED1 and LED2 pulses			50		µs
	LED current DAC leakage current	LED_ON = 0		1		µA
		LED_ON = 1		50		µA
	LED current DAC linearity	Percent of full-scale current		0.5%		
	Output current settling time (with resistive load)	From zero current to 50 mA		7		µs
		From 50 mA to zero current		7		µs
DIAGNOSTICS						
	Duration of diagnostics state machine	Start of diagnostics after the DIAG_EN register bit is set. End of diagnostic is indicated by DIAG_END going high.		16		ms
	Open fault resistance			> 100		kΩ
	Short fault resistance			< 10		kΩ
INTERNAL OSCILLATOR						
f_{CLKOUT}	CLKOUT frequency	With an 8-MHz crystal connected to the XIN, XOUT pins		4		MHz
	CLKOUT duty cycle			50%		
	Crystal oscillator start-up time	With an 8-MHz crystal connected to the XIN, XOUT pins		200		µs

ELECTRICAL CHARACTERISTICS (continued)

Minimum and maximum specifications are at T_A = –20°C to +85°C. Typical specifications are at +25°C.
All specifications are at RX_ANA_SUP = RX_DIG_SUP = 3 V, TX_CTRL_SUP = LED_DRV_SUP = 3.3 V, stage 2 amplifier disabled, and f_{CLK} = 8 MHz, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXTERNAL CLOCK						
	Maximum allowable external clock jitter	For SPO2 applications		50		ps
		For optical heart rate only			1000	ps
	External clock input frequency	±10%		8		MHz
	External clock input voltage	Voltage input high (V_{IH})	0.75 × RX_DIG_SUP			V
		Voltage input low (V_{IL})	0.25 × RX_DIG_SUP			V
TIMING						
	Wake-up time from complete power-down			1000		ms
	Wake-up time from Rx power-down			100		µs
	Wake-up time from Tx power-down			1000		ms
$t_{\overline{RESET}}$	Active low $\overline{RESET}$ pulse duration			1		ms
$t_{DIAGEND}$	DIAG_END pulse duration at the completion of diagnostics			4		CLKOUT cycles
t_{ADCRDY}	ADC_RDY pulse duration			1		CLKOUT cycle
DIGITAL SIGNAL CHARACTERISTICS						
V_{IH}	Logic high input voltage	AFE_$\overline{PDN}$, SCLK, SPISIMO, SPISTE, $\overline{RESET}$	0.8 DVDD	> 1.3	DVDD + 0.1	V
V_{IL}	Logic low input voltage	AFE_$\overline{PDN}$, SCLK, SPISIMO, SPISTE, $\overline{RESET}$	–0.1	< 0.4	0.2 DVDD	V
I_{IN}	Logic input current	0 V < $V_{DigitalInput}$ < DVDD	–10		10	µA
V_{OH}	Logic high output voltage	DIAG_END, LED_ALM, PD_ALM, SPISOMI, ADC_RDY, CLKOUT	0.9 DVDD	> (RX_DIG_SUP – 0.2 V)		V
V_{OL}	Logic low output voltage	DIAG_END, LED_ALM, PD_ALM, SPISOMI, ADC_RDY, CLKOUT		< 0.4	0.1 DVDD	V
SUPPLY CURRENT						
	Receiver analog supply current	RX_ANA_SUP = 3.0 V, with 8-MHz clock running, Rx stage 2 disabled		0.6		mA
		RX_ANA_SUP = 3.0 V, with 8-MHz clock running, Rx stage 2 enabled		0.7		mA
	Receiver digital supply current	RX_DIG_SUP = 3.0 V		0.27		mA
LED_DRV_SUP	LED driver supply current	With zero LED current setting		55		µA
TX_CTRL_SUP	Transmitter control supply current			15		µA
	Complete power-down (using AFE_PDN pin)	Receiver current only (RX_ANA_SUP)		3		µA
		Receiver current only (RX_DIG_SUP)		3		µA
		Transmitter current only (LED_DRV_SUP)		1		µA
		Transmitter current only (TX_CTRL_SUP)		1		µA
	Power-down Rx alone	Receiver current only (RX_ANA_SUP)		220		µA
		Receiver current only (RX_DIG_SUP)		220		µA
	Power-down Tx alone	Transmitter current only (LED_DRV_SUP)		2		µA
		Transmitter current only (TX_CTRL_SUP)		2		µA

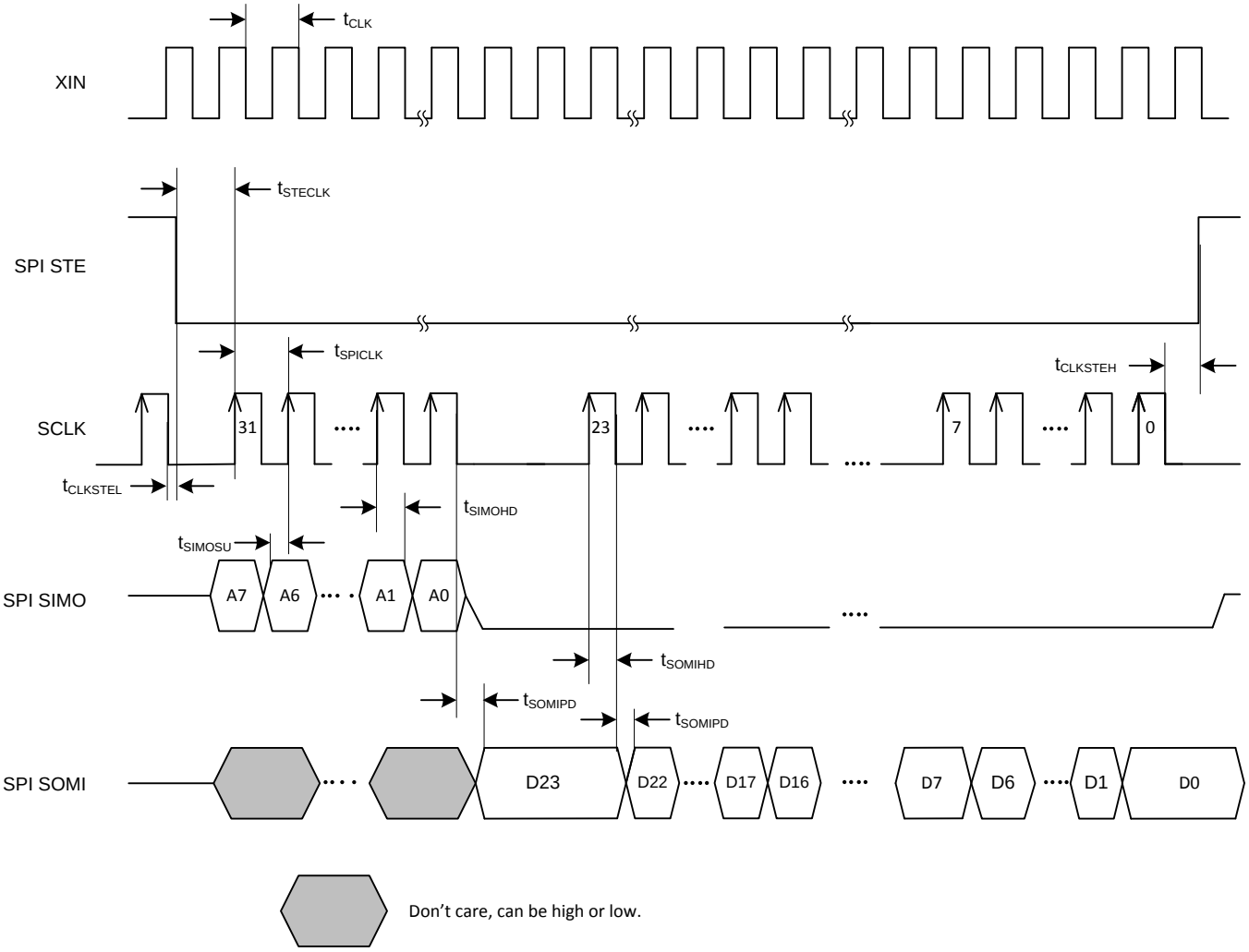
ELECTRICAL CHARACTERISTICS (continued)

Minimum and maximum specifications are at T_A = –20°C to +85°C. Typical specifications are at +25°C.
All specifications are at RX_ANA_SUP = RX_DIG_SUP = 3 V, TX_CTRL_SUP = LED_DRV_SUP = 3.3 V, stage 2 amplifier disabled, and f_{CLK} = 8 MHz, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER DISSIPATION						
Quiescent power dissipation		Normal operation (excluding LEDs)		2.84		mW
		Power-down		0.1		mW
Power-down with the AFE_PDN pin	LED_DRV_SUP	LED_DRV_SUP current value. Does not include LED current.		1		µA
	TX_CTRL_SUP			1		µA
	RX_ANA_SUP			5		µA
	RX_DIG_SUP			0.1		µA
Power-down with the PDNAFE register bit	LED_DRV_SUP	LED_DRV_SUP current value. Does not include LED current.		1		µA
	TX_CTRL_SUP			1		µA
	RX_ANA_SUP			15		µA
	RX_DIG_SUP			20		µA
Power-down Rx	LED_DRV_SUP	LED_DRV_SUP current value. Does not include LED current.		50		µA
	TX_CTRL_SUP			15		µA
	RX_ANA_SUP			220		µA
	RX_DIG_SUP			220		µA
Power-down Tx	LED_DRV_SUP	LED_DRV_SUP current value. Does not include LED current.		2		µA
	TX_CTRL_SUP			2		µA
	RX_ANA_SUP			600		µA
	RX_DIG_SUP			230		µA
After reset, with 8-MHz clock running	LED_DRV_SUP	LED_DRV_SUP current value. Does not include LED current.		55		µA
	TX_CTRL_SUP			15		µA
	RX_ANA_SUP			600		µA
	RX_DIG_SUP			230		µA
With stage 2 mode enabled and 8-MHz clock running	LED_DRV_SUP	LED_DRV_SUP current value. Does not include LED current.		55		µA
	TX_CTRL_SUP			15		µA
	RX_ANA_SUP			700		µA
	RX_DIG_SUP			270		µA

PARAMETRIC MEASUREMENT INFORMATION

SERIAL INTERFACE TIMING



(1) The SPI_READ register bit must be enabled before attempting a register read.

(2) Specify the register address whose contents must be read back on A[7:0].

(3) The AFE outputs the contents of the specified register on the SOMI pin.

Figure 1. Serial Interface Timing Diagram, Read Operation (1)(2)(3)

PARAMETRIC MEASUREMENT INFORMATION (continued)

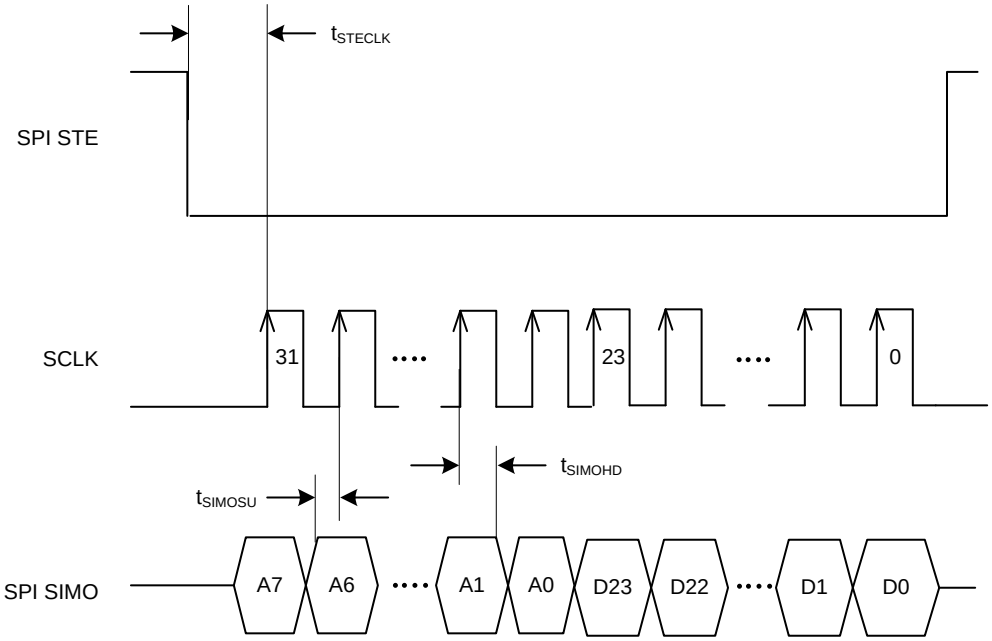


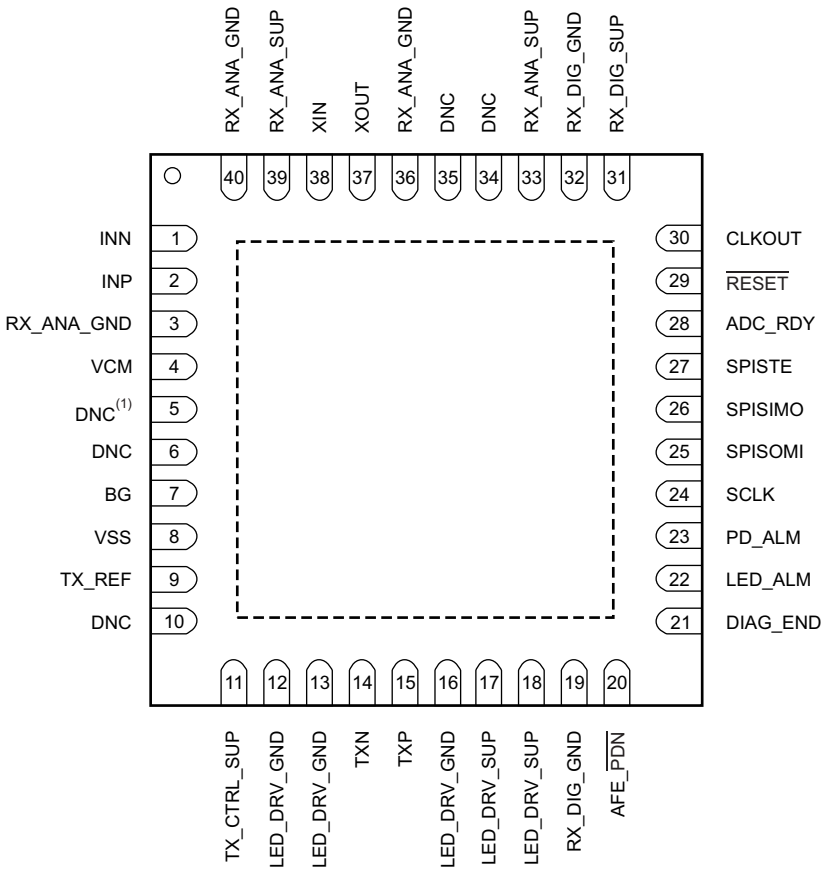
Figure 2. Serial Interface Timing Diagram, Write Operation

Table 1. Timing Requirements for Figure 1 and Figure 2

PARAMETER		MIN	TYP	MAX	UNIT
t_{CLK}	Clock frequency on XIN pin		8		MHz
t_{SCLK}	Serial shift clock period	62.5			ns
t_{STECLK}	STE low to SCLK rising edge, setup time	10			ns
$t_{CLKSTEH,L}$	SCLK transition to SPI STE high or low	10			ns
t_{SIMOSU}	SIMO data to SCLK rising edge, setup time	10			ns
t_{SIMOHD}	Valid SIMO data after SCLK rising edge, hold time	10			ns
t_{SOMIPD}	SCLK falling edge to valid SOMI, setup time	17			ns
t_{SOMIHD}	SCLK rising edge to invalid data, hold time	0.5			t_{SCLK}

PIN CONFIGURATION

RHA PACKAGE
QFN-40
(Top View)



(1) DNC = Do not connect.

PIN DESCRIPTIONS

NAME	NO.	FUNCTION	DESCRIPTION
ADC_RDY	28	Digital	Output signal that indicates ADC conversion completion. Can be connected to the interrupt input pin of an external microcontroller.
AFE_$\overline{\text{PDN}}$	20	Digital	AFE-only power-down input; active low. Can be connected to the port pin of an external microcontroller.
BG	7	Reference	Decoupling capacitor for internal band-gap voltage to ground. (2.2-µF decoupling capacitor to ground)
CLKOUT	30	Digital	Buffered 4-MHz output clock output. Can be connected to the clock input pin of an external microcontroller.
DIAG_END	21	Digital	Output signal that indicates completion of diagnostics. Can be connected to the port pin of an external microcontroller.
DNC(1)	5, 6, 10, 34, 35	—	Do not connect these pins. Leave as open circuit.
INN	1	Analog	Receiver input pin. Connect to photodiode anode.
INP	2	Analog	Receiver input pin. Connect to photodiode cathode.
LED_DRV_GND	12, 13, 16	Supply	LED driver ground pin, H-bridge. Connect to common board ground.
LED_DRV_SUP	17, 18	Supply	LED driver supply pin, H-bridge. Connect to an external power supply capable of supplying the large LED current, which is drawn by this supply pin.
LED_ALM	22	Digital	Output signal that indicates an LED cable fault. Can be connected to the port pin of an external microcontroller.
PD_ALM	23	Digital	Output signal that indicates a PD sensor or cable fault. Can be connected to the port pin of an external microcontroller.
$\overline{\text{RESET}}$	29	Digital	AFE-only reset input, active low. Can be connected to the port pin of an external microcontroller
RX_ANA_GND	3, 36, 40	Supply	Rx analog ground pin. Connect to common board ground.
RX_ANA_SUP	33, 39	Supply	Rx analog supply pin; 0.1-µF decoupling capacitor to ground
RX_DIG_GND	19, 32	Supply	Rx digital ground pin. Connect to common board ground.
RX_DIG_SUP	31	Supply	Rx digital supply pin; 0.1-µF decoupling capacitor to ground
SCLK	24	SPI	SPI clock pin
SPISIMO	26	SPI	SPI serial in master out
SPISOMI	25	SPI	SPI serial out master in
SPISTE	27	SPI	SPI serial interface enable
TX_CTRL_SUP	11	Supply	Transmit control supply pin (0.1-µF decoupling capacitor to ground)
TX_REF	9	Reference	Transmitter reference voltage, 0.75 V default after reset. Connect a 2.2-µF decoupling capacitor to ground.
TXN	14	Analog	LED driver out B, H-bridge output. Connect to LED.
TXP	15	Analog	LED driver out B, H-bridge output. Connect to LED.
VCM	4	Reference	Input common-mode voltage output. Connect a series resistor (1 kΩ) and a decoupling capacitor (10 nF) to ground. The voltage across the capacitor can be used to shield (guard) the INP, INM traces.
VSS	8	Supply	Substrate ground. Connect to common board ground.
XOUT	37	Digital	Crystal oscillator pins. Connect an external 8-MHz crystal between these pins with the correct load capacitor (as specified by vendor) to ground.
XIN	38	Digital	Crystal oscillator pins. Connect an external 8-MHz crystal between these pins with the correct load capacitor (as specified by vendor) to ground.

(1) Leave pins as open circuit. Do not connect.

TYPICAL CHARACTERISTICS

At T_A = +25°C, RX_ANA_SUP = RX_DIG_SUP = 3.0 V, TX_CTRL_SUP = LED_DRV_SUP = 3.3 V, and f_{CLK} = 8 MHz, unless otherwise noted.

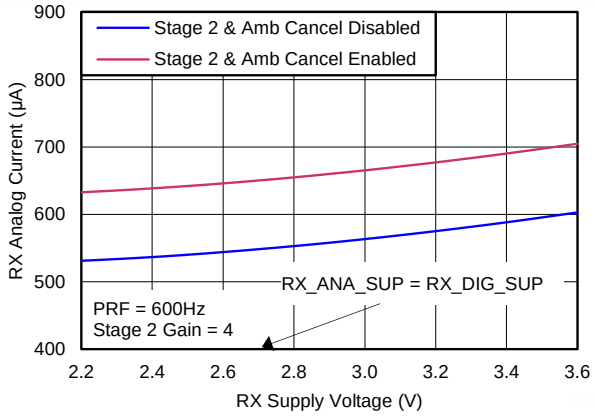


Figure 3. TOTAL Rx CURRENT vs Rx SUPPLY VOLTAGE

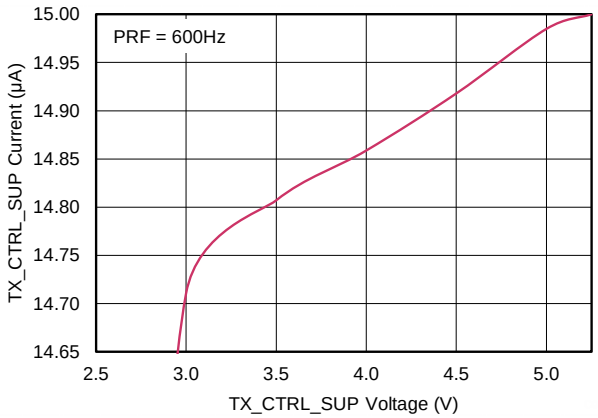


Figure 4. TX_CTRL_SUP CURRENT vs TX_CTRL_SUP VOLTAGE

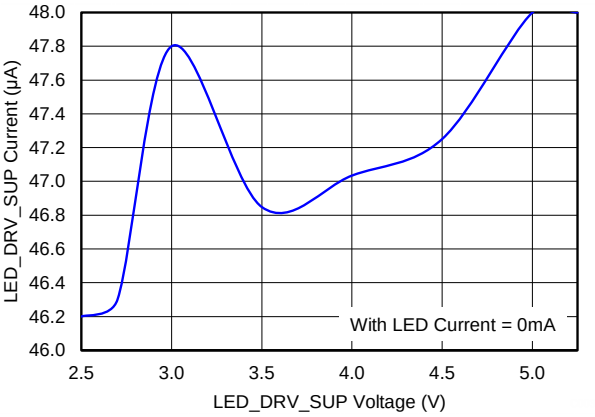


Figure 5. LED_DRV_SUP CURRENT vs LED_DRV_SUP VOLTAGE

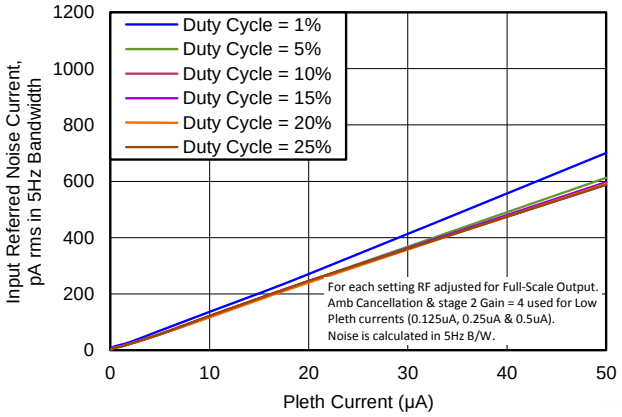


Figure 6. INPUT-REFERRED NOISE CURRENT vs PLETH CURRENT (PRF = 100 Hz)

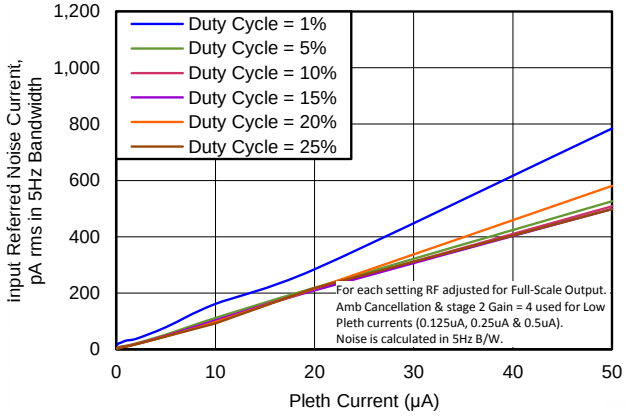


Figure 7. INPUT-REFERRED NOISE CURRENT vs PLETH CURRENT (PRF = 300 Hz)

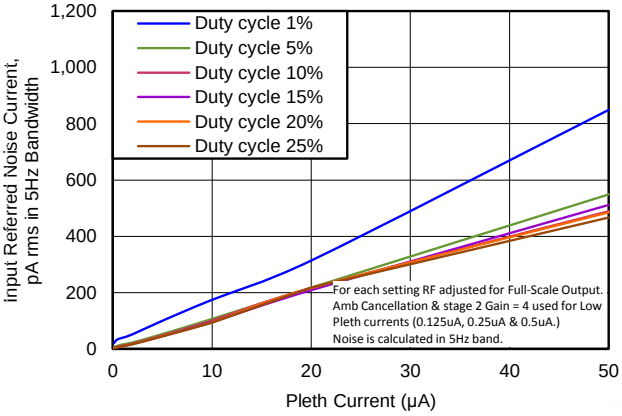


Figure 8. INPUT-REFERRED NOISE CURRENT vs PLETH CURRENT (PRF = 600 Hz)

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, RX_ANA_SUP = RX_DIG_SUP = 3.0 V, TX_CTRL_SUP = LED_DRV_SUP = 3.3 V, and f_{CLK} = 8 MHz, unless otherwise noted.

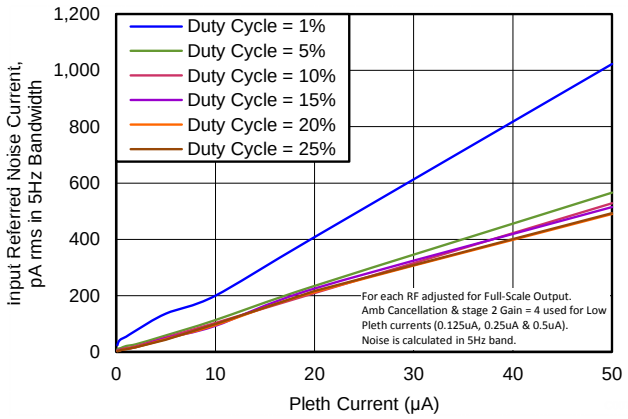


Figure 9. INPUT-REFERRED NOISE CURRENT vs PLETH CURRENT (PRF = 1200 Hz)

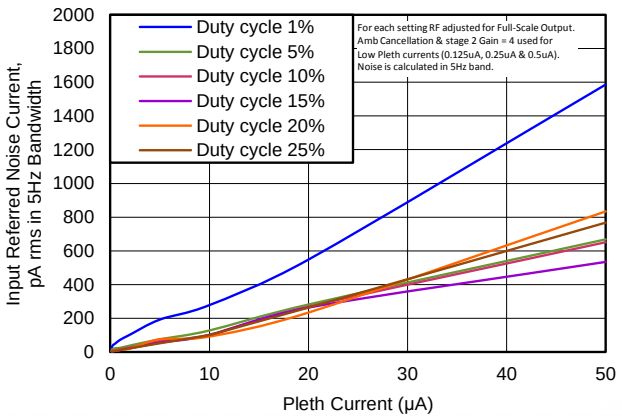


Figure 10. INPUT-REFERRED NOISE CURRENT vs PLETH CURRENT (PRF = 2500 Hz)

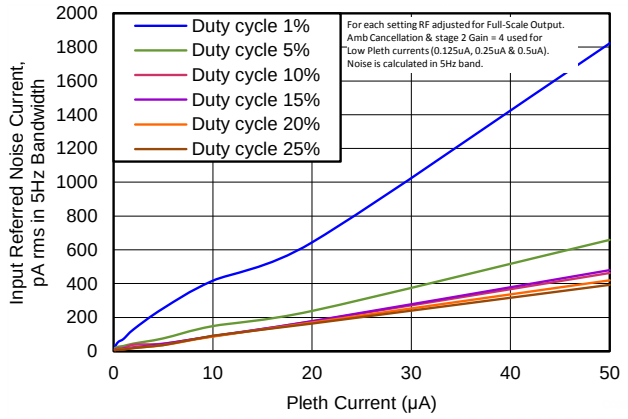


Figure 11. INPUT-REFERRED NOISE CURRENT vs PLETH CURRENT (PRF = 5000 Hz)

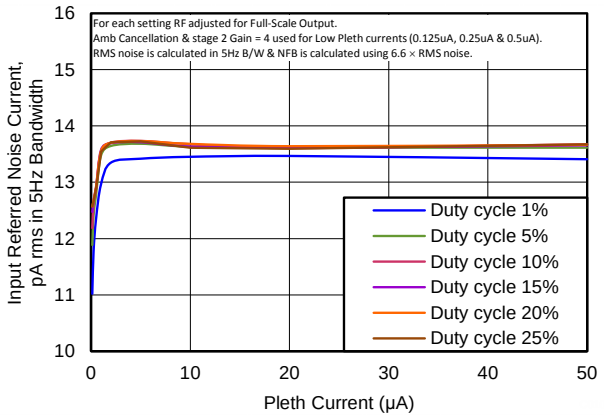


Figure 12. NOISE-FREE BITS vs PLETH CURRENT (PRF = 100 Hz)

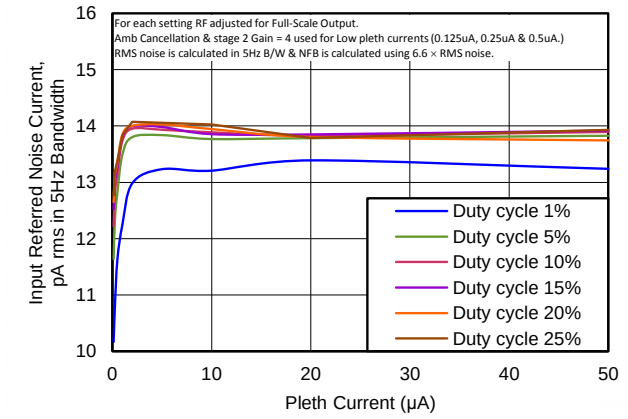


Figure 13. NOISE-FREE BITS vs PLETH CURRENT (PRF = 300 Hz)

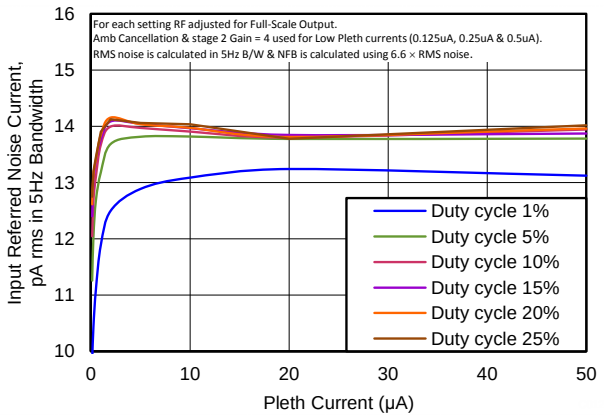


Figure 14. NOISE-FREE BITS vs PLETH CURRENT (PRF = 600 Hz)

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, RX_ANA_SUP = RX_DIG_SUP = 3.0 V, TX_CTRL_SUP = LED_DRV_SUP = 3.3 V, and f_{CLK} = 8 MHz, unless otherwise noted.

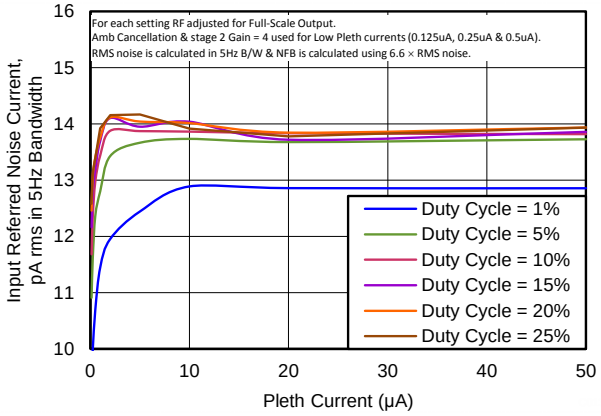


Figure 15. NOISE-FREE BITS vs PLETH CURRENT (PRF = 1200 Hz)

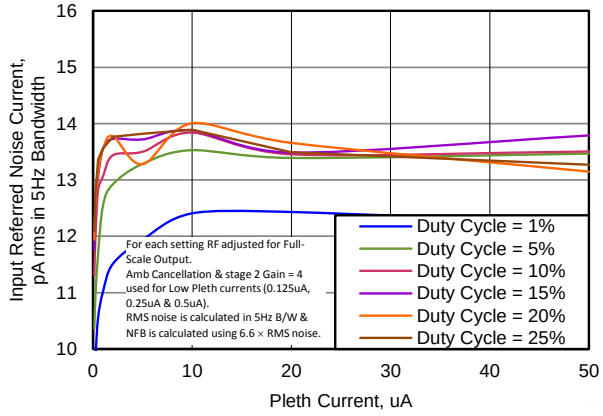


Figure 16. NOISE-FREE BITS vs PLETH CURRENT (PRF = 2500 Hz)

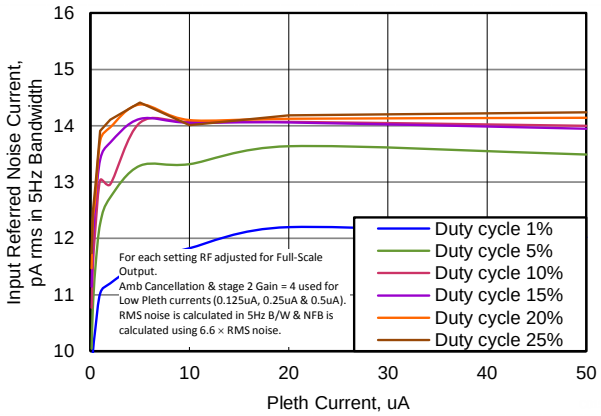


Figure 17. NOISE-FREE BITS vs PLETH CURRENT (PRF = 5000 Hz)

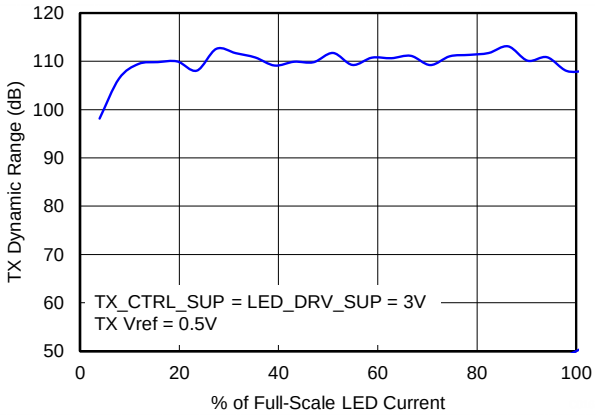


Figure 18. TRANSMITTER DYNAMIC RANGE (5-Hz BW)

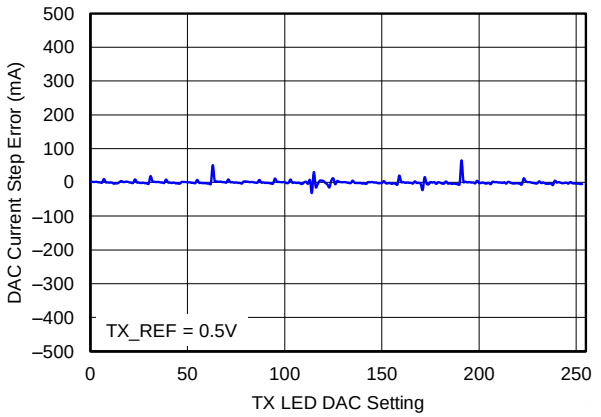


Figure 19. TRANSMITTER DAC CURRENT STEP ERROR (50 mA, Max)

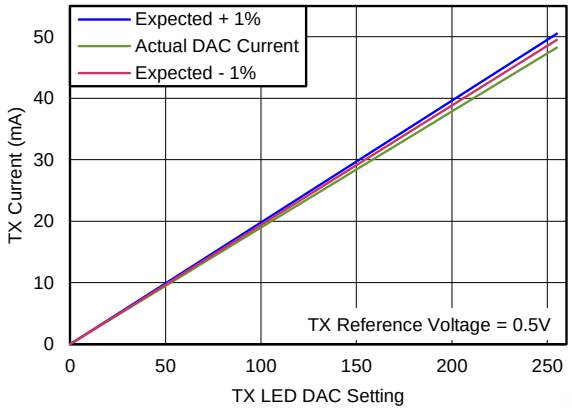


Figure 20. TRANSMITTER CURRENT LINEARITY (50-mA Range)

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, RX_ANA_SUP = RX_DIG_SUP = 3.0 V, TX_CTRL_SUP = LED_DRV_SUP = 3.3 V, and f_{CLK} = 8 MHz, unless otherwise noted.

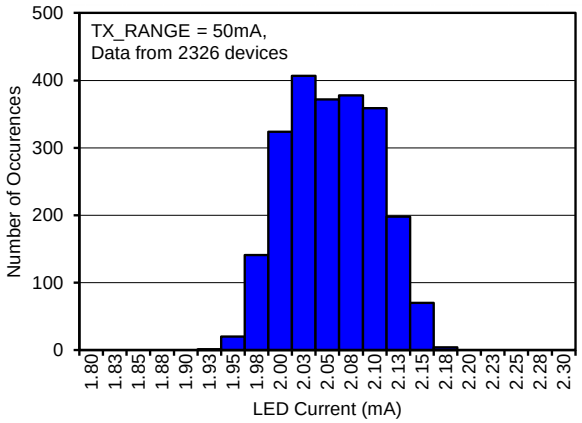


Figure 21. LED CURRENT WITH Tx DAC SETTING = 10 (2 mA)

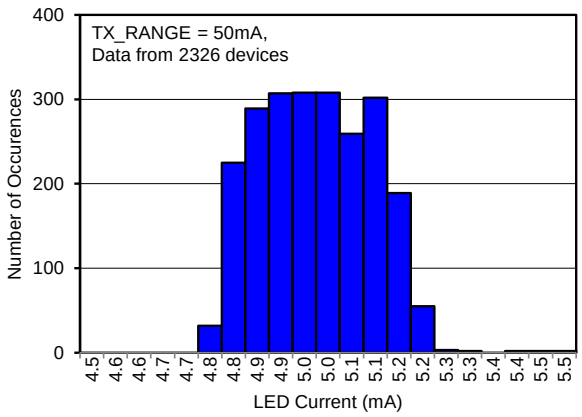


Figure 22. LED CURRENT WITH Tx DAC SETTING = 25 (5 mA)

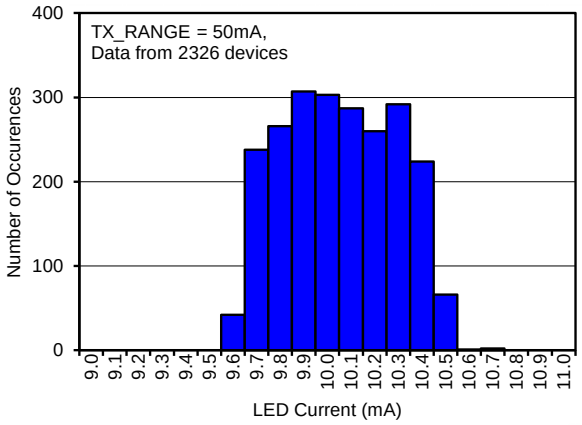


Figure 23. LED CURRENT WITH Tx DAC SETTING = 51 (10 mA)

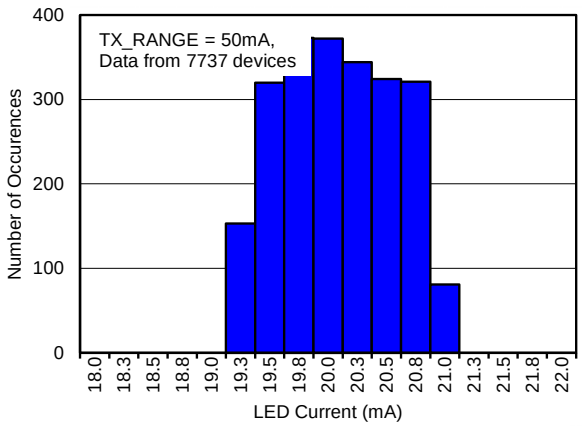


Figure 24. LED CURRENT WITH Tx DAC SETTING = 102 (20 mA)

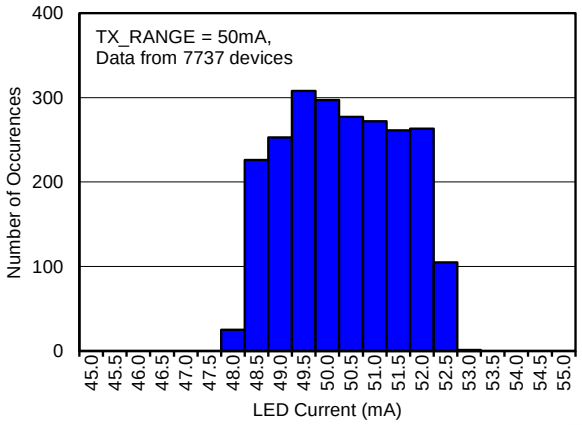


Figure 25. LED CURRENT WITH Tx DAC SETTING = 255 (50 mA)

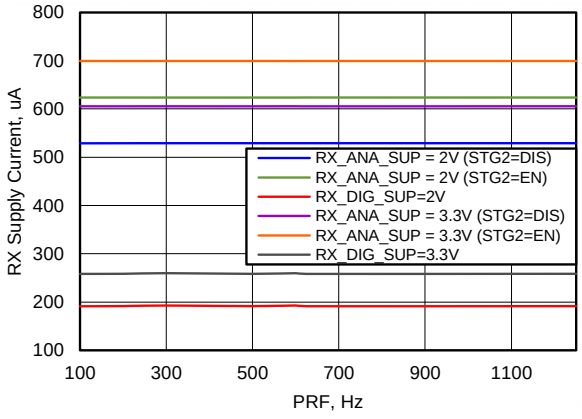


Figure 26. RECEIVER SUPPLIES vs PRF

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, RX_ANA_SUP = RX_DIG_SUP = 3.0 V, TX_CTRL_SUP = LED_DRV_SUP = 3.3 V, and f_{CLK} = 8 MHz, unless otherwise noted.

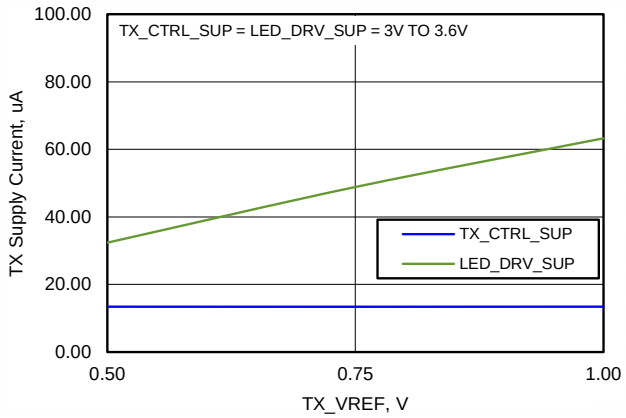


Figure 27. TRANSMITTER SUPPLIES vs TX_REF

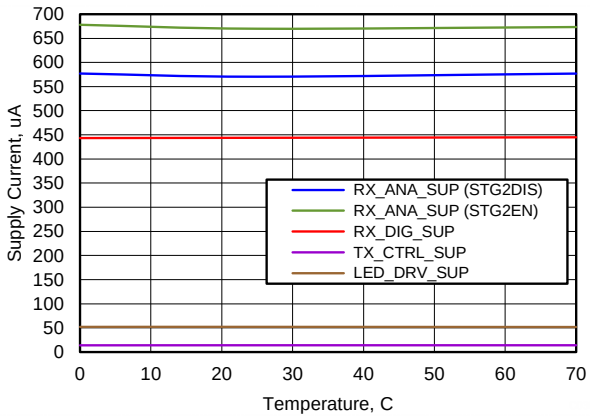


Figure 28. POWER SUPPLIES vs TEMPERATURE

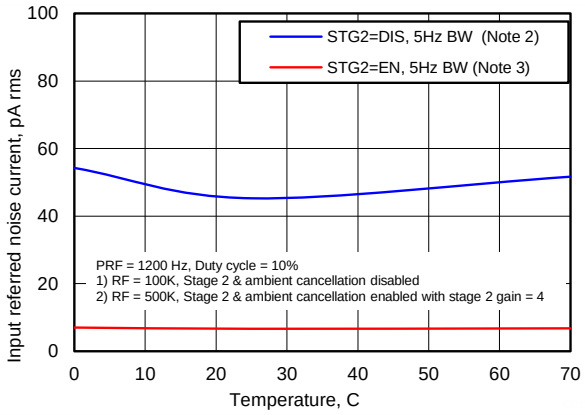


Figure 29. INPUT-REFERRED NOISE vs TEMPERATURE

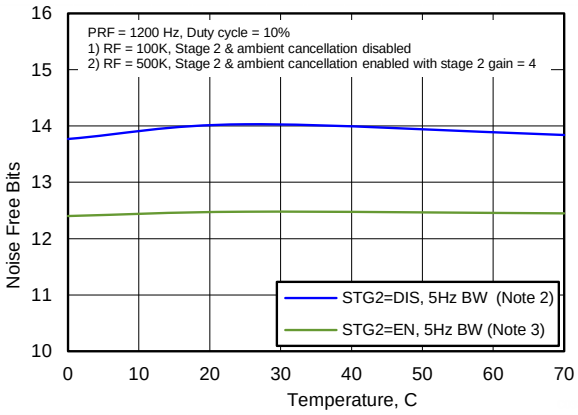


Figure 30. NOISE-FREE BITS vs TEMPERATURE

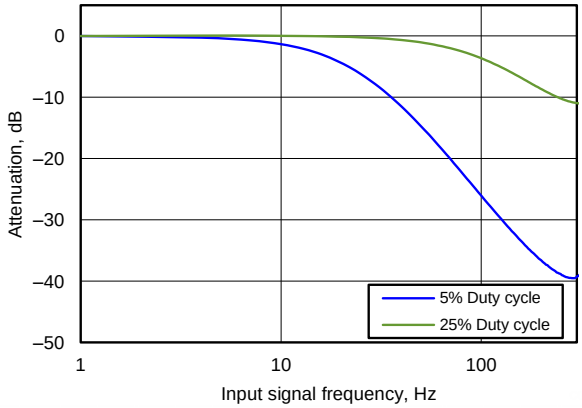


Figure 31. FILTER RESPONSE vs DUTY CYCLE

OVERVIEW

The AFE4400 is a complete analog front-end (AFE) solution targeted for pulse oximeter applications. The device consists of a low-noise receiver channel, an LED transmit section, and diagnostics for sensor and LED fault detection. To ease clocking requirements and provide the low-jitter clock to the AFE, an oscillator is also integrated that functions from an external crystal. The device communicates to an external microcontroller or host processor using an SPI interface. Figure 32 shows a detailed block diagram for the AFE4400. The blocks are described in more detail in the following sections.

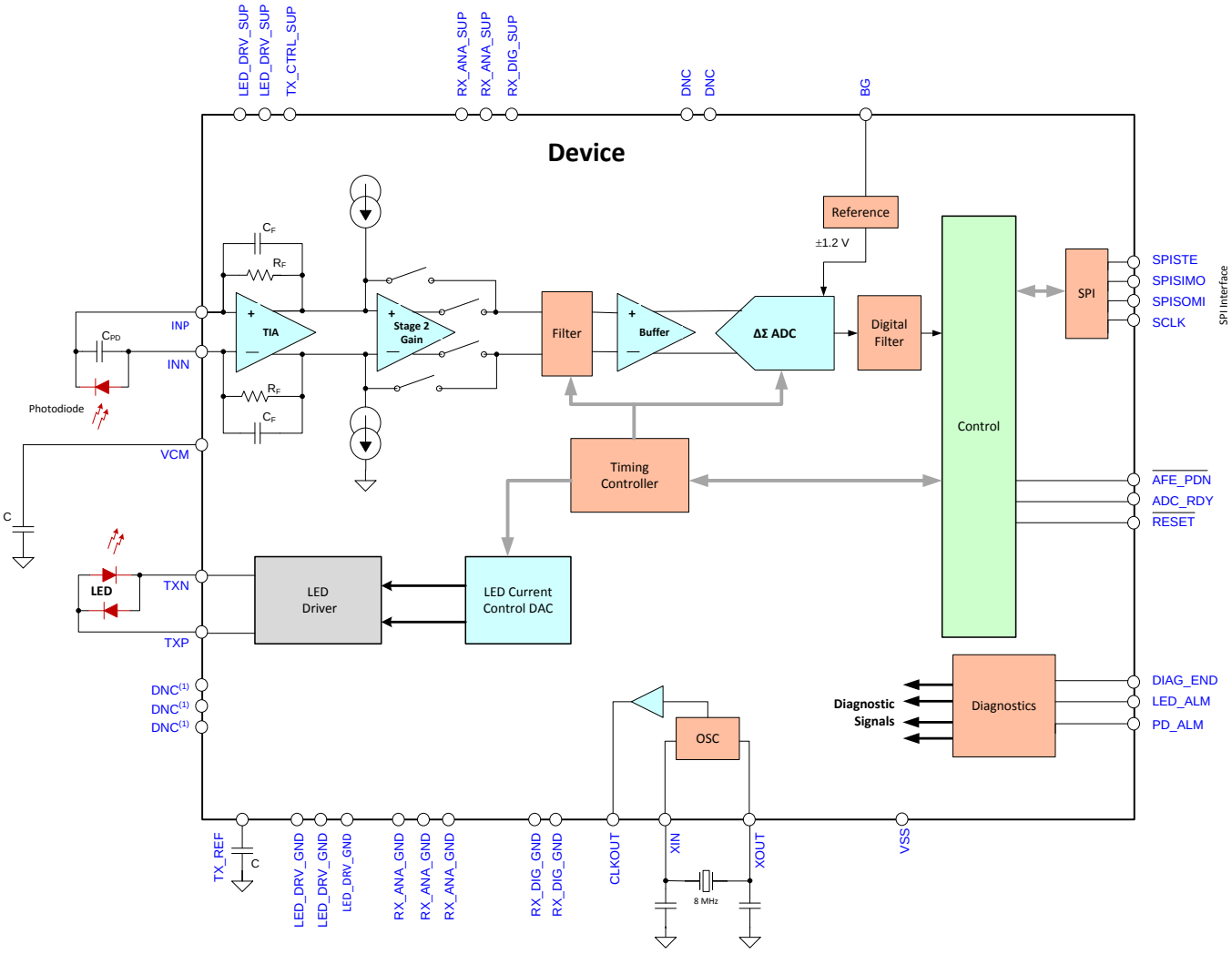


Figure 32. Detailed Block Diagram

RECEIVER CHANNEL

This section describes the functionality of the receiver channel.

Receiver Front-End

The receiver consists of a differential current-to-voltage (I-V) transimpedance amplifier that converts the input photodiode current into an appropriate voltage, as shown in Figure 33. The feedback resistor of the amplifier (R_F) is programmable to support a wide range of photodiode currents. Available R_F values include: 1 MΩ, 500 kΩ, 250 kΩ, 100 kΩ, 50 kΩ, 25 kΩ, and 10 kΩ.

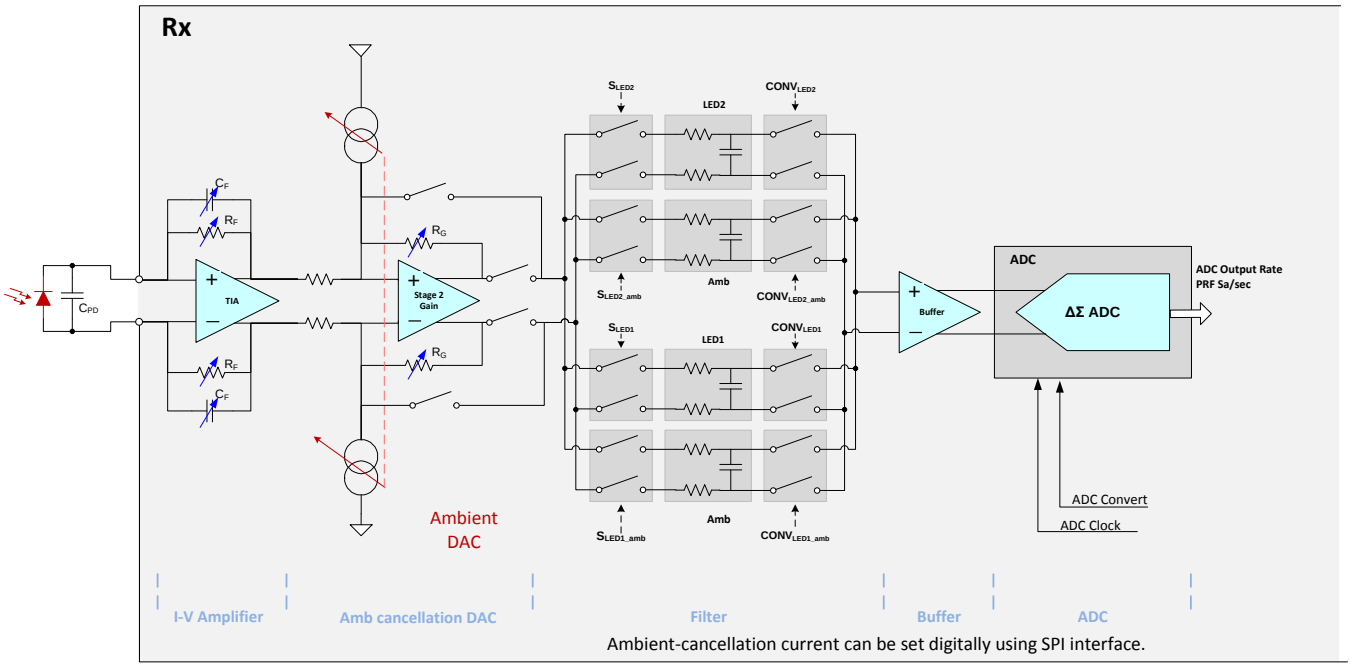


Figure 33. Receiver Front-End

The R_F amplifier and the feedback capacitor (C_F) form a low-pass filter for the input signal current. Always ensure that the low-pass filter RC time constant has sufficiently high bandwidth (as shown by Equation 1) because the input current consists of pulses. For this reason, the feedback capacitor is also programmable. Available C_F values include: 5 pF, 10 pF, 25 pF, 50 pF, 100 pF, and 250 pF. Any combination of these capacitors can also be used.

$$R_F \times C_F \leq \frac{\text{Rx Sample Time}}{10} \quad (1)$$

The output voltage of the I-V amplifier includes the pleth component (the desired signal) and a component resulting from the ambient light leakage; see . The I-V amplifier is followed by the second stage, which consists of a current digital-to-analog converter (DAC) that sources the cancellation current and an amplifier that gains up the pleth component alone. The amplifier has five programmable gain settings: 0 dB, 3.5 dB, 6 dB, 9.5 dB, and 12 dB. The gained-up pleth signal is then low-pass filtered (500-Hz bandwidth) and buffered before driving a 22-bit ADC. The current DAC has a cancellation current range of 10 µA with 10 steps (1 µA each). The DAC value can be digitally specified with the SPI interface. Using ambient compensation with the ambient DAC allows the dc-biased signal to be centered to near mid-point of the amplifier (±0.9 V). Using the gain of the second stage allows for more of the available ADC dynamic range to be used.

The output of the ambient cancellation amplifier is separated into LED2 and LED1 channels. When LED2 is on, the amplifier output is filtered and sampled on capacitor C_R. Similarly, the LED1 signal is sampled on the C_{LED1} capacitor when LED1 is ON. In between the LED2 and LED1 pulses, the idle amplifier output is sampled to estimate the ambient signal on capacitors C_{LED2_amb} and C_{LED1_amb}.

The sampling duration is termed the *Rx sample time* and is programmable for each signal, independently. The sampling can start after the I-V amplifier output is stable (to account for LED and cable settling times). The Rx sample time is used for all dynamic range calculations; the minimum time supported is 50 µs.

A single, 22-bit ADC converts the sampled LED2, LED1, and ambient signals sequentially. Each conversion takes 25% of the pulse repetition period and provides a single digital code at the ADC output. As discussed in the *Receiver Timing* section, the conversions are staggered so that the LED2 conversion starts after the end of the LED2 sample phase, and so on. This configuration also means that the Rx sample time for each signal is no greater than 25% of the pulse repetition period.

Note that four data streams are available at the ADC output (LED2, LED1, ambient LED2, and ambient LED1) at the same rate as the pulse repetition frequency. The ADC is followed by a digital ambient subtraction block that additionally outputs the (LED2 – ambient LED2) and (LED1 – ambient LED1) data values.

Ambient Cancellation Scheme

The receiver provides digital samples corresponding to ambient duration. The host processor (external to the AFE) can use these ambient values to estimate the amount of ambient light leakage. The processor must then set the value of the ambient cancellation DAC using the SPI, as shown in Figure 34.

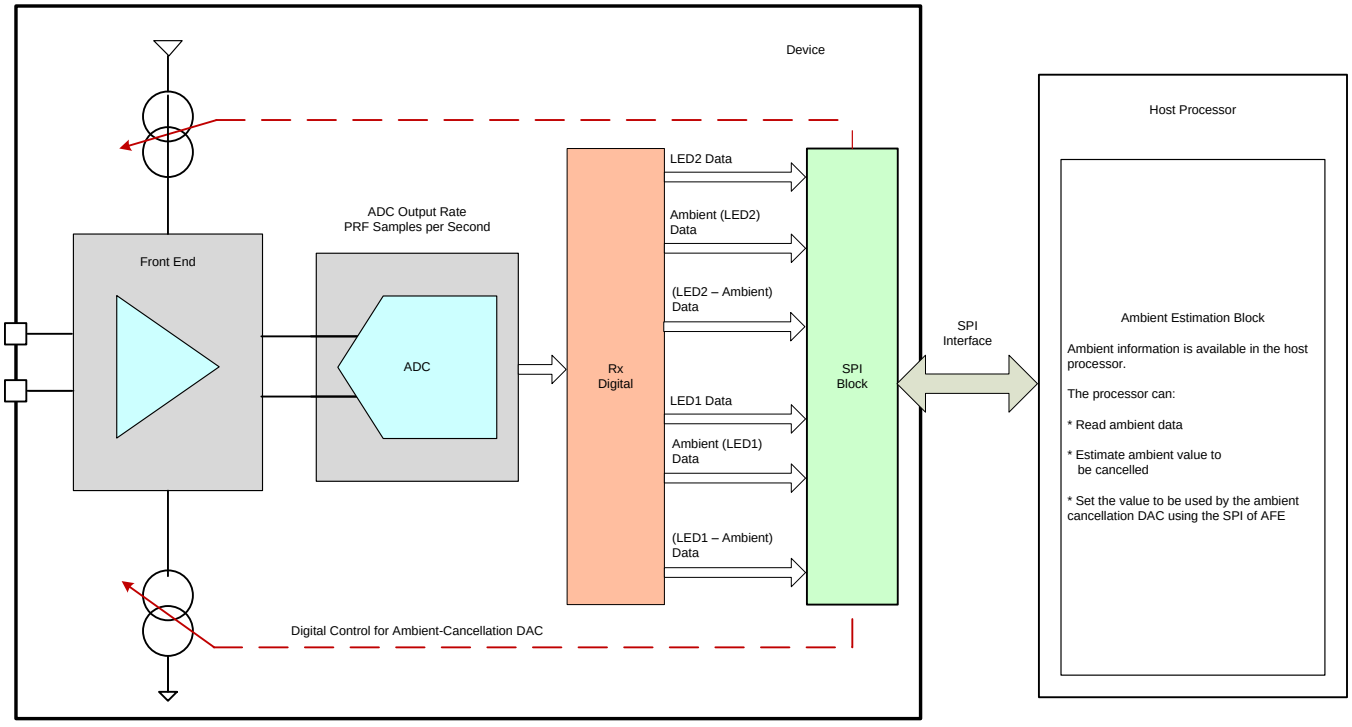


Figure 34. Ambient Cancellation Loop (Closed by the Host Processor)

Using the set value, the ambient cancellation stage subtracts the ambient component and gains up only the pleth component of the received signal; see Figure 35. The amplifier gain is programmable to 0 dB, 3.5 dB, 6 dB, 9.5 dB, and 12 dB.

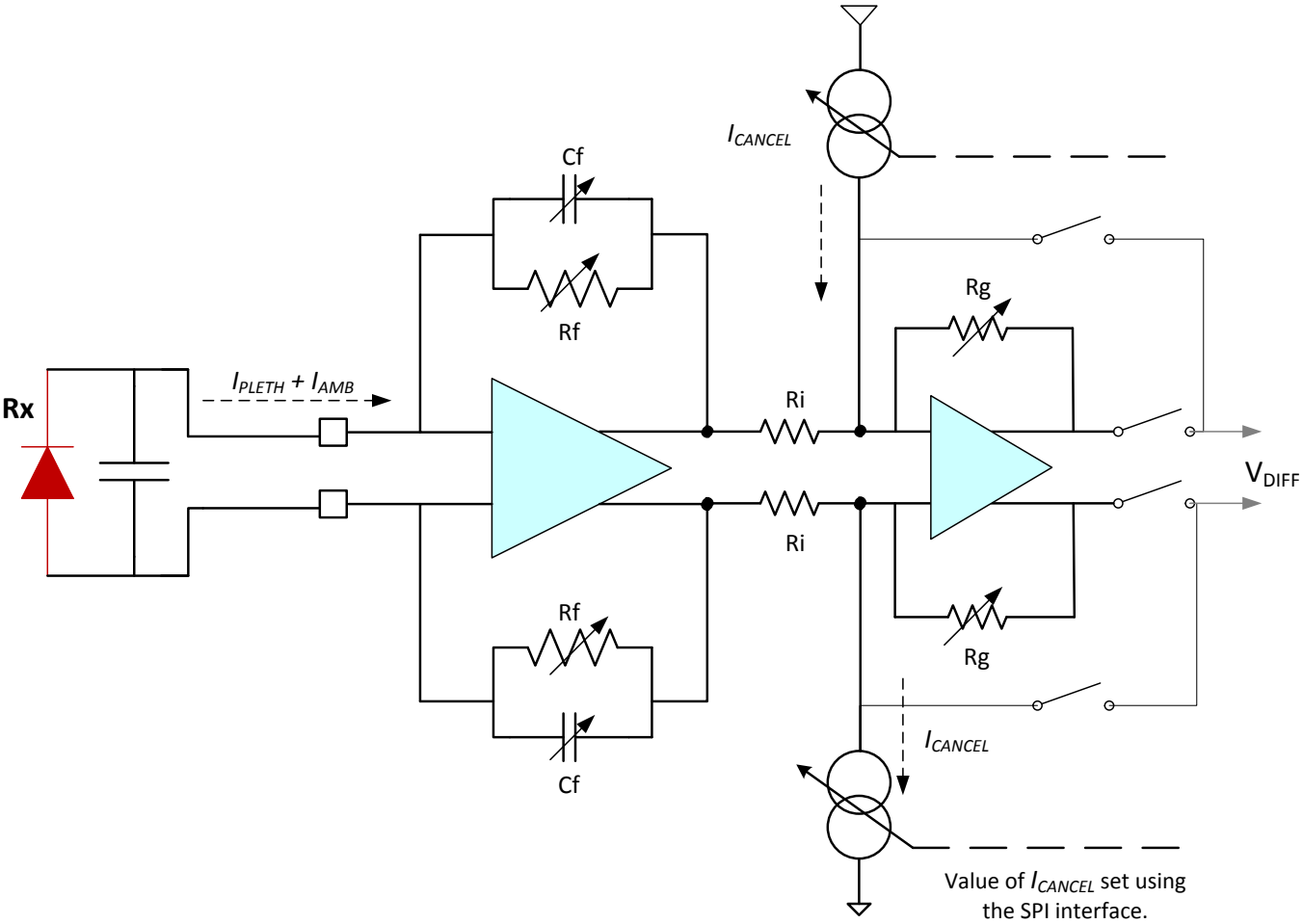


Figure 35. Front-End (I-V Amplifier and Cancellation Stage)

The differential output of the second stage is V_{DIFF}, as given by Equation 2:

$$V_{DIFF} = 2 \times \left(I_{PLETH} \times \frac{R_F}{R_I} + I_{AMB} \times \frac{R_F}{R_I} - I_{CANCEL} \right) \times R_G \quad (2)$$

where:

- R_I = 100 kΩ,
- I_{PLETH} = photodiode current pleth component,
- I_{AMB} = photodiode current ambient component, and
- I_{CANCEL} = the cancellation current DAC value (as estimated by the host processor).

R_G values with various gain settings are listed in Table 2.

Table 2. R_G Values

R_G (dB)	GAIN (kΩ)
0 (x1)	100
3.5 (x1.5)	150
6 (x2)	200
9.5 (x3)	300
12 (x4)	400

Receiver Control Signals

LED2 sample phase (S_{LED2}): When this signal is high, the amplifier output corresponds to the LED2 on-time. The amplifier output is filtered and sampled into capacitor C_{LED2}. To avoid settling effects resulting from the LED or cable, program S_{LED2} to start after the LED turns on. This settling delay is programmable.

Ambient sample phase (S_{LED2_amb}): When this signal is high, the amplifier output corresponds to the LED2 off-time and can be used to estimate the ambient signal (for the LED2 phase). The amplifier output is filtered and sampled into capacitor C_{LED2_amb}.

LED1 sample phase (S_{LED1}): When this signal is high, the amplifier output corresponds to the LED1 on-time. The amplifier output is filtered and sampled into capacitor C_{LED1}. To avoid settling effects resulting from the LED or cable, program S_{LED1} to start after the LED turns on. This settling delay is programmable.

Ambient sample phase (S_{LED1_amb}): When this signal is high, the amplifier output corresponds to the LED1 off-time and can be used to estimate the ambient signal (for the LED1 phase). The amplifier output is filtered and sampled into capacitor C_{LED1_amb}.

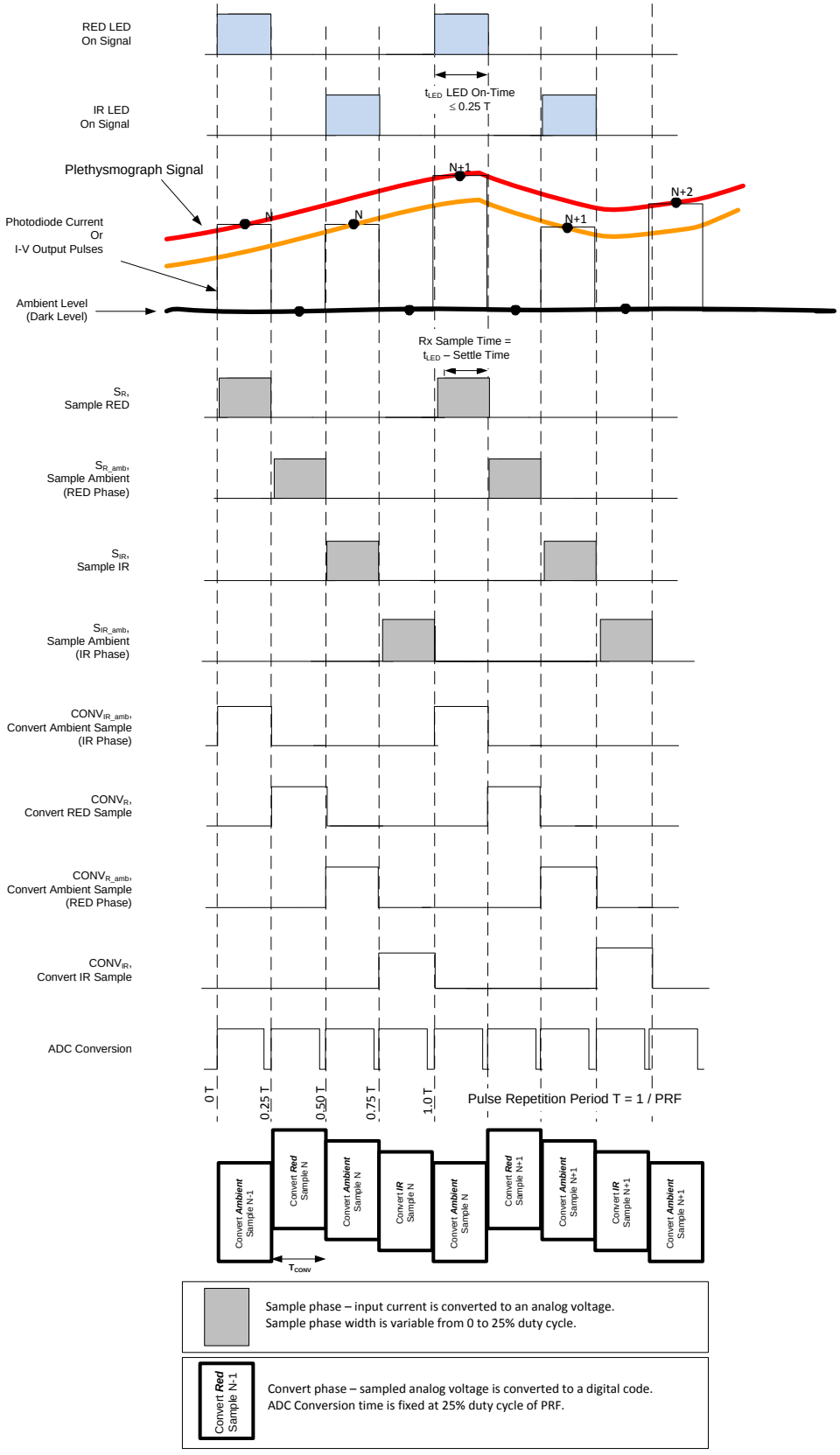
LED2 convert phase ($CONV_{LED2}$): When this signal is high, the voltage sampled on C_{LED2} is buffered and applied to the ADC for conversion. The conversion time duration is always 25% of the pulse repetition period. At the end of the conversion, the ADC provides a single digital code corresponding to the LED2 sample.

Ambient convert phases ($CONV_{LED2\_amb}$, $CONV_{LED1\_amb}$): When this signal is high, the voltage sampled on C_{LED2_amb} (or C_{LED1_amb}) is buffered and applied to the ADC for conversion. The conversion time duration is always 25% of the pulse repetition period. At the end of the conversion, the ADC provides a single digital code corresponding to the ambient sample.

LED1 convert phase ($CONV_{LED1}$): When this signal is high, the voltage sampled on C_{LED1} is buffered and applied to the ADC for conversion. The conversion time duration is always 25% of the pulse repetition period. At the end of the conversion, the ADC provides a single digital code corresponding to the LED1 sample.

Receiver Timing

See Figure 36 for a timing diagram detailing the control signals related to the LED on-time, Rx sample time, and the ADC conversion times for each channel.



NOTE: Relationship to the AFE4400 EVM is: LED1 = IR and LED2 = RED.

Figure 36. Rx Timing Diagram

CLOCKING AND TIMING SIGNAL GENERATION

The crystal oscillator generates a master clock signal using an external 8-MHz crystal. A divide-by-2 block converts the 8-MHz clock to 4 MHz, which is used by the AFE to operate the timer modules, ADC, and diagnostics. The 4-MHz clock is buffered and output from the AFE in order to clock an external microcontroller. The clocking functionality is shown in Figure 37.

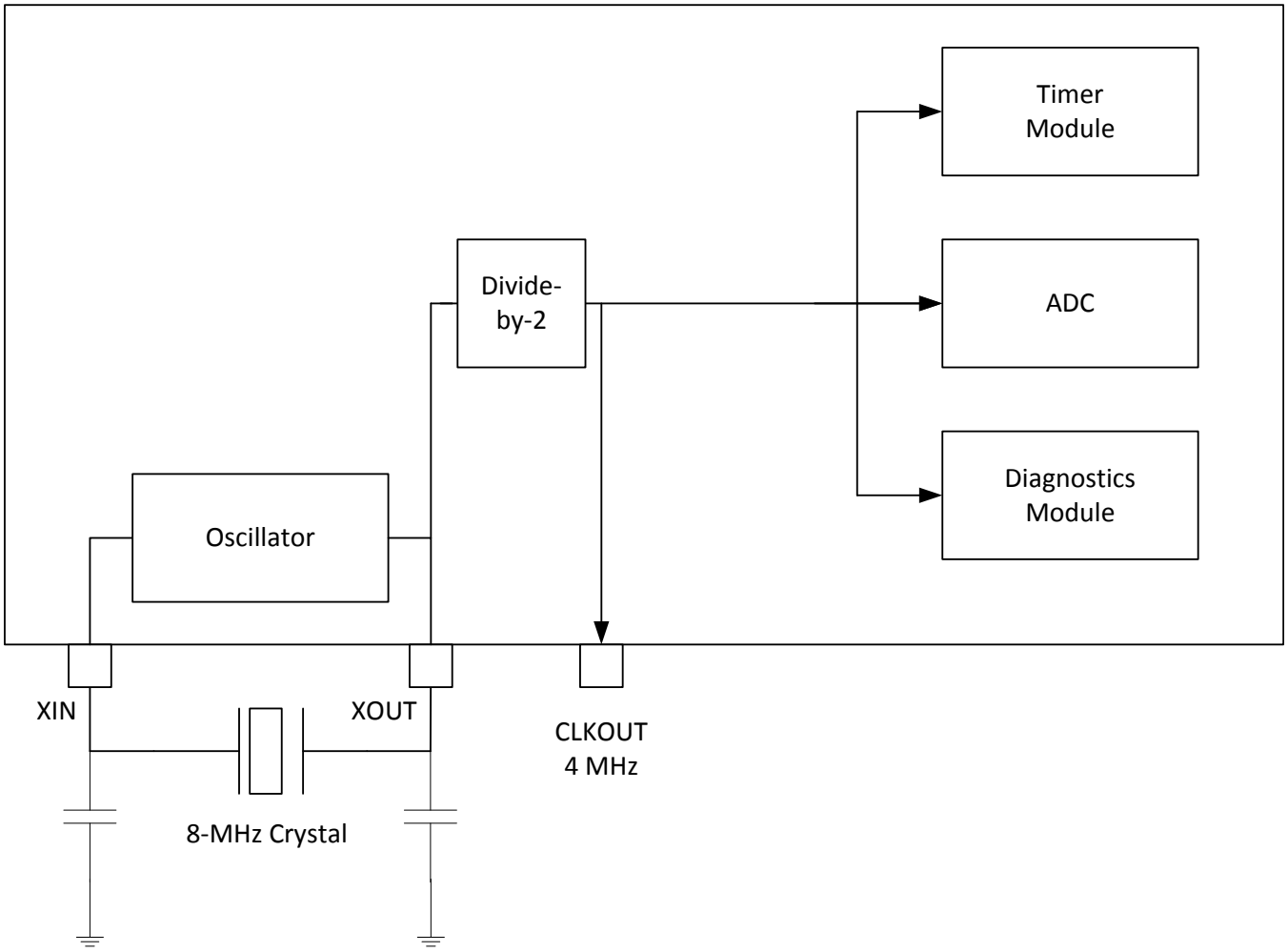
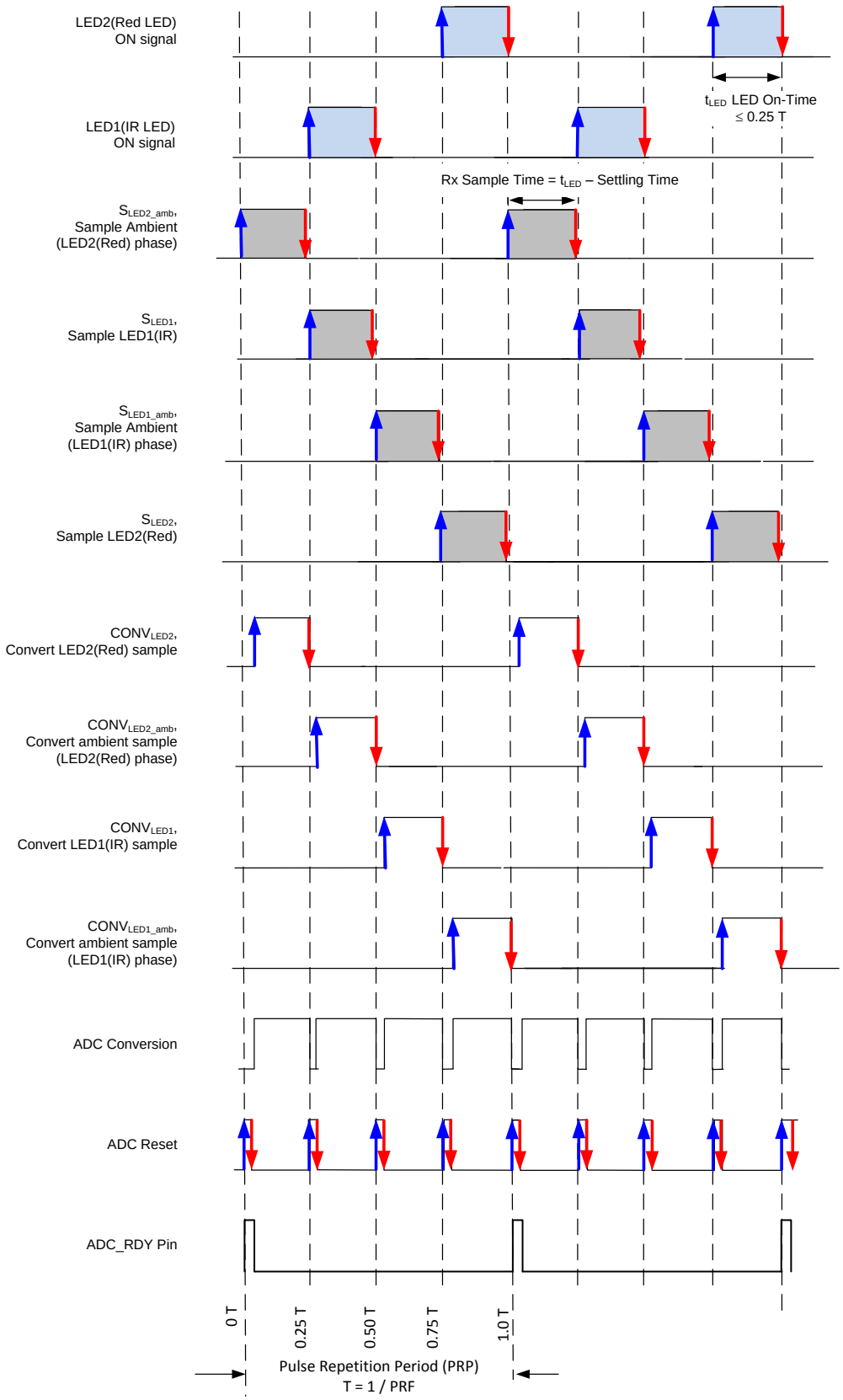


Figure 37. AFE Clocking

TIMER MODULE

See Figure 38 for a timing diagram detailing the various timing edges that are programmable using the timer module. The rising and falling edge positions of 11 signals can be controlled. The module uses a single 16-bit counter (running off of the 4-MHz clock) to set the time-base.

All timing signals are set with reference to the pulse repetition period (PRP). Therefore, a dedicated compare register compares the 16-bit counter value with the reference value specified in the PRF register. Every time that the 16-bit counter value is equal to the reference value in the PRF register, the counter is reset to '0'.



NOTE: Programmable edges are shown in blue and red.

Figure 38. AFE Control Signals

For the 11 signals in Figure 36, the start and stop edge positions are programmable with respect to the PRF period. Each signal uses a separate timer compare module that compares the counter value with preprogrammed reference values for the start and stop edges. All reference values can be set using the SPI interface.

When the counter value equals the start reference value, the output signal is set. When the counter value equals the stop reference value, the output signal is reset. Figure 39 shows a diagram of the timer compare register. With a 4-MHz clock, the edge placement resolution is 0.25 µs. The ADC conversion signal requires four pulses in each PRF clock period. The 11th timer compare register uses four sets of start and stop registers to control the ADC conversion signal.

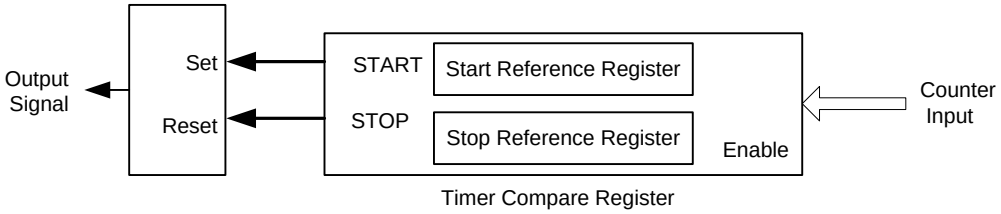


Figure 39. Compare Register

The ADC conversion signal requires four pulses in each PRF clock period. Timer compare register 11 uses four sets of start and stop registers to control the ADC conversion signal, as shown in Figure 40.

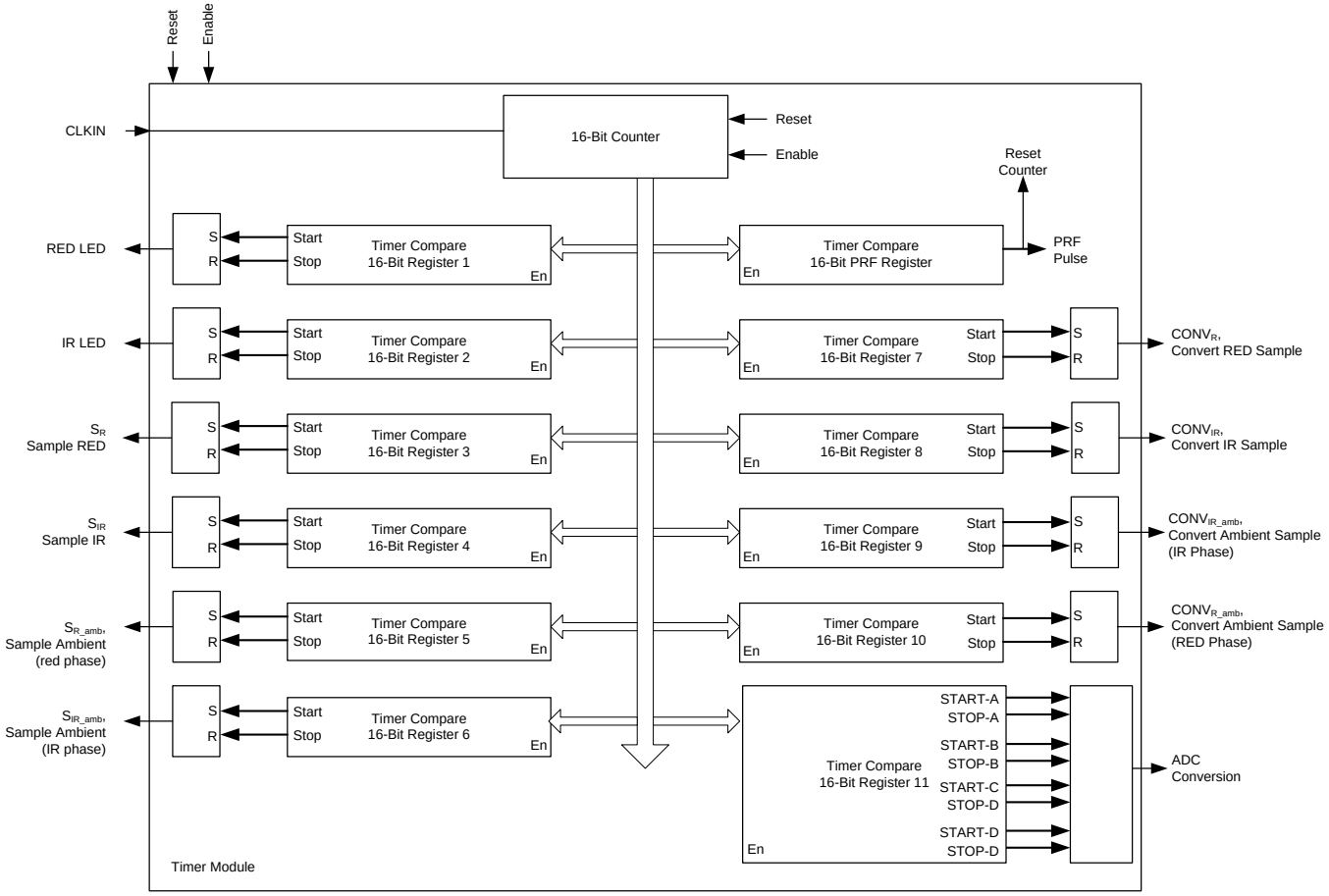


Figure 40. Timer Module

Using the Timer Module

The timer module registers can be used to program the start and end instants in units of 4-MHz clock cycles. These timing instants and the corresponding registers are listed in Table 3.

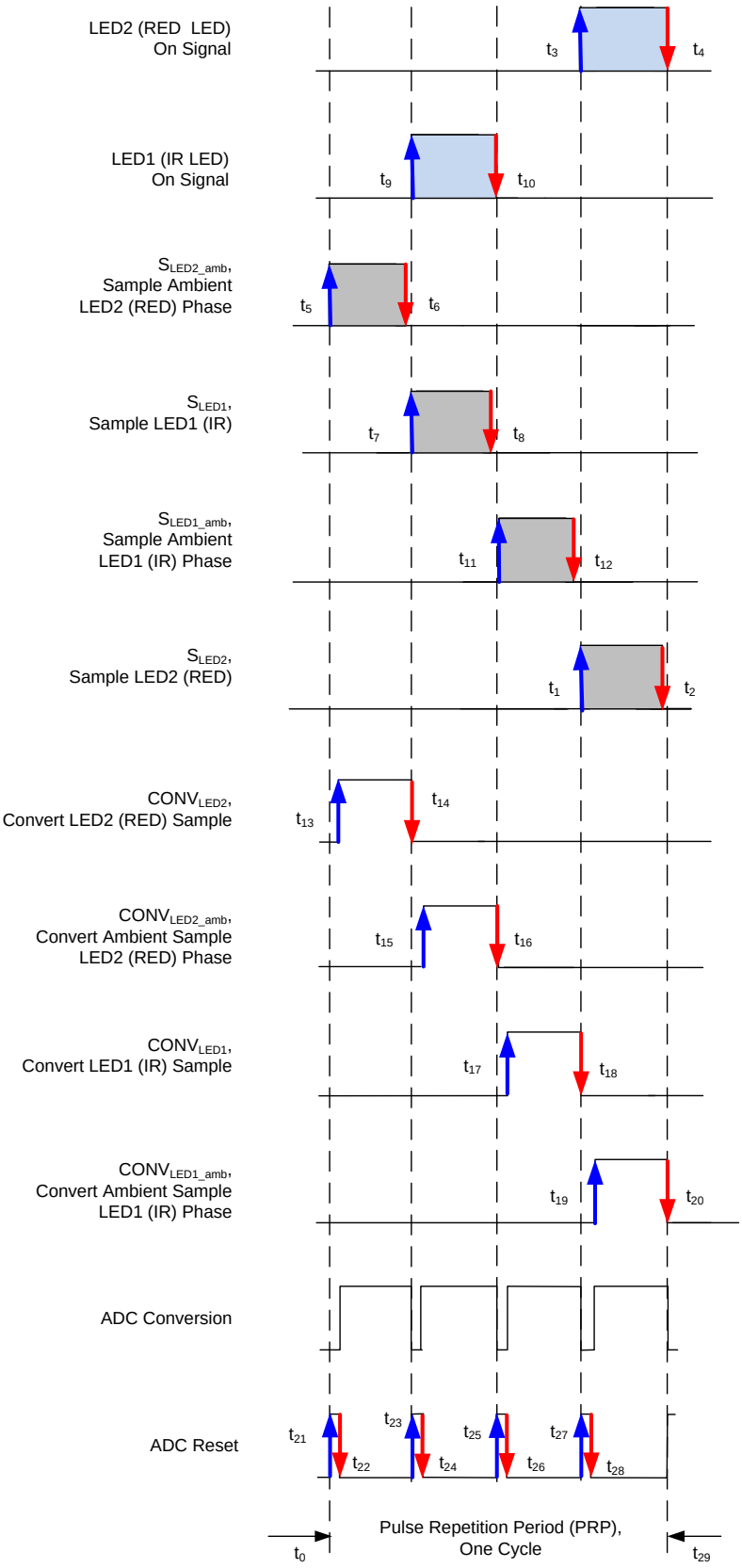
Note that the device does not restrict the values in these registers; thus, the start and end edges can be positioned anywhere within the pulse repetition period. Care must be taken by the user to program suitable values in these registers to avoid overlapping the signals and to make sure none of the edges exceed the value programmed in the PRP register. Writing the same value in the start and end registers results in a pulse duration of one clock cycle. The following steps describe the timer sequencing configuration:

1. With respect to the start of the PRP period (indicated by timing instant t_0 in Figure 41), the following sequence of conversions must be followed in order: convert LED2 → LED2 ambient → LED1 → LED1 ambient.
2. Also, starting from t_0, the sequence of sampling instants must be staggered with respect to the respective conversions as follows: sample LED2 ambient → LED1 → LED1 ambient → LED2.
3. Finally, align the edges for the two LED pulses with the respective sampling instants.

Table 3. Clock Edge Mapping to SPI Registers

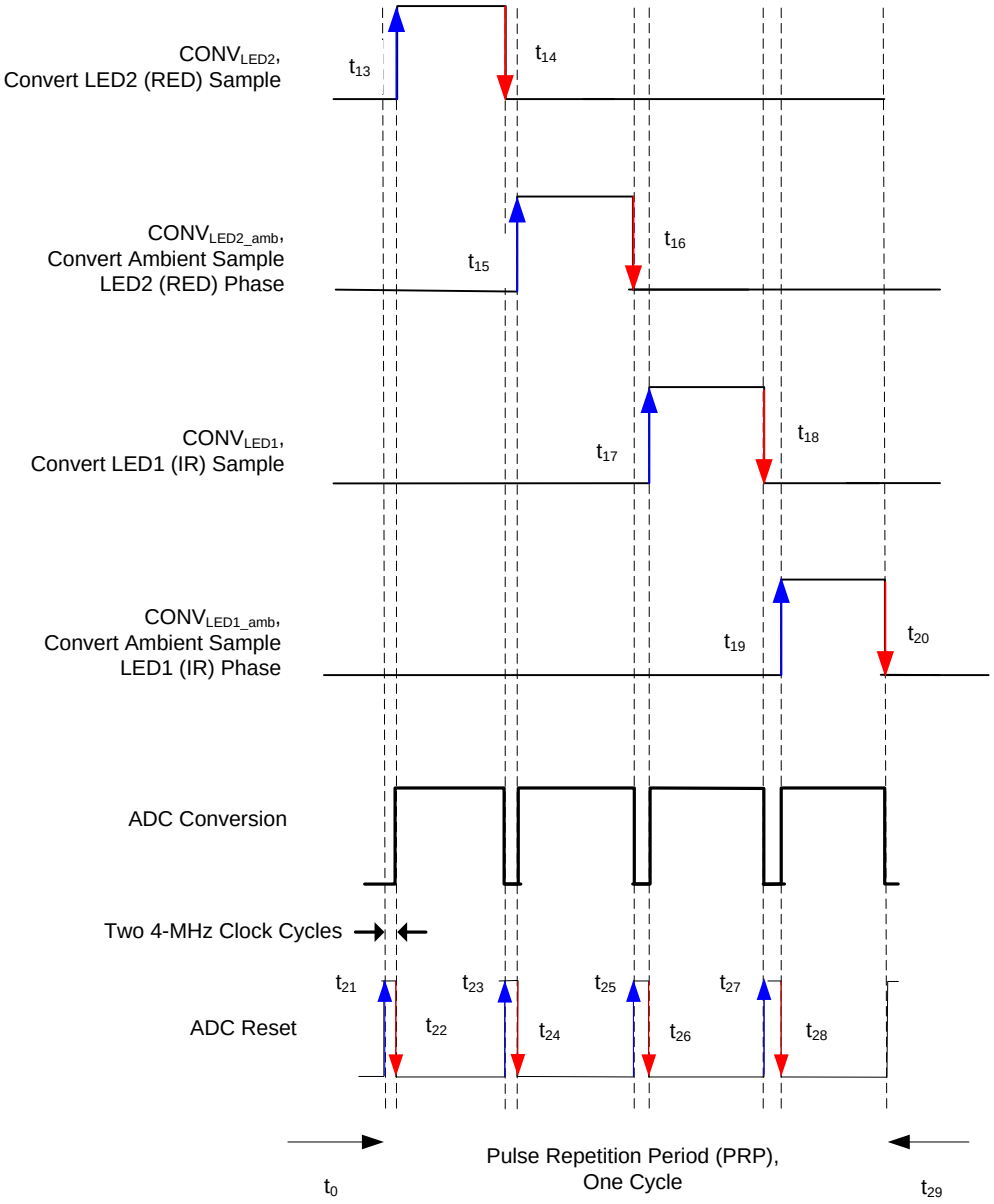
TIME INSTANT (See Figure 41 and Figure 42)	DESCRIPTION	CORRESPONDING REGISTER ADDRESS AND REGISTER BITS	EXAMPLE(1) (Decimal)
t_0	Start of pulse repetition period	No register control	—
t_1	Start of sample LED2 pulse	LED2STC[15:0], register 01h	6000
t_2	End of sample LED2 pulse	LED2ENDC[15:0], register 02h	7999
t_3	Start of LED2 pulse	LED2LEDSTC[15:0], register 03h	6000
t_4	End of LED2 pulse	LED2LEDENDC[15:0], register 04h	7998
t_5	Start of sample LED2 ambient pulse	ALED2STC[15:0], register 05h	0
t_6	End of sample LED2 ambient pulse	ALED2ENDC[15:0], register 06h	1998
t_7	Start of sample LED1 pulse	LED1STC[15:0], register 07h	2000
t_8	End of sample LED1 pulse	LED1ENDC[15:0], register 08h	3998
t_9	Start of LED1 pulse	LED1LEDSTC[15:0], register 09h	2000
t_{10}	End of LED1 pulse	LED1LEDENDC[15:0], register 0Ah	3999
t_{11}	Start of sample LED1 ambient pulse	ALED1STC[15:0], register 0Bh	4000
t_{12}	End of sample LED1 ambient pulse	ALED1ENDC[15:0], register 0Ch	5998
t_{13}	Start of convert LED2 pulse	LED2CONVST[15:0], register 0Dh Must start one AFE clock cycle after the ADC reset pulse ends.	2
t_{14}	End of convert LED2 pulse	LED2CONVEND[15:0], register 0Eh	1999
t_{15}	Start of convert LED2 ambient pulse	ALED2CONVST[15:0], register 0Fh Must start one AFE clock cycle after the ADC reset pulse ends.	2002
t_{16}	End of convert LED2 ambient pulse	ALED2CONVEND[15:0], register 10h	3999
t_{17}	Start of convert LED1 pulse	LED1CONVST[15:0], register 11h Must start one AFE clock cycle after the ADC reset pulse ends.	4002
t_{18}	End of convert LED1 pulse	LED1CONVEND[15:0], register 12h	5999
t_{19}	Start of convert LED1 ambient pulse	ALED1CONVST[15:0], register 13h Must start one AFE clock cycle after the ADC reset pulse ends.	6002
t_{20}	End of convert LED1 ambient pulse	ALED1CONVEND[15:0], register 14h	7999
t_{21}	Start of first ADC conversion reset pulse	ADCRSTSTCT0[15:0], register 15h	0
t_{22}	End of first ADC conversion reset pulse	ADCRSTENDCT0[15:0], register 16h	2
t_{23}	Start of second ADC conversion reset pulse	ADCRSTSTCT1[15:0], register 17h	2000
t_{24}	End of second ADC conversion reset pulse	ADCRSTENDCT1[15:0], register 18h	2002
t_{25}	Start of third ADC conversion reset pulse	ADCRSTSTCT2[15:0], register 19h	4000
t_{26}	End of third ADC conversion reset pulse	ADCRSTENDCT2[15:0], register 1Ah	4002
t_{27}	Start of fourth ADC conversion reset pulse	ADCRSTSTCT3[15:0], register 1Bh	6000
t_{28}	End of fourth ADC conversion reset pulse	ADCRSTENDCT3[15:0], register 1Ch	6002
t_{29}	End of pulse repetition period	PRPCOUNT[15:0], register 1Dh	7999

(1) Values are based off of a pulse repetition frequency (PRF) = 500 Hz and duty cycle = 25%.



(1) RED = LED2, IR = LED1.

Figure 41. Programmable Clock Edges



(1) RED = LED2, IR = LED1.

Figure 42. Relationship Between the ADC Reset and ADC Conversion Signals

ADC OPERATION AND AVERAGING MODULE

The ADC reset signal must be positioned at 25% intervals of the pulse repetition period (that is, 0%, 25%, 50%, and 75%). After the falling edge of the ADC reset signal, the ADC conversion phase starts (refer to Figure 42). Each ADC conversion takes 50 µs.

The ADC operates with averaging. The averaging module averages multiple ADC samples and reduce noise to improve dynamic range because the ADC conversion time is usually shorter than 25% of the pulse repetition period. Figure 43 shows a diagram of the averaging module. The ADC output format is in 22-bit twos complement. The two MSB bits of the 24-bit data can be ignored.

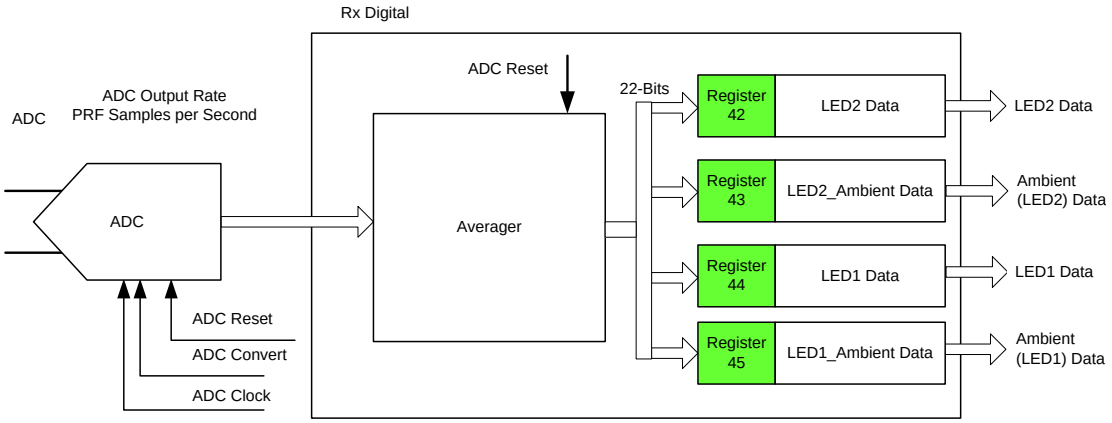


Figure 43. Averaging Module

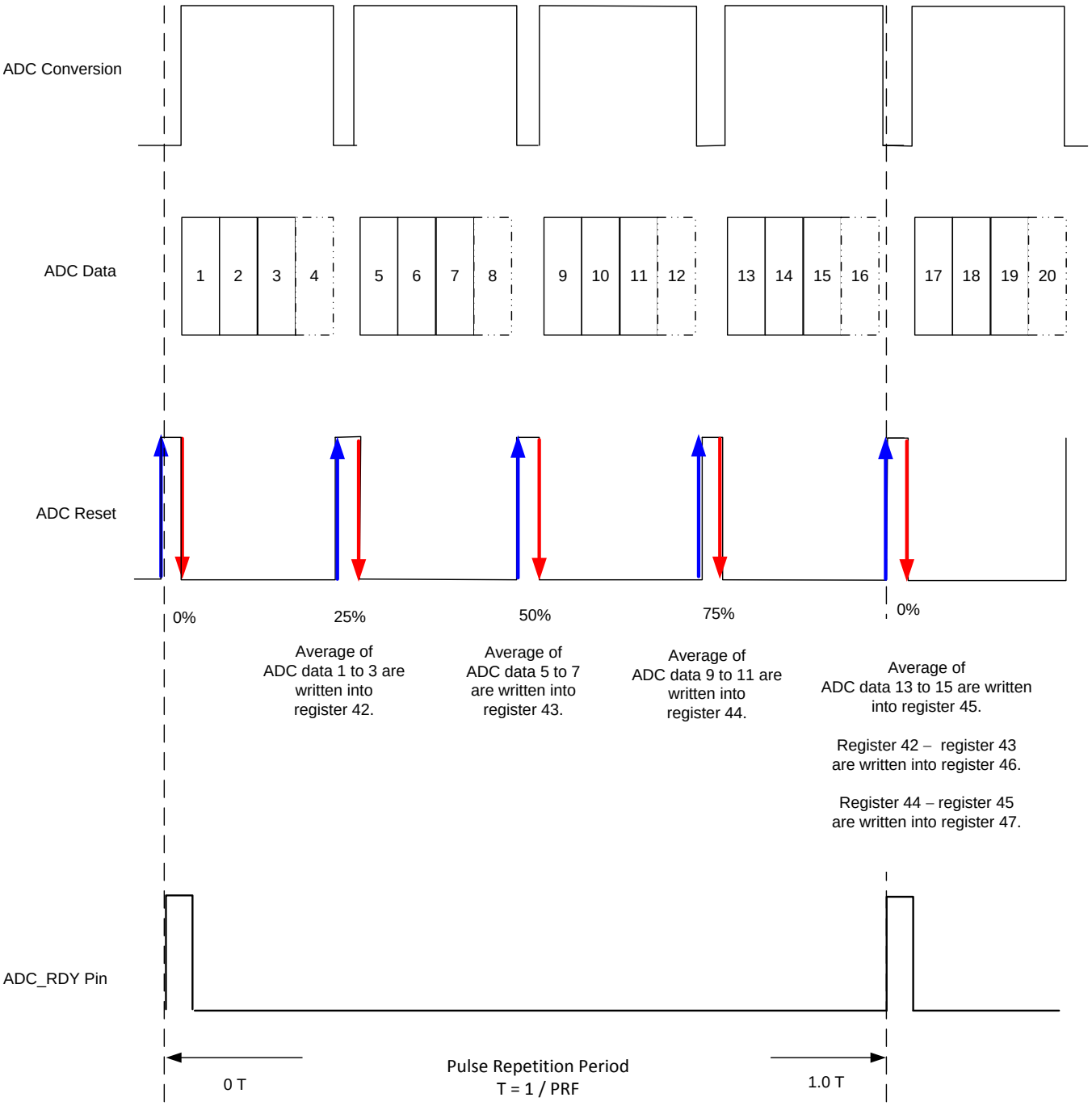
Operation

The ADC digital samples are accumulated and averaged after every 50 µs. At the next rising edge of the ADC reset signal, the average value (22-bit) is written into the output registers sequentially as follows (see Figure 44):

- At the 25% reset signal, the averaged 22-bit word is written to register 2Ah.
- At the 50% reset signal, the averaged 22-bit word is written to register 2Bh.
- At the 75% reset signal, the averaged 22-bit word is written to register 2Ch.
- At the next 0% reset signal, the averaged 22-bit word is written to register 2Dh. The contents of registers 2Ah and 2Bh are written to register 2Eh and the contents of registers 2Ch and 2Dh are written to register 2Fh.

At the rising edge of the ADC_RDY signal, the contents of all six result registers can be read out.

The number of samples to be used per conversion phase is preset to 2.



NOTE: This example shows three data averages.

Figure 44. ADC Data with Averaging

RECEIVER SUBSYSTEM POWER PATH

The block diagram in Figure 45 shows the AFE4400 Rx subsystem power routing.

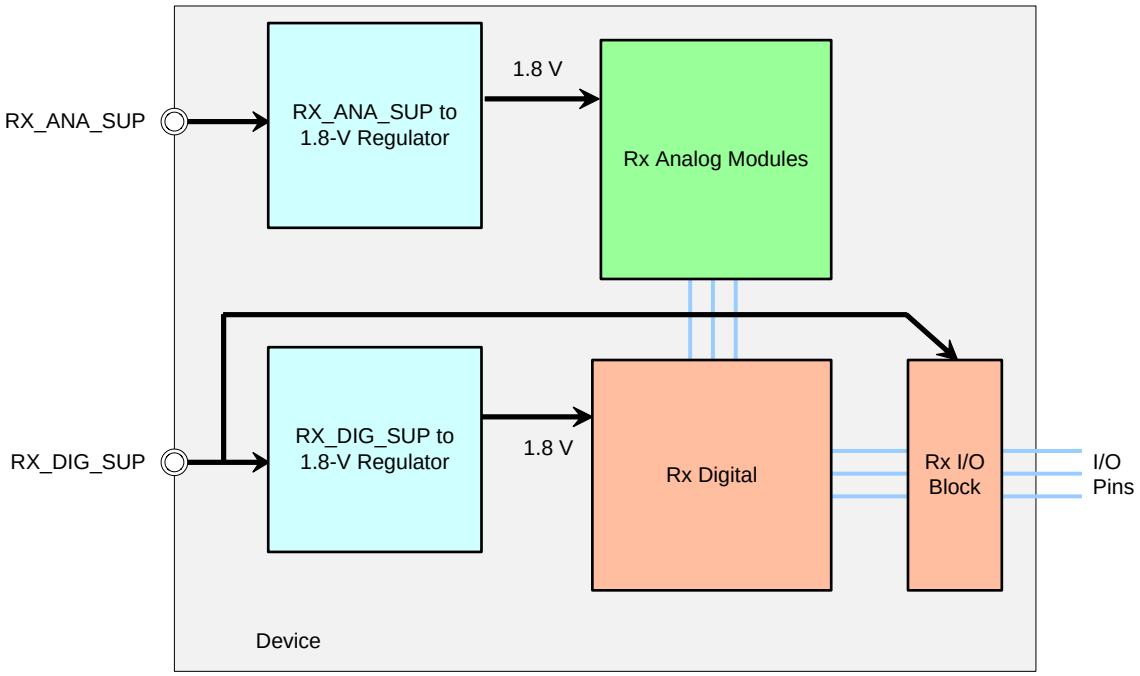


Figure 45. Receive Subsystem Power Routing

TRANSMIT SECTION

The transmit section integrates the LED driver and the LED current control section with 8-bit resolution. This integration is designed to meet a dynamic range of better than 105 dB (based on a 1-sigma LED current noise).

The RED and IR LED reference currents can be independently set. The current source (I_{LED}) locally regulates and ensures that the actual LED current tracks the specified reference. The transmitter section uses an internal 0.5-V reference voltage for operation. This reference voltage is available on the REF_TX pin and must be decoupled to ground with a 2.2-µF capacitor. The TX_REF voltage is derived from the TX_CTRL_SUP. The maximum LED current setting supports up to 50-mA LED current.

Note that reducing the value of the band gap reference capacitor on pin 7 reduces the time required for the device to wake-up and settle. However, this reduction in time is a trade-off between wake-up time and noise performance.

The minimum LED_DRV_SUP voltage required for operation depends on:

- Voltage drop across the LED (V_{LED}),
- Voltage drop across the external cable, connector, and any other component in series with the LED (V_{CABLE}), and
- Transmitter reference voltage.

Using the internal 0.5-V reference voltage, the minimum LED_DRV_SUP voltage can be as low as 3.0 V, provided that [3.0 V – (VLED + VCABLE) > 1.4 V] is met. See the Recommended Operating Conditions for further details.

Two LED driver schemes are supported:

- An H-bridge drive for a two-terminal back-to-back LED package, as shown in Figure 46.
- A push-pull drive for a three-terminal LED package; see Figure 47.

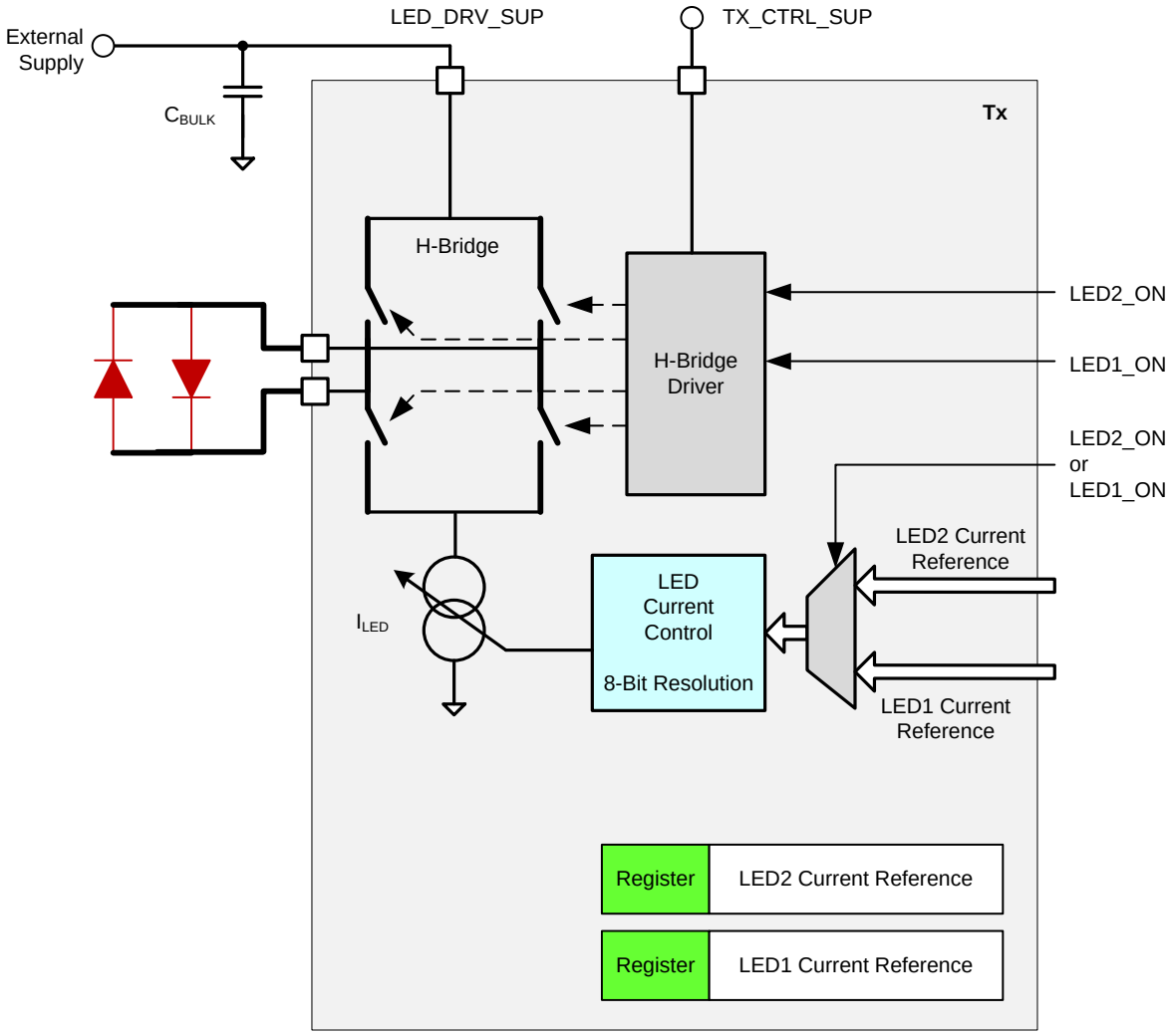


Figure 46. Transmit: H-Bridge Drive

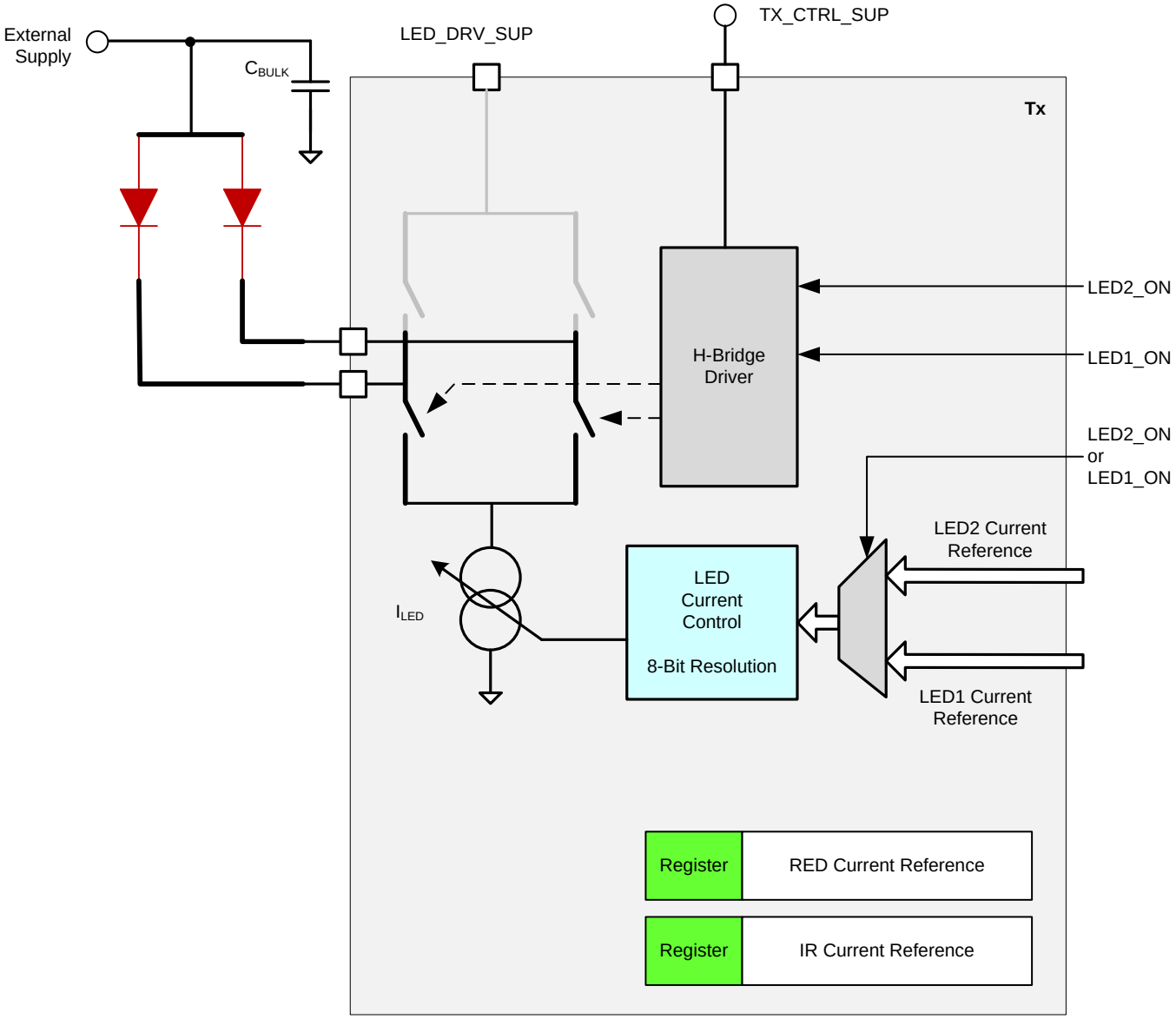


Figure 47. Transmit: Push-Pull LED Drive for Common Anode LED Configuration

Transmitter Power Path

The block diagram in Figure 48 shows the AFE4400 Tx subsystem power routing.

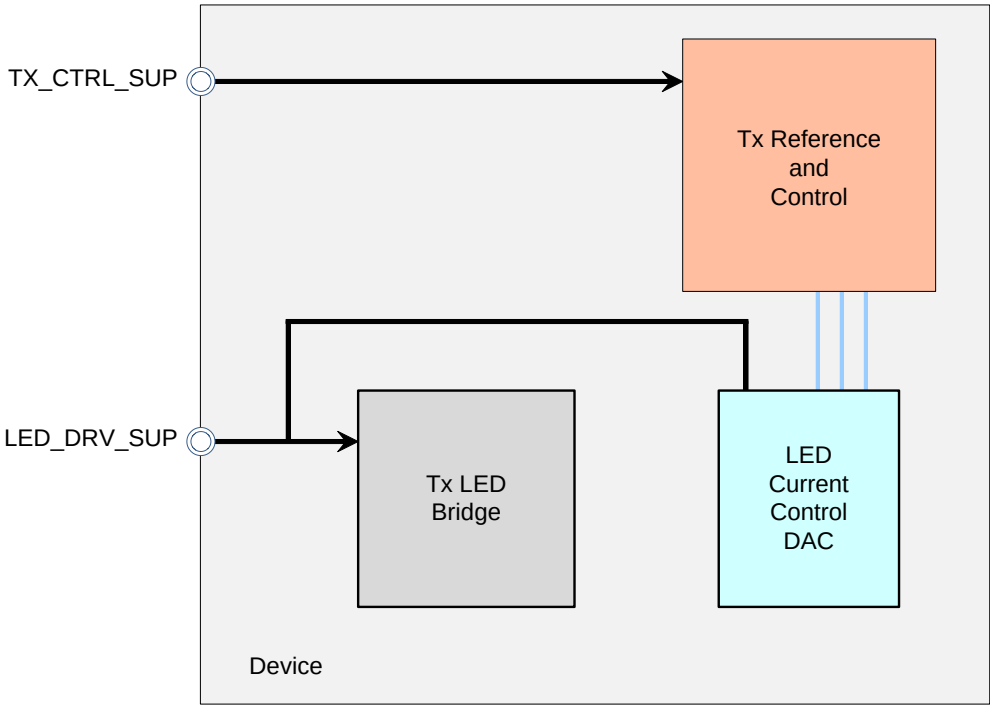


Figure 48. Transmit Subsystem Power Routing

LED Power Reduction During Periods of Inactivity

The diagram in Figure 49 shows how LED bias current passes 50 µA whenever LED_ON occurs. In order to minimize power consumption in periods of inactivity, the LED_ON control must be turned off. Furthermore, the TIMEREN bit in the CONTROL1 register should be disabled by setting the value to '0'.

Note that depending on the LEDs used, the LED may sometimes appear dimly lit even when the LED current is set to 0 mA. This appearance is because of the switching leakage currents (as shown in Figure 49) inherent to the timer function. The dimmed appearance does not effect the ambient light level measurement because during the ambient cycle, LED_ON is turned off for the duration of the ambient measurement.

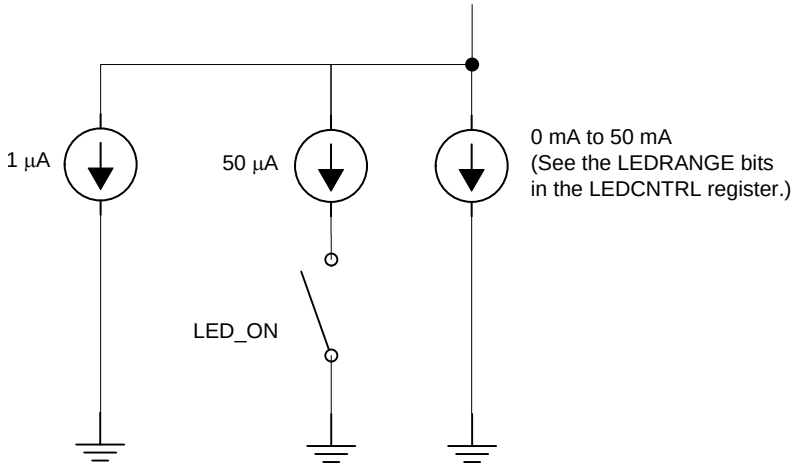


Figure 49. LED Bias Current

DIAGNOSTICS

The device includes diagnostics to detect open or short conditions of the LED and photosensor, LED current profile feedback, and cable on or off detection.

Photodiode-Side Fault Detection

Figure 50 shows the diagnostic for the photodiode-side fault detection.

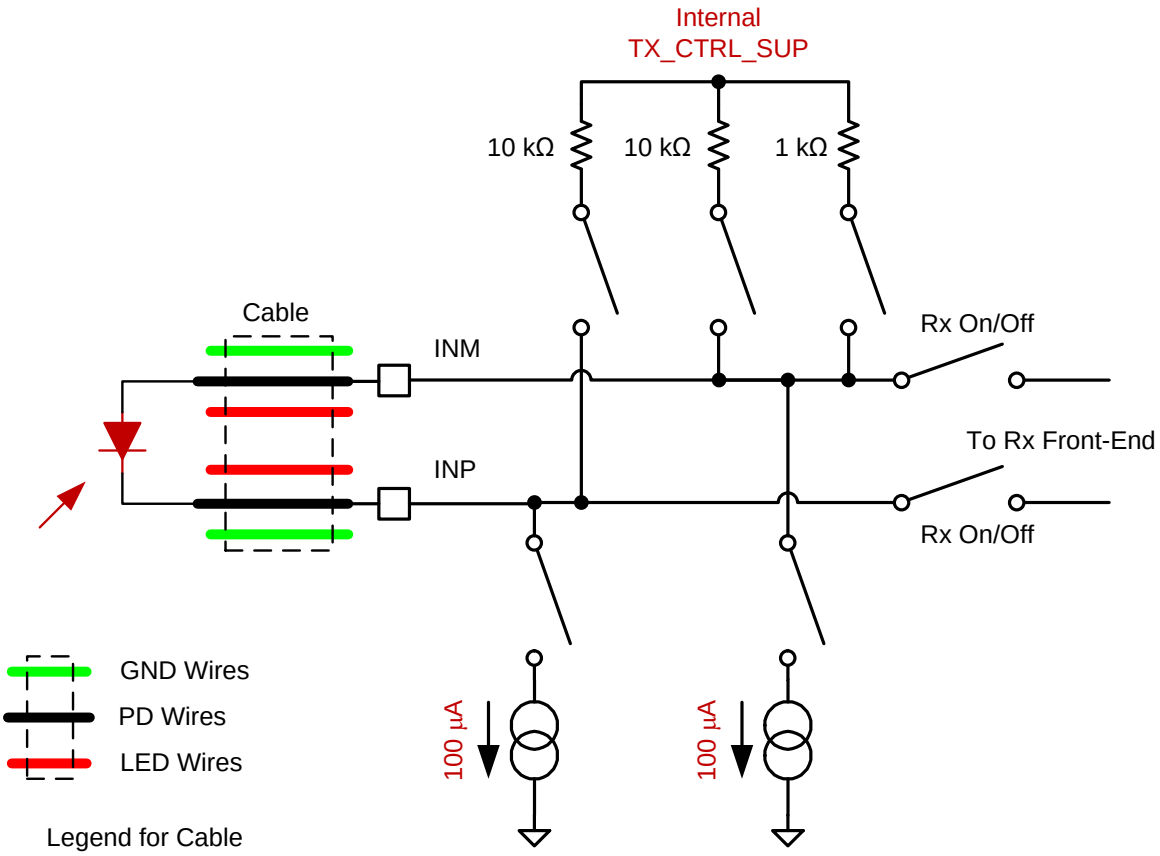


Figure 50. Photodiode Diagnostic

Transmitter-Side Fault Detection

Figure 51 shows the diagnostic for the transmitter-side fault detection.

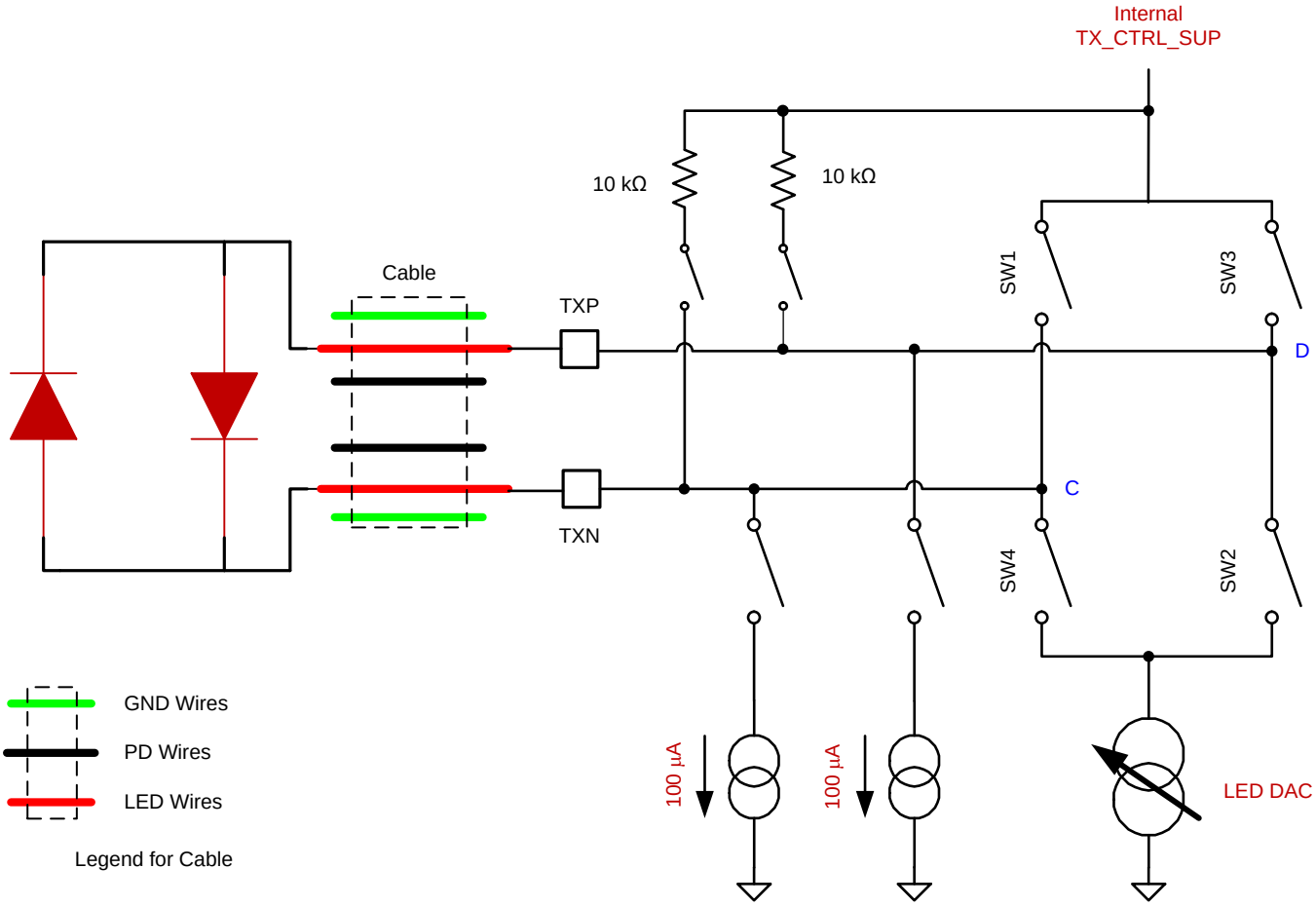


Figure 51. Transmitter Diagnostic

Diagnostics Module

The diagnostics module, when enabled, checks for nine types of faults sequentially. The results of all faults are latched in 11 separate flags. At the end of the sequence, the state of the 11 flags are combined to generate two interrupt signals: PD_ALM for photodiode-related faults and LED_ALM for transmit-related faults. The status of all flags can also be read using the SPI interface. Table 4 details each fault and flag used. Note that the diagnostics module requires all AFE blocks to be enabled in order to function reliably.

Table 4. Fault and Flag Diagnostics(1)

MODULE	SEQ.	FAULT	FLAG1	FLAG2	FLAG3	FLAG4	FLAG5	FLAG6	FLAG7	FLAG8	FLAG9	FLAG10	FLAG11
—	—	No fault	0	0	0	0	0	0	0	0	0	0	0
PD	1	Rx INP cable shorted to LED cable	1										
	2	Rx INM cable shorted to LED cable		1									
	3	Rx INP cable shorted to GND cable			1								
	4	Rx INM cable shorted to GND cable				1							
	5	PD open or shorted					1	1					
LED	6	Tx OUTM line shorted to GND cable							1				
	7	Tx OUTP line shorted to GND cable								1			
	8	LED open or shorted									1	1	
	9	LED open or shorted											1

(1) Resistances below 10 kΩ are considered to be shorted.

Figure 52 shows the timing for the diagnostic function.

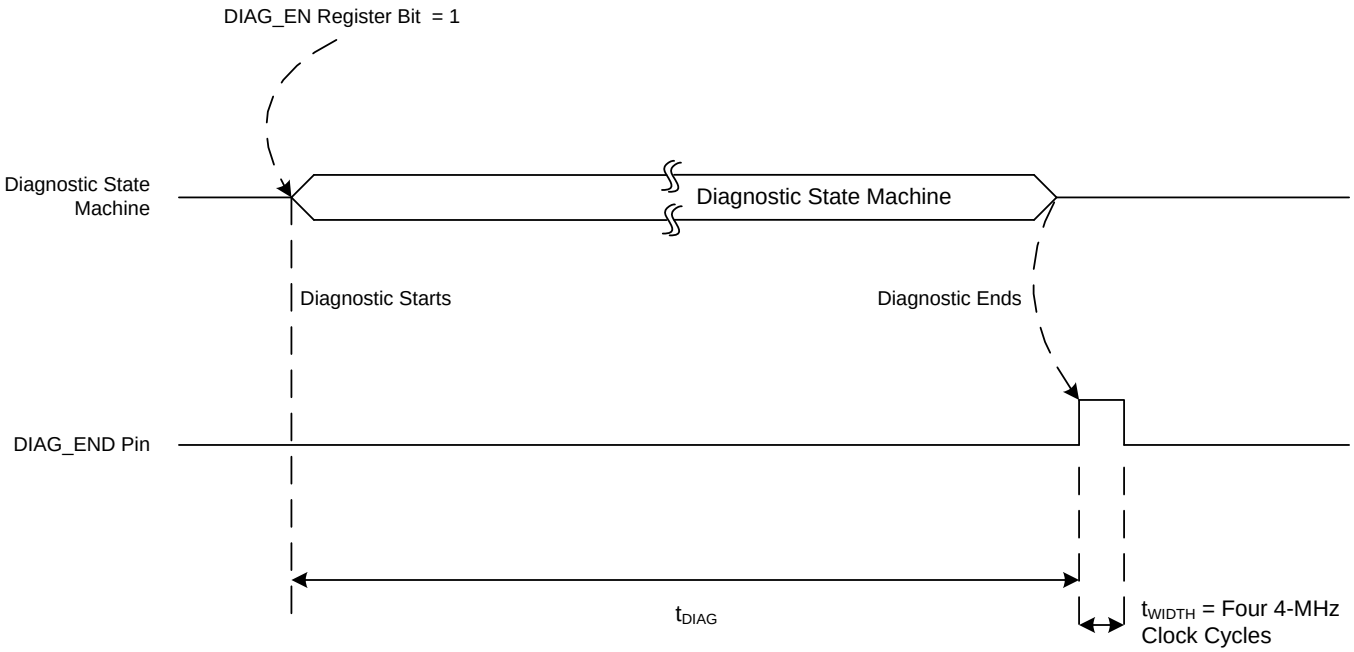


Figure 52. Diagnostic Timing Diagram

By default, the diagnostic function takes t_{DIAG} = 16 ms to complete. After the diagnostics function completes, the AFE4400 filter must be allowed time to settle. See the Electrical Characteristics for the filter settling time.

SERIAL PROGRAMMING INTERFACE

The SPI-compatible serial interface consists of four signals: SCLK (serial clock), SPISOMI (serial interface data output), SPISIMO (serial interface data input), and SPISTE (serial interface enable).

The serial clock (SCLK) is the serial peripheral interface (SPI) serial clock. SCLK shifts in commands and shifts out data from the device. SCLK features a Schmitt-triggered input and clocks data out on the SPISOMI. Data are clocked in on the SPISIMO pin. Even though the input has hysteresis, TI recommends keeping SCLK as clean as possible to prevent glitches from accidentally shifting the data. When the serial interface is idle, hold SCLK low.

The SPI serial out master in (SPISOMI) pin is used with SCLK to clock out the AFE4400 data. The SPI serial in master out (SPISIMO) pin is used with SCLK to clock in data to the AFE4400. The SPI serial interface enable (SPISTE) pin enables the serial interface to clock data on the SPISIMO pin in to the device.

READING AND WRITING DATA

The device has a set of internal registers that can be accessed by the serial programming interface formed by the SPISTE, SCLK, SPISIMO, and SPISOMI pins.

Writing Data

The SPI_READ register bit must be first set to '0' before writing to a register. When SPISTE is low,

- Serially shifting bits into the device is enabled.
- Serial data (on the SPISIMO pin) are latched at every SCLK rising edge.
- The serial data are loaded into the register at every 32nd SCLK rising edge.

In case the word length exceeds a multiple of 32 bits, the excess bits are ignored. Data can be loaded in multiples of 32-bit words within a single active SPISTE pulse. The first eight bits form the register address and the remaining 24 bits form the register data. Figure 53 shows an SPI timing diagram for a single write operation. For multiple read and write cycles, refer to the *Multiple Data Reads and Writes* section.

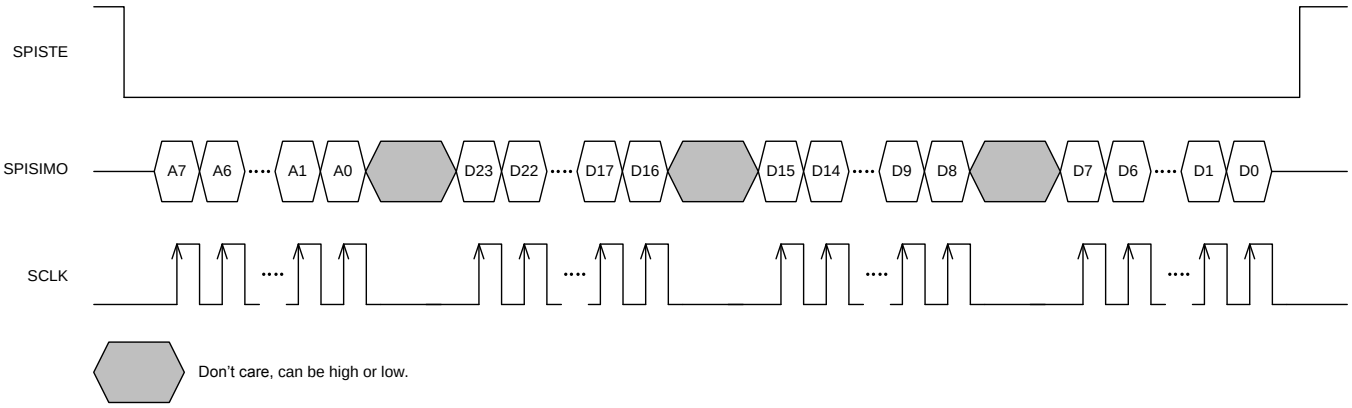
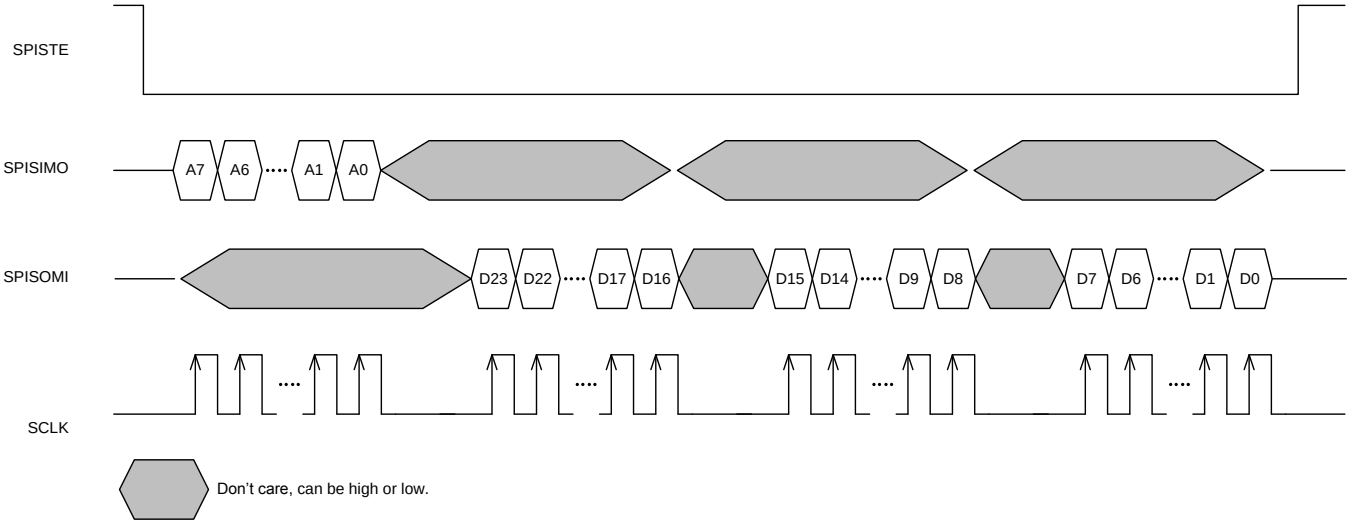


Figure 53. AFE SPI Write Timing Diagram

Reading Data

The SPI_READ register bit must be first set to '1' before reading from a register. The AFE4400 includes a mode where the contents of the internal registers can be read back on the SPISOMI pin. This mode may be useful as a diagnostic check to verify the serial interface communication between the external controller and the AFE. To enable this mode, first set the SPI_READ register bit using the SPI write command, as described in the *Writing Data* section. In the next command, specify the SPI register address with the desired content to be read. Within the same SPI command sequence, the AFE outputs the contents of the specified register on the SPISOMI pin. Figure 54 shows an SPI timing diagram for a single read operation. For multiple read and write cycles, refer to the *Multiple Data Reads and Writes* section.



(1) The SPI_READ register bit must be enabled before attempting a serial readout from the AFE.

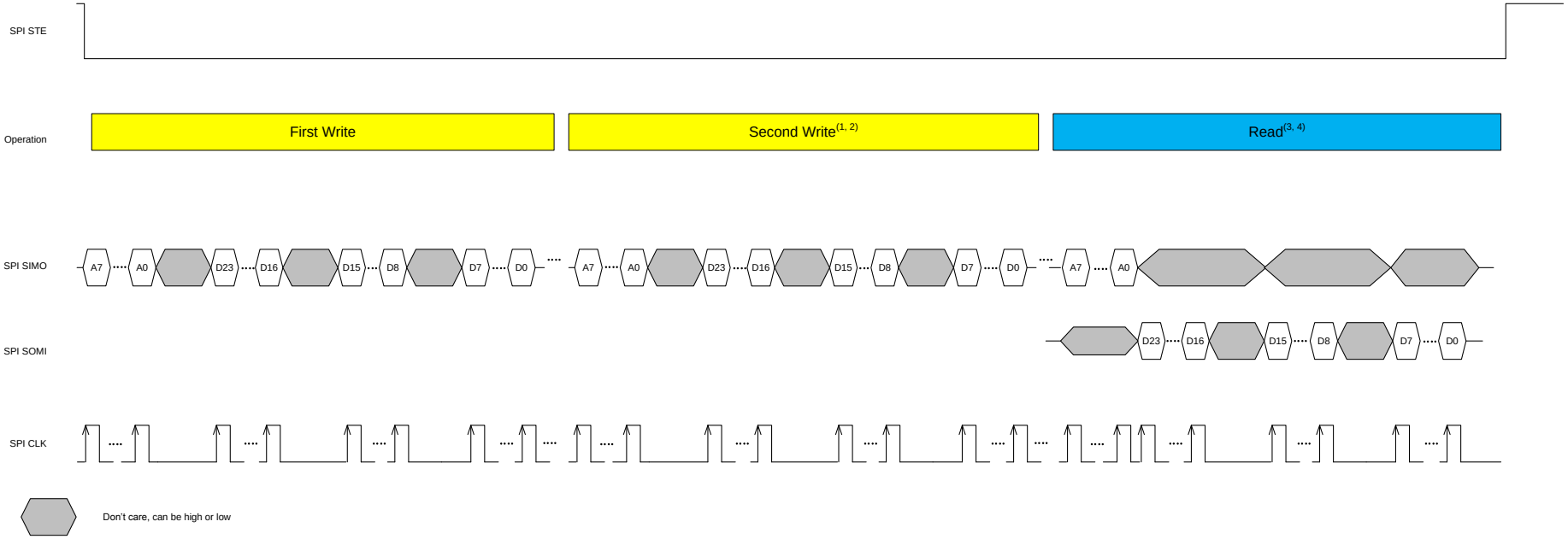
(2) Specify the register address of the content that must be readback on bits A[7:0].

(3) The AFE outputs the contents of the specified register on the SPISOMI pin.

Figure 54. AFE SPI Read Timing Diagram

Multiple Data Reads and Writes

The device includes functionality where multiple read and write operations can be performed during a single SPISTE event. To enable this functionality, the first eight bits determine the register address to be written and the remaining 24 bits determine the register data. Perform two writes with the SPI read bit enabled during the second write operation in order to prepare for the read operation, as described in the *Writing Data* section. In the next command, specify the SPI register address with the desired content to be read. Within the same SPI command sequence, the AFE outputs the contents of the specified register on the SPISOMI pin. This functionality is described in the *Writing Data* and *Reading Data* sections. Figure 55 shows a timing diagram for the SPI multiple read and write operations.



(1) The SPI read register bit must be enabled before attempting a serial readout from the AFE.

(2) The second write operation must be configured for register 0 with data 000001h.

(3) Specify the register address whose contents must be read back on A[7:0].

(4) The AFE outputs the contents of the specified register on the SOMI pin.

Figure 55. Serial Multiple Read and Write Operations

Register Initialization

After power-up, the internal registers **must** be initialized to the default values. This initialization can be done in one of two ways:

- Through a hardware reset by applying a low-going pulse on the $\overline{\text{RESET}}$ pin, or
- By applying a software reset. Using the serial interface, set SW_RESET (bit D3 in register 00h) high. This setting initializes the internal registers to the default values and then self-resets to '0'. In this case, the $\overline{\text{RESET}}$ pin is kept high (inactive).

AFE SPI Interface Design Considerations

Note that when the AFE4400 is deselected, the SPISOMI, CLKOUT, ADC_RDY, PD_ALM, LED_ALM, and DIAG_END digital output pins do not enter a 3-state mode. This condition, therefore, must be taken into account when connecting multiple devices to the SPI port and for power-management considerations. In order to avoid loading the SPI bus when multiple devices are connected, the DIGOUT_TRISTATE register bit must be to '1' whenever the AFE SPI is inactive.

AFE REGISTER MAP

The AFE consists of a set of registers that can be used to configure it, such as receiver timings, I-V amplifier settings, transmit LED currents, and so forth. The registers and their contents are listed in Table 5. These registers can be accessed using the AFE SPI interface.

Table 5. AFE Register Map

NAME	REGISTER CONTROL(1)	ADDRESS		REGISTER DATA																						
		Hex	Dec	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL0	W	00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SW_RST	DIAG_EN	TIM_COUNT_RST	SPI_READ
LED2STC	R/W	01	1	0	0	0	0	0	0	0	0	LED2STC[15:0]															
LED2ENDC	R/W	02	2	0	0	0	0	0	0	0	0	LED2ENDC[15:0]															
LED2LEDSTC	R/W	03	3	0	0	0	0	0	0	0	0	LED2LEDSTC[15:0]															
LED2LEDENDC	R/W	04	4	0	0	0	0	0	0	0	0	LED2LEDENDC[15:0]															
ALED2STC	R/W	05	5	0	0	0	0	0	0	0	0	ALED2STC[15:0]															
ALED2ENDC	R/W	06	6	0	0	0	0	0	0	0	0	ALED2ENDC[15:0]															
LED1STC	R/W	07	7	0	0	0	0	0	0	0	0	LED1STC[15:0]															
LED1ENDC	R/W	08	8	0	0	0	0	0	0	0	0	LED1ENDC[15:0]															
LED1LEDSTC	R/W	09	9	0	0	0	0	0	0	0	0	LED1LEDSTC[15:0]															
LED1LEDENDC	R/W	0A	10	0	0	0	0	0	0	0	0	LED1LEDENDC[15:0]															
ALED1STC	R/W	0B	11	0	0	0	0	0	0	0	0	ALED1STC[15:0]															
ALED1ENDC	R/W	0C	12	0	0	0	0	0	0	0	0	ALED1ENDC[15:0]															
LED2CONVST	R/W	0D	13	0	0	0	0	0	0	0	0	LED2CONVST[15:0]															
LED2CONVEND	R/W	0E	14	0	0	0	0	0	0	0	0	LED2CONVEND[15:0]															
ALED2CONVST	R/W	0F	15	0	0	0	0	0	0	0	0	ALED2CONVST[15:0]															
ALED2CONVEND	R/W	10	16	0	0	0	0	0	0	0	0	ALED2CONVEND[15:0]															
LED1CONVST	R/W	11	17	0	0	0	0	0	0	0	0	LED1CONVST[15:0]															
LED1CONVEND	R/W	12	18	0	0	0	0	0	0	0	0	LED1CONVEND[15:0]															
ALED1CONVST	R/W	13	19	0	0	0	0	0	0	0	0	ALED1CONVST[15:0]															
ALED1CONVEND	R/W	14	20	0	0	0	0	0	0	0	0	ALED1CONVEND[15:0]															
ADCRSTSTCT0	R/W	15	21	0	0	0	0	0	0	0	0	ADCRSTCT0[15:0]															
ADCRSTENDCT0	R/W	16	22	0	0	0	0	0	0	0	0	ADCRENDCT0[15:0]															
ADCRSTSTCT1	R/W	17	23	0	0	0	0	0	0	0	0	ADCRSTCT1[15:0]															
ADCRSTENDCT1	R/W	18	24	0	0	0	0	0	0	0	0	ADCRENDCT1[15:0]															
ADCRSTSTCT2	R/W	19	25	0	0	0	0	0	0	0	0	ADCRSTCT2[15:0]															
ADCRSTENDCT2	R/W	1A	26	0	0	0	0	0	0	0	0	ADCRENDCT2[15:0]															
ADCRSTSTCT3	R/W	1B	27	0	0	0	0	0	0	0	0	ADCRSTCT3[15:0]															
ADCRSTENDCT3	R/W	1C	28	0	0	0	0	0	0	0	0	ADCRENDCT3[15:0]															
PRPCOUNT	R/W	1D	29	0	0	0	0	0	0	0	0	PRPCT[15:0]															
CONTROL1	R/W	1E	30	0	0	0	0	0	0	0	0	0	0	0	0	CLKALMPIN[2:0]			TIMEREN	0	0	0	0	0	0	1	0

(1) R = read only, R/W = read or write, N/A = not available, and W = write only.

Table 5. AFE Register Map (continued)

NAME	REGISTER CONTROL(1)	ADDRESS		REGISTER DATA																							
		Hex	Dec	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SPARE1	N/A	1F	31	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
TIAGAIN	R/W	20	32	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
TIA_AMB_GAIN	R/W	21	33	0	0	0	0	AMBDAC[3:0]				0	STAGE2EN	0	0	0	STG2GAIN[2:0]			CF_LED[4:0]					RF_LED[2:0]		
LEDCNTRL	R/W	22	34	0	0	0	0	0	0	LEDCUROFF	1	LED1[7:0]								LED2[7:0]							
CONTROL2	R/W	23	35	0	0	0	0	0	0	1	0	0	0	0	0	TXBRGMOD	DIGOUT_TRISTATE	XTALDIS	1	0	0	0	0	0	PDNTX	PDNRX	PDNAFE
SPARE2	N/A	24	36	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SPARE3	N/A	25	37	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SPARE4	N/A	26	38	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED1	N/A	27	39	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESERVED2	N/A	28	40	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ALARM	R/W	29	41	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ALMPINCLKEN	0	0	0	0	0	0	0
LED2VAL	R	2A	42	LED2VAL[23:0]																							
ALED2VAL	R	2B	43	ALED2VAL[23:0]																							
LED1VAL	R	2C	44	LED1VAL[23:0]																							
ALED1VAL	R	2D	45	ALED1VAL[23:0]																							
LED2-ALED2VAL	R	2E	46	LED2-ALED2VAL[23:0]																							
LED1-ALED1VAL	R	2F	47	LED1-ALED1VAL[23:0]																							
DIAG	R	30	48	0	0	0	0	0	0	0	0	0	0	0	PD_ALM	LED_ALM	LED1OPEN	LED2OPEN	LEDSC	OUTPSHGND	OUTNSHGND	PDOC	PDSC	INNSCGND	INPSCGND	INNSCLED	INPSCLED

AFE REGISTER DESCRIPTION

CONTROL0: Control Register 0 (Address = 00h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	0	0	0	0

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	SW_RST	DIAG_EN	TIM_ COUNT_ RST	SPI_ READ

This register is write-only. CONTROL0 is used for AFE software and count timer reset, diagnostics enable, and SPI read functions.

Bits D[23:4] **Must be '0'**

Bit D3 **SW_RST: Software reset**

0 = No action (default after reset)
1 = Software reset applied; resets all internal registers to the default values and self-clears to '0'

Bit D2 **DIAG_EN: Diagnostic enable**

0 = No action (default after reset)
1 = Diagnostic mode is enabled and the diagnostics sequence starts when this bit is set. At the end of the sequence, all fault status are stored in the DIAG: Diagnostics Flag Register. Afterwards, the DIAG_EN register bit self-clears to '0'.
Note that the diagnostics enable bit is automatically reset after the diagnostics completes (16 ms). During the diagnostics mode, ADC data are invalid because of the toggling diagnostics switches.

Bit D1 **TIM_CNT_RST: Timer counter reset**

0 = Disables timer counter reset, required for normal timer operation (default after reset)
1 = Timer counters are in reset state

Bit D0 **SPI READ: SPI read**

0 = SPI read is disabled (default after reset)
1 = SPI read is enabled

LED2STC: Sample LED2 Start Count Register (Address = 01h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED2STC[15:0]			

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED2STC[15:0]											

This register sets the start timing value for the LED2 signal sample.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **LED2STC[15:0]: Sample LED2 start count**

The contents of this register can be used to position the start of the sample LED2 signal with respect to the pulse repetition period (PRP), as specified in the PRPCOUNT register. The count is specified as the number of
4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

LED2ENDC: Sample LED2 End Count Register (Address = 02h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED2ENDC[15:0]			

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED2ENDC[15:0]											

This register sets the end timing value for the LED2 signal sample.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **LED2ENDC[15:0]: Sample LED2 end count**

The contents of this register can be used to position the end of the sample LED2 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

LED2LEDSTC: LED2 LED Start Count Register (Address = 03h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED2LEDSTC[15:0]			

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED2LEDSTC[15:0]											

This register sets the start timing value for when the LED2 signal turns on.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **LED2LEDSTC[15:0]: LED2 start count**

The contents of this register can be used to position the start of the LED2 with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

LED2LEDENDC: LED2 LED End Count Register (Address = 04h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED2LEDENDC[15:0]			

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED2LEDENDC[15:0]											

This register sets the end timing value for when the LED2 signal turns off.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **LED2LEDENDC[15:0]: LED2 end count**

The contents of this register can be used to position the end of the LED2 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

ALED2STC: Sample Ambient LED2 Start Count Register (Address = 05h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ALED2STC[15:0]			

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALED2STC[15:0]											

This register sets the start timing value for the ambient LED2 signal sample.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **ALED2STC[15:0]: Sample ambient LED2 start count**

The contents of this register can be used to position the start of the sample ambient LED2 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

ALED2ENDC: Sample Ambient LED2 End Count Register (Address = 06h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ALED2ENDC[15:0]			

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALED2ENDC[15:0]											

This register sets the end timing value for the ambient LED2 signal sample.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **ALED2ENDC[15:0]: Sample ambient LED2 end count**

The contents of this register can be used to position the end of the sample ambient LED2 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

LED1STC: Sample LED1 Start Count Register (Address = 07h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED1STC[15:0]			

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED1STC[15:0]											

This register sets the start timing value for the LED1 signal sample.

Bits D[23:17] **Must be '0'**

Bits D[16:0] **LED1STC[15:0]: Sample LED1 start count**

The contents of this register can be used to position the start of the sample LED1 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of
4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

LED1ENDC: Sample LED1 End Count (Address = 08h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED1ENDC[15:0]			

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED1ENDC[15:0]											

This register sets the end timing value for the LED1 signal sample.

Bits D[23:17] **Must be '0'**

Bits D[16:0] **LED1ENDC[15:0]: Sample LED1 end count**

The contents of this register can be used to position the end of the sample LED1 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of
4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

LED1LEDSTC: LED1 LED Start Count Register (Address = 09h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED1LEDSTC[15:0]			

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED1LEDSTC[15:0]											

This register sets the start timing value for when the LED1 signal turns on.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **LED1LEDSTC[15:0]: LED1 start count**

The contents of this register can be used to position the start of the LED1 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

LED1LEDENDC: LED1 LED End Count Register (Address = 0Ah, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED1LEDENDC[15:0]			

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED1LEDENDC[15:0]											

This register sets the end timing value for when the LED1 signal turns off.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **LED1LEDENDC[15:0]: LED1 end count**

The contents of this register can be used to position the end of the LED1 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

ALED1STC: Sample Ambient LED1 Start Count Register (Address = 0Bh, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ALED1STC[15:0]			

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALED1STC[15:0]											

This register sets the start timing value for the ambient LED1 signal sample.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **ALED1STC[15:0]: Sample ambient LED1 start count**

The contents of this register can be used to position the start of the sample ambient LED1 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

ALED1ENDC: Sample Ambient LED1 End Count Register (Address = 0Ch, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ALED1ENDC[15:0]			

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALED1ENDC[15:0]											

This register sets the end timing value for the ambient LED1 signal sample.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **ALED1ENDC[15:0]: Sample ambient LED1 end count**

The contents of this register can be used to position the end of the sample ambient LED1 signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

LED2CONVST: LED2 Convert Start Count Register (Address = 0Dh, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED2CONVST[15:0]			

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED2CONVST[15:0]											

This register sets the start timing value for the LED2 conversion.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **LED2CONVST[15:0]: LED2 convert start count**

The contents of this register can be used to position the start of the LED2 conversion signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

LED2CONVEND: LED2 Convert End Count Register (Address = 0Eh, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED2CONVEND[15:0]			

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED2CONVEND[15:0]											

This register sets the end timing value for the LED2 conversion.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **LED2CONVEND[15:0]: LED2 convert end count**

The contents of this register can be used to position the end of the LED2 conversion signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

ALED2CONVST: LED2 Ambient Convert Start Count Register (Address = 0Fh, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ALED2CONVST[15:0]			

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALED2CONVST[15:0]											

This register sets the start timing value for the ambient LED2 conversion.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **ALED2CONVST[15:0]: LED2 ambient convert start count**

The contents of this register can be used to position the start of the LED2 ambient conversion signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

ALED2CONVEND: LED2 Ambient Convert End Count Register (Address = 10h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ALED2CONVEND[15:0]			

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALED2CONVEND[15:0]											

This register sets the end timing value for the ambient LED2 conversion.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **ALED2CONVEND[15:0]: LED2 ambient convert end count**

The contents of this register can be used to position the end of the LED2 ambient conversion signal with respect to the PRP. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

LED1CONVST: LED1 Convert Start Count Register (Address = 11h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED1CONVST[15:0]			

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED1CONVST[15:0]											

This register sets the start timing value for the LED1 conversion.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **LED1CONVST[15:0]: LED1 convert start count**

The contents of this register can be used to position the start of the LED1 conversion signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

LED1CONVEND: LED1 Convert End Count Register (Address = 12h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	LED1CONVEND[15:0]			

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED1CONVEND[15:0]											

This register sets the end timing value for the LED1 conversion.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **LED1CONVEND[15:0]: LED1 convert end count**

The contents of this register can be used to position the end of the LED1 conversion signal with respect to the PRP. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

ALED1CONVST: LED1 Ambient Convert Start Count Register (Address = 13h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ALED1CONVST[15:0]			

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALED1CONVST[15:0]											

This register sets the start timing value for the ambient LED1 conversion.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **ALED1CONVST[15:0]: LED1 ambient convert start count**

The contents of this register can be used to position the start of the LED1 ambient conversion signal with respect to the PRP, as specified in the PRPCOUNT register. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

ALED1CONVEND: LED1 Ambient Convert End Count Register (Address = 14h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ALED1CONVEND[15:0]			

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALED1CONVEND[15:0]											

This register sets the end timing value for the ambient LED1 conversion.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **ALED1CONVEND[15:0]: LED1 ambient convert end count**

The contents of this register can be used to position the end of the LED1 ambient conversion signal with respect to the PRP. The count is specified as the number of 4-MHz clock cycles. Refer to the *Using the Timer Module* section for details.

ADCRSTSTCT0: ADC Reset 0 Start Count Register (Address = 15h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ADCRSTSTCT0[15:0]			

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADCRSTSTCT0[15:0]											

This register sets the start position of the ADC0 reset conversion signal.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **ADCRSTSTCT0[15:0]: ADC RESET 0 start count**

The contents of this register can be used to position the start of the ADC reset conversion signal (default value after reset is 0000h). Refer to the *Using the Timer Module* section for details.

ADCRSTENDCT0: ADC Reset 0 End Count Register (Address = 16h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ADCRSTENDCT0[15:0]			

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADCRSTENDCT0[15:0]											

This register sets the end position of the ADC0 reset conversion signal.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **ADCRSTENDCT0[15:0]: ADC RESET 0 end count**

The contents of this register can be used to position the end of the ADC reset conversion signal (default value after reset is 0000h). Refer to the *Using the Timer Module* section for details.

ADCRSTSTCT1: ADC Reset 1 Start Count Register (Address = 17h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ADCRSTSTCT1[15:0]			

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADCRSTSTCT1[15:0]											

This register sets the start position of the ADC1 reset conversion signal.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **ADCRSTSTCT1[15:0]: ADC RESET 1 start count**

The contents of this register can be used to position the start of the ADC reset conversion. Refer to the *Using the Timer Module* section for details.

ADCRSTENDCT1: ADC Reset 1 End Count Register (Address = 18h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ADCRSTENDCT1[15:0]			

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADCRSTENDCT1[15:0]											

This register sets the end position of the ADC1 reset conversion signal.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **ADCRSTENDCT1[15:0]: ADC RESET 1 end count**

The contents of this register can be used to position the end of the ADC reset conversion. Refer to the *Using the Timer Module* section for details.

ADCRSTSTCT2: ADC Reset 2 Start Count Register (Address = 19h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ADCRSTSTCT2[15:0]			

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADCRSTSTCT2[15:0]											

This register sets the start position of the ADC2 reset conversion signal.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **ADCRSTSTCT2[15:0]: ADC RESET 2 start count**

The contents of this register can be used to position the start of the ADC reset conversion. Refer to the *Using the Timer Module* section for details.

ADCRSTENDCT2: ADC Reset 2 End Count Register (Address = 1Ah, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ADCRSTENDCT2[15:0]			

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADCRSTENDCT2[15:0]											

This register sets the end position of the ADC2 reset conversion signal.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **ADCRSTENDCT2[15:0]: ADC RESET 2 end count**

The contents of this register can be used to position the end of the ADC reset conversion. Refer to the *Using the Timer Module* section for details.

ADCRSTSTCT3: ADC Reset 3 Start Count Register (Address = 1Bh, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ADCRSTSTCT3[15:0]			

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADCRSTSTCT3[15:0]											

This register sets the start position of the ADC3 reset conversion signal.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **ADCRSTSTCT3[15:0]: ADC RESET 3 start count**

The contents of this register can be used to position the start of the ADC reset conversion. Refer to the *Using the Timer Module* section for details.

ADCRSTENDCT3: ADC Reset 3 End Count Register (Address = 1Ch, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	ADCRSTENDCT3[15:0]			

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADCRSTENDCT3[15:0]											

This register sets the end position of the ADC3 reset conversion signal.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **ADCRSTENDCT3[15:0]: ADC RESET 3 end count**

The contents of this register can be used to position the end of the ADC reset conversion signal (default value after reset is 0000h). Refer to the *Using the Timer Module* section for details.

PRPCOUNT: Pulse Repetition Period Count Register (Address = 1Dh, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	PRPCOUNT[15:0]			

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PRPCOUNT[15:0]											

This register sets the device pulse repetition period count.

Bits D[23:16] **Must be '0'**

Bits D[15:0] **PRPCOUNT[15:0]: Pulse repetition period count**

The contents of this register can be used to set the pulse repetition period (in number of clock cycles of the 4-MHz clock). The PRPCOUNT value must be set in the range of 800 to 64000. Values below 800 do not allow sufficient sample time for the four samples; see the Electrical Characteristics table.

CONTROL1: Control Register 1 (Address = 1Eh, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	0	0	0	0

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CLKALMPIN[2:0]			TIMEREN	0	0	0	0	0	0	1	0

This register configures the clock alarm pin and timer.

Bits D[23:12] **Must be '0'**

Bits D[11:9] **CLKALMPIN[2:0]: Clocks on ALM pins**

Internal clocks can be brought to the PD_ALM and LED_ALM pins for monitoring. Note that the ALMPINCLKEN register bit must be set before using this register bit. Table 6 defines the settings for the two alarm pins.

Bit D8 **TIMEREN: Timer enable**

0 = Timer module is disabled and all internal clocks are off (default after reset)
1 = Timer module is enabled

Bits D[7:2] **Must be '0'**

Bit D1 **Must be '1'**

Bit D0 **Must be '0'**

Table 6. PD_ALM and LED_ALM Pin Settings

CLKALMPIN[2:0]	PD_ALM PIN SIGNAL	LED_ALM PIN SIGNAL
000	Sample LED2 pulse	Sample LED1 pulse
001	LED2 LED pulse	LED1 LED pulse
010	Sample LED2 ambient pulse	Sample LED1 ambient pulse
011	LED2 convert	LED1 convert
100	LED2 ambient convert	LED1 ambient convert
101	No output	No output
110	No output	No output
111	No output	No output

SPARE1: SPARE1 Register For Future Use (Address = 1Fh, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	0	0	0	0

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0

This register is a spare register and is reserved for future use.

Bits D[23:0] Must be '0'

TIAGAIN: Transimpedance Amplifier Gain Setting Register (Address = 20h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	0	0	0	0

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0

This register is reserved for factory use.

Bits D[23:0] Must be '0'

TIA_AMB_GAIN: Transimpedance Amplifier and Ambient Cancellation Stage Gain Register (Address = 21h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	AMBDAC[3:0]				0	STAGE2EN	0	0

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	STG2GAIN[2:0]			CF_LED[4:0]					RF_LED[2:0]		

This register configures the ambient light cancellation amplifier gain, cancellation current, and filter corner frequency.

Bits D[23:20] **Must be '0'**

Bits D[19:16] **AMBDAC[3:0]: Ambient DAC value**

These bits set the value of the cancellation current.

0000 = 0 µA (default after reset)
0001 = 1 µA
0010 = 2 µA
0011 = 3 µA
0100 = 4 µA
0101 = 5 µA
0110 = 6 µA
0111 = 7 µA
1000 = 8 µA
1001 = 9 µA
1010 = 10 µA
1011 = Do not use
1100 = Do not use
1101 = Do not use
1110 = Do not use
1111 = Do not use

Bit D15 **Must be '0'**

Bit D14 **STAGE2EN: Stage 2 enable**

0 = Stage 2 is bypassed (default after reset)
1 = Stage 2 is enabled with the gain value specified by the STG2GAIN[2:0] bits

Bits D[13:11] **Must be '0'**

Bits D[10:8] **STG2GAIN[2:0]: Stage 2 gain setting**

000 = 0 dB, or linear gain of 1 (default after reset)
001 = 3.5 dB, or linear gain of 1.5
010 = 6 dB, or linear gain of 2
011 = 9.5 dB, or linear gain of 3
100 = 12 dB, or linear gain of 4
101 = Do not use
110 = Do not use
111 = Do not use

Bits D[7:3] **CF_LED[4:0]: Program C_F for LEDs**

00000 = 5 pF (default after reset)
00001 = 5 pF + 5 pF
00010 = 15 pF + 5 pF
00100 = 25 pF + 5 pF
01000 = 50 pF + 5 pF
10000 = 150 pF + 5 pF

Note that any combination of these C_F settings is also supported by setting multiple bits to '1'. For example, to obtain C_F = 100 pF, set D[7:3] = 01111.

Bits D[2:0] **RF_LED[2:0]: Program R_F for LEDs**

000 = 500 kΩ
001 = 250 kΩ
010 = 100 kΩ
011 = 50 kΩ
100 = 25 kΩ
101 = 10 kΩ
110 = 1 MΩ
111 = None

LEDCNTRL: LED Control Register (Address = 22h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	LEDCUR OFF	1	LED1[7:0]			

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED1[7:0]				LED2[7:0]							

This register sets the LED current range and the LED1 and LED2 drive current.

Bits D[23:18] **Must be '0'**

Bit D17 **LEDCUROFF: Turns the LED current source on or off**

0 = On (50 mA)
1 = Off

Bit D16 **Must be '1'**

Bits D[15:8] **LED1[7:0]: Program LED current for LED1 signal**

Use these register bits to specify the LED current setting for LED1 (default after reset is 00h).
The nominal value of the LED current is given by Equation 3, where the full-scale LED current is 50 mA.

Bits D[7:0] **LED2[7:0]: Program LED current for LED2 signal**

Use these register bits to specify the LED current setting for LED2 (default after reset is 00h).
The nominal value of LED current is given by Equation 4, where the full-scale LED current is 50 mA.

$$\frac{\text{LED1[7:0]}}{256} \times \text{Full-Scale Current} \quad (3)$$

$$\frac{\text{LED2[7:0]}}{256} \times \text{Full-Scale Current} \quad (4)$$

CONTROL2: Control Register 2 (Address = 23h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	1	0	0	0	0	0

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TXBRG MOD	DIGOUT_ TRI STATE	XTAL DIS	1	0	0	0	0	0	PDNTX	PDNRX	PDNAFE

This register controls the LED transmitter, crystal, and the AFE, transmitter, and receiver power modes.

Bits D[23:18] **Must be '0'**

Bit D17 **Must be '1'**

Bits D[16:12] **Must be '0'**

Bit D11 **TXBRGMOD: Tx bridge mode**

0 = LED driver is configured as an H-bridge (default after reset)
1 = LED driver is configured as a push-pull

Bit D10 **DIGOUT_TRISTATE: Digital output 3-state mode**

This bit determines the state of the device digital output pins, including the clock output pin and SPI output pins. In order to avoid loading the SPI bus when multiple devices are connected, this bit must be set to '1' (3-state mode) whenever the device SPI is inactive.

0 = Normal operation (default)
1 = 3-state mode

Bit D9 **XTALDIS: Crystal disable mode**

0 = The crystal module is enabled; the 8-MHz crystal must be connected to the XIN and XOUT pins
1 = The crystal module is disabled; an external 8-MHz clock must be applied to the XIN pin

Bit D8 **Must be '1'**

Bits D[7:3] **Must be '0'**

Bit D2 **PDN_TX: Tx power-down**

0 = The Tx is powered up (default after reset)
1 = Only the Tx module is powered down

Bit D1 **PDN_RX: Rx power-down**

0 = The Rx is powered up (default after reset)
1 = Only the Rx module is powered down

Bit D0 **PDN_AFE: AFE power-down**

0 = The AFE is powered up (default after reset)
1 = The entire AFE is powered down (including the Tx, Rx, and diagnostics blocks)

SPARE2: SPARE2 Register For Future Use (Address = 24h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	0	0	0	0

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0

This register is a spare register and is reserved for future use.

Bits D[23:0] **Must be '0'**

SPARE3: SPARE3 Register For Future Use (Address = 25h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	0	0	0	0

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0

This register is a spare register and is reserved for future use.

Bits D[23:0] Must be '0'

SPARE4: SPARE4 Register For Future Use (Address = 26h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	0	0	0	0

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0

This register is a spare register and is reserved for future use.

Bits D[23:0] Must be '0'

RESERVED1: RESERVED1 Register For Factory Use Only (Address = 27h, Reset Value = XXXXh)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
X(1)	X	X	X	X	X	X	X	X	X	X	X

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X

(1) X = don't care.

This register is reserved for factory use. Readback values vary between devices.

RESERVED2: RESERVED2 Register For Factory Use Only (Address = 28h, Reset Value = XXXXh)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
X(1)	X	X	X	X	X	X	X	X	X	X	X

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X

(1) X = don't care.

This register is reserved for factory use. Readback values vary between devices.

ALARM: Alarm Register (Address = 29h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	0	0	0	0

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	ALMPIN CLKEN	0	0	0	0	0	0	0

This register controls the Alarm pin functionality.

Bits D[23:8] **Must be '0'**

Bit D7 **ALMPINCLKEN: Alarm pin clock enable**

0 = Disables the monitoring of internal clocks; the PD_ALM and LED_ALM pins function as diagnostic fault alarm output pins (default after reset)
1 = Enables the monitoring of internal clocks; these clocks can be brought out on PD_ALM and LED_ALM selectively (depending on the value of the CLKALMPIN[2:0] register bits).

Bits D[6:0] **Must be '0'**

LED2VAL: LED2 Digital Sample Value Register (Address = 2Ah, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
LED2VAL[23:0]											

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED2VAL[23:0]											

Bits D[23:0] **LED2VAL[23:0]: LED2 digital value**

This register contains the digital value of the latest LED2 sample converted by the ADC. The ADC_RDY signal goes high each time that the contents of this register are updated. The host processor must readout this register before the next sample is converted by the AFE.

ALED2VAL: Ambient LED2 Digital Sample Value Register (Address = 2Bh, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
ALED2VAL[23:0]											

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALED2VAL[23:0]											

Bits D[23:0] **ALED2VAL[23:0]: LED2 ambient digital value**

This register contains the digital value of the latest LED2 ambient sample converted by the ADC. The ADC_RDY signal goes high each time that the contents of this register are updated. The host processor must readout this register before the next sample is converted by the AFE.

LED1VAL: LED1 Digital Sample Value Register (Address = 2Ch, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
LED1VAL[23:0]											

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED1VAL[23:0]											

Bits D[23:0] **LED1VAL[23:0]: LED1 digital value**

This register contains the digital value of the latest LED1 sample converted by the ADC. The ADC_RDY signal goes high each time that the contents of this register are updated. The host processor must readout this register before the next sample is converted by the AFE.

ALED1VAL: Ambient LED1 Digital Sample Value Register (Address = 2Dh, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
ALED1VAL[23:0]											

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALED1VAL[23:0]											

Bits D[23:0] **ALED1VAL[23:0]: LED1 ambient digital value**

This register contains the digital value of the latest LED1 ambient sample converted by the ADC. The ADC_RDY signal goes high each time that the contents of this register are updated. The host processor must readout this register before the next sample is converted by the AFE.

LED2-ALED2VAL: LED2-Ambient LED2 Digital Sample Value Register (Address = 2Eh, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
LED2-ALED2VAL[23:0]											

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED2-ALED2VAL[23:0]											

Bits D[23:0] **LED2-ALED2VAL[23:0]: (LED2 – LED2 ambient) digital value**

This register contains the digital value of the LED2 sample after the LED2 ambient is subtracted. The host processor must readout this register before the next sample is converted by the AFE.
Note that this value is inverted when compared to waveforms shown in many publications.

LED1-ALED1VAL: LED1-Ambient LED1 Digital Sample Value Register (Address = 2Fh, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
LED1-ALED1VAL[23:0]											

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED1-ALED1VAL[23:0]											

Bits D[23:0] **LED1-ALED1VAL[23:0]: (LED1 – LED1 ambient) digital value**

This register contains the digital value of the LED1 sample after the LED1 ambient is subtracted from it. The host processor must readout this register before the next sample is converted by the AFE.
Note that this value is inverted when compared to waveforms shown in many publications.

DIAG: Diagnostics Flag Register (Address = 30h, Reset Value = 0000h)

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	0	0	0	0	0	0	0	0	0	0	PD_ALM

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LED_ ALM	LED1 OPEN	LED2 OPEN	LEDSC	OUTPSH GND	OUTNSH GND	PDOC	PDSC	INNSC GND	INPSC GND	INNSC LED	INPSC LED

This register is read only. This register contains the status of all diagnostic flags at the end of the diagnostics sequence. The end of the diagnostics sequence is indicated by the signal going high on DIAG_END pin.

Bits D[23:13] **Read only**

Bit D12 **PD_ALM: Power-down alarm status diagnostic flag**

This bit indicates the status of PD_ALM (and the PD_ALM pin).
0 = No fault (default after reset)
1 = Fault present

Bit D11 **LED_ALM: LED alarm status diagnostic flag**

This bit indicates the status of LED_ALM (and the LED_ALM pin).
0 = No fault (default after reset)
1 = Fault present

Bit D10 **LED1OPEN: LED1 open diagnostic flag**

This bit indicates that LED1 is open.
0 = No fault (default after reset)
1 = Fault present

Bit D9 **LED2OPEN: LED2 open diagnostic flag**

This bit indicates that LED2 is open.
0 = No fault (default after reset)
1 = Fault present

Bit D8 **LEDSC: LED short diagnostic flag**

This bit indicates an LED short.
0 = No fault (default after reset)
1 = Fault present

Bit D7 **OUTPSHGND: OUTP to GND diagnostic flag**

This bit indicates that OUTP is shorted to the GND cable.
0 = No fault (default after reset)
1 = Fault present

Bit D6 **OUTNSHGND: OUTN to GND diagnostic flag**

This bit indicates that OUTN is shorted to the GND cable.
0 = No fault (default after reset)
1 = Fault present

Bit D5 **PDOC: PD open diagnostic flag**

This bit indicates that PD is open.
0 = No fault (default after reset)
1 = Fault present

Bit D4 **PDSC: PD short diagnostic flag**

This bit indicates a PD short.
0 = No fault (default after reset)
1 = Fault present

Bit D3 **INNSCGND: INN to GND diagnostic flag**

This bit indicates a short from the INN pin to the GND cable.
0 = No fault (default after reset)
1 = Fault present

Bit D2 **INPSCGND: INP to GND diagnostic flag**

This bit indicates a short from the INP pin to the GND cable.
0 = No fault (default after reset)
1 = Fault present

Bit D1 **INNSCLED: INN to LED diagnostic flag**

This bit indicates a short from the INN pin to the LED cable.
0 = No fault (default after reset)
1 = Fault present

Bit D0 **INPSCLED: INP to LED diagnostic flag**

This bit indicates a short from the INP pin to the LED cable.
0 = No fault (default after reset)
1 = Fault present

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (October 2013) to Revision F **Page**

- Changed footnote 1 in Recommended Operating Conditions table ... 3
- Changed LED_DRV_SUP parameter in Recommended Operating Conditions table ... 3
- Changed *TXM* to *TXN* in V_{LED} footnote of Recommended Operating Conditions table ... 3
- Changed Transmitter, *Voltage on TXP (or TXN) pin* parameter in Electrical Characteristics table ... 5
- Changed Figure 51 (changed TXP and TXN pin names, deleted LED 1 and LED 2 pin names) ... 37

Changes from Revision D (May 2013) to Revision E **Page**

- Deleted chip graphic ... 1
- Changed 1st sub-bullet of 3rd Features bullet ... 1
- Changed last sub-bullet of Supplies Features bullet ... 1
- Updated front page graphic ... 1
- Changed Tx Power Supply column in Family and Ordering Information table ... 2
- Changed *TX_CTRL_SUP* value in Recommended Operating Conditions table ... 3
- Changed conditions for Electrical Characteristics table ... 4
- Changed Performance, *PRF* parameter minimum specification in Electrical Characteristics table ... 4
- Deleted Performance, I_{IN_FS} parameter from Electrical Characteristics table ... 4
- Changed Performance, *CMRR* parameter in Electrical Characteristics table ... 4
- Changed Performance (Full-Signal Chain), *Total integrated noise current* and N_{FB} parameter test conditions in Electrical Characteristics table ... 4
- Changed Receiver Functional Block Level Specification, *Total integrated noise current* parameter test conditions in Electrical Characteristics table ... 4
- Changed Ambient Cancellation Stage, *Gain* parameter in Electrical Characteristics table ... 5
- Added Low-Pass Filter, *Filter settling time* parameter to Electrical Characteristics table ... 5
- Changed Diagnostics, *Duration of diagnostics state machine* parameter unit value in Electrical Characteristics table ... 5
- Changed External Clock, *Maximum allowable external clock jitter* parameter in Electrical Characteristics table ... 6
- Changed *TX_REF* description in Pin Descriptions table ... 11
- Updated Figure 6 to Figure 8 ... 12
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- Updated Figure 15 to Figure 17 ... 13
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- Changed second sentence in second paragraph of *Receiver Front-End* section ... 18
- Changed third paragraph of *Receiver Front-End* section ... 18
- Changed second paragraph of *Ambient Cancellation Scheme* section ... 20
- Added last paragraph and Table 2 to *Ambient Cancellation Scheme* section ... 21
- Updated Figure 36 ... 22
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- Added footnote 1 to Table 3 ... 26
- Changed example column in Table 3 ... 26
- Added last sentence to third column of row t_{13} in Table 3 ... 26
- Deleted last sentence from third column of row t_{14} in Table 3 ... 26

- Changed corresponding register address name in row t_{21} of Table 3 26
- Updated Figure 41 27
- Updated Figure 42 28
- Changed second paragraph of the *ADC Operation and Averaging Module* section 29
- Updated Figure 43 29
- Changed *Operation* section title and first sentence 29
- Changed last sentence of the *Operation With Averaging* section 29
- Updated Figure 44 30
- Updated Figure 45 31
- Changed entire *Transmit Section* 32
- Changed last paragraph of *Diagnostics Module* section 39
- Added first and last sentence to *Writing Data* section 40
- Changed second to last sentence in *Writing Data* section 40
- Added first and last sentence to *Reading Data* section 41
- Changed second to last sentence in *Reading Data* section 41
- Added *Multiple Data Reads and Writes* section 42
- Added last sentence to the *AFE SPI Interface Design Considerations* section 43
- Added Register Control column to Table 5 44
- Changed name of ADCRSTSTCT0 register (address 15h) in Table 5 44
- Changed bit D10 in CONTROL2 row of Table 5 45
- Changed CONTROL0 paragraph description 46
- Added note to bit D2 description of CONTROL0 register 46
- Corrected bit names in ADCRSTSTCT0 register 53
- Changed PRPCOUNT[15:0] (bits D[15:0]) description of PRPCOUNT register 56
- Changed note within CLKALMPIN[2:0] (bits D[11:9]) description of CONTROL1 register 56
- Changed second and third columns of Table 6 56
- Changed *001* and *011* bit settings for the STG2GAIN[2:0] bits (bits D[10:8]) in the TIA_AMB_GAIN register 58
- Changed bit D10 of the CONTROL2 register 60

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AFE4400RHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	AFE4400	Samples
AFE4400RHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	AFE4400	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

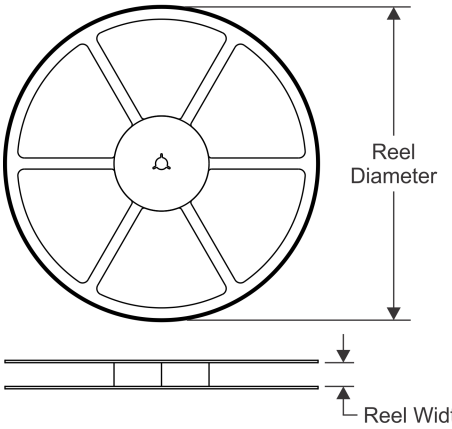
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

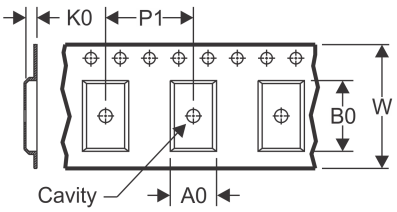
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

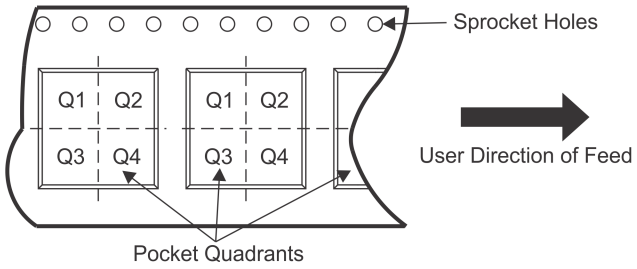


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

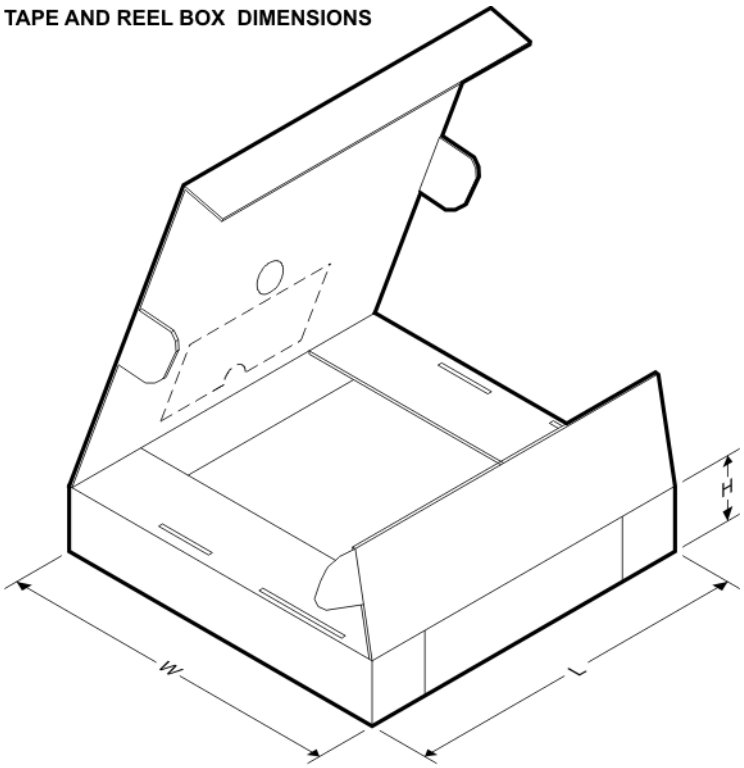
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AFE4400RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2
AFE4400RHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2

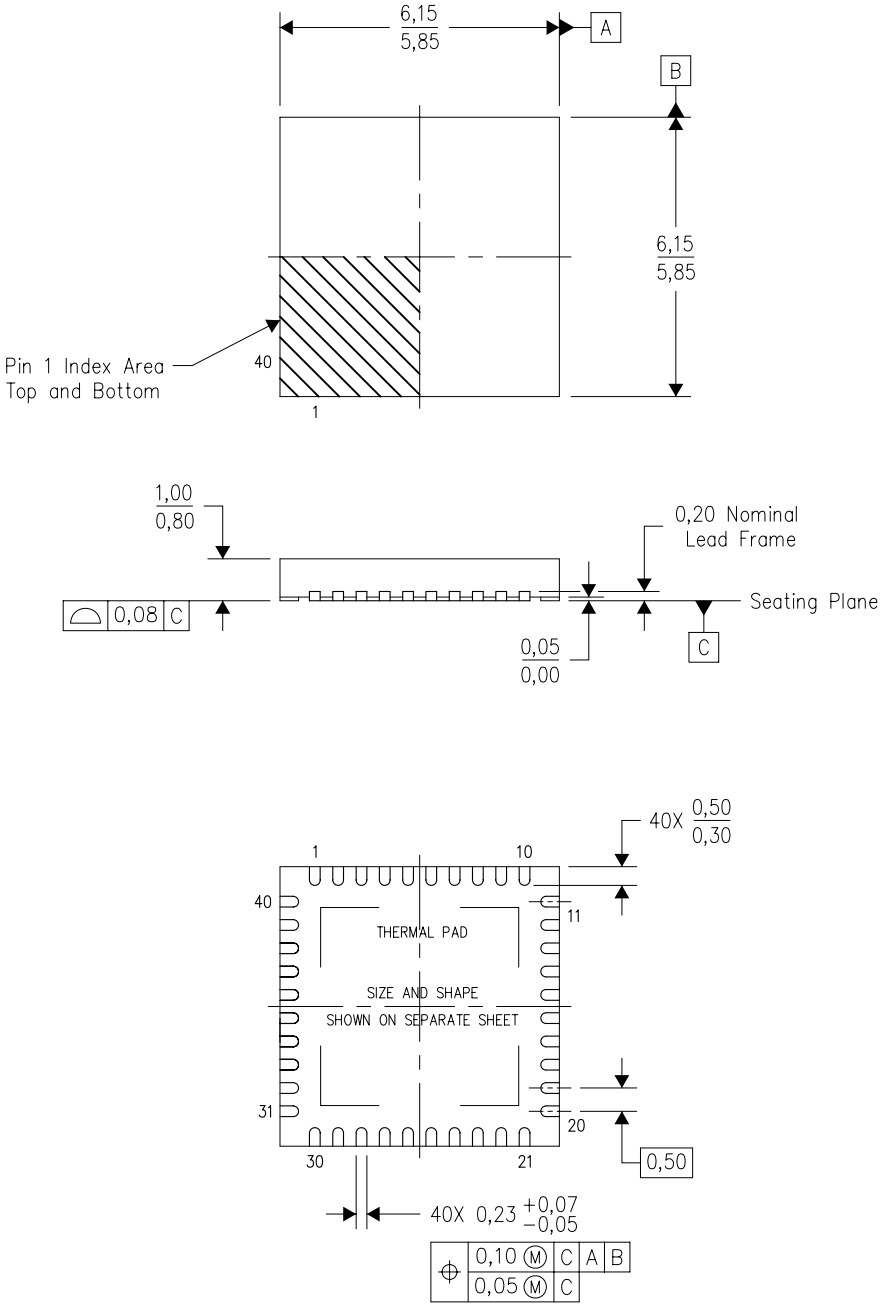
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AFE4400RHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
AFE4400RHAT	VQFN	RHA	40	250	210.0	185.0	35.0

RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



Bottom View

4204276/E 06/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Package complies to JEDEC MO–220 variation VJJD–2.

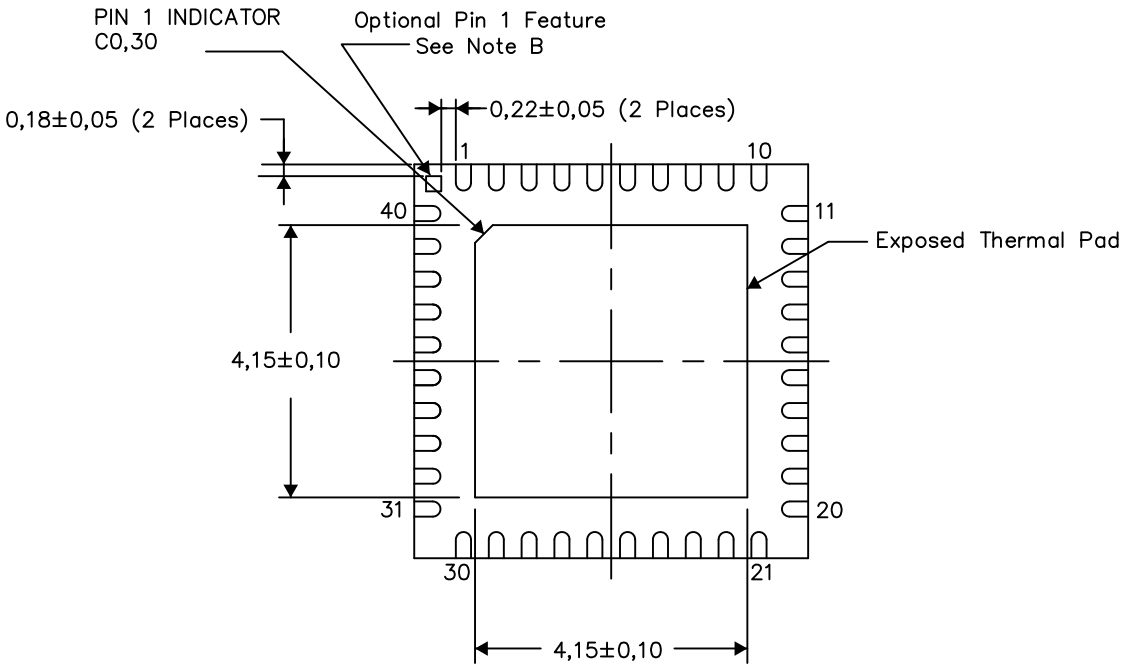
RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

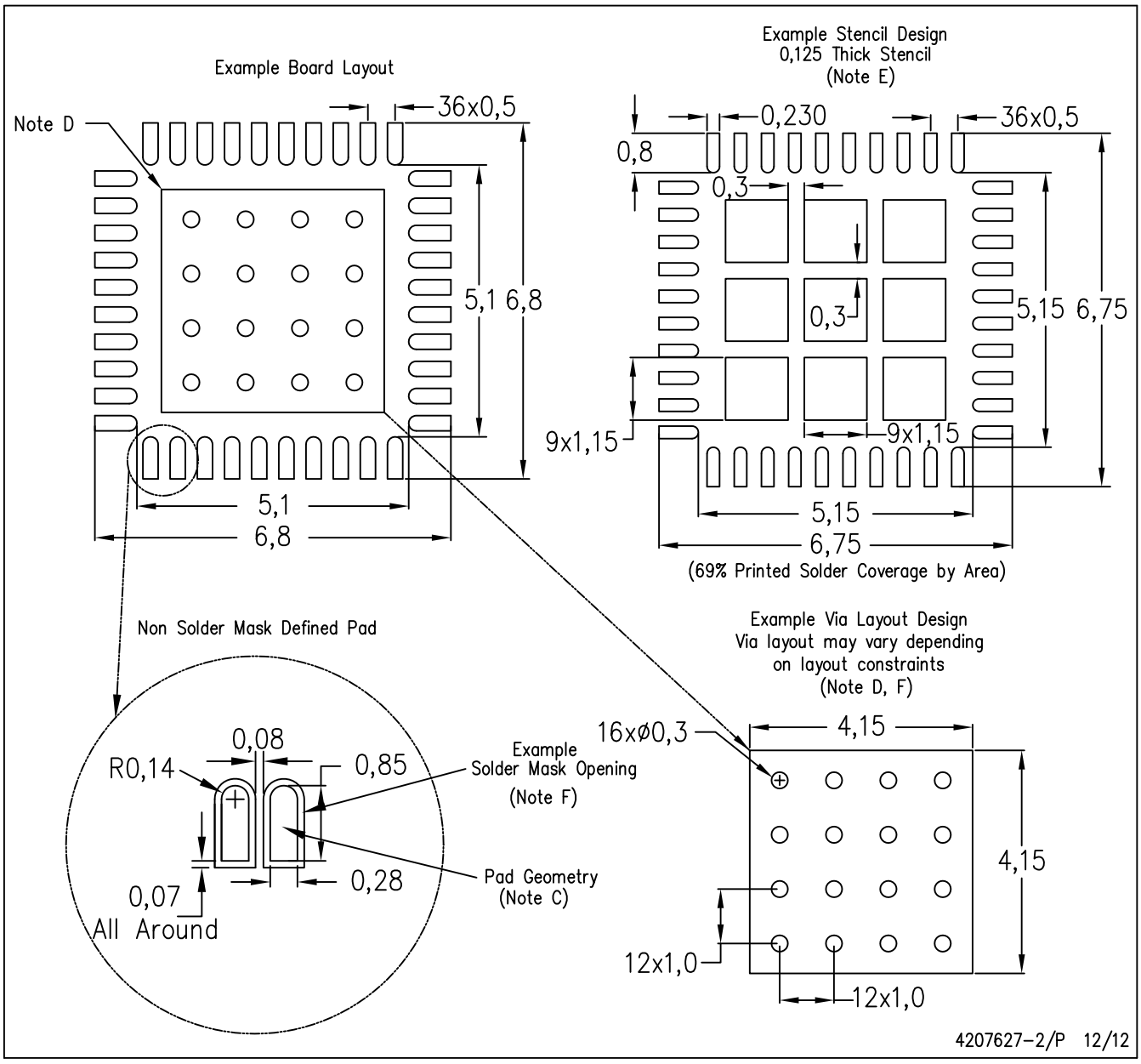
Exposed Thermal Pad Dimensions

4206355–2/U 12/12

NOTES: A. All linear dimensions are in millimeters

B. The Pin 1 Identification mark is an optional feature that may be present on some devices In addition, this Pin 1 feature if present is electrically connected to the center thermal pad and therefore should be considered when routing the board layout.

RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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