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ISL70444SEHEVAL1Z Evaluation Board User's Guide

Introduction

The ISL70444SEHEVAL1Z evaluation platform is designed to evaluate the ISL70444SEH. The ISL70444SEH contains four high speed and low power op amps designed to take advantage of its full dynamic input and output voltage range with rail-to-rail operation. By offering low power, low offset voltage, and low temperature drift coupled with its high bandwidth and enhanced slew rates upwards of 50V/µs, these op amps make it ideal for applications requiring both high DC accuracy and AC performance. This amplifier is designed to operate over a single supply range of 2.7V to 40V or a split supply voltage range of ±1.35V to ±20V. The ISL70444SEH is manufactured in Intersil's PR40, silicon on insulator, BiCMOS process. This process assures the device is immune to a single event latch-up and provides excellent radiation tolerance. This makes it the ideal choice for high reliability applications in harsh radiation-prone environments.

Reference Documents

- ISL70444SEH Data Sheet FN8411
- ISL70444SEH SMD 5962-13214
- ISL70444SEH Radiation Test Report

Evaluation Board Key Features

- Single or dual supply operation: ±1.35V to ±20V or 2.7V to 40V
- Singled-ended or differential input operation with gain (G = 10V/V)
- External VREF input
- Banana Jack connectors for power supply and VREF inputs
- BNC connectors for op amp input and output terminals
- Convenient PCB pads for op amp input/output impedance loading

Power Supply Connections

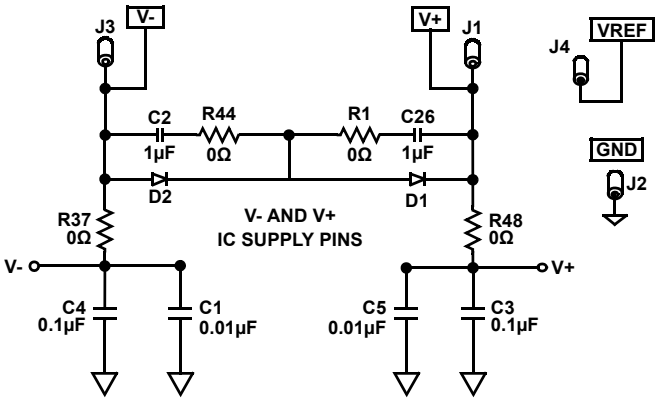

FIGURE 1. POWER SUPPLY CIRCUIT

Figure 1 demonstrates the power supply connections, decoupling and protection circuitry. External power connections are made through the V+, V-, VREF, and GND banana jack connections on the evaluation board. De-coupling capacitors C2 and C26 provide low-frequency power-supply filtering, while additional capacitors (C1, C3, C4 and C5, connected close to the part) filter out high frequency noise, and are connected to their respective supplies through R37 and R48 resistors. These resistors are 0Ω but can be changed by the user to provide additional power supply filtering, or to reduce the supply voltage rate-of-rise time. Anti-reverse diodes D1 and D2 protect the circuit in case of momentarily reversing the power supplies accidentally to the evaluation board. The VREF pin can be connected to ground to establish a ground referenced input for split supply operation.

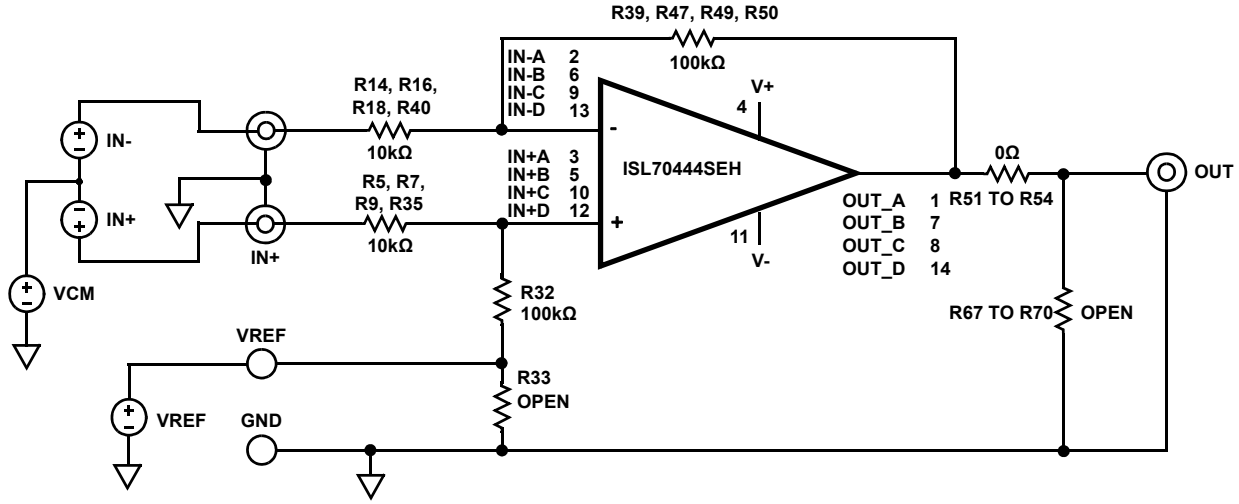

FIGURE 2. BASIC DIFFERENTIAL AMPLIFIER CONFIGURATION

Amplifier Configuration

A simplified schematic of the evaluation board is shown in Figure 2. The input stage with the components supplied is shown in Figure 3. The circuit implements a Hi-Z differential input with unbalanced common mode impedance. The differential amplifier gain is expressed in Equation 1:

$$V_{OUT} = (V_{IN+} - V_{IN-}) \bullet (R_F / R_{IN}) + V_{REF} \quad \text{(EQ. 1)}$$

For a single-ended input with an inverting gain G = -10V/V, the IN+ input is grounded and the signal is supplied to the IN- input. VREF must be connected to a reference voltage between the V+ and V- supply rails. For a non-inverting operation with G = 11V/V, the negative input (IN-) is grounded and the signal is supplied to the positive input (IN+). The non-inverting gain is strongly dependent on any resistance from IN- to GND. For good gain accuracy, a 0Ω resistor should be installed on the empty R11 pad.

User-selectable Options

Component pads are included to enable a variety of user-selectable circuits to be added to the amplifier inputs, the VREF input, outputs and the amplifier feedback loops.

A voltage divider can be added to establish a power supply-tracking common mode reference using the VREF input. The inverting and non-inverting inputs have additional resistor and capacitor placements for adding input attenuation or feedback capacitors (Figure 3).

The outputs (Figure 4) also have additional resistor and capacitor placements for filtering and loading.

Note: Operational amplifiers are sensitive to output capacitance and may oscillate. In the event of oscillation, reduce output capacitance by using shorter cables, or add a resistor in series with the output.

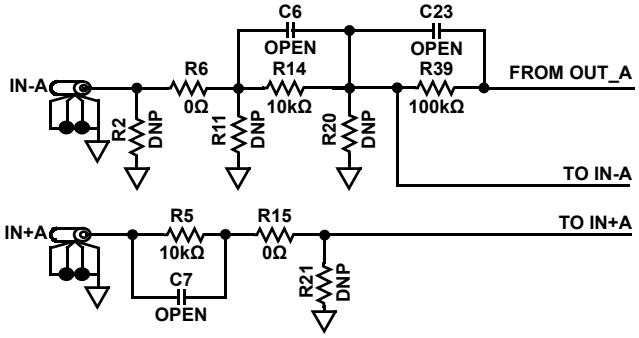

FIGURE 3. INPUT STAGE

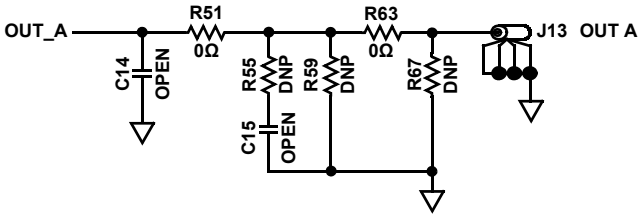

FIGURE 4. OUTPUT STAGE

TABLE 1. ISL70444SEHEVAL1Z COMPONENTS PARTS LIST

DEVICE #	DESCRIPTION	COMMENTS
C1, C5	CAP, SMD, 0805, 0.01µF, 50V, 10%, X7R, ROHS	Power Supply Decoupling
C2, C26	CAP, SMD, 1210, 1µF, 50V, 10%, X7R, ROHS	Power Supply Decoupling
C3, C4	CAP, SMD, 0805, 0.1µF, 25V, 10%, X7R, ROHS	Power Supply Decoupling
C6 - C25	CAP, SMD, 0603, Open-Place Holder, ROHS	User Selectable Capacitors - Not Populated
D1, D2	40V Schottky Barrier Diode	Reverse Power Protection
J1 - J4	Johnson Components Standard Type Banana Jack, 108-0740-001	Power Supply and Reference Voltage Connector
J5 - J16	AMPHENOL BNC Connector, 31-5329-52RFX	Connections for Input and Output
R32	Resistor, SMD, 0603, 100kΩ, 1%, ROHS	VREF Resistor Divider
R5, R7, R9, R14, R16, R18, R35, R40	Resistor, SMD, 0603, 10kΩ, 1%, 1/16W, ROHS	Gain Setting Resistor
R39, R47, R49, R50	Resistor, SMD, 0603, 100kΩ, 1%, 1/16W, ROHS	Gain Setting Feedback Resistor
R2, R3, R4, R11, R12, R13, R20, R21, R22, R23, R25, R26, R28, R30, R31, R33, R34, R38, R42, R43, R46, R55, R56, R57, R58, R59, R60, R61, R62, R62, R67, R68, R69, R70	Resistor, SMD, 0603, DNP-Place Holder, ROHS	User Selectable Resistors - Not Populated
U1	ISL70444SEH, 40V Radiation Hardened, Low Noise Quad Operational Amplifier	

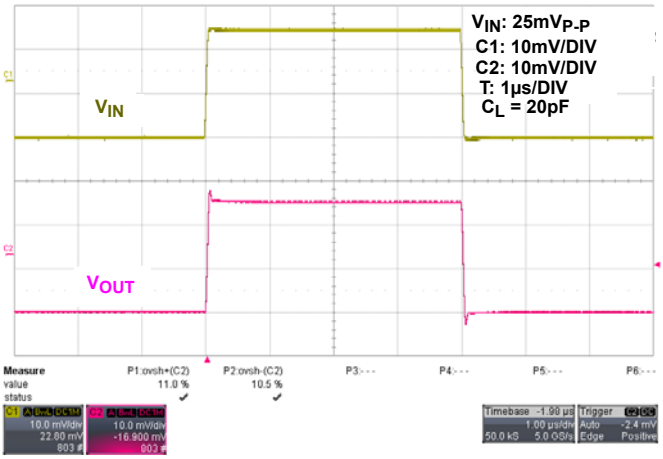

FIGURE 5. SMALL SIGNAL STEP RESPONSE (±18V)

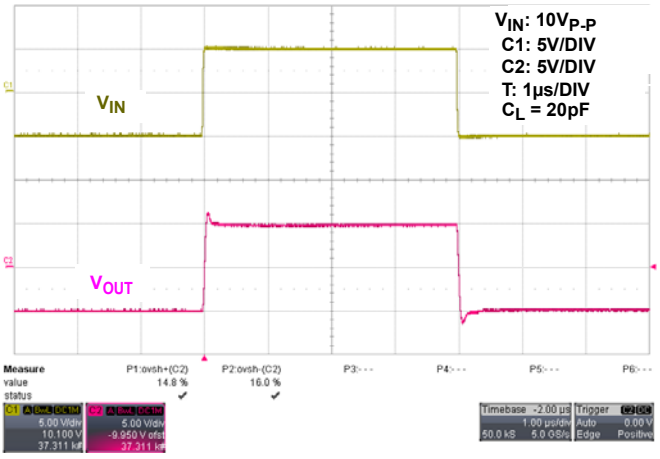

FIGURE 6. LARGE SIGNAL STEP RESPONSE (±18V)

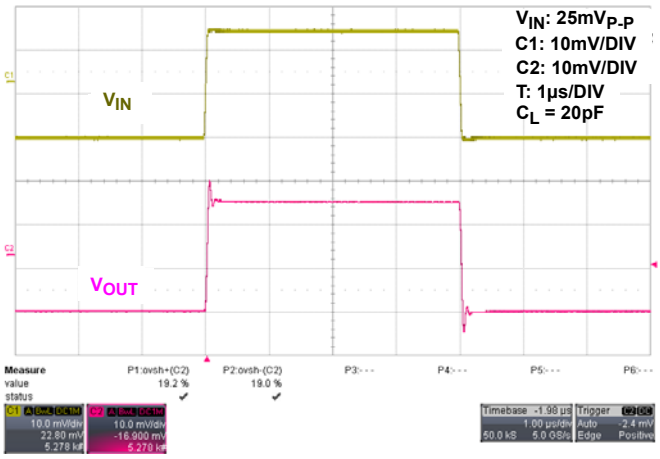

FIGURE 7. SMALL SIGNAL STEP RESPONSE (±2.5V)

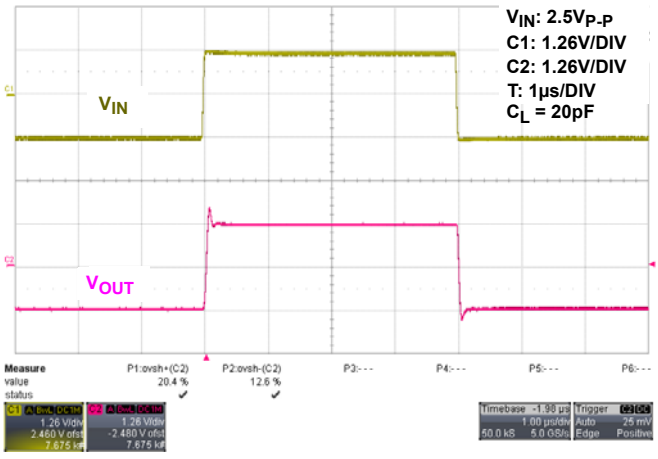

FIGURE 8. LARGE SIGNAL STEP RESPONSE (±2.5V)

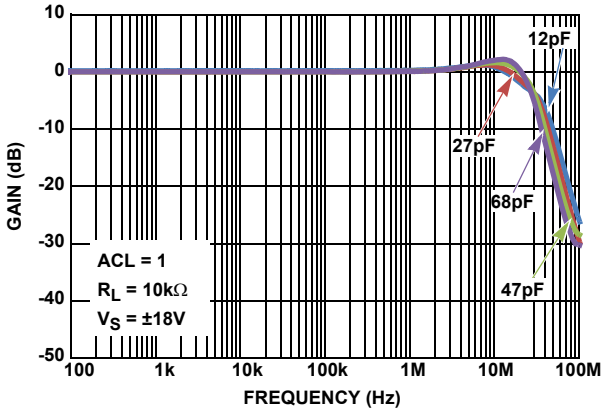

FIGURE 9. (V_S = ±18V) UNITY GAIN RESPONSE vs CL

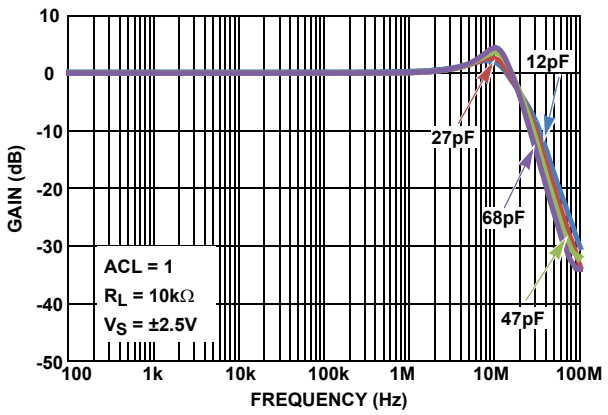

FIGURE 10. (V_S = ±2.5V) UNITY GAIN RESPONSE vs CL

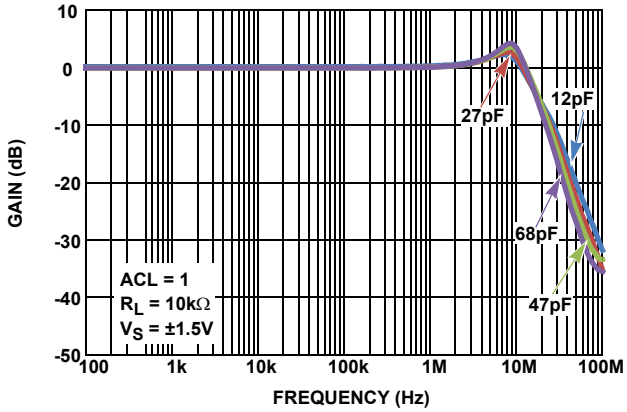

FIGURE 11. (V_S = ±1.5V) UNITY GAIN RESPONSE vs CL

ISL70444SEHEVAL1Z Layout

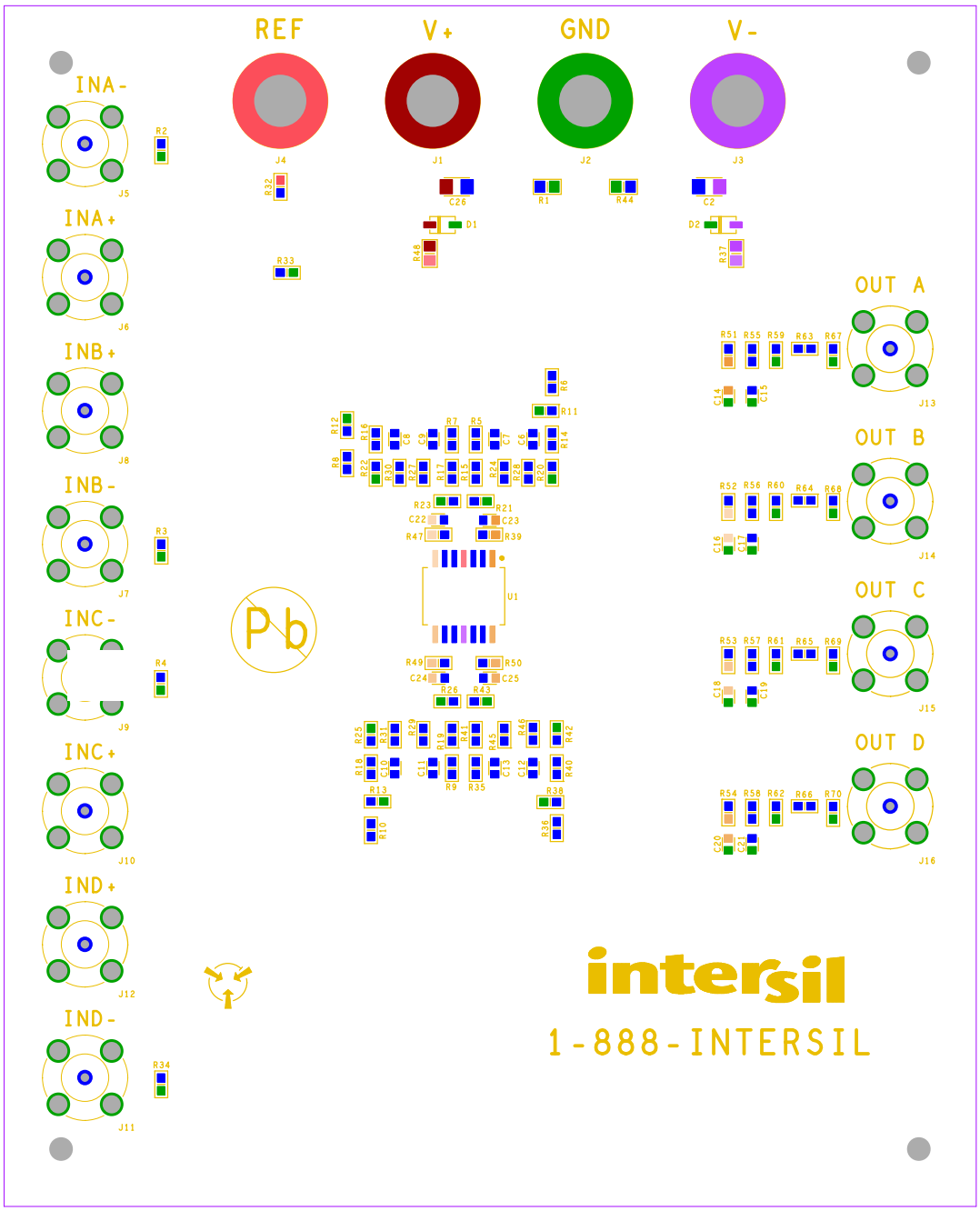

FIGURE 12. TOP VIEW

ISL70444SEHEVAL1Z Layout (Continued)

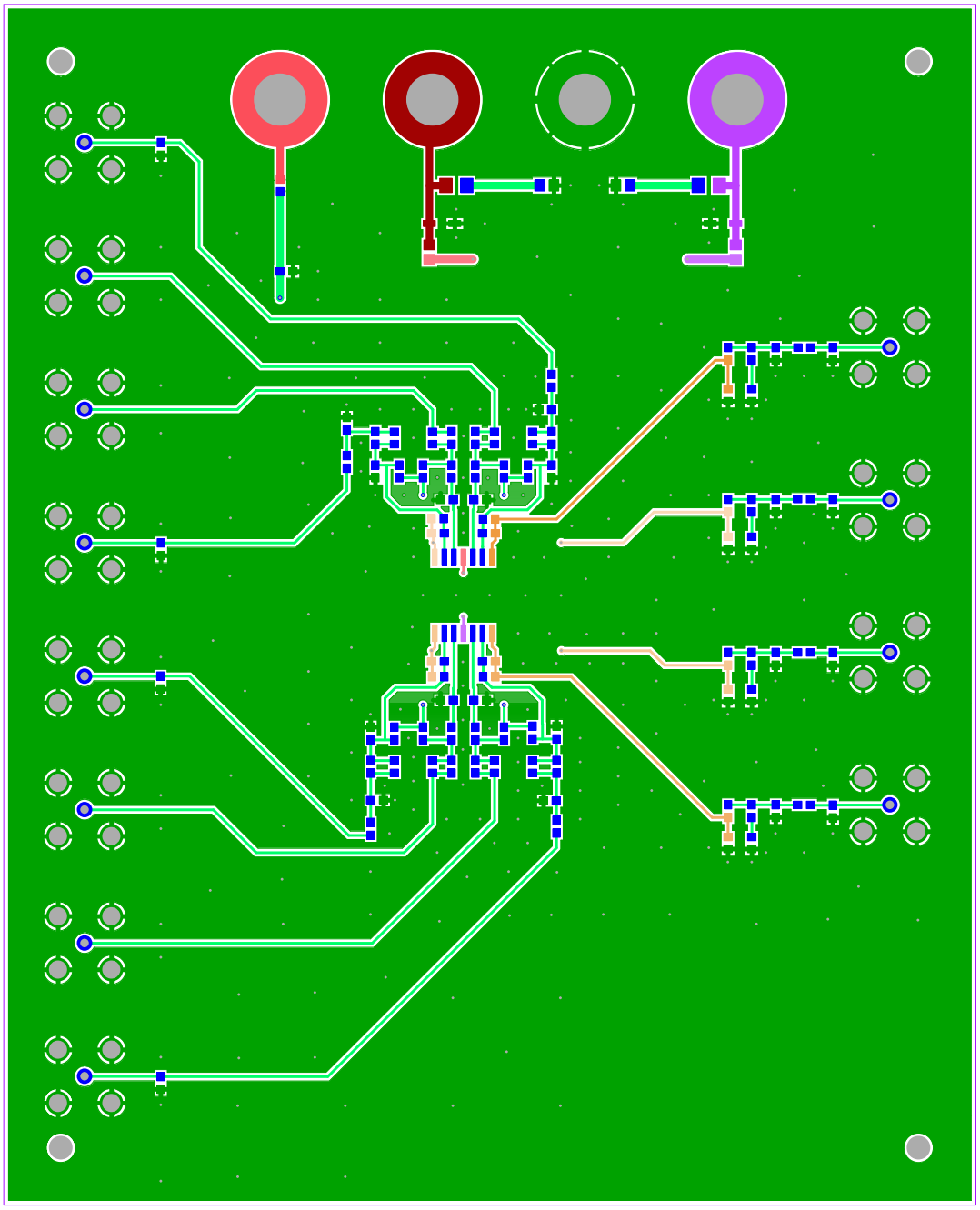

FIGURE 13. TOP LAYER

ISL70444SEHEVAL1Z Layout (Continued)

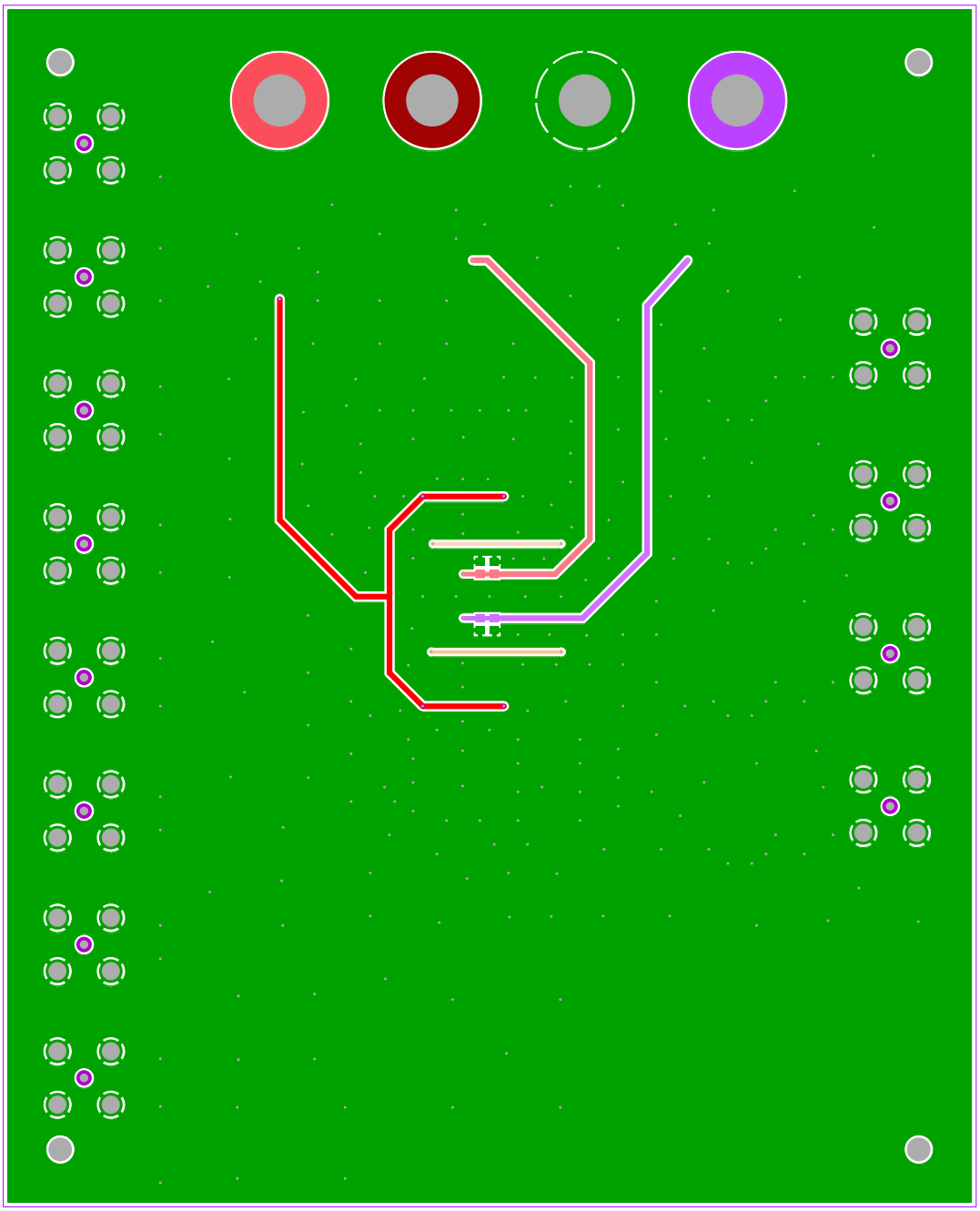

FIGURE 14. BOTTOM LAYER

ISL70444SEHEVAL1Z Schematic Diagram