AT91SAM ARM-based Embedded MPU

SAM9X25

SUMMARY DATASHEET

Description

The SAM9X25 is a high-performance ARM926EJ-S™-based embedded microprocessor unit, running at 400 MHz and featuring multiple networking/connectivity peripherals, optimized for industrial applications such as building automation, gateways and medical.

The SAM9X25 features two 2.0A/B compatible Controller Area Network (CAN) interfaces and two IEEE Std 802.3-compatible 10/100 Mbps Ethernet MACs. Additional communication interfaces include a soft modem supporting exclusively the Conexant SmartDAA line driver, HS USB Device and Host, FS USB Host, two HS SDCard/SDIO/MMC interfaces, USARTs, SPIs, I2S, TWIs and 10-bit ADC.

To ensure uninterrupted data transfer with minimum processor overhead, the SAM9X25 offers a 10-layer bus matrix coupled with 2 x 8 central DMA channels and dedicated DMAs for the high-speed connectivity peripherals.

The External Bus Interface incorporates controllers for 4-bank and 8-bank DDR2/LPDDR, SDRAM/LPSDRAM, static memories, and specific circuitry for MLC/SLC NAND Flash with integrated ECC.

The SAM9X25 is available in a 217-ball BGA package with 0.8 mm ball pitch.

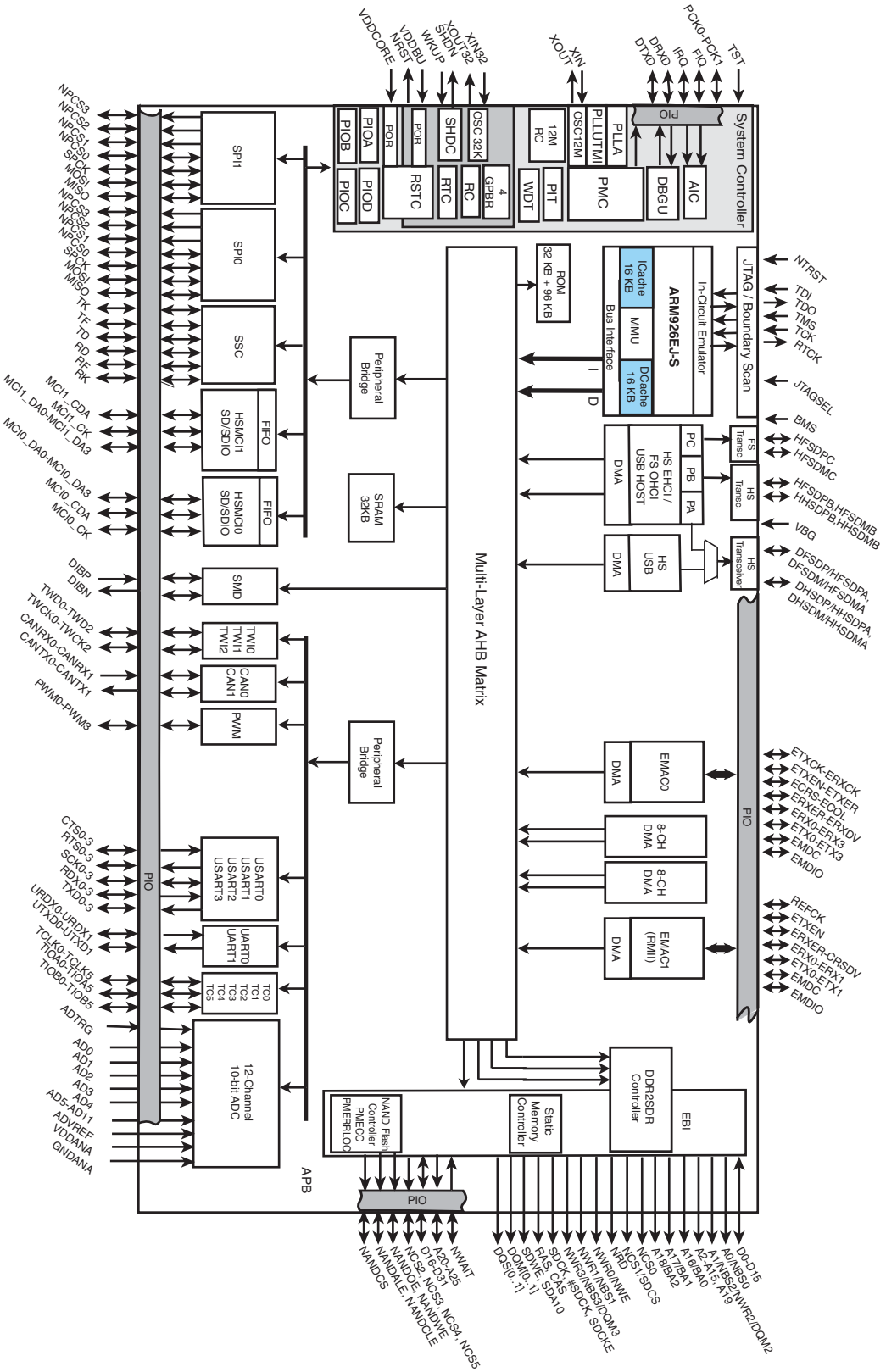
This is a summary document. The complete document is available on the Atmel website at www.atmel.com.

1. Features

- Core
  - ARM926EJ-S™ ARM® Thumb® Processor running at up to 400 MHz @ 1.0V +/- 10%
  - 16 Kbytes Data Cache, 16 Kbytes Instruction Cache, Memory Management Unit
- Memories
  - One 64-Kbyte internal ROM embedding bootstrap routine: Boot on NAND Flash, SDCard, DataFlash® or serial DataFlash. Programmable order.
  - One 32-Kbyte internal SRAM, single-cycle access at system speed
  - High Bandwidth Multi-port DDR2 Controller
  - 32-bit External Bus Interface supporting 4-bank and 8-bank DDR2/LPDDR, SDR/LPSDR, Static Memories
  - MLC/SLC 8-bit NAND Controller, with up to 24-bit Programmable Multi-bit Error Correcting Code (PMECC)
- System running at up to 133 MHz
  - Power-on Reset Cells, Reset Controller, Shut Down Controller, Periodic Interval Timer, Watchdog Timer and Real Time Clock
  - Boot Mode Select Option, Remap Command
  - Internal Low Power 32 kHz RC and Fast 12 MHz RC Oscillators
  - Selectable 32768 Hz Low-power Oscillator and 12 MHz Oscillator
  - One PLL for the system and one PLL at 480 MHz optimized for USB High Speed
  - Twelve 32-bit-layer AHB Bus Matrix for large Bandwidth transfers
  - Dual Peripheral Bridge with dedicated programmable clock for best performance
  - Two dual port 8-channel DMA Controllers
  - Advanced Interrupt Controller and Debug Unit
  - Two Programmable External Clock Signals
- Low Power Mode
  - Shut Down Controller with four 32-bit Battery Backup Registers
  - Clock Generator and Power Management Controller
  - Very Slow Clock Operating Mode, Software Programmable Power Optimization Capabilities
- Peripherals
  - USB Device High Speed, USB Host High Speed and USB Host Full Speed with dedicated On-Chip Transceiver
  - Two 10/100 Mbps Ethernet MAC Controllers
  - Two High Speed Memory Card Hosts
  - Two CAN Controllers
  - Two Master/Slave Serial Peripheral Interface
  - Two 3-channel 32-bit Timer/Counters
  - One Synchronous Serial Controller
  - One 4-channel 16-bit PWM Controller
  - Three Two-wire Interfaces
  - Four USARTs, two UARTs, one DBGU
  - One 12-channel 10-bit Analog-to-Digital Converter
  - Soft Modem
  - Write Protected Registers
- I/O
  - Four 32-bit Parallel Input/Output Controllers
  - 105 Programmable I/O Lines Multiplexed with up to Three Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line, optional Schmitt trigger input
  - Individually Programmable Open-drain, Pull-up and pull-down resistor, Synchronous Output
- Package
  - 217-ball BGA, pitch 0.8 mm

2. Block Diagram

Figure 2-1. SAM9X25 Block Diagram



3. Signal Description

Table 3-1 gives details on the signal names classified by peripheral.

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level
Clocks, Oscillators and PLLs			
XIN	Main Oscillator Input	Input	
XOUT	Main Oscillator Output	Output	
XIN32	Slow Clock Oscillator Input	Input	
XOUT32	Slow Clock Oscillator Output	Output	
VBG	Bias Voltage Reference for USB	Analog	
PCK0-PCK1	Programmable Clock Output	Output	
Shutdown, Wakeup Logic			
SHDN	Shut-Down Control	Output	
WKUP	Wake-Up Input	Input	
ICE and JTAG			
TCK	Test Clock	Input	
TDI	Test Data In	Input	
TDO	Test Data Out	Output	
TMS	Test Mode Select	Input	
JTAGSEL	JTAG Selection	Input	
RTCK	Return Test Clock	Output	
Reset/Test			
NRST	Microcontroller Reset	I/O	Low
TST	Test Mode Select	Input	
NTRST	Test Reset Signal	Input	
BMS	Boot Mode Select	**Input**	
Debug Unit - DBGU			
DRXD	Debug Receive Data	Input	
DTXD	Debug Transmit Data	Output	
Advanced Interrupt Controller - AIC			
IRQ	External Interrupt Input	Input	
FIQ	Fast Interrupt Input	Input	
PIO Controller - PIOA - PIOB - PIOC - PIOD			
PA0-PA31	Parallel IO Controller A	I/O	
PB0-PB18	Parallel IO Controller B	I/O	
PC0-PC31	Parallel IO Controller C	I/O	
PD0-PD21	Parallel IO Controller D	I/O	

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level
External Bus Interface - EBI			
D0-D15	Data Bus	I/O	
D16-D31	Data Bus	I/O	
A0-A25	Address Bus	Output	
NWAIT	External Wait Signal	Input	Low
Static Memory Controller - SMC			
NCS0-NCS5	Chip Select Lines	Output	Low
NWR0-NWR3	Write Signal	Output	Low
NRD	Read Signal	Output	Low
NWE	Write Enable	Output	Low
NBS0-NBS3	Byte Mask Signal	Output	Low
NAND Flash Support			
NFD0-NFD16	NAND Flash I/O	I/O	
NANDCS	NAND Flash Chip Select	Output	Low
NANDOE	NAND Flash Output Enable	Output	Low
NANDWE	NAND Flash Write Enable	Output	Low
DDR2/SDRAM/LPDDR Controller			
SDCK,#SDCK	DDR2/SDRAM Differential Clock	Output	
SDCKE	DDR2/SDRAM Clock Enable	Output	High
SDCS	DDR2/SDRAM Controller Chip Select	Output	Low
BA[0..2]	Bank Select	Output	Low
SDWE	DDR2/SDRAM Write Enable	Output	Low
RAS-CAS	Row and Column Signal	Output	Low
SDA10	SDRAM Address 10 Line	Output	
DQS[0..1]	Data Strobe	I/O	
DQM[0..3]	Write Data Mask	Output	
High Speed MultiMedia Card Interface - HSMCI0-1			
MCI0_CK, MCI1_CK	Multimedia Card Clock	I/O	
MCI0_CDA, MCI1_CDA	Multimedia Card Slot Command	I/O	
MCI0_DA0-MCI0_DA3	Multimedia Card 0 Slot A Data	I/O	
MCI1_DA0-MCI1_DA3	Multimedia Card 1 Slot A Data	I/O	

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level
Universal Synchronous Asynchronous Receiver Transmitter - USARTx			
SCKx	USARTx Serial Clock	I/O	
TXDx	USARTx Transmit Data	Output	
RXDx	USARTx Receive Data	Input	
RTSx	USARTx Request To Send	Output	
CTSx	USARTx Clear To Send	Input	
Universal Asynchronous Receiver Transmitter - UARTx			
UTXDx	UARTx Transmit Data	Output	
URXDx	UARTx Receive Data	Input	
Synchronous Serial Controller - SSC			
TD	SSC Transmit Data	Output	
RD	SSC Receive Data	Input	
TK	SSC Transmit Clock	I/O	
RK	SSC Receive Clock	I/O	
TF	SSC Transmit Frame Sync	I/O	
RF	SSC Receive Frame Sync	I/O	
Timer/Counter - TCx x=0..5			
TCLKx	TC Channel x External Clock Input	Input	
TIOAx	TC Channel x I/O Line A	I/O	
TIOBx	TC Channel x I/O Line B	I/O	
Serial Peripheral Interface - SPIx			
SPIx_MISO	Master In Slave Out	I/O	
SPIx_MOSI	Master Out Slave In	I/O	
SPIx_SPCK	SPI Serial Clock	I/O	
SPIx_NPCS0	SPI Peripheral Chip Select 0	I/O	Low
SPIx_NPCS1-SPIx_NPCS3	SPI Peripheral Chip Select	Output	Low
Two-Wire Interface - TWIx			
TWDx	Two-wire Serial Data	I/O	
TWCKx	Two-wire Serial Clock	I/O	

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level
Pulse Width Modulation Controller - PWMC			
PWM0-PWM3	Pulse Width Modulation Output	Output	
USB Host High Speed Port - UHPHS			
HFSDPA	USB Host Port A Full Speed Data +	Analog	
HFSDMA	USB Host Port A Full Speed Data -	Analog	
HHSDPA	USB Host Port A High Speed Data +	Analog	
HHSDMA	USB Host Port A High Speed Data -	Analog	
HFSDPB	USB Host Port B Full Speed Data +	Analog	
HFSDMB	USB Host Port B Full Speed Data -	Analog	
HHSDPB	USB Host Port B High Speed Data +	Analog	
HHSDMB	USB Host Port B High Speed Data -	Analog	
HFSDMC	USB Host Port C Full Speed Data -	Analog	
HFSDPC	USB Host Port C Full Speed Data +	Analog	
USB Device High Speed Port - UDPHS			
DFSDM	USB Device Full Speed Data -	Analog	
DFSDP	USB Device Full Speed Data +	Analog	
DHSDM	USB Device High Speed Data -	Analog	
DHSDP	USB Device High Speed Data +	Analog	
Ethernet 10/100 - EMAC0			
ETXCK	Transmit Clock or Reference Clock	Input	
ERXCK	Receive Clock	Input	
ETXEN	Transmit Enable	Output	
ETX0-ETX3	Transmit Data	Output	
ETXER	Transmit Coding Error	Output	
ERXDV	Receive Data Valid	Input	
ERX0-ERX3	Receive Data	Input	
ERXER	Receive Error	Input	
ECRS	Carrier Sense and Data Valid	Input	
ECOL	Collision Detect	Input	
EMDC	Management Data Clock	Output	
EMDIO	Management Data Input/Output	I/O	
RMII Ethernet 10/100 - EMAC1			
REFCK	Transmit Clock or Reference Clock	Input	
ETXEN	Transmit Enable	Output	
ETX0-ETX1	Transmit Data	Output	
CRSDV	Receive Data Valid	Input	
ERX0-ERX1	Receive Data	Input	

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level
ERXER	Receive Error	Input	
EMDC	Management Data Clock	Output	
EMDIO	Management Data Input/Output	I/O	
Analog-to-Digital Converter - ADC			
AD0-AD11	12 Analog Inputs	Analog	
ADTRG	ADC Trigger	Input	
ADVREF	ADC Reference	Analog	
CAN Controller - CANx			
CANRXx	CAN input	Input	
CANTXx	CAN output	Output	
Soft Modem - SMD			
DIBN	Soft Modem Signal	I/O	
DIBP	Soft Modem Signal	I/O	

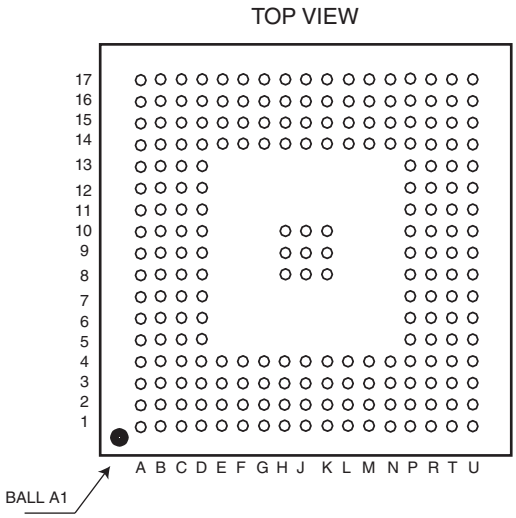
4. Package and Pinout

The SAM9X25 is available in 217-ball BGA package.

4.1 Overview of the 217-ball BGA Package

Figure 4-1 shows the orientation of the 217-ball BGA Package.

Figure 4-1. Orientation of the 217-ball BGA Package



4.2 217-ball BGA Package Pinout

Table 4-1. Pin Description BGA217

			Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
Ball	Power Rail	I/O Type	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, ST
L3	VDDIOP0	GPIO	PA0	I/O			TXD0	O	SPI1_NPCS1	O			PIO, I, PU, ST
P1	VDDIOP0	GPIO	PA1	I/O			RXD0	I	SPI0_NPCS2	O			PIO, I, PU, ST
L4	VDDIOP0	GPIO	PA2	I/O			RTS0	O	MCI1_DA1	I/O	E0_TX0	O	PIO, I, PU, ST
N4	VDDIOP0	GPIO	PA3	I/O			CTS0	I	MCI1_DA2	I/O	E0_TX1	O	PIO, I, PU, ST
T3	VDDIOP0	GPIO	PA4	I/O			SCK0	I/O	MCI1_DA3	I/O	E0_TXER	O	PIO, I, PU, ST
R1	VDDIOP0	GPIO	PA5	I/O			TXD1	O	CANTX1	O			PIO, I, PU, ST
R4	VDDIOP0	GPIO	PA6	I/O			RXD1	I	CANRX1	I			PIO, I, PU, ST
R3	VDDIOP0	GPIO	PA7	I/O			TXD2	O	SPI0_NPCS1	O			PIO, I, PU, ST
P4	VDDIOP0	GPIO	PA8	I/O			RXD2	I	SPI1_NPCS0	I/O			PIO, I, PU, ST
U3	VDDIOP0	GPIO	PA9	I/O			DRXD	I	CANRX0	I			PIO, I, PU, ST
T1	VDDIOP0	GPIO	PA10	I/O			DTXD	O	CANTX0	O			PIO, I, PU, ST
U1	VDDIOP0	GPIO	PA11	I/O			SPI0_MISO	I/O	MCI1_DA0	I/O			PIO, I, PU, ST
T2	VDDIOP0	GPIO	PA12	I/O			SPI0_MOSI	I/O	MCI1_CDA	I/O			PIO, I, PU, ST
T4	VDDIOP0	GPIO_CLK	PA13	I/O			SPI0_SPCK	I/O	MCI1_CK	I/O			PIO, I, PU, ST
U2	VDDIOP0	GPIO	PA14	I/O			SPI0_NPCS0	I/O					PIO, I, PU, ST
U4	VDDIOP0	GPIO	PA15	I/O			MCI0_DA0	I/O					PIO, I, PU, ST
P5	VDDIOP0	GPIO	PA16	I/O			MCI0_CDA	I/O					PIO, I, PU, ST
R5	VDDIOP0	GPIO_CLK	PA17	I/O			MCI0_CK	I/O					PIO, I, PU, ST
U5	VDDIOP0	GPIO	PA18	I/O			MCI0_DA1	I/O					PIO, I, PU, ST
T5	VDDIOP0	GPIO	PA19	I/O			MCI0_DA2	I/O					PIO, I, PU, ST
U6	VDDIOP0	GPIO	PA20	I/O			MCI0_DA3	I/O					PIO, I, PU, ST
T6	VDDIOP0	GPIO	PA21	I/O			TIOA0	I/O	SPI1_MISO	I/O			PIO, I, PU, ST
R6	VDDIOP0	GPIO	PA22	I/O			TIOA1	I/O	SPI1_MOSI	I/O			PIO, I, PU, ST
U7	VDDIOP0	GPIO_CLK	PA23	I/O			TIOA2	I/O	SPI1_SPCK	I/O			PIO, I, PU, ST
T7	VDDIOP0	GPIO	PA24	I/O			TCLK0	I	TK	I/O			PIO, I, PU, ST
T8	VDDIOP0	GPIO	PA25	I/O			TCLK1	I	TF	I/O			PIO, I, PU, ST
R7	VDDIOP0	GPIO	PA26	I/O			TCLK2	I	TD	O			PIO, I, PU, ST
P8	VDDIOP0	GPIO	PA27	I/O			TIOB0	I/O	RD	I			PIO, I, PU, ST
U8	VDDIOP0	GPIO	PA28	I/O			TIOB1	I/O	RK	I/O			PIO, I, PU, ST
R9	VDDIOP0	GPIO	PA29	I/O			TIOB2	I/O	RF	I/O			PIO, I, PU, ST
R8	VDDIOP0	GPIO	PA30	I/O			TWD0	I/O	SPI1_NPCS3	O	E0_MDC	O	PIO, I, PU, ST
U9	VDDIOP0	GPIO	PA31	I/O			TWCK0	O	SPI1_NPCS2	O	E0_TXEN	O	PIO, I, PU, ST
D3	VDDANA	GPIO	PB0	I/O			E0_RX0	I	RTS2	O			PIO, I, PU, ST
D4	VDDANA	GPIO	PB1	I/O			E0_RX1	I	CTS2	I			PIO, I, PU, ST
D2	VDDANA	GPIO	PB2	I/O			E0_RXER	I	SCK2	I/O			PIO, I, PU, ST
E4	VDDANA	GPIO	PB3	I/O			E0_RXDV	I	SPI0_NPCS3	O			PIO, I, PU, ST
D1	VDDANA	GPIO_CLK	PB4	I/O			E0_TXCK	I	TWD2	I/O			PIO, I, PU, ST
E3	VDDANA	GPIO	PB5	I/O			E0_MDIO	I/O	TWCK2	O			PIO, I, PU, ST
B3	VDDANA	GPIO_ANA	PB6	I/O	AD7	I	E0_MDC	O					PIO, I, PU, ST

Table 4-1. Pin Description BGA217 (Continued)

			Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
Ball	Power Rail	I/O Type	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, ST
C2	VDDANA	GPIO_ANA	PB7	I/O	AD8	I	E0_TXEN	O					PIO, I, PU, ST
C5	VDDANA	GPIO_ANA	PB8	I/O	AD9	I	E0_TXER	O					PIO, I, PU, ST
C1	VDDANA	GPIO_ANA	PB9	I/O	AD10	I	E0_TX0	O	PCK1	O			PIO, I, PU, ST
B2	VDDANA	GPIO_ANA	PB10	I/O	AD11	I	E0_TX1	O	PCK0	O			PIO, I, PU, ST
A3	VDDANA	GPIO_ANA	PB11	I/O	AD0	I	E0_TX2	O	PWM0	O			PIO, I, PU, ST
B4	VDDANA	GPIO_ANA	PB12	I/O	AD1	I	E0_TX3	O	PWM1	O			PIO, I, PU, ST
A2	VDDANA	GPIO_ANA	PB13	I/O	AD2	I	E0_RX2	I	PWM2	O			PIO, I, PU, ST
C4	VDDANA	GPIO_ANA	PB14	I/O	AD3	I	E0_RX3	I	PWM3	O			PIO, I, PU, ST
C3	VDDANA	GPIO_ANA	PB15	I/O	AD4	I	E0_RXCK	I					PIO, I, PU, ST
A1	VDDANA	GPIO_ANA	PB16	I/O	AD5	I	E0_CRS	I		I			PIO, I, PU, ST
B1	VDDANA	GPIO_ANA	PB17	I/O	AD6	I	E0_COL	I		I			PIO, I, PU, ST
D5	VDDANA	GPIO	PB18	I/O			IRQ	I	ADTRG	I			PIO, I, PU, ST
E2	VDDIOP1	GPIO	PC0	I/O							TWD1	I/O	PIO, I, PU, ST
F4	VDDIOP1	GPIO	PC1	I/O							TWCK1	O	PIO, I, PU, ST
F3	VDDIOP1	GPIO	PC2	I/O							TIOA3	I/O	PIO, I, PU, ST
H2	VDDIOP1	GPIO	PC3	I/O							TIOB3	I/O	PIO, I, PU, ST
E1	VDDIOP1	GPIO	PC4	I/O							TCLK3	I	PIO, I, PU, ST
G4	VDDIOP1	GPIO	PC5	I/O							TIOA4	I/O	PIO, I, PU, ST
F2	VDDIOP1	GPIO	PC6	I/O							TIOB4	I/O	PIO, I, PU, ST
F1	VDDIOP1	GPIO	PC7	I/O							TCLK4	I	PIO, I, PU, ST
G1	VDDIOP1	GPIO	PC8	I/O							UTXD0	O	PIO, I, PU, ST
G3	VDDIOP1	GPIO	PC9	I/O							URXD0	I	PIO, I, PU, ST
G2	VDDIOP1	GPIO	PC10	I/O							PWM0	O	PIO, I, PU, ST
H3	VDDIOP1	GPIO	PC11	I/O							PWM1	O	PIO, I, PU, ST
J3	VDDIOP1	GPIO	PC12	I/O							TIOA5	I/O	PIO, I, PU, ST
L2	VDDIOP1	GPIO	PC13	I/O							TIOB5	I/O	PIO, I, PU, ST
H1	VDDIOP1	GPIO	PC14	I/O							TCLK5	I	PIO, I, PU, ST
J2	VDDIOP1	GPIO_CLK	PC15	I/O							PCK0	O	PIO, I, PU, ST
J1	VDDIOP1	GPIO	PC16	I/O					E1_RXER	I	UTXD1	O	PIO, I, PU, ST
L1	VDDIOP1	GPIO	PC17	I/O							URXD1	I	PIO, I, PU, ST
K2	VDDIOP1	GPIO	PC18	I/O					E1_TX0	O	PWM0	O	PIO, I, PU, ST
N3	VDDIOP1	GPIO	PC19	I/O					E1_TX1	O	PWM1	O	PIO, I, PU, ST
K1	VDDIOP1	GPIO	PC20	I/O					E1_RX0	I	PWM2	O	PIO, I, PU, ST
M3	VDDIOP1	GPIO	PC21	I/O					E1_RX1	I	PWM3	O	PIO, I, PU, ST
P3	VDDIOP1	GPIO	PC22	I/O					TXD3	O			PIO, I, PU, ST
J4	VDDIOP1	GPIO	PC23	I/O					RXD3	I			PIO, I, PU, ST
K3	VDDIOP1	GPIO	PC24	I/O					RTS3	O			PIO, I, PU, ST
M2	VDDIOP1	GPIO	PC25	I/O					CTS3	I			PIO, I, PU, ST
P2	VDDIOP1	GPIO	PC26	I/O					SCK3	I/O			PIO, I, PU, ST
M1	VDDIOP1	GPIO	PC27	I/O					E1_TXEN	O	RTS1	O	PIO, I, PU, ST
K4	VDDIOP1	GPIO	PC28	I/O					E1_CRSDV	I	CTS1	I	PIO, I, PU, ST

Table 4-1. Pin Description BGA217 (Continued)

			Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
Ball	**Power Rail**	**I/O Type**	**Signal**	**Dir**	**Signal**	**Dir**	**Signal**	**Dir**	**Signal**	**Dir**	**Signal**	**Dir**	**Signal, Dir, PU, PD, ST**
N1	VDDIOP1	GPIO_CLK	PC29	I/O					E1_TXCK	I	SCK1	I/O	PIO, I, PU, ST
R2	VDDIOP1	GPIO_CLK2	PC30	I/O					E1_MDC	O			PIO, I, PU, ST
N2	VDDIOP1	GPIO	PC31	I/O			FIQ	I	E1_MDIO	I/O	PCK1	O	PIO, I, PU, ST
P13	VDDNF	EBI	PD0	I/O			NANDOE	O					PIO, I, PU
R14	VDDNF	EBI	PD1	I/O			NANDWE	O					PIO, I, PU
R13	VDDNF	EBI	PD2	I/O			A21/NANDALE	O					A21,O, PD
P15	VDDNF	EBI	PD3	I/O			A22/NANDCLE	O					A22,O, PD
P12	VDDNF	EBI	PD4	I/O			NCS3	O					PIO, I, PU
P14	VDDNF	EBI	PD5	I/O			NWAIT	I					PIO, I, PU
N14	VDDNF	EBI	PD6	I/O			D16	O					PIO, I, PU
R15	VDDNF	EBI	PD7	I/O			D17	O					PIO, I, PU
M14	VDDNF	EBI	PD8	I/O			D18	O					PIO, I, PU
N16	VDDNF	EBI	PD9	I/O			D19	O					PIO, I, PU
N17	VDDNF	EBI	PD10	I/O			D20	O					PIO, I, PU
N15	VDDNF	EBI	PD11	I/O			D21	O					PIO, I, PU
K15	VDDNF	EBI	PD12	I/O			D22	O					PIO, I, PU
M15	VDDNF	EBI	PD13	I/O			D23	O					PIO, I, PU
L14	VDDNF	EBI	PD14	I/O			D24	O					PIO, I, PU
M16	VDDNF	EBI	PD15	I/O			D25	O	A20	O			A20, O, PD
L16	VDDNF	EBI	PD16	I/O			D26	O	A23	O			A23, O, PD
L15	VDDNF	EBI	PD17	I/O			D27	O	A24	O			A24, O, PD
K17	VDDNF	EBI	PD18	I/O			D28	O	A25	O			A25, O, PD
J17	VDDNF	EBI	PD19	I/O			D29	O	NCS2	O			PIO, I, PU
K16	VDDNF	EBI	PD20	I/O			D30	O	NCS4	O			PIO, I, PU
J16	VDDNF	EBI	PD21	I/O			D31	O	NCS5	O			PIO, I, PU
D10, D13, F14	VDDIOM	POWER	VDDIOM	I									I
J14, K14	VDDNF	POWER	VDDNF	I									I
H9, H10, J9, J10	GNDIOM	GND	GNDIOM	I									I
P7	VDDIOP0	POWER	VDDIOP0	I									I
H4	VDDIOP1	POWER	VDDIOP1	I									I
M4, P6	GNDIOP	GND	GNDIOP	I									I
B5	VDDBU	POWER	VDDBU	I									I
B6	GNDBU	GND	GNDBU	I									I
C6	VDDANA	POWER	VDDANA	I									I
D6	GNDANA	GND	GNDANA	I									I
R12	VDDPLLA	POWER	VDDPLLA	I									I
T13	VDDOSC	POWER	VDDOSC	I									I

Table 4-1. Pin Description BGA217 (Continued)

			Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
Ball	**Power Rail**	**I/O Type**	**Signal**	**Dir**	**Signal**	**Dir**	**Signal**	**Dir**	**Signal**	**Dir**	**Signal**	**Dir**	**Signal, Dir, PU, PD, ST**
U13	GNDOSC	GND	GNDOSC	I									I
H14, K8, K9	VDDCORE	POWER	VDDCORE	I									I
H8, J8, K10	GNDCORE	GND	GNDCORE	I									I
U16	VDDUTMII	POWER	VDDUTMII	I									I
T17	VDDUTMIC	POWER	VDDUTMIC	I									I
T16	GNDUTMI	GND	GNDUTMI	I									I
D14	VDDIOM	EBI	D0	I/O									O, PD
D15	VDDIOM	EBI	D1	I/O									O, PD
A16	VDDIOM	EBI	D2	I/O									O, PD
B16	VDDIOM	EBI	D3	I/O									O, PD
A17	VDDIOM	EBI	D4	I/O									O, PD
B15	VDDIOM	EBI	D5	I/O									O, PD
C14	VDDIOM	EBI	D6	I/O									O, PD
B14	VDDIOM	EBI	D7	I/O									O, PD
A15	VDDIOM	EBI	D8	I/O									O, PD
C15	VDDIOM	EBI	D9	I/O									O, PD
D12	VDDIOM	EBI	D10	I/O									O, PD
C13	VDDIOM	EBI	D11	I/O									O, PD
A14	VDDIOM	EBI	D12	I/O									O, PD
B13	VDDIOM	EBI	D13	I/O									O, PD
A13	VDDIOM	EBI	D14	I/O									O, PD
C12	VDDIOM	EBI	D15	I/O									O, PD
J15	VDDIOM	EBI_O	A0	O	NBS0	O							O, PD
H16	VDDIOM	EBI_O	A1	O	NBS2/DQM/ NWR2	O							O, PD
H15	VDDIOM	EBI_O	A2	O									O, PD
H17	VDDIOM	EBI_O	A3	O									O, PD
G17	VDDIOM	EBI_O	A4	O									O, PD
G16	VDDIOM	EBI_O	A5	O									O, PD
F17	VDDIOM	EBI_O	A6	O									O, PD
E17	VDDIOM	EBI_O	A7	O									O, PD
F16	VDDIOM	EBI_O	A8	O									O, PD
G15	VDDIOM	EBI_O	A9	O									O, PD
G14	VDDIOM	EBI_O	A10	O									O, PD
F15	VDDIOM	EBI_O	A11	O									O, PD
D17	VDDIOM	EBI_O	A12	O									O, PD
C17	VDDIOM	EBI_O	A13	O									O, PD
E16	VDDIOM	EBI_O	A14	O									O, PD
D16	VDDIOM	EBI_O	A15	O									O, PD

Table 4-1. Pin Description BGA217 (Continued)

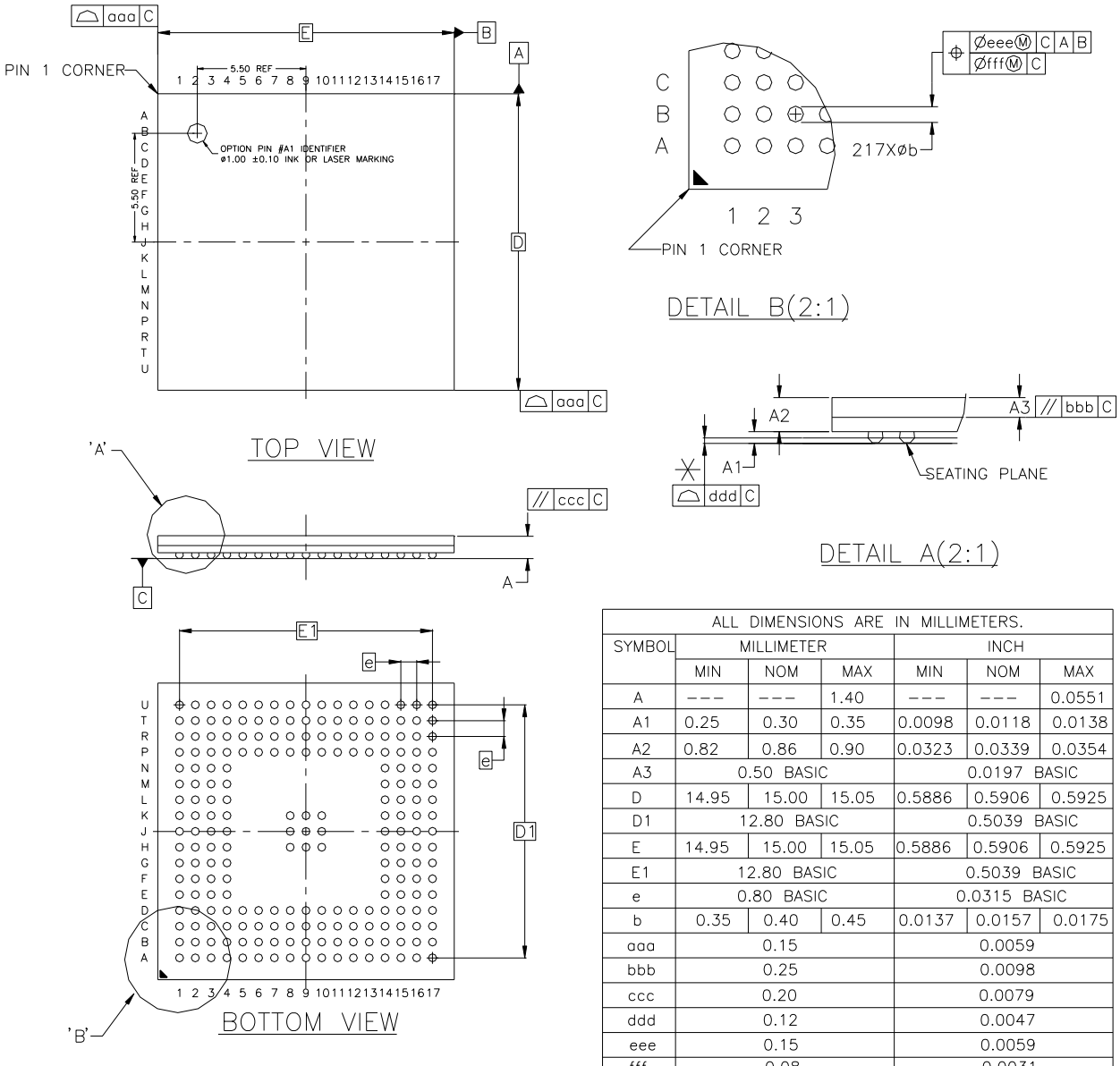
			Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
Ball	Power Rail	I/O Type	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, ST
C16	VDDIOM	EBI_O	A16	O	BA0	O							O, PD
B17	VDDIOM	EBI_O	A17	O	BA1	O							O, PD
E15	VDDIOM	EBI_O	A18	O	BA2	O							O, PD
E14	VDDIOM	EBI_O	A19	O									O, PD
B9	VDDIOM	EBI_O	NCS0	O									O, PU
B8	VDDIOM	EBI_O	NCS1	O	SDCS	O							O, PU
D9	VDDIOM	EBI_O	NRD	O									O, PU
C9	VDDIOM	EBI_O	NWR0	O	NWRE	O							O, PU
C7	VDDIOM	EBI_O	NWR1	O	NBS1	O							O, PU
A8	VDDIOM	EBI_O	NWR3	O	NBS3/DQM3	O							O, PU
D11	VDDIOM	EBI_CLK	SDCK	O									O
C11	VDDIOM	EBI_CLK	#SDCK	O									O
B12	VDDIOM	EBI_O	SDCKE	O									O, PU
B11	VDDIOM	EBI_O	RAS	O									O, PU
C10	VDDIOM	EBI_O	CAS	O									O, PU
A12	VDDIOM	EBI_O	SDWE	O									O, PU
C8	VDDIOM	EBI_O	SDA10	O									O, PU
A10	VDDIOM	EBI_O	DQM0	O									O, PU
B10	VDDIOM	EBI_O	DQM1	O									O, PU
A11	VDDIOM	EBI	DQS0	I/O									O, PD
A9	VDDIOM	EBI	DQS1	I/O									O, PD
A4	VDDANA	POWER	ADVREF	I									I
U17	VDDUTMIC	VBG	VBG	I									I
T14	VDDUTMII	USBFS	HFSDPA	I/O	DFSDP	I/O							O, PD
T15	VDDUTMII	USBFS	HFSDMA	I/O	DFSDM	I/O							O, PD
U14	VDDUTMII	USBHS	HHSDPA	I/O	DHSDP	I/O							O, PD
U15	VDDUTMII	USBHS	HHSDMA	I/O	DHSDM	I/O							O, PD
R16	VDDUTMII	USBFS	HFSDPB	I/O									O, PD
P16	VDDUTMII	USBFS	HFSDMB	I/O									O, PD
R17	VDDUTMII	USBHS	HHSDPB	I/O									O, PD
P17	VDDUTMII	USBHS	HHSDMB	I/O									O, PD
L17	VDDUTMII	USBFS	HFSDPC	I/O									O, PD
M17	VDDUTMII	USBFS	HFSDMC	I/O									O, PD
R11	VDDIOP0	DIB	DIBN	I/O									O, PU
P11	VDDIOP0	DIB	DIBP	I/O									O, PU
A7	VDDBU	SYSC	WKUP	I									I, ST
D8	VDDBU	SYSC	SHDN	O									O, PU
P9	VDDIOP0	RSTJTAG	BMS	I									I, PD, ST
D7	VDDBU	SYSC	JTAGSEL	I									I, PD
B7	VDDBU	SYSC	TST	I									I, PD, ST
U10	VDDIOP0	RSTJTAG	TCK	I									I, ST

Table 4-1. Pin Description BGA217 (Continued)

			Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
Ball	**Power Rail**	**I/O Type**	**Signal**	**Dir**	**Signal**	**Dir**	**Signal**	**Dir**	**Signal**	**Dir**	**Signal**	**Dir**	**Signal, Dir, PU, PD, ST**
T9	VDDIOP0	RSTJTAG	TDI	I									I, ST
T10	VDDIOP0	RSTJTAG	TDO	O									O
U11	VDDIOP0	RSTJTAG	TMS	I									I, ST
R10	VDDIOP0	RSTJTAG	RTCK	O									O
P10	VDDIOP0	RSTJTAG	NRST	I/O									I, PU, ST
T11	VDDIOP0	RSTJTAG	NTRST	I									I, PU, ST
A6	VDDBU	CLOCK	XIN32	I									I
A5	VDDBU	CLOCK	XOUT32	O									O
T12	VDDOSC	CLOCK	XIN	I									I
U12	VDDOSC	CLOCK	XOUT	O									O

5. Mechanical Overview

Figure 5-1. 217-ball BGA Package Drawing



ALL DIMENSIONS ARE IN MILLIMETERS.						
SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.40	---	---	0.0551
A1	0.25	0.30	0.35	0.0098	0.0118	0.0138
A2	0.82	0.86	0.90	0.0323	0.0339	0.0354
A3	0.50 BASIC			0.0197 BASIC		
D	14.95	15.00	15.05	0.5886	0.5906	0.5925
D1	12.80 BASIC			0.5039 BASIC		
E	14.95	15.00	15.05	0.5886	0.5906	0.5925
E1	12.80 BASIC			0.5039 BASIC		
e	0.80 BASIC			0.0315 BASIC		
b	0.35	0.40	0.45	0.0137	0.0157	0.0175
aaa	0.15			0.0059		
bbb	0.25			0.0098		
ccc	0.20			0.0079		
ddd	0.12			0.0047		
eee	0.15			0.0059		
fff	0.08			0.0031		

Table 5-1. Device and 217-ball BGA Package Maximum Weight

450	mg

Table 5-2. 217-ball BGA Package Characteristics

Moisture Sensitivity Level	3

Table 5-3. Package Reference

JEDEC Drawing Reference	MO-205
JESD97 Classification	e1

Table 5-4. Package Information

Ball Land	0.43 mm ± 0.05
Solder Mask Opening	0.30 mm ± 0.05

6. SAM9X25 Ordering Information

Table 6-1. SAM9X25 Ordering Information

Ordering Code	Package	Package Type	Temperature Operating Range
AT91SAM9X25-CU	BGA217	Green	Industrial -40°C to 85°C

Revision History

In the tables that follow, the most recent version of the document appears first.

“rfo” indicates changes requested during the document review and approval loop.

Doc. Rev 11054BS	Comments	Change Request Ref.
	“Description”, added “4-bank” references to the DDR2 characteristics.	8282
	Section 1. “Features”:	
	- added “4-bank” references to the DDR2 characteristics in the “Memories” list	8282
	- replaced “MLC/SLC NAND Controller“ with “MLC/SLC 8-bit NAND Controller” in the “Memories” list	8403
	- added “DBGU” and “Write Protected Registers” in the “Peripherals” list	8213
	Section 2. “Block Diagram”, replaced TSADVREF with ADVREF in Figure 2-1 “SAM9X25 Block Diagram”.	8454
	Section 5. “Mechanical Overview”, updated the table title in Table 5-4 “Package Information”.	8186

Doc. Rev 11054AS	Comments	Change Request Ref.
	First issue.	

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