Sound Processor Series for Car Audio

Sound Processors with Built-in 2-band Equalizer

BD37511FS,BD37512FS

No.10085EAT10

●Description

BD37511FS, BD37512FS are sound processors built-in 2-band equalizer for car audio. The functions are stereo 4ch input selector(About BD37511FS, 3ch input selector are available), input-gain control, main volume, 4ch fader volume. Moreover, “Advanced switch circuit”, that is ROHM original technology, can reduce various switching noise (ex. No-signal, low frequency likes 20Hz & large signal inputs). “Advanced switch” makes control of microcomputer easier, and can construct high quality car audio system.

●Features

1) Reduce switching noise of mute, main volume, fader volume, bass, trebles by using advanced switch circuit [Possible to control all steps]
2) Built-in 1 differential input selector(BD37512FS) and 3 single-ended input selectors.
3) Built-in ground isolation amplifier inputs, ideal for external stereo input. (BD37512FS)
4) Decrease the number of external components by built-in 2-band equalizer filter.
5) It is possible for the bass, treble to the gain adjustment quantity of ±20dB and 1 dB step gain adjustment.
6) Bi-CMOS process is suitable for the design of low current and low energy. And it provides more quality for small scale regulator and heat in a set.
7) Package is SSOP-A20. Putting input-terminals together and output-terminals together can make PCB layout easier and can makes area of PCB smaller.
8) It is possible to control by 3.3V / 5V for I^2C BUS.

●Applications

It is the optimal for the car audio. Besides, it is possible to use for the audio equipment of mini Compo, micro Compo, TV etc with all kinds.

●Line up matrix

Function	BD37511FS	BD37512FS	Specifications
Input selector	○	○	・Stereo 3 input
	×	○	・Differential 1 input
Input gain	○	○	・0～20dB
Mute	○	○	・Possible to use “Advanced switch” for prevention of switching noise.
Volume	○	○	・0dB～-40dB（1dB step） ・Possible to use “Advanced switch” for prevention of switching noise.
Bass	○	○	・-20～+20dB（1dB step） ・Q=1 ・fo=100Hz ・Possible to use advanced switch at changing gain
Treble	○	○	・-20～+20dB（1dB step） ・Q=1 ・fo=10kHz ・Possible to use advanced switch at changing gain
Fader	○	○	・0dB～-62dB(1dB step), −∞dB ・Possible to use “Advanced switch” for prevention of switching noise.

●Absolute maximum ratings (Ta=25℃)

Item	Symbol	Rating	Unit
Power supply Voltage	VCC	10.0	V
Input voltage	Vin	VCC+0.3～GND-0.3	V
Power Dissipation	Pd	940 ※1	mW
Storage Temperature	Tastg	-55～+150	℃

※This value decreases 7.5mW/℃ for Ta=25℃ or more.
ROHM standard board shall be mounted.
Thermal resistance θja = 133(℃/W)
ROHM Standard board
Size：70×70×1.6(㎜)
Material：A FR4 grass epoxy board(3% or less of copper foil area)

●Operating conditions

Item	Symbol	MIN	TYP	MAX	Unit
Power supply Voltage	VCC	7.0	—	9.5	V
Temperature	Topr	-40	—	+85	℃

●Electrical characteristics

(Unless specified particularly, Ta=25℃, VCC=8.5V, f=1kHz, Vin=1Vrms, Rg=600Ω, R_L=10kΩ, A input, Input gain 0dB, Mute off, Volume 0dB, Tone control 0dB, Loudness 0dB, Fader 0dB)

BLOCK	Item	Symbol	Limit			Unit	Condition
			Min.	Typ.	Max.		
GENERAL	Current upon no signal	I_Q	—	15	30	mA	No signal
	Voltage gain	G_V	-1.5	0	1.5	dB	Gv=20log(VOUT/VIN)
	Channel balance	CB	-1.5	0	1.5	dB	CB = GV1-GV2
	Total harmonic distortion	THD+N1	—	0.005	0.05	%	VOUT=1Vrms BW=400-30KHz
	Output noise voltage ＊	V_{NO1}	—	6	25	μVrms	Rg = 0Ω BW = IHF-A
	Residual output noise voltage＊	V_{NOR}	—	2	10	μVrms	Fader = -∞dB Rg = 0Ω BW = IHF-A
	Cross-talk between channels＊	CTC	—	-100	-90	dB	Rg = 0Ω CTC=20log(VOUT/VIN) BW = IHF-A
	Ripple rejection	RR	—	-70	-40	dB	f=1kHz VRR=100mVrms RR=20log(VCC IN/VOUT)
INPUT SELECTOR	Input impedance(A, B, C)	R_{IN_S}	70	100	130	kΩ	
	Input impedance (D) (BD37512FS)	R_{IN_D}	35	50	65	kΩ	
	Maximum input voltage	V_{IM}	2.1	2.3	—	Vrms	VIM at THD+N(VOUT)=1% BW=400-30KHz
	Cross-talk between selectors＊	CTS	—	-100	-90	dB	Rg = 0Ω CTS=20log(VOUT/VIN) BW = IHF-A
	Common mode rejection ratio＊ (BD37512FS)	CMRR	50	65	—	dB	DP1 and DN input DP2 and DN input CMRR=20log(VIN/VOUT) BW = IHF-A
INPUT GAIN	Minimum input gain	$G_{IN\ MIN}$	-2	0	+2	dB	Input gain 0dB VIN=100mVrms Gin=20log(VOUT/VIN)
	Maximum input gain	$G_{IN\ MAX}$	18	20	22	dB	Input gain 20dB VIN=100mVrms Gin=20log(VOUT/VIN)
	Gain set error	$G_{IN\ ERR}$	-2	0	+2	dB	GAIN=+1～+20dB

BLOCK	Item	Symbol	Limit			Unit	Condition
			Min.	Typ.	Max.		
MUTE	Mute attenuation ∗	G_{MUTE}	—	-105	-85	dB	Mute ON Gmute=20log(VOUT/VIN) BW = IHF-A
VOLUME	Maximum attenuation	$G_{V\ MIN}$	-43	-40	-37	dB	Volume = -40dB Gv=20log(VOUT/VIN)
	Attenuation set error 1	$G_{V\ ERR1}$	-2	0	2	dB	GAIN & ATT=0dB～-15dB
	Attenuation set error 2	$G_{V\ ERR2}$	-3	0	3	dB	ATT=-16dB～-40dB
BASS	Maximum boost gain	$G_{B\ BST}$	18	20	22	dB	Gain=+20dB f=100Hz VIN=100mVrms G_B=20log (VOUT/VIN)
	Maximum cut gain	$G_{B\ CUT}$	-22	-20	-18	dB	Gain=-20dB f=100Hz VIN=2Vrms G_B=20log (VOUT/VIN)
	Gain set error	$G_{B\ ERR}$	-2	0	2	dB	Gain=-20～+20dB f=100Hz
TREBLE	Maximum boost gain	$G_{T\ BST}$	18	20	22	dB	Gain=+20dB f=10kHz VIN=100mVrms G_T=20log (VOUT/VIN)
	Maximum cut gain	$G_{T\ CUT}$	-22	-20	-18	dB	Gain=-20dB f=10kHz VIN=2Vrms G_T=20log (VOUT/VIN)
	Gain set error	$G_{T\ ERR}$	-2	0	2	dB	Gain=-20～+20dB f=10kHz
FADER	Maximum attenuation ∗	$G_{F\ MIN}$	—	-100	-90	dB	Fader = -∞dB G_F=20log(VOUT/VIN) BW = IHF-A
	Attenuation set error 1	$G_{F\ ERR1}$	-2	0	2	dB	ATT=0～-15dB
	Attenuation set error 2	$G_{F\ ERR2}$	-3	0	3	dB	ATT=-16～-47dB
	Attenuation set error 3	$G_{F\ ERR3}$	-4	0	4	dB	ATT=-48～-62dB
	Output impedance	R_{OUT}	-	—	50	Ω	VIN=100mVrms
	Maximum output voltage	V_{OM}	2	2.2	—	Vrms	THD+N=1% BW=400-30KHz

VP-9690A(Average value detection, effective value display) filter by Matsushita Communication is used for ∗ measurement.
Phase between input / output is same.

●Electrical characteristic curves (Reference data)

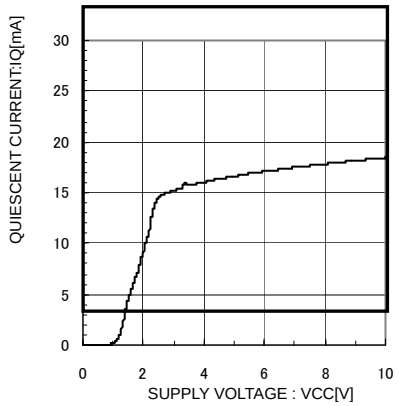


Fig.1 Iq vs Vcc

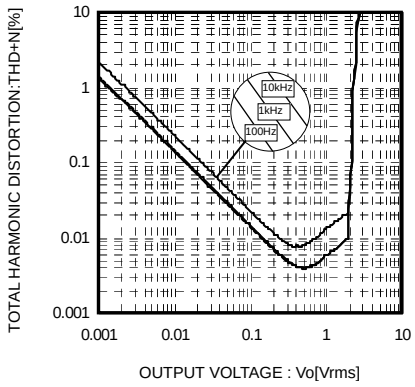


Fig.2Thd vs Vo

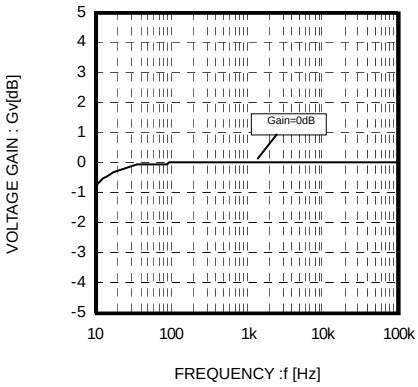


Fig.3 Gain vs Freq

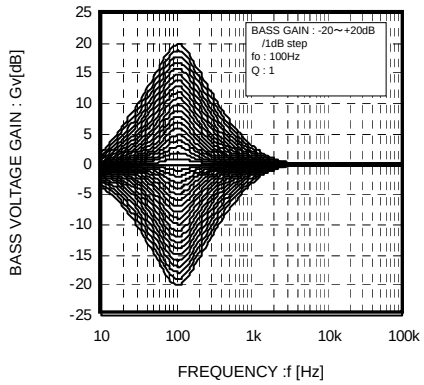


Fig.4 Bass Gain vs Freq

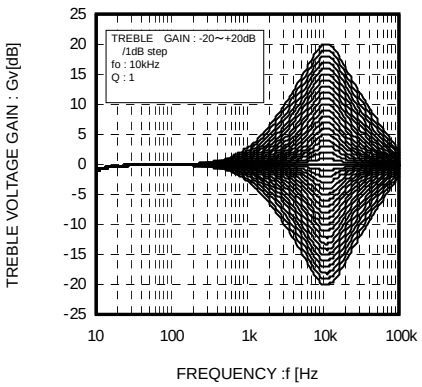


Fig.5 Treble Gain vs Freq

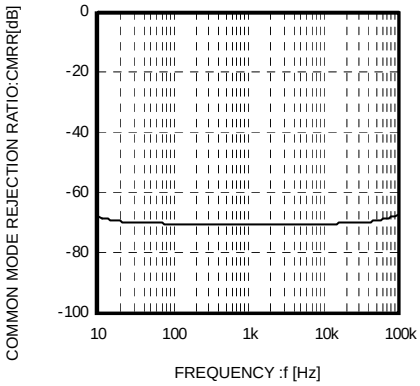


Fig.6 CMRR vs Freq

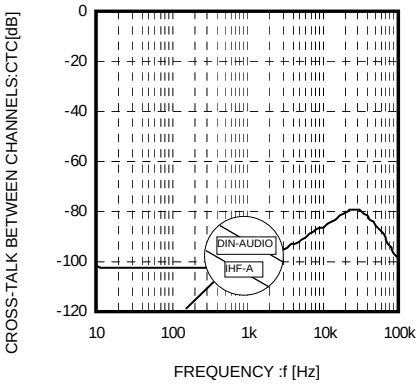


Fig.7 Cross-Talk vs Freq

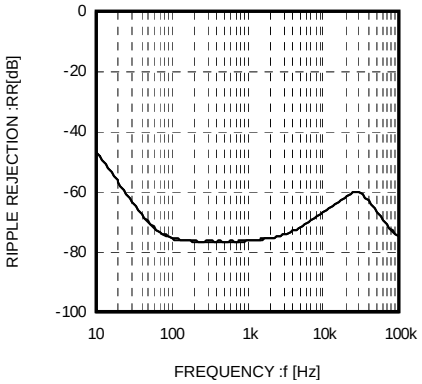


Fig.8 RIPPLE REJECTION RATIO

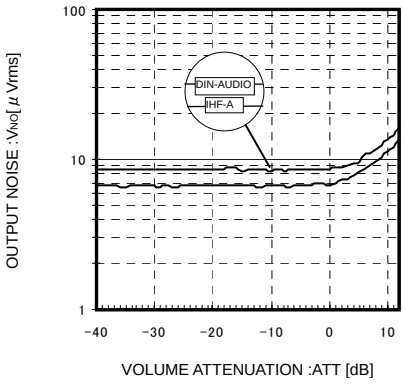


Fig.9 Volume Gain vs Noise

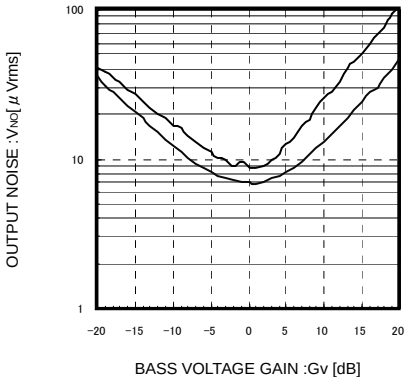


Fig.10 Bass Gain vs Noise

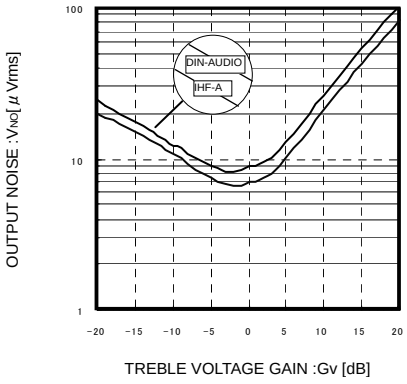


Fig.11 Treble Gain vs Noise

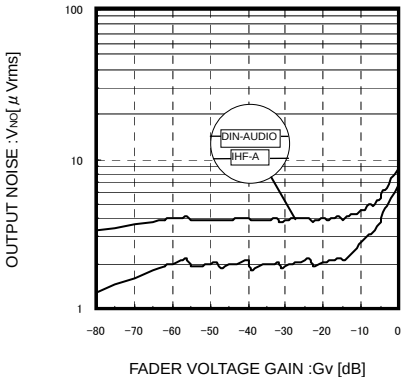


Fig.12 Fader Gain vs Noise

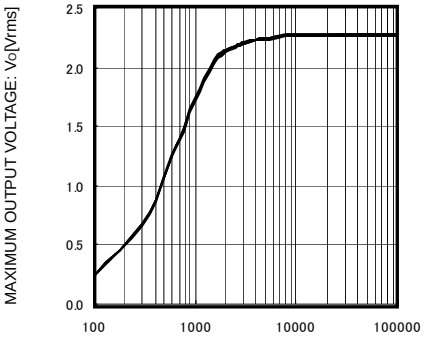


Fig.13 Rload vs Vo

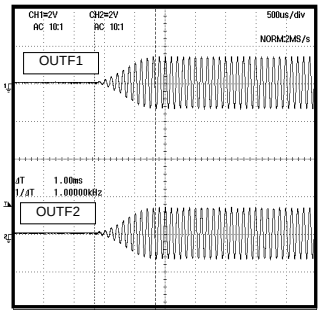


Fig.14Advanced Switch 1

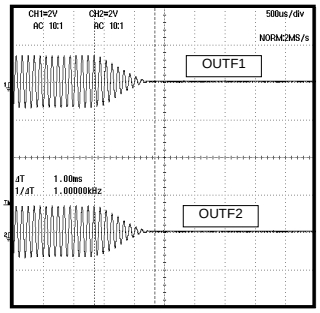


Fig. 15 Advanced Switch 2

●Block diagram and pin configuration

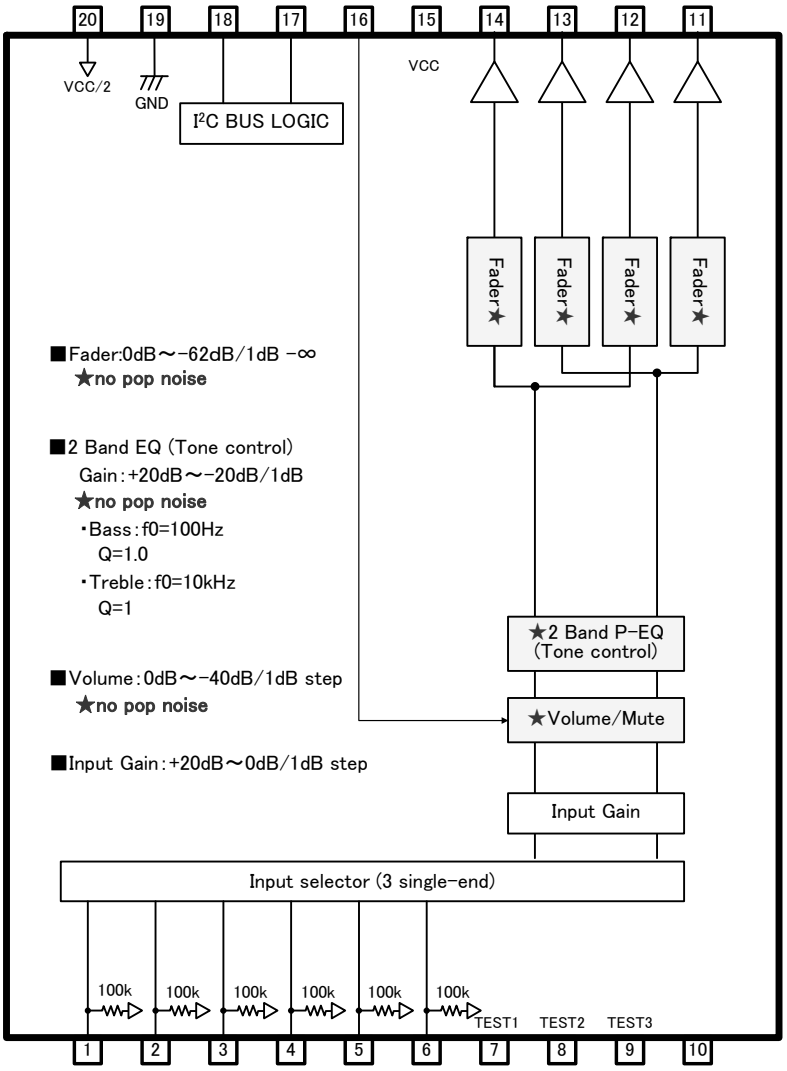


Fig.16 BD37511FS

Descriptions of terminal

Terminal No.	Terminal Name	Description	Terminal No.	Terminal Name	Description
1	A1	A input terminal of 1ch	11	OUTR2	Rear output terminal of 2ch
2	A2	A input terminal of 2ch	12	OUTR1	Rear output terminal of 1ch
3	B1	B input terminal of 1ch	13	OUTF2	Front output terminal of 2ch
4	B2	B input terminal of 2ch	14	OUTF1	Front output terminal of 1ch
5	C1	C input terminal of 1ch	15	VCC	Power supply terminal
6	C2	C input terminal of 2ch	16	MUTE	External compulsory mute terminal
7	TEST1	Test Pin	17	SCL	I²C Communication clock terminal
8	TEST2	Test Pin	18	SDA	I²C Communication data terminal
9	TEST3	Test Pin	19	GND	GND terminal
10	N.C.	No Connection	20	FIL	VCC/2 terminal

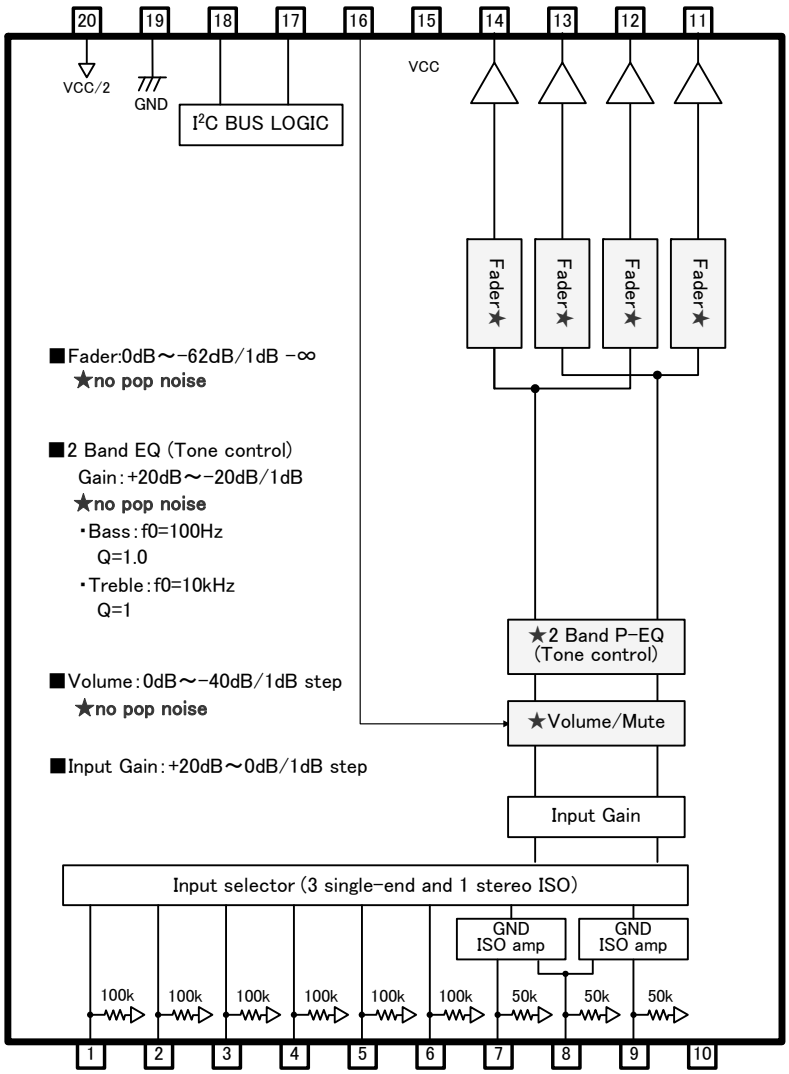


Fig.17 BD37512FS

Descriptions of terminal

Terminal No.	Terminal Name	Description	Terminal No.	Terminal Name	Description
1	A1	A input terminal of 1ch	11	OUTR2	Rear output terminal of 2ch
2	A2	A input terminal of 2ch	12	OUTR1	Rear output terminal of 1ch
3	B1	B input terminal of 1ch	13	OUTF2	Front output terminal of 2ch
4	B2	B input terminal of 2ch	14	OUTF1	Front output terminal of 1ch
5	C1	C input terminal of 1ch	15	VCC	Power supply terminal
6	C2	C input terminal of 2ch	16	MUTE	External compulsory mute terminal
7	DP1	D positive input terminal of 1ch	17	SCL	I^2C Communication clock terminal
8	DN	D negative input terminal	18	SDA	I^2C Communication data terminal
9	DP2	D positive input terminal of 2ch	19	GND	GND terminal
10	N.C.	No Connection	20	FIL	VCC/2 terminal

●Timming Chart

CONTROL SIGNAL SPECIFICATION

(1) Electrical specifications and timing for bus lines and I/O stages

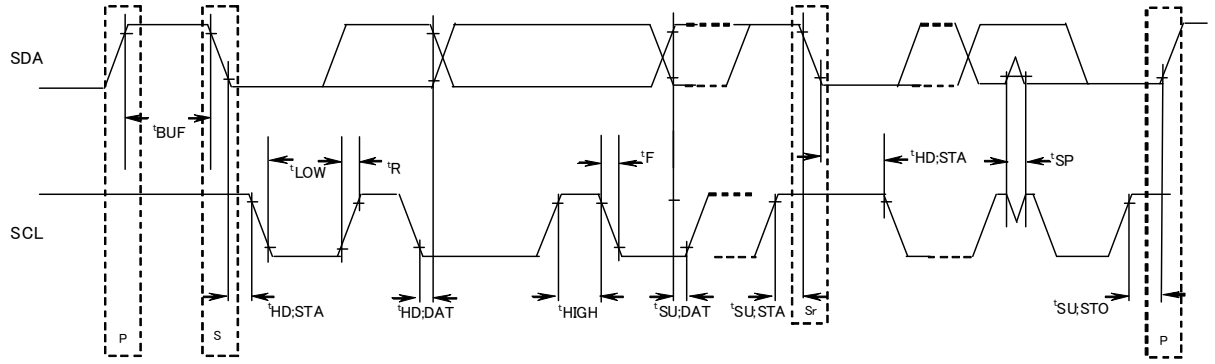


Fig.18 Definition of timing on the I^2C-bus

Table 1 Characteristics of the SDA and SCL bus lines for I^2C-bus devices

Parameter		Symbol	Fast-mode I^2C-bus		Unit
			Min.	Max.	
1	SCL clock frequency	f SCL	0	400	kHz
2	Bus free time between a STOP and START condition	tBUF	1.3	—	μS
3	Hold time (repeated) START condition. After this period, the first clock pulse is generated	tHD;STA	0.6	—	μS
4	LOW period of the SCL clock	tLOW	1.3	—	μS
5	HIGH period of the SCL clock	tHIGH	0.6	—	μS
6	Set-up time for a repeated START condition	tSU;STA	0.6	—	μS
7	Data hold time:	tHD;DAT	0.7*	—	μS
8	Data set-up time	tSU;DAT	700	—	ns
9	Set-up time for STOP condition	tSU;STO	0.6	—	μS

All values referred to VIH min. and VIL max. Levels (see Table 2).

* A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIH min. of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
About 7(tHD;DAT), 8(tSU;DAT), make it the setup which a margin is fully in .

Table 2 Characteristics of the SDA and SCL I/O stages for I^2C-bus devices

	Parameter	Symbol	Fast-mode devices		Unit
			Min.	Max.	
10	LOW level input voltage:	VIL	-0.3	1	V
11	HIGH level input voltage:	VIH	2.3	5	V
12	Pulse width of spikes which must be suppressed by the input filter.	tSP	0	50	ns
13	LOW level output voltage: at 3mA sink current	VOL1	0	0.4	V
14	Input current each I/O pin with an input voltage between 0.4V and 4.5V.	Ii	-10	10	μA

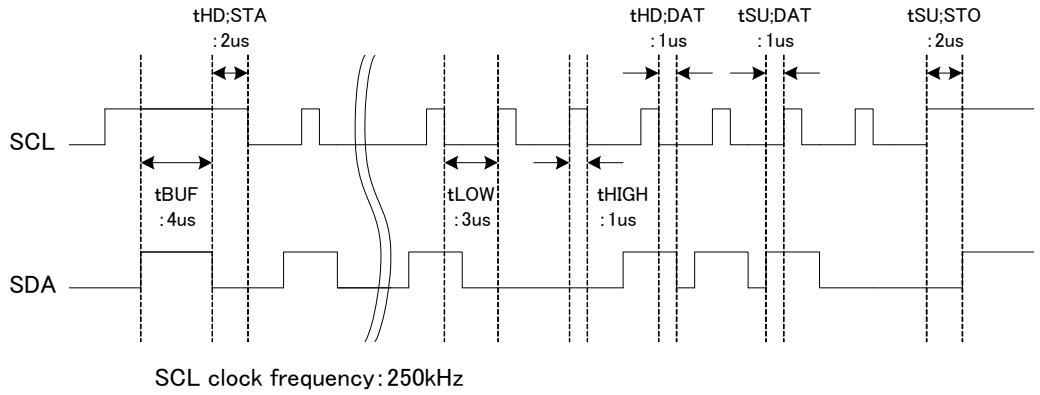


Fig.19 A command timing example in the I2C data transmission

（２）I²C BUS FORMAT

	MSB LSB		MSB LSB		MSB LSB		
S	Slave Address	A	Select Address	A	Data	A	P
1bit	8bit	1bit	8bit	1bit	8bit	1bit	1bit

S = Start conditions (Recognition of start bit)
Slave Address = Recognition of slave address. 7 bits in upper order are voluntary. The least significant bit is “L” due to writing.
A = ACKNOWLEDGE bit (Recognition of acknowledgement)
Select Address = Select every of volume, bass and treble.
Data = Data on every volume and tone.
P = Stop condition (Recognition of stop bit)

（３）I²C BUS Interface Protocol

1) Basic form

S	Slave Address	A	Select Address	A	Data	A	P
	MSB LSB		MSB LSB		MSB LSB		

2) Automatic increment (Select Address increases (+1) according to the number of data.)

S	Slave Address	A	Select Address	A	Data1	A	Data2	A	····	DataN	A	P
	MSB LSB		MSB LSB		MSB LSB		MSB LSB			MSB LSB		

(Example)①Data1 shall be set as data of address specified by Select Address.
②Data2 shall be set as data of address specified by Select Address +1.
③DataN shall be set as data of address specified by Select Address +N-1.

3) Configuration unavailable for transmission (In this case, only Select Address1 is set.)

S	Slave Address	A	Select Address1	A	Data	A	Select Address 2	A	Data	A	P
	MSB LSB		MSB LSB		MSB LSB		MSB LSB		MSB LSB		

(Note) If any data is transmitted as Select Address 2 next to data, it is recognized as data, not as Select Address 2.

（４）Slave address

MSB							LSB	
A6	A5	A4	A3	A2	A1	A0	R/W	
1	0	0	0	0	0	0	0	80H

（５）Select Address & Data

Items	Select Address (hex)	MSB Data LSB							
		D7	D6	D5	D4	D3	D2	D1	D0
Initial setup 1	01	Advanced switch ON/OFF	0	Advanced switch time of Volume/Tone/Fader		0	0	Advanced switch time of Mute	
Input Selector	04	0	0	0	0	0	Input selector		
Input gain	06	Mute ON/OFF	0	0	Input Gain				
Volume gain	20	1	0	Volume Attenuation					
Fader 1ch Front	28	1	0	Fader Attenuation					
Fader 2ch Front	29	1	0	Fader Attenuation					
Fader 1ch Rear	2A	1	0	Fader Attenuation					
Fader 2ch Rear	2B	1	0	Fader Attenuation					
Bass gain	51	Bass Boost/ Cut	0	0	Bass Gain				
Treble gain	57	Treble Boost/ Cut	0	0	Treble Gain				
System Reset	FE	1	0	0	0	0	0	0	1

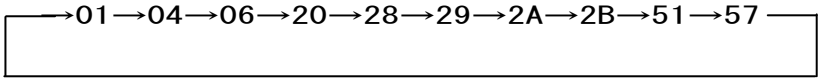
Advanced switch

Note

1. In function changing of the hatching part, it works Advanced switch.

2. When changing a tone into the cut from the boost, or the cut and the boost, always go via the condition of the tone 0dB.

3. Upon continuous data transfer, the Select Address is circulated by the automatic increment function, as shown below.



4. For the function of input selector etc, it is not corresponded for advanced switch. Therefore, please apply mute on the side of a set when changes these setting.

5. When using mute function of this IC at the time of changing input selector, please switch mute ON/OFF for waiting advanced-mute time.

Select address 01 (hex)

Mode	MSB		Advanced switch time of Mute					LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0.6msec	Advanced Switch ON/OFF	0	Advanced switch time of Volume/Tone/Fader		0	0	0	0
1.2msec							0	1
2.4msec							1	0
4.8msec							1	1

Mode	MSB		Advanced switch time of Volume/Tone/Fader					LSB
	D7	D6	D5	D4	D3	D2	D1	D0
4.6 msec	Advanced Switch ON/OFF	0	0	0	0	0	Advanced switch Time of Mute	
9.3 msec			0	1				
18.6 msec			1	0				
37.2 msec			1	1				

Mode	MSB		Advanced switch ON/OFF					LSB
	D7	D6	D5	D4	D3	D2	D1	D0
OFF	0	0	Advanced switch time of Volume/Tone/Fader		0	0	Advanced switch Time of Mute	
ON	1							

Select address 04(hex)

Mode	MSB		Input Selector					LSB
	D7	D6	D5	D4	D3	D2	D1	D0
A	0	0	0	0	0	0	0	0
B						0	0	1
C						0	1	0
D						1	0	0
SHORT						1	0	1
INPUT MUTE						1	1	0
						1	1	1

(D is available only BD37512FS.)

:Initial condition

SHORT: The input impedance of each input terminal is lowered from 100kΩ(TYP) to 6 kΩ(TYP).
(For quick charge of coupling capacitor)

INPUT MUTE: Mute is done at the input signal in the part of Input Selector.

Select address 06 (hex)

Gain	MSB Input Gain LSB							
	D7	D6	D5	D4	D3	D2	D1	D0
0dB	Mute ON/OFF	0	0	0	0	0	0	0
1dB				0	0	0	0	1
2dB				0	0	0	1	0
3dB				0	0	0	1	1
4dB				0	0	1	0	0
5dB				0	0	1	0	1
6dB				0	0	1	1	0
7dB				0	0	1	1	1
8dB				0	1	0	0	0
9dB				0	1	0	0	1
10dB				0	1	0	1	0
11dB				0	1	0	1	1
12dB				0	1	1	0	0
13dB				0	1	1	0	1
14dB				0	1	1	1	0
15dB				0	1	1	1	1
16dB				1	0	0	0	0
17dB				1	0	0	0	1
18dB				1	0	0	1	0
19dB				1	0	0	1	1
20dB				1	0	1	0	0
Prohibition				1	1	0	1	1
				:	:	:	:	:
				1	1	1	1	1

※In case sending prohibited data, 0dB is set.

Mode	MSB Mute ON/OFF LSB							
	D7	D6	D5	D4	D3	D2	D1	D0
OFF	0	0	0	Input Gain				
ON	1							

:Initial condition

Select address 20 (hex)

Gain & ATT	MSB		Vol Attenuation					LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0dB	1	0	0	0	0	0	0	0
-1dB			0	0	0	0	0	1
-2dB			0	0	0	0	1	0
・ ・ ・			・ ・ ・	・ ・ ・	・ ・ ・	・ ・ ・	・ ・ ・	・ ・ ・
-38dB			1	0	0	1	1	0
-39dB			1	0	0	1	1	1
-40dB			1	0	1	0	0	0
Prohibition			1	0	1	0	0	1
			:	:	:	:	:	:
			1	1	1	1	1	0
			1	1	1	1	1	1

※In case sending prohibited data, -40dB is set.

Select address 28, 29, 2A, 2B (hex)

Gain & ATT	MSB		Fader Attenuation					LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0dB	1	0	0	0	0	0	0	0
-1dB			0	0	0	0	0	1
-2dB			0	0	0	0	1	0
・ ・ ・			・ ・ ・	・ ・ ・	・ ・ ・	・ ・ ・	・ ・ ・	・ ・ ・
-61dB			1	1	1	1	0	1
-62dB			1	1	1	1	1	0
-∞dB			1	1	1	1	1	1

: Initial condition

Select address 51, 57 (hex)

Gain	MSB			Bass/Treble Gain				LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0dB	Bass/ Treble Boost /cut	0	0	0	0	0	0	0
1dB				0	0	0	0	1
2dB				0	0	0	1	0
3dB				0	0	0	1	1
4dB				0	0	1	0	0
5dB				0	0	1	0	1
6dB				0	0	1	1	0
7dB				0	0	1	1	1
8dB				0	1	0	0	0
9dB				0	1	0	0	1
10dB				0	1	0	1	0
11dB				0	1	0	1	1
12dB				0	1	1	0	0
13dB				0	1	1	0	1
14dB				0	1	1	1	0
15dB				0	1	1	1	1
16dB				1	0	0	0	0
17dB				1	0	0	0	1
18dB				1	0	0	1	0
19dB				1	0	0	1	1
20dB				1	0	1	0	0
Prohibition				1	0	1	0	1
				:	:	:	:	:
				1	1	1	1	0
				1	1	1	1	1

※In case sending prohibited data, 0dB is set.

Mode	MSB			Bass/Treble Boost/Cut				LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Boost	0	0	0	Bass/Treble Gain				
Cut	1							

:Initial condition

（6）About power on reset

At on of supply voltage circuit made initialization inside IC is built-in. Please send data to all address as initial data at supply voltage on. And please supply mute at set side until this initial data is sent.

Item	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Rise time of VCC	Trise	20	—	—	usec	VCC rise time from 0V to 3V
VCC voltage of release power on reset	Vpor	—	4.1	—	V	

（7）About external compulsory mute terminal

Mute is possible forcibly than the outside after input again department, by the setting of the MUTE terminal.

Mute Voltage Condition	Mode
GND～1.0V	MUTE ON
2.3V～VCC	MUTE OFF

Establish the voltage of MUTE in the condition to have been defined.

Volume / Fader volume attenuation of the details

(dB)	D7	D6	D5	D4	D3	D2	D1	D0		(dB)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	0	0		-32	1	0	1	0	0	0	0	0
-1			0	0	0	0	0	1		-33			1	0	0	0	0	1
-2			0	0	0	0	1	0		-34			1	0	0	0	1	0
-3			0	0	0	0	1	1		-35			1	0	0	0	1	1
-4			0	0	0	1	0	0		-36			1	0	0	1	0	0
-5			0	0	0	1	0	1		-37			1	0	0	1	0	1
-6			0	0	0	1	1	0		-38			1	0	0	1	1	0
-7			0	0	0	1	1	1		-39			1	0	0	1	1	1
-8			0	0	1	0	0	0		-40			1	0	1	0	0	0
-9			0	0	1	0	0	1		-41			1	0	1	0	0	1
-10			0	0	1	0	1	0		-42			1	0	1	0	1	0
-11			0	0	1	0	1	1		-43			1	0	1	0	1	1
-12			0	0	1	1	0	0		-44			1	0	1	1	0	0
-13			0	0	1	1	0	1		-45			1	0	1	1	0	1
-14			0	0	1	1	1	0		-46			1	0	1	1	1	0
-15			0	0	1	1	1	1		-47			1	0	1	1	1	1
-16			0	1	0	0	0	0		-48			1	1	0	0	0	0
-17			0	1	0	0	0	1		-49			1	1	0	0	0	1
-18			0	1	0	0	1	0		-50			1	1	0	0	1	0
-19			0	1	0	0	1	1		-51			1	1	0	0	1	1
-20			0	1	0	1	0	0		-52			1	1	0	1	0	0
-21			0	1	0	1	0	1		-53			1	1	0	1	0	1
-22			0	1	0	1	1	0		-54			1	1	0	1	1	0
-23			0	1	0	1	1	1		-55			1	1	0	1	1	1
-24			0	1	1	0	0	0		-56			1	1	1	0	0	0
-25			0	1	1	0	0	1		-57			1	1	1	0	0	1
-26			0	1	1	0	1	0		-58			1	1	1	0	1	0
-27			0	1	1	0	1	1		-59			1	1	1	0	1	1
-28			0	1	1	1	0	0		-60			1	1	1	1	0	0
-29			0	1	1	1	0	1		-61			1	1	1	1	0	1
-30			0	1	1	1	1	0		-62			1	1	1	1	1	0
-31			0	1	1	1	1	1		-∞			1	1	1	1	1	1

About Volume attenuation, only 0dB～-40dB are available.

: Initial condition

●Application circuit

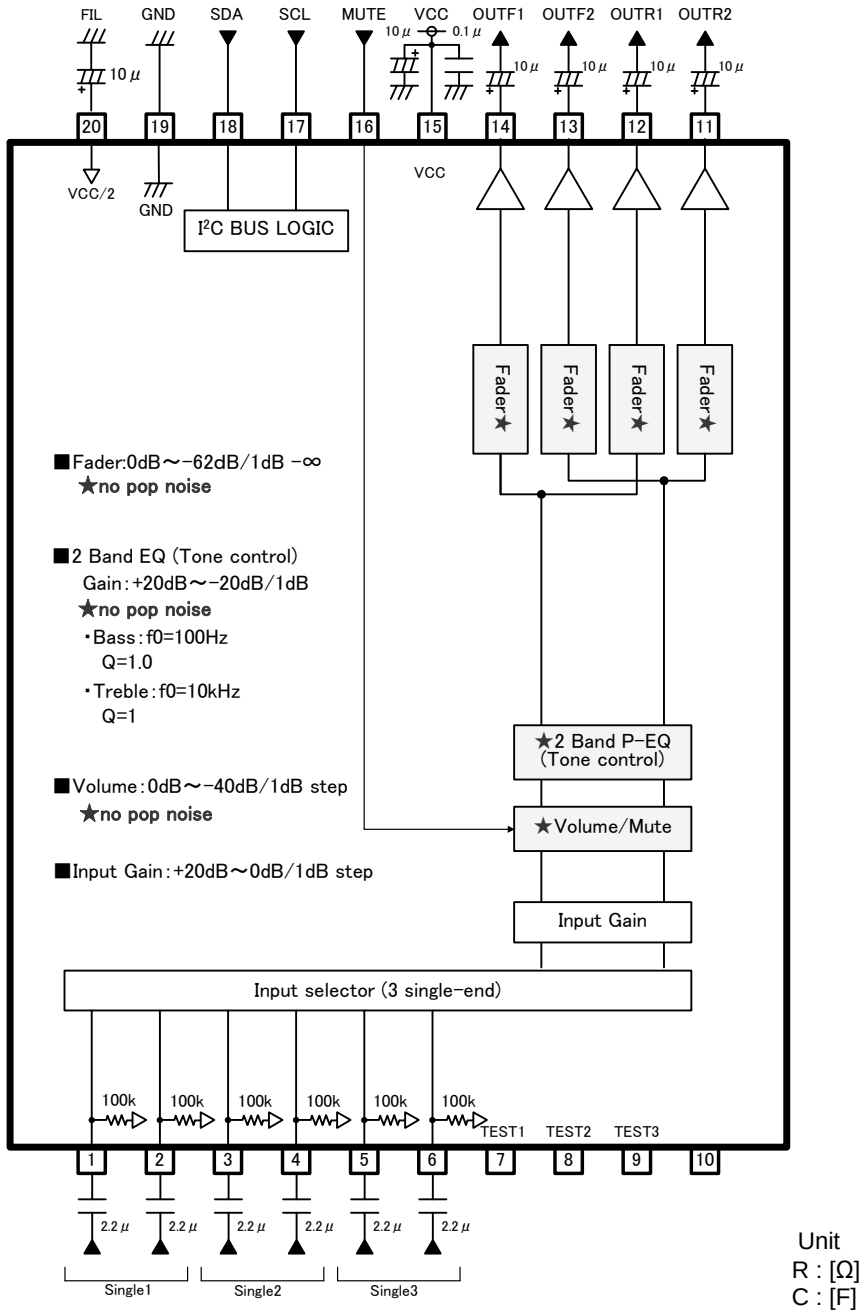


Fig.20 BD37511FS

Notes on wiring

① Please connect the decoupling capacitor of a power supply in the shortest distance as much as possible to GND.
② Lines of GND shall be one-point connected.
③ Wiring pattern of Digital shall be away from that of analog unit and cross-talk shall not be acceptable.
④ Lines of SCL and SDA of I²C BUS shall not be parallel if possible.
The lines shall be shielded, if they are adjacent to each other.
⑤ Lines of analog input shall not be parallel if possible. The lines shall be shielded, if they are adjacent to each other.
⑥ About TEST pin(7,8,9pin), please use with OPEN.

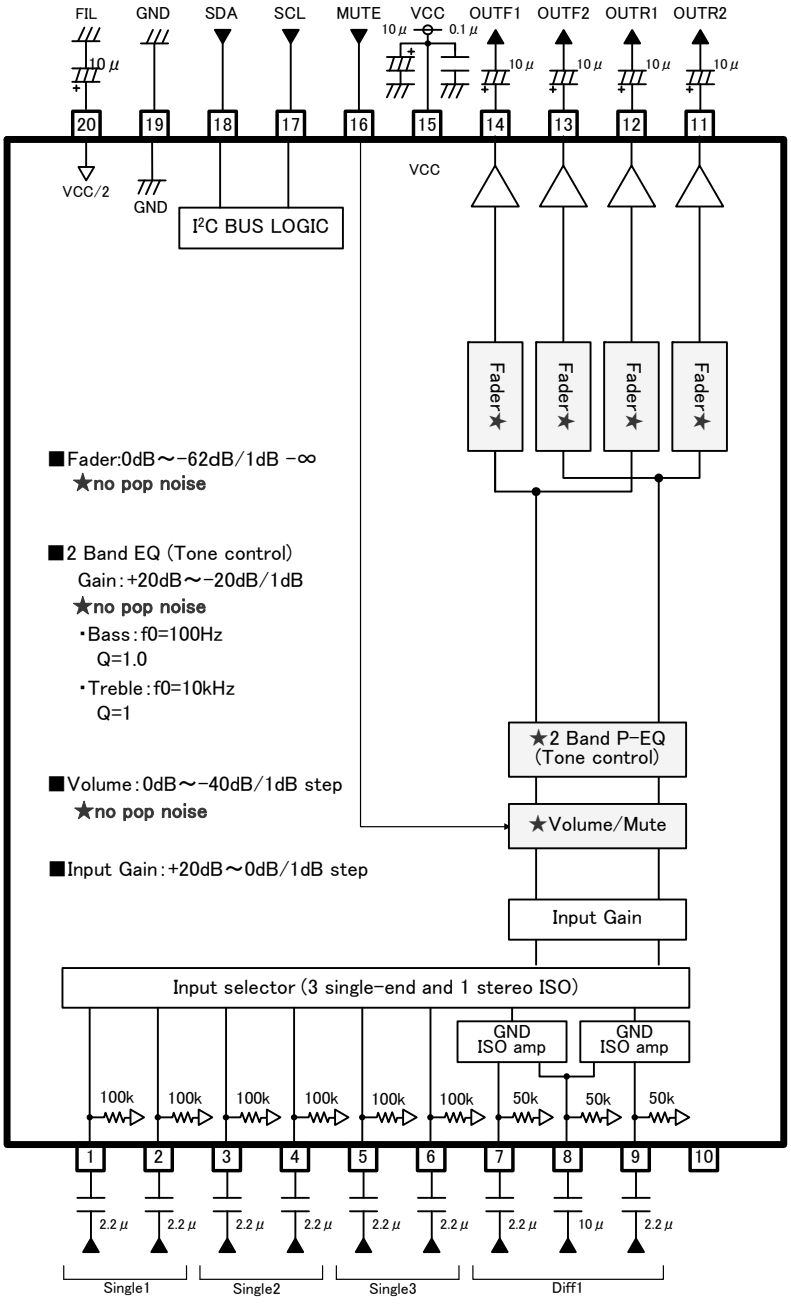
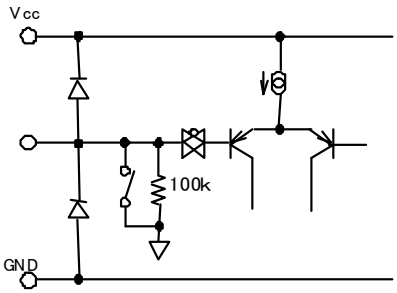
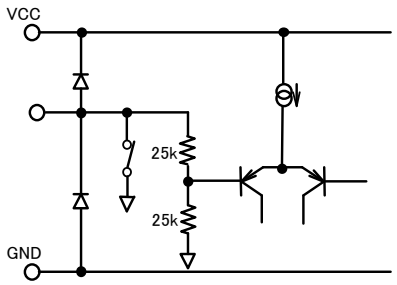
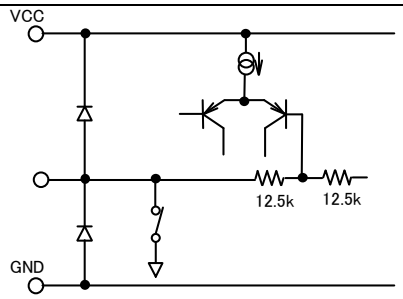
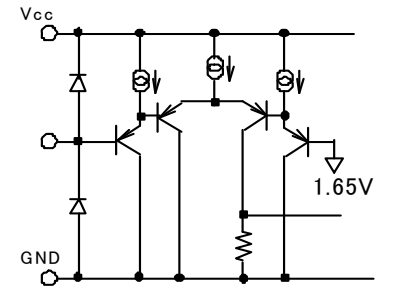
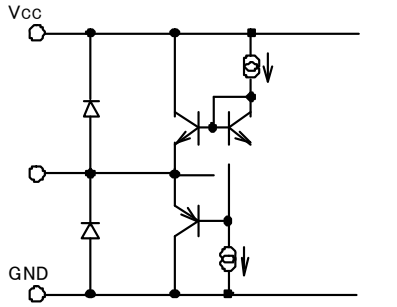


Fig.21 BD37512FS

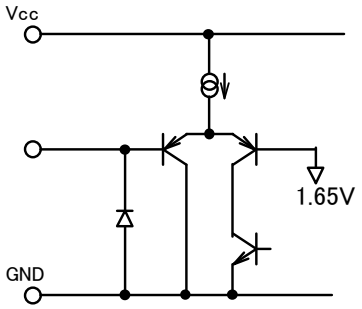
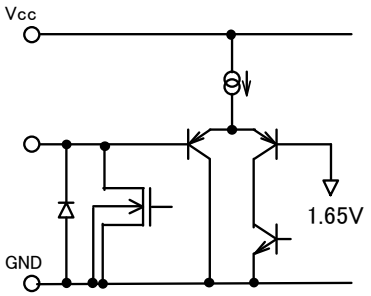
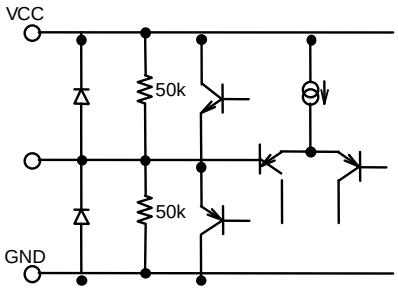
Notes on wiring

① Please connect the decoupling capacitor of a power supply in the shortest distance as much as possible to GND.
② Lines of GND shall be one-point connected.
③ Wiring pattern of Digital shall be away from that of analog unit and cross-talk shall not be acceptable.
④ Lines of SCL and SDA of I²C BUS shall not be parallel if possible.
The lines shall be shielded, if they are adjacent to each other.
⑤ Lines of analog input shall not be parallel if possible. The lines shall be shielded, if they are adjacent to each other.

●**Interfaces**

Terminal No.	Terminal Name	Terminal Voltage	Equivalent Circuit	Terminal Description
1 2 3 4 5 6	A1 A2 B1 B2 C1 C2	4.25		A terminal for signal input. The input impedance is 100kΩ(typ).
7 9	DP1 DP1	4.25		A terminal for positive input of ground isolation amplifier.(BD37512FS) The input impedance is 50kΩ(typ).
8	DN	4.25		A terminal for negative input of ground isolation amplifier. (BD37512FS) The input impedance is 12.5kΩ(typ).
16	MUTE	—		A terminal for external compulsory mute. If terminal voltage is High level, the mute is off. And if the terminal voltage is Low level, the mute is on.
11 12 13 14	OUTR2 OUTR1 OUTF2 OUTF1	4.25		A terminal for fader and Subwoofer output.

The figure in the pin explanation and input/output equivalent circuit is reference value, it doesn't guarantee the value.

Terminal No.	Terminal Name	Terminal Voltage	Equivalent Circuit	Terminal Description
15	VCC	8.5		Power supply terminal.
17	SCL	—		A terminal for clock input of I²C BUS communication.
18	SDA	—		A terminal for data input of I²C BUS communication.
19	GND	0		Ground terminal.
20	FIL	4.25		Voltage for reference bias of analog signal system. The simple precharge circuit and simple discharge circuit for an external capacitor are built in.
7 8 9	TEST1 TEST2 TEST3	-		TEST terminal. (BD37511FS)

The figure in the pin explanation and input/output equivalent circuit is reference value, it doesn't guarantee the value.

●Notes for use

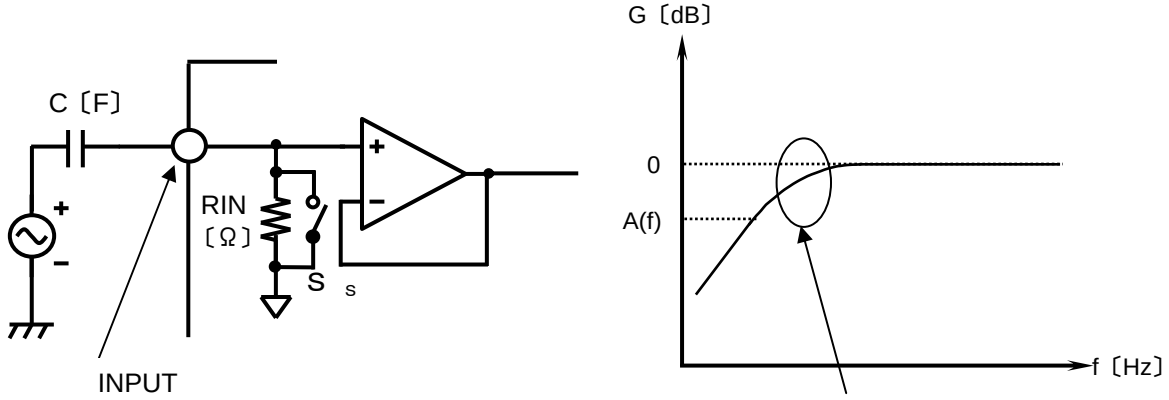
1. Absolute maximum rating voltage

When it impressed the voltage on VCC more than the absolute maximum rating voltage, circuit currents increase rapidly, and there is absolutely a case to reach characteristic deterioration and destruction of a device. In particular in a serge examination of a set, when it is expected the impressing serge at VCC terminal (15pin), please do not impress the large and over the absolute maximum rating voltage (including a operating voltage + serge ingredient (around 14V)).

2. About a signal input part

1) About constant set up of input coupling capacitor

In the signal input terminal, the constant setting of input coupling capacitor C(F) be sufficient input impedance R_{IN}(Ω) inside IC and please decide. The first HPF characteristic of RC is composed.



$$A(f) = \sqrt{\frac{(2\pi fCR_{IN})^2}{1+(2\pi fCR_{IN})^2}}$$

2) About the input selector SHORT

SHORT mode is the command which makes switch S_{SH} =ON an input selector part and input impedance RIN of all terminals, and makes resistance small. Switch S_{SH} is OFF when not choosing a SHORT command.
A constant time becomes small at the time of this command twisting to the resistance inside the capacitor connected outside and LSI. The charge time of a capacitor becomes short.
Since SHORT mode turns ON the switch of S_{SH} and makes it low impedance, please use it at the time of a non-signal.

3. About Mute terminal(11pin) when power supply is off

Any voltage shall not be supplied to Mute terminal (16pin) when power-supply is off.
Please insert a resistor (about 2.2kΩ) to Mute terminal in series, if voltage is supplied to mute terminal in case. (Please refer Application Circuit Diagram.)

4. About TEST Pin

About TEST Pin, please use with OPEN.
About BD37511FS, 7, 8,9pin is TEST Pin.

●Thermal Derating Curve

About the thermal design by the IC

Characteristics of an IC have a great deal to do with the temperature at which it is used, and exceeding absolute maximum ratings may degrade and destroy elements. Careful consideration must be given to the heat of the IC from the two standpoints of immediate damage and long-term reliability of operation.

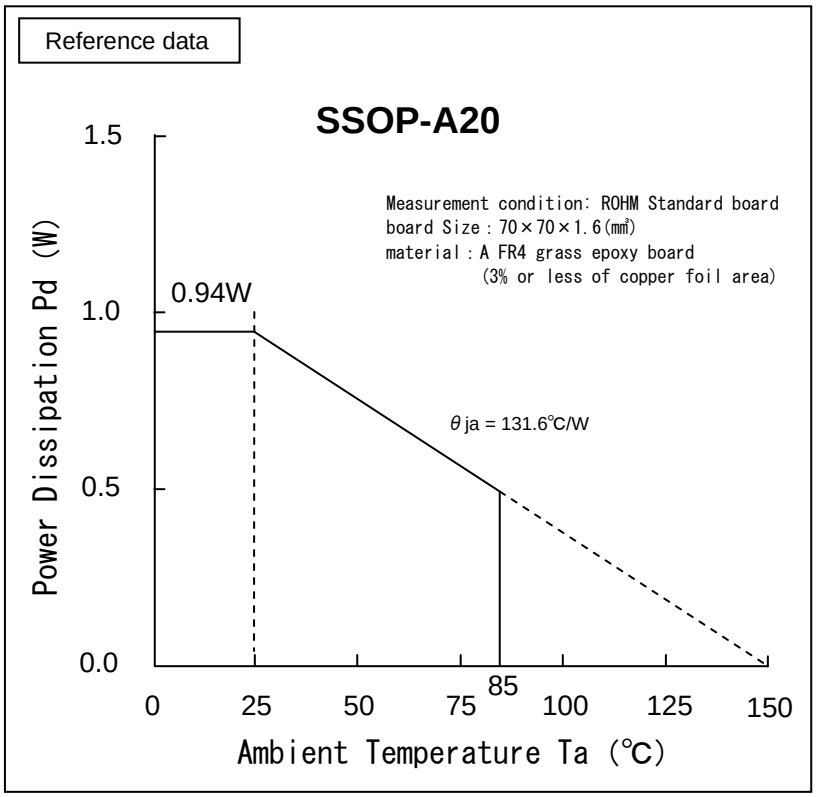


Fig.22 Temperature Derating Curve

Note) Values are actual measurements and are not guaranteed.

Power dissipation values vary according to the board on which the IC is mounted.

●Ordering part number

B	D	3	7	5	1	1	F	S	-	E	2

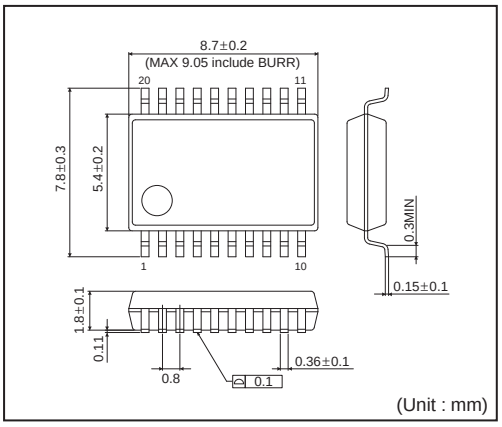
Part No.

Part No.
37511
37512

Package
FS : SSOP-A20

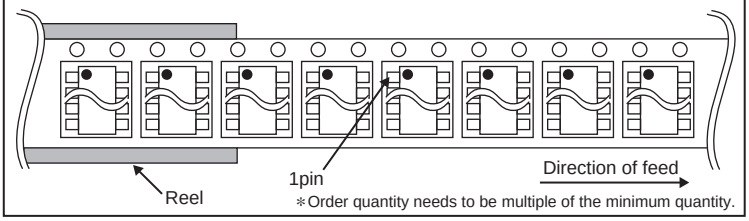
Packaging and forming specification
E2: Embossed tape and reel

SSOP-A20



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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