Sound Processor Series for Car Audio

Sound Processors with Built-in 2-band Equalizer

BD37522FS,BD37523FS

No.10085EAT04

●Description

BD37522FS, BD37523FS are sound processors built-in 2-band equalizer for car audio. The functions are stereo 5ch input selector, input-gain control, main volume, loudness, 5ch fader volume (About BD37522FS, 4ch fader volume are available). Moreover, “Advanced switch circuit”, that is ROHM original technology, can reduce various switching noise (ex. No-signal, low frequency likes 20Hz & large signal inputs). “Advanced switch” makes control of microcomputer easier, and can construct high quality car audio system.

●Features

1) Reduce switching noise of input gain control, mute, main volume, fader volume, bass, treble, loudness by using advanced switch circuit [Possible to control all steps]
2) Built-in 1 differential input selector and 4 single-ended input selectors
3) Built-in ground isolation amplifier inputs, ideal for external stereo input.
4) Built-in input gain controller reduces switching noise for volume of a portable audio input.
5) Decrease the number of external components by built-in 2-band equalizer filter, LPF for subwoofer (BD37523FS), loudness filter. And, possible to control Q, Gv, fo of 2-band equalizer and fc(BD37523FS) of LPF, Gv of loudness by I^2C BUS control freely
6) It is possible for the bass, treble to the gain adjustment quantity of ±20dB and 1 dB step gain adjustment.
7) Terminals for the subwoofer outputs are equipped.
8) Bi-CMOS process is suitable for the design of low current and low energy. And it provides more quality for small scale regulator and heat in a set.
9) Package is SSOP-A24. Putting input-terminals together and output-terminals together can make PCB layout easier and can makes area of PCB smaller.
10) It is possible to control by 3.3V / 5V for I^2C BUS.

●Applications

It is the optimal for the car audio. Besides, it is possible to use for the audio equipment of mini Compo, micro Compo, TV etc with all kinds.

● **Line up matrix**

Function	BD37522FS	BD37523FS	Specifications
Input selector	○	○	・Stereo 4 input ・Differential 1 input
Input gain	○	○	・0～20dB（1dB step） ・Possible to use “Advanced switch” for prevention of switching noise.
Mute	○	○	・Possible to use “Advanced switch” for prevention of switching noise.
Volume	○	○	・+15dB～-79dB（1dB step）, -∞ ・Possible to use “Advanced switch” for prevention of switching noise.
Bass	○	○	・-20～+20dB（1dB step） ・Q=0.5, 1, 1.5, 2 variable ・fo=60, 80, 100, 120Hz ・Possible to use “Advanced switch” at changing gain
Treble	○	○	・-20～+20dB（1dB step） ・Q=0.75, 1.25 variable ・fo=7.5k, 10k, 12.5k, 15kHz ・Possible to use “Advanced switch” at changing gain
Fader	○	○	・+15dB～-79dB(1dB step), -∞dB(BD37522FS : 0dB～-79dB, -∞dB) ・Possible to use “Advanced switch” for prevention of switching noise.
Loudness	○	○	・0dB～20dB(1dB step) ・fo=800Hz ・Possible to use “Advanced switch” for prevention of switching noise.
LPF	×	○	・fc=55/85/120/160Hz, pass ・Phase shift (0°/180°)

●**Absolute maximum ratings** (Ta=25℃)

Item	Symbol	Rating	Unit
Power supply Voltage	VCC	10.0	V
Input voltage	Vin	VCC+0.3～GND-0.3	V
Power Dissipation	Pd	1000 ※1	mW
Storage Temperature	Tastg	-55～+150	℃

※This value decreases 8mW/℃ for Ta=25℃ or more.
ROHM standard board shall be mounted.
Thermal resistance θja = 125(℃/W)
ROHM Standard board
Size：70×70×1.6(㎜)
Material：A FR4 grass epoxy board(3% or less of copper foil area)

●**Operating conditions**

Item	Symbol	MIN	TYP	MAX	Unit
Power supply Voltage	VCC	7.0	－	9.5	V
Temperature	Topr	-40	－	+85	℃

●Electrical characteristics

(Unless specified particularly, Ta=25℃, VCC=8.5V, f=1kHz, Vin=1Vrms, Rg=600Ω, R_L=10kΩ, A1 input, Input gain 0dB, Mute off, Volume 0dB, Tone control 0dB, Loudness 0dB, LPF OFF(BD37523FS), Fader 0dB)

BLOCK	Item	Symbol	Limit			Unit	Condition
			Min.	Typ.	Max.		
GENERAL	Current upon no signal	I_Q	—	38	48	mA	No signal
	Voltage gain	G_V	-1.5	0	+1.5	dB	Gv=20log(VOUT/VIN)
	Channel balance	CB	-1.5	0	+1.5	dB	CB = GV1-GV2
	Total harmonic distortion 1 (FRONT,REAR)		—	0.001	0.05	%	VOUT=1Vrms BW=400-30KHz
	Total harmonic distortion 2 (SUBWOOFER) (BD37523FS)	THD+N2	—	0.002	0.05	%	VOUT=1Vrms BW=400-30KHz
	Output noise voltage 1 (FRONT,REAR) ∗	V_{NO1}	—	3.8	15	μVrms	Rg = 0Ω BW = IHF-A
	Output noise voltage 2 (SUBWOOFER) ∗ (BD37523FS)	V_{NO2}	—	4.8	15	μVrms	Rg = 0Ω BW = IHF-A
	Residual output noise voltage ∗	V_{NOR}	—	1.8	10	μVrms	Fader = -∞dB Rg = 0Ω BW = IHF-A
	Cross-talk between channels ∗	CTC	—	-100	-90	dB	Rg = 0Ω CTC=20log(VOUT/VIN) BW = IHF-A
	Ripple rejection	RR	—	-70	-40	dB	f=1kHz VRR=100mVrms RR=20log(VCC IN/VOUT)
INPUT SELECTOR	Input impedance(A, B)	R_{IN_S}	70	100	130	kΩ	
	Input impedance (C,D,E)	R_{IN_D}	175	250	325	kΩ	
	Maximum input voltage	V_{IM}	2.1	2.3	—	Vrms	VIM at THD+N(VOUT)=1% BW=400-30KHz
	Cross-talk between selectors ∗	CTS	—	-100	-90	dB	Rg = 0Ω CTS=20log(VOUT/VIN) BW = IHF-A
	Common mode rejection ratio ∗	CMRR	50	65	—	dB	CP1 and CN input CP2 and CN input CMRR=20log(VIN/VOUT) BW = IHF-A
INPUT GAIN	Minimum input gain	$G_{IN\ MIN}$	-2	0	+2	dB	Input gain 0dB VIN=100mVrms Gin=20log(VOUT/VIN)
	Maximum input gain	$G_{IN\ MAX}$	+18	+20	+22	dB	Input gain +20dB VIN=100mVrms Gin=20log(VOUT/VIN)
	Gain set error	$G_{IN\ ERR}$	-2	0	+2	dB	GAIN=+20～+1dB
MUTE	Mute attenuation ∗	G_{MUTE}	—	-105	-85	dB	Mute ON Gmute=20log(VOUT/VIN) BW = IHF-A
VOLUME	Maximum gain	$G_{V\ MAX}$	+13	+15	+17	dB	Volume = +15dB VIN=100mVrms Gv=20log(VOUT/VIN)
	Maximum attenuation ∗	$G_{V\ MIN}$	—	-100	-85	dB	Volume = -∞dB Gv=20log(VOUT/VIN) BW = IHF-A
	Attenuation set error 1	$G_{V\ ERR1}$	-2	0	+2	dB	GAIN & ATT=+15dB～-15dB
	Attenuation set error 2	$G_{V\ ERR2}$	-3	0	+3	dB	ATT=-16dB～-47dB
	Attenuation set error 3	$G_{V\ ERR3}$	-4	0	+4	dB	ATT=-48dB～-79dB

BLOCK	Item	Symbol	Limit			Unit	Condition
			Min.	Typ.	Max.		
BASS	Maximum boost gain	$G_{B\ BST}$	18	20	22	dB	Gain=+20dB f=100Hz VIN=100mVrms G_B=20log (VOUT/VIN)
	Maximum cut gain	$G_{B\ CUT}$	-22	-20	-18	dB	Gain=-20dB f=100Hz VIN=2Vrms G_B=20log (VOUT/VIN)
	Gain set error	$G_{B\ ERR}$	-2	0	2	dB	Gain=-20～+20dB f=100Hz
TREBLE	Maximum boost gain	$G_{T\ BST}$	17	20	23	dB	Gain=+20dB f=10kHz VIN=100mVrms G_T=20log (VOUT/VIN)
	Maximum cut gain	$G_{T\ CUT}$	-23	-20	-17	dB	Gain=-20dB f=10kHz VIN=2Vrms G_T=20log (VOUT/VIN)
	Gain set error	$G_{T\ ERR}$	-2	0	2	dB	Gain=-20～+20dB f=10kHz
FADER / SUBWOOFER	Maximum boost gain (BD37523FS)	$G_{F\ BST}$	+13	+15	+17	dB	Fader=+15dB V_{IN}=100mVrms G_F=20log(VOUT/VIN)
	Maximum attenuation *	$G_{F\ MIN}$	—	-100	-90	dB	Fader = -∞dB G_F=20log(VOUT/VIN) BW = IHF-A
	Gain set error (BD37523FS)	$G_{F\ ERR}$	-2	0	+2	dB	Gain=+15～+1dB
	Attenuation set error 1	$G_{F\ ERR1}$	-2	0	2	dB	ATT=-1～-15dB
	Attenuation set error 2	$G_{F\ ERR2}$	-3	0	3	dB	ATT=-16～-47dB
	Attenuation set error 3	$G_{F\ ERR3}$	-4	0	4	dB	ATT=-48～-79dB
	Output impedance	R_{OUT}	-	—	50	Ω	VIN=100mVrms
	Maximum output voltage	V_{OM}	2	2.2	—	Vrms	THD+N=1% BW=400-30KHz
LOUDNESS	Maximum gain	$G_{L\ MAX}$	17	20	23	dB	Gain 20dB VIN=100mVrms G_L=20log(VOUT/VIN)
	Gain set error	$G_{L\ ERR}$	-2	0	2	dB	GAIN=+20～+1dB

VP-9690A(Average value detection, effective value display) filter by Matsushita Communication is used for * measurement.
Phase between input / output is same.

●Electrical characteristic curves (Reference data)

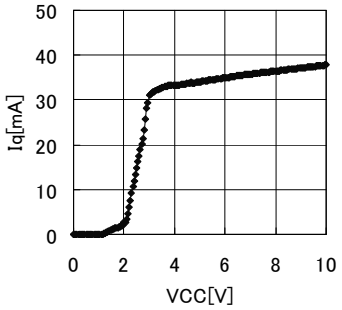


Fig.1 Iq vs Vcc

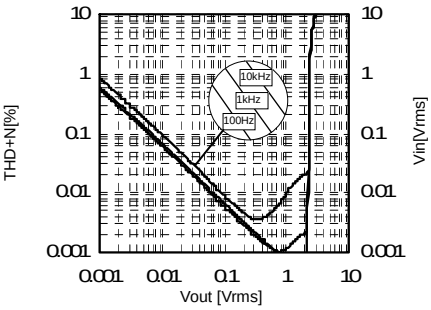


Fig.2 Thd vs Vo

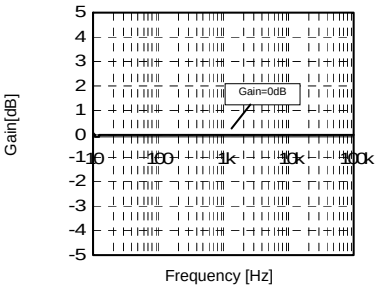


Fig.3 Gain vs Freq

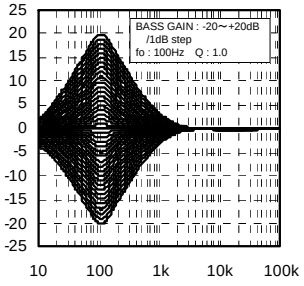


Fig.4 Bass Gain vs Freq

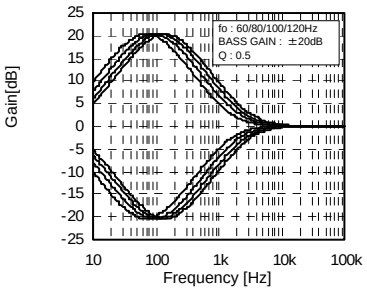


Fig.5 Bass fo vs Freq

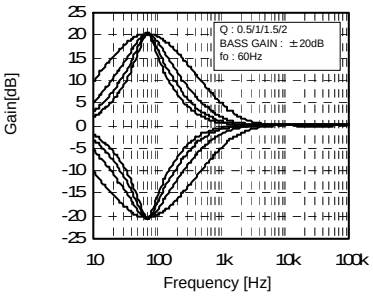


Fig.6 Bass Q vs Freq

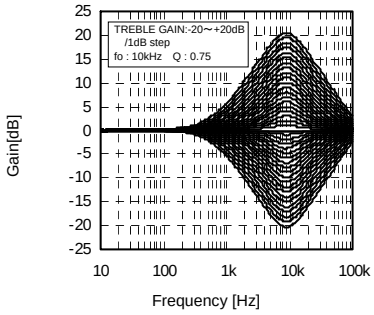


Fig.7 Treble Gain vs Freq

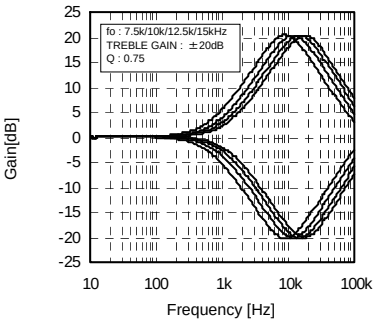


Fig.8 Treble fo vs Freq

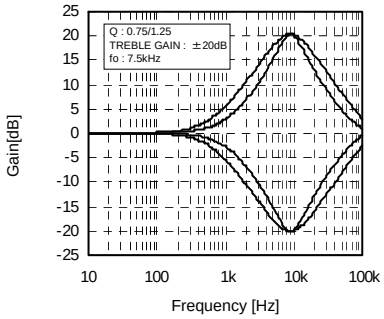


Fig.9Treble Q vs Freq

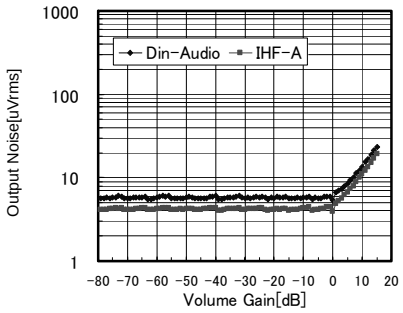


Fig.10 Volume Gain vs Noise

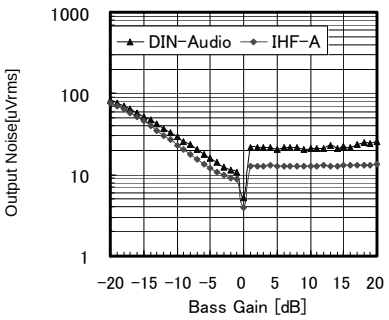


Fig.11 Bass Gain vs Noise

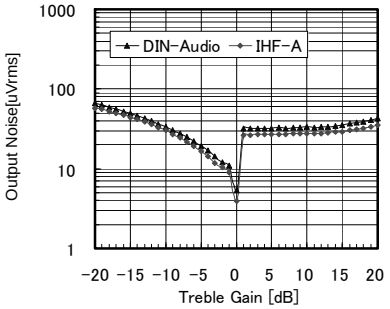


Fig.12 Treble Gain vs Noise

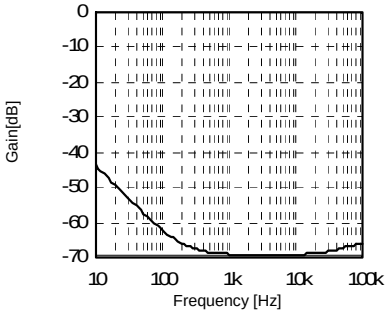


Fig.13 CMRR vs Freq

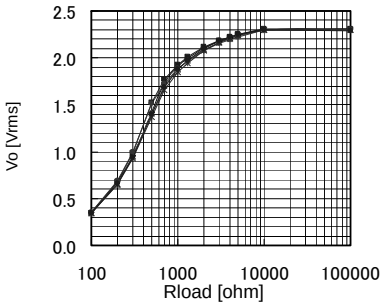


Fig.14 Rload vs Vo

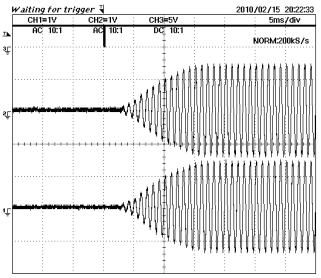


Fig.15 Advanced Switch 1

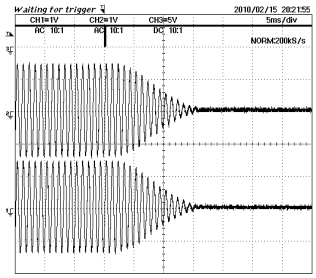


Fig.16Advanced Switch 2

●Block diagram and pin configuration

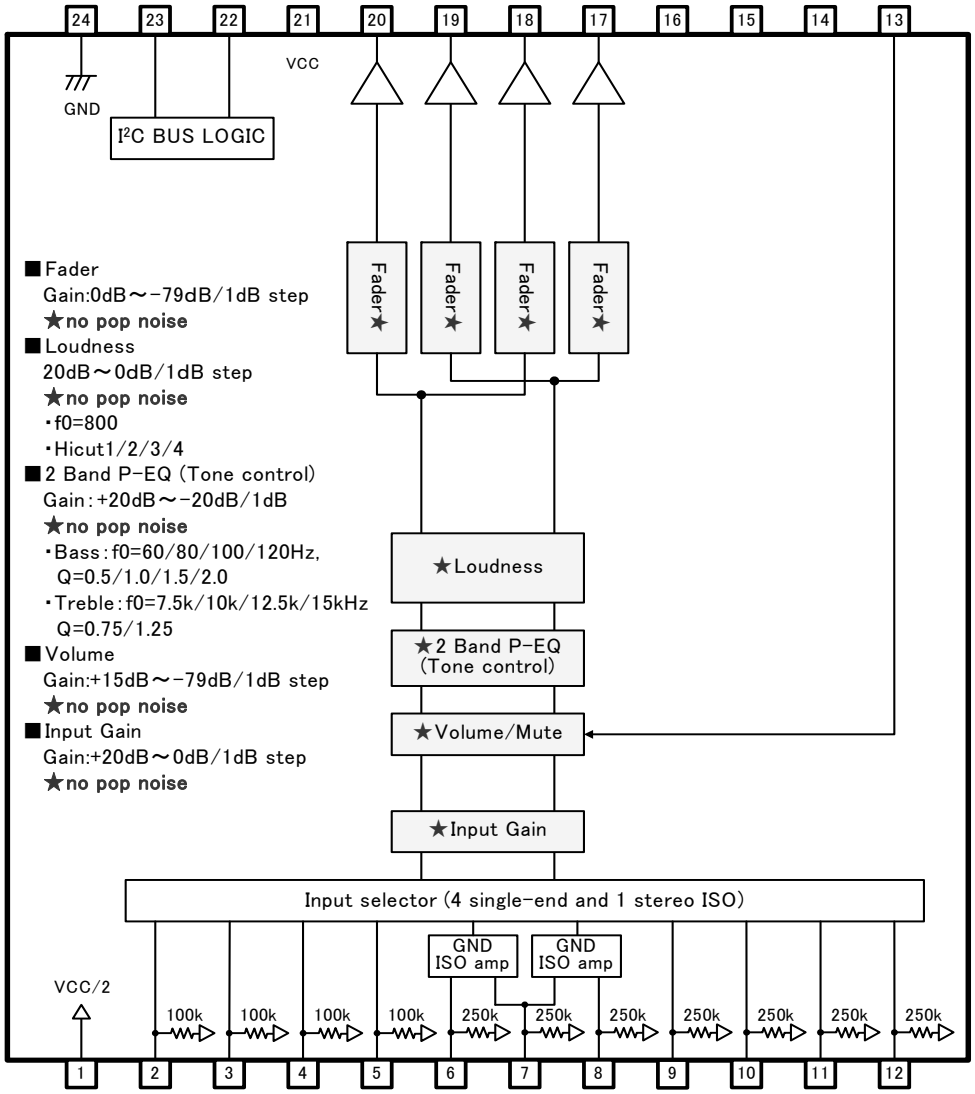


Fig.17 BD37522FS

Descriptions of terminal

Terminal No.	Terminal Name	Description	Terminal No.	Terminal Name	Description
1	FIL	VCC/2 terminal	13	MUTE	External compulsory mute terminal
2	A1	A input terminal of 1ch	14	TEST1	Test Pin
3	A2	A input terminal of 2ch	15	TEST2	Test Pin
4	B1	B input terminal of 1ch	16	TEST3	Test Pin
5	B2	B input terminal of 2ch	17	OUTR2	Rear output terminal of 2ch
6	CP1	C positive input terminal of 1ch	18	OUTR1	Rear output terminal of 1ch
7	CN	C negative input terminal	19	OUTF2	Front output terminal of 2ch
8	CP2	C positive input terminal of 2ch	20	OUTF1	Front output terminal of 1ch
9	D1	D input terminal of 1ch	21	VCC	Power supply terminal
10	D2	D input terminal of 2ch	22	SCL	I^2C Communication clock terminal
11	E1	E input terminal of 1ch	23	SDA	I^2C Communication data terminal
12	E2	E input terminal of 2ch	24	GND	GND terminal

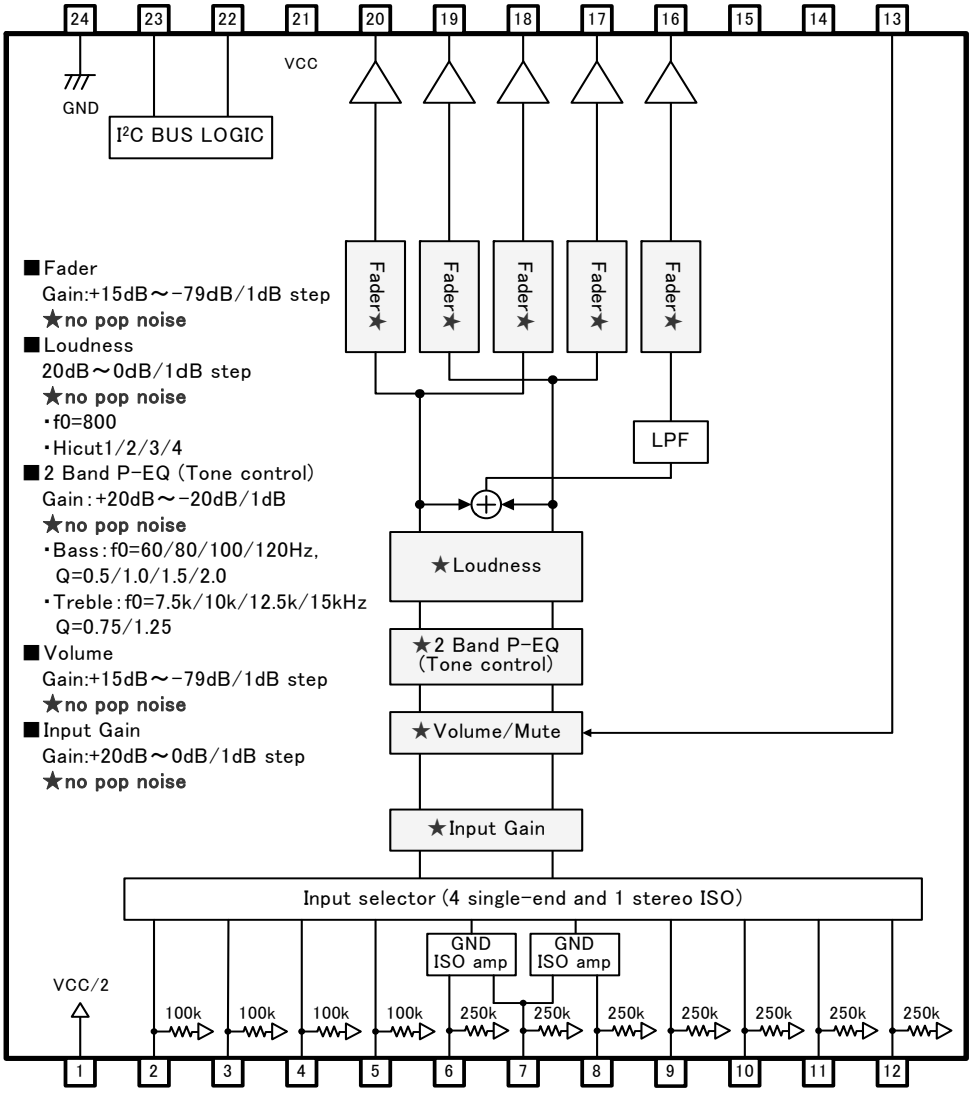


Fig.18 BD37523FS

Descriptions of terminal

Terminal No.	Terminal Name	Description	Terminal No.	Terminal Name	Description
1	FIL	VCC/2 terminal	13	MUTE	External compulsory mute terminal
2	A1	A input terminal of 1ch	14	TEST1	Test Pin
3	A2	A input terminal of 2ch	15	TEST2	Test Pin
4	B1	B input terminal of 1ch	16	OUTS	Subwoofer output terminal
5	B2	B input terminal of 2ch	17	OUTR2	Rear output terminal of 2ch
6	CP1	C positive input terminal of 1ch	18	OUTR1	Rear output terminal of 1ch
7	CN	C negative input terminal	19	OUTF2	Front output terminal of 2ch
8	CP2	C positive input terminal of 2ch	20	OUTF1	Front output terminal of 1ch
9	D1	D input terminal of 1ch	21	VCC	Power supply terminal
10	D2	D input terminal of 2ch	22	SCL	I^2C Communication clock terminal
11	E1	E input terminal of 1ch	23	SDA	I^2C Communication data terminal
12	E2	E input terminal of 2ch	24	GND	GND terminal

●**Timming Chart**

CONTROL SIGNAL SPECIFICATION

(1) Electrical specifications and timing for bus lines and I/O stages

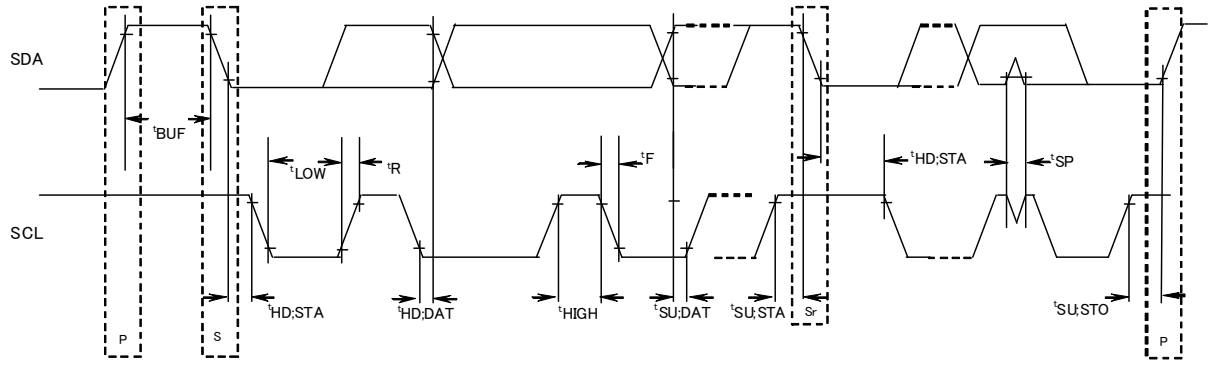


Fig.19 Definition of timing on the I²C-bus

Table 1 Characteristics of the SDA and SCL bus lines for I²C-bus devices
(Unless specified particularly, Ta=25℃, VCC=8.5V)

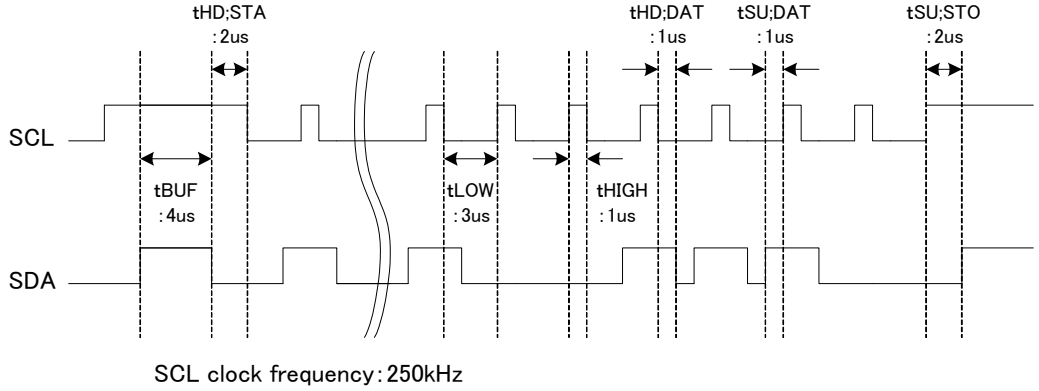
	Parameter	Symbol	Fast-mode I²C-bus		Unit
			Min.	Max.	
1	SCL clock frequency	f SCL	0	400	kHz
2	Bus free time between a STOP and START condition	tBUF	1.3	—	μS
3	Hold time (repeated) START condition. After this period, the first clock pulse is generated	tHD;STA	0.6	—	μS
4	LOW period of the SCL clock	tLOW	1.3	—	μS
5	HIGH period of the SCL clock	tHIGH	0.6	—	μS
6	Set-up time for a repeated START condition	tSU;STA	0.6	—	μS
7	Data hold time:	tHD;DAT	0.06*	—	μS
8	Data set-up time	tSU;DAT	120	—	ns
9	Set-up time for STOP condition	tSU;STO	0.6	—	μS

All values referred to VIH min. and VIL max. Levels (see Table 2).

* A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIH min. of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
About 7(tHD;DAT), 8(tSU;DAT), make it the setup which a margin is fully in .

Table 2 Characteristics of the SDA and SCL I/O stages for I^2C-bus devices

	Parameter	Symbol	Fast-mode devices		Unit
			Min.	Max.	
10	LOW level input voltage:	VIL	-0.3	1	V
11	HIGH level input voltage:	VIH	2.3	5	V
12	Pulse width of spikes which must be suppressed by the input filter.	tSP	0	50	ns
13	LOW level output voltage: at 3mA sink current	VOL1	0	0.4	V
14	Input current each I/O pin with an input voltage between 0.4V and 4.5V.	Ii	-10	10	μA



SCL clock frequency:250kHz

Fig.20 A command timing example in the I2C data transmission

（２）I²C BUS FORMAT

	MSB LSB		MSB LSB		MSB LSB		
S	Slave Address	A	Select Address	A	Data	A	P
1bit	8bit	1bit	8bit	1bit	8bit	1bit	1bit

S = Start conditions (Recognition of start bit)
Slave Address = Recognition of slave address. 7 bits in upper order are voluntary. The least significant bit is “L” due to writing.
A = ACKNOWLEDGE bit (Recognition of acknowledgement)
Select Address = Select every of volume, bass and treble.
Data = Data on every volume and tone.
P = Stop condition (Recognition of stop bit)

（３）I²C BUS Interface Protocol

1) Basic form

S	Slave Address	A	Select Address	A	Data	A	P
	MSB LSB		MSB LSB		MSB LSB		

2) Automatic increment (Select Address increases (+1) according to the number of data.

S	Slave Address	A	Select Address	A	Data1	A	Data2	A	····	DataN	A	P
	MSB LSB		MSB LSB		MSB LSB		MSB LSB			MSB LSB		

(Example) ①Data1 shall be set as data of address specified by Select Address.
②Data2 shall be set as data of address specified by Select Address +1.
③DataN shall be set as data of address specified by Select Address +N-1.

3) Configuration unavailable for transmission (In this case, only Select Address1 is set.

S	Slave Address	A	Select Address1	A	Data	A	Select Address 2	A	Data	A	P
	MSB LSB		MSB LSB		MSB LSB		MSB LSB		MSB LSB		

(Note) If any data is transmitted as Select Address 2 next to data, it is recognized as data, not as Select Address 2.

（４）Slave address

MSB							LSB	
A6	A5	A4	A3	A2	A1	A0	R/W	
1	0	0	0	0	0	0	0	80H

（5）Select Address & Data

BD37522FS

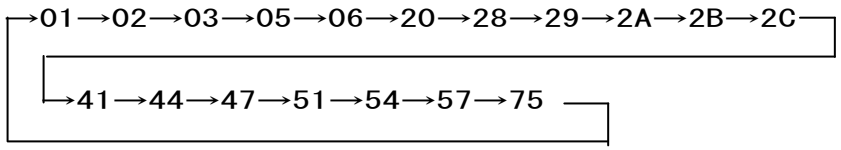
Items	Select Address (hex)	MSB Data LSB							
		D7	D6	D5	D4	D3	D2	D1	D0
Initial setup 1	01	Advanced switch ON/OFF	0	Advanced switch time of Input Gain/Volume Tone/Fader/Loudness		0	0	Advanced switch time of Mute	
Initial setup 2	02	0	0	0	0	0	0	0	0
Initial setup 3	03	0	0	0	1	0	0	0	1
Input Selector	05	0	0	0	Input selector				
Input gain	06	Mute ON/OFF	0	0	Input Gain				
Volume gain	20	Volume / Attenuation							
Fader 1ch Front	28	Fader Attenuation							
Fader 2ch Front	29	Fader Attenuation							
Fader 1ch Rear	2A	Fader Attenuation							
Fader 2ch Rear	2B	Fader Attenuation							
Test mode 1	2C	1	1	1	1	1	1	1	1
Bass setup	41	0	0	Bass fo		0	0	Bass Q	
Test mode 2	44	0	0	0	0	0	0	0	0
Treble setup	47	0	0	Treble fo		0	0	0	Treble Q
Bass gain	51	Bass Boost/ Cut	0	0	Bass Gain				
Test mode 3	54	0	0	0	0	0	0	0	0
Treble gain	57	Treble Boost/ Cut	0	0	Treble Gain				
Loudness Gain	75	0	Loudness Hicut		Loudness Gain				
System Reset	FE	1	0	0	0	0	0	0	1

Advanced switch

Note

1. In function changing of the hatching part, it works Advanced switch.

2. Upon continuous data transfer, the Select Address is circulated by the automatic increment function, as shown below.



3. For the function of input selector etc, it is not corresponded for advanced switch. Therefore, please apply mute on the side of a set when changes these setting.

4. When using mute function of this IC at the time of changing input selector, please switch mute ON/OFF for waiting advanced-mute time.

BD37523FS

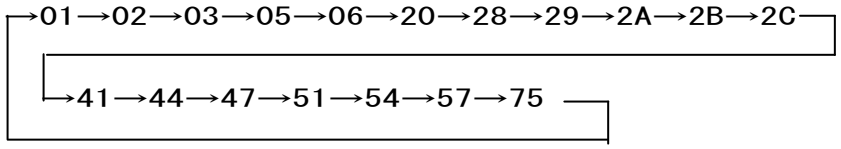
Items	Select Address (hex)	MSB Data LSB							
		D7	D6	D5	D4	D3	D2	D1	D0
Initial setup 1	01	Advanced switch ON/OFF	0	Advanced switch time of Input Gain/Volume Tone/Fader/Loudness		0	0	Advanced switch time of Mute	
Initial setup 2	02	LPF Phase	0	0	0	0	Subwoofer LPF fc		
Initial setup 3	03	0	0	0	1	0	0	0	1
Input Selector	05	0	0	0	Input selector				
Input gain	06	Mute ON/OFF	0	0	Input Gain				
Volume gain	20	Volume Gain / Attenuation							
Fader 1ch Front	28	Fader Gain / Attenuation							
Fader 2ch Front	29	Fader Gain / Attenuation							
Fader 1ch Rear	2A	Fader Gain / Attenuation							
Fader 2ch Rear	2B	Fader Gain / Attenuation							
Fader Subwoofer	2C	Fader Gain / Attenuation							
Bass setup	41	0	0	Bass fo		0	0	Bass Q	
Test mode 1	44	0	0	0	0	0	0	0	0
Treble setup	47	0	0	Treble fo		0	0	0	Treble Q
Bass gain	51	Bass Boost/ Cut	0	0	Bass Gain				
Test mode 2	54	0	0	0	0	0	0	0	0
Treble gain	57	Treble Boost/ Cut	0	0	Treble Gain				
Loudness Gain	75	0	Loudness Hicut		Loudness Gain				
System Reset	FE	1	0	0	0	0	0	0	1

Advanced switch

Note

1. In function changing of the hatching part, it works Advanced switch.

2. Upon continuous data transfer, the Select Address is circulated by the automatic increment function, as shown below.



3. For the function of input selector etc, it is not corresponded for advanced switch. Therefore, please apply mute on the side of a set when changes these setting.

4. When using mute function of this IC at the time of changing input selector, please switch mute ON/OFF for waiting advanced-mute time.

Select address 01 (hex)

Time	MSB Advanced switch time of Mute LSB							
	D7	D6	D5	D4	D3	D2	D1	D0
0.6msec	Advanced Switch ON/OFF	0	Advanced switch time of Input gain/Volume Tone/Fader/Loudness		0	0	0	0
1.0msec							0	1
1.4msec							1	0
3.2msec							1	1

Time	MSB Advanced switch time of Input gain/Volume/Tone/Fader/Loudness LSB							
	D7	D6	D5	D4	D3	D2	D1	D0
4.7 msec	Advanced Switch ON/OFF	0	0	0	0	0	Advanced switch Time of Mute	
7.1 msec			0	1				
11.2 msec			1	0				
14.4 msec			1	1				

Mode	MSB Advanced switch ON/OFF LSB							
	D7	D6	D5	D4	D3	D2	D1	D0
OFF	0	0	Advanced switch time of Input gain/Volume Tone/Fader/Loudness		0	0	Advanced switch Time of Mute	
ON	1							

Select address 02(hex)

fc	MSB Subwoofer LPF fc LSB							
	D7	D6	D5	D4	D3	D2	D1	D0
OFF	LPF Phase	0	0	0	0	0	0	0
55Hz						0	0	1
85Hz						0	1	0
120Hz						0	1	1
160Hz						1	0	0
Prohibition						Other setting		

(Available only BD37523FS)

Phase	MSB LPF Phase LSB							
	D7	D6	D5	D4	D3	D2	D1	D0
0°	0	0	0	0	0	Subwoofer LPF fc		
180°	1							

(Available only BD37523FS)

Select address 05(hex)

Mode	OUT F1/R1	OUT F2/R2	MSB Input Selector LSB							
			D7	D6	D5	D4	D3	D2	D1	D0
A	A1	A2	0	0	0	0	0	0	0	1
B	B1	B2					0	0	1	0
C diff	CP1	CP2					0	1	1	0
D	D1	D2					1	0	1	0
E	E1	E2					1	0	1	1
Input SHORT							1	0	0	1
Prohibition							Other setting			

Input SHORT : The input impedance of each input terminal is lowered from 100kΩ(TYP) to 6 kΩ(TYP).
(For quick charge of coupling capacitor)

: Initial condition

Select address 06 (hex)

Gain	MSB Input Gain LSB							
	D7	D6	D5	D4	D3	D2	D1	D0
0dB	Mute ON/OFF	0	0	0	0	0	0	0
1dB				0	0	0	0	1
2dB				0	0	0	1	0
3dB				0	0	0	1	1
4dB				0	0	1	0	0
5dB				0	0	1	0	1
6dB				0	0	1	1	0
7dB				0	0	1	1	1
8dB				0	1	0	0	0
9dB				0	1	0	0	1
10dB				0	1	0	1	0
11dB				0	1	0	1	1
12dB				0	1	1	0	0
13dB				0	1	1	0	1
14dB				0	1	1	1	0
15dB				0	1	1	1	1
16dB				1	0	0	0	0
17dB				1	0	0	0	1
18dB				1	0	0	1	0
19dB				1	0	0	1	1
20dB				1	0	1	0	0
Prohibition				1	1	0	1	1
				:	:	:	:	:
				1	1	1	1	1

Mode	MSB Mute ON/OFF LSB							
	D7	D6	D5	D4	D3	D2	D1	D0
OFF	0	0	0	Input Gain				
ON	1							

Select address 20, 28, 29, 2A, 2B, 2C (hex)

Gain & ATT	MSB Vol, Fader Gain / Attenuation LSB							
	D7	D6	D5	D4	D3	D2	D1	D0
Prohibition	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	1
	:	:	:	:	:	:	:	:
	0	1	1	1	0	0	0	0
15dB	0	1	1	1	0	0	0	1
14dB	0	1	1	1	0	0	1	0
13dB	0	1	1	1	0	0	1	1
:	:	:	:	:	:	:	:	:
-77dB	1	1	0	0	1	1	0	1
-78dB	1	1	0	0	1	1	1	0
-79dB	1	1	0	0	1	1	1	1
Prohibition	1	1	0	1	0	0	0	0
	:	:	:	:	:	:	:	:
	1	1	1	1	1	1	1	0
-∞dB	1	1	1	1	1	1	1	1

(About BD37522FS, only 0dB～-∞dB are available at address 28, 29, 2A, 2B)

: Initial condition

Select address 41(hex)

Q factor	MSB		Bass Q factor					LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0.5	0	0	Bass fo		0	0	0	0
1.0							0	1
1.5							1	0
2.0							1	1

fo	MSB		Bass fo				LSB	
	D7	D6	D5	D4	D3	D2	D1	D0
60Hz	0	0	0	0	0	0	Bass Q factor	
80Hz			0	1				
100Hz			1	0				
120Hz			1	1				

Select address 47 (hex)

Q factor	MSB		Treble Q factor					LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0.75	0	0	Treble fo		0	0	0	0
1.25								1

fo	MSB		Treble fo					LSB
	D7	D6	D5	D4	D3	D2	D1	D0
7.5kHz	0	0	0	0	0	0	0	Treble Q factor
10kHz			0	1				
12.5kHz			1	0				
15kHz			1	1				

: Initial condition

Select address 51, 57 (hex)

Gain	MSB Bass/ Treble Gain LSB							
	D7	D6	D5	D4	D3	D2	D1	D0
0dB	Bass/ Treble Boost /cut	0	0	0	0	0	0	0
1dB				0	0	0	0	1
2dB				0	0	0	1	0
3dB				0	0	0	1	1
4dB				0	0	1	0	0
5dB				0	0	1	0	1
6dB				0	0	1	1	0
7dB				0	0	1	1	1
8dB				0	1	0	0	0
9dB				0	1	0	0	1
10dB				0	1	0	1	0
11dB				0	1	0	1	1
12dB				0	1	1	0	0
13dB				0	1	1	0	1
14dB				0	1	1	1	0
15dB				0	1	1	1	1
16dB				1	0	0	0	0
17dB				1	0	0	0	1
18dB				1	0	0	1	0
19dB				1	0	0	1	1
20dB				1	0	1	0	0
Prohibition				1	0	1	0	1
				:	:	:	:	:
				1	1	1	1	0
				1	1	1	1	1

Mode	MSB Bass/ Treble Boost/Cut LSB							
	D7	D6	D5	D4	D3	D2	D1	D0
Boost	0	0	0	Bass/Treble Gain				
Cut	1							

: Initial condition

Select address 75 (hex)

Mode	MSB			Loudness Hicut				LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Hicut1	0	0	0	Loudness Gain				
Hicut2		0	1					
Hicut3		1	0					
Hicut4		1	1					

Gain	MSB			Loudness Gain				LSB
	D7	D6	D5	D4	D3	D2	D1	D0
0dB	0	Loudness Hicut		0	0	0	0	0
1dB				0	0	0	0	1
2dB				0	0	0	1	0
3dB				0	0	0	1	1
4dB				0	0	1	0	0
5dB				0	0	1	0	1
6dB				0	0	1	1	0
7dB				0	0	1	1	1
8dB				0	1	0	0	0
9dB				0	1	0	0	1
10dB				0	1	0	1	0
11dB				0	1	0	1	1
12dB				0	1	1	0	0
13dB				0	1	1	0	1
14dB				0	1	1	1	0
15dB				0	1	1	1	1
16dB				1	0	0	0	0
17dB				1	0	0	0	1
18dB				1	0	0	1	0
19dB				1	0	0	1	1
20dB				1	0	1	0	0
Prohibition				1	0	1	0	1
				:	:	:	:	:
				1	1	1	1	1

: Initial condition

(6) About power on reset

At on of supply voltage circuit made initialization inside IC is built-in. Please send data to all address as initial data at supply voltage on. And please supply mute at set side until this initial data is sent.

Item	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Rise time of VCC	Trise	33	—	—	usec	VCC rise time from 0V to 5V
VCC voltage of release power on reset	Vpor	—	4.1	—	V	

(7) About external compulsory mute terminal

Mute is possible forcibly than the outside after input again department, by the setting of the MUTE terminal.

Mute Voltage Condition	Mode
GND～1.0V	MUTE ON
2.3V～VCC	MUTE OFF

Establish the voltage of MUTE in the condition to have been defined.

Volume / Fader volume attenuation of the details

(dB)	D7	D6	D5	D4	D3	D2	D1	D0		(dB)	D7	D6	D5	D4	D3	D2	D1	D0
+15	0	1	1	1	0	0	0	1		-33	1	0	1	0	0	0	0	1
+14	0	1	1	1	0	0	1	0		-34	1	0	1	0	0	0	1	0
+13	0	1	1	1	0	0	1	1		-35	1	0	1	0	0	0	1	1
+12	0	1	1	1	0	1	0	0		-36	1	0	1	0	0	1	0	0
+11	0	1	1	1	0	1	0	1		-37	1	0	1	0	0	1	0	1
+10	0	1	1	1	0	1	1	0		-38	1	0	1	0	0	1	1	0
+9	0	1	1	1	0	1	1	1		-39	1	0	1	0	0	1	1	1
+8	0	1	1	1	1	0	0	0		-40	1	0	1	0	1	0	0	0
+7	0	1	1	1	1	0	0	1		-41	1	0	1	0	1	0	0	1
+6	0	1	1	1	1	0	1	0		-42	1	0	1	0	1	0	1	0
+5	0	1	1	1	1	0	1	1		-43	1	0	1	0	1	0	1	1
+4	0	1	1	1	1	1	0	0		-44	1	0	1	0	1	1	0	0
+3	0	1	1	1	1	1	0	1		-45	1	0	1	0	1	1	0	1
+2	0	1	1	1	1	1	1	0		-46	1	0	1	0	1	1	1	0
+1	0	1	1	1	1	1	1	1		-47	1	0	1	0	1	1	1	1
0	1	0	0	0	0	0	0	0		-48	1	0	1	1	0	0	0	0
-1	1	0	0	0	0	0	0	1		-49	1	0	1	1	0	0	0	1
-2	1	0	0	0	0	0	1	0		-50	1	0	1	1	0	0	1	0
-3	1	0	0	0	0	0	1	1		-51	1	0	1	1	0	0	1	1
-4	1	0	0	0	0	1	0	0		-52	1	0	1	1	0	1	0	0
-5	1	0	0	0	0	1	0	1		-53	1	0	1	1	0	1	0	1
-6	1	0	0	0	0	1	1	0		-54	1	0	1	1	0	1	1	0
-7	1	0	0	0	0	1	1	1		-55	1	0	1	1	0	1	1	1
-8	1	0	0	0	1	0	0	0		-56	1	0	1	1	1	0	0	0
-9	1	0	0	0	1	0	0	1		-57	1	0	1	1	1	0	0	1
-10	1	0	0	0	1	0	1	0		-58	1	0	1	1	1	0	1	0
-11	1	0	0	0	1	0	1	1		-59	1	0	1	1	1	0	1	1
-12	1	0	0	0	1	1	0	0		-60	1	0	1	1	1	1	0	0
-13	1	0	0	0	1	1	0	1		-61	1	0	1	1	1	1	0	1
-14	1	0	0	0	1	1	1	0		-62	1	0	1	1	1	1	1	0
-15	1	0	0	0	1	1	1	1		-63	1	0	1	1	1	1	1	1
-16	1	0	0	1	0	0	0	0		-64	1	1	0	0	0	0	0	0
-17	1	0	0	1	0	0	0	1		-65	1	1	0	0	0	0	0	1
-18	1	0	0	1	0	0	1	0		-66	1	1	0	0	0	0	1	0
-19	1	0	0	1	0	0	1	1		-67	1	1	0	0	0	0	1	1
-20	1	0	0	1	0	1	0	0		-68	1	1	0	0	0	1	0	0
-21	1	0	0	1	0	1	0	1		-69	1	1	0	0	0	1	0	1
-22	1	0	0	1	0	1	1	0		-70	1	1	0	0	0	1	1	0
-23	1	0	0	1	0	1	1	1		-71	1	1	0	0	0	1	1	1
-24	1	0	0	1	1	0	0	0		-72	1	1	0	0	1	0	0	0
-25	1	0	0	1	1	0	0	1		-73	1	1	0	0	1	0	0	1
-26	1	0	0	1	1	0	1	0		-74	1	1	0	0	1	0	1	0
-27	1	0	0	1	1	0	1	1		-75	1	1	0	0	1	0	1	1
-28	1	0	0	1	1	1	0	0		-76	1	1	0	0	1	1	0	0
-29	1	0	0	1	1	1	0	1		-77	1	1	0	0	1	1	0	1
-30	1	0	0	1	1	1	1	0		-78	1	1	0	0	1	1	1	0
-31	1	0	0	1	1	1	1	1		-79	1	1	0	0	1	1	1	1
-32	1	0	1	0	0	0	0	0		-∞	1	1	1	1	1	1	1	1

About BD37522FS, Fader Volume only 0dB～-∞dB are available.

: Initial condition

●**Application circuit**

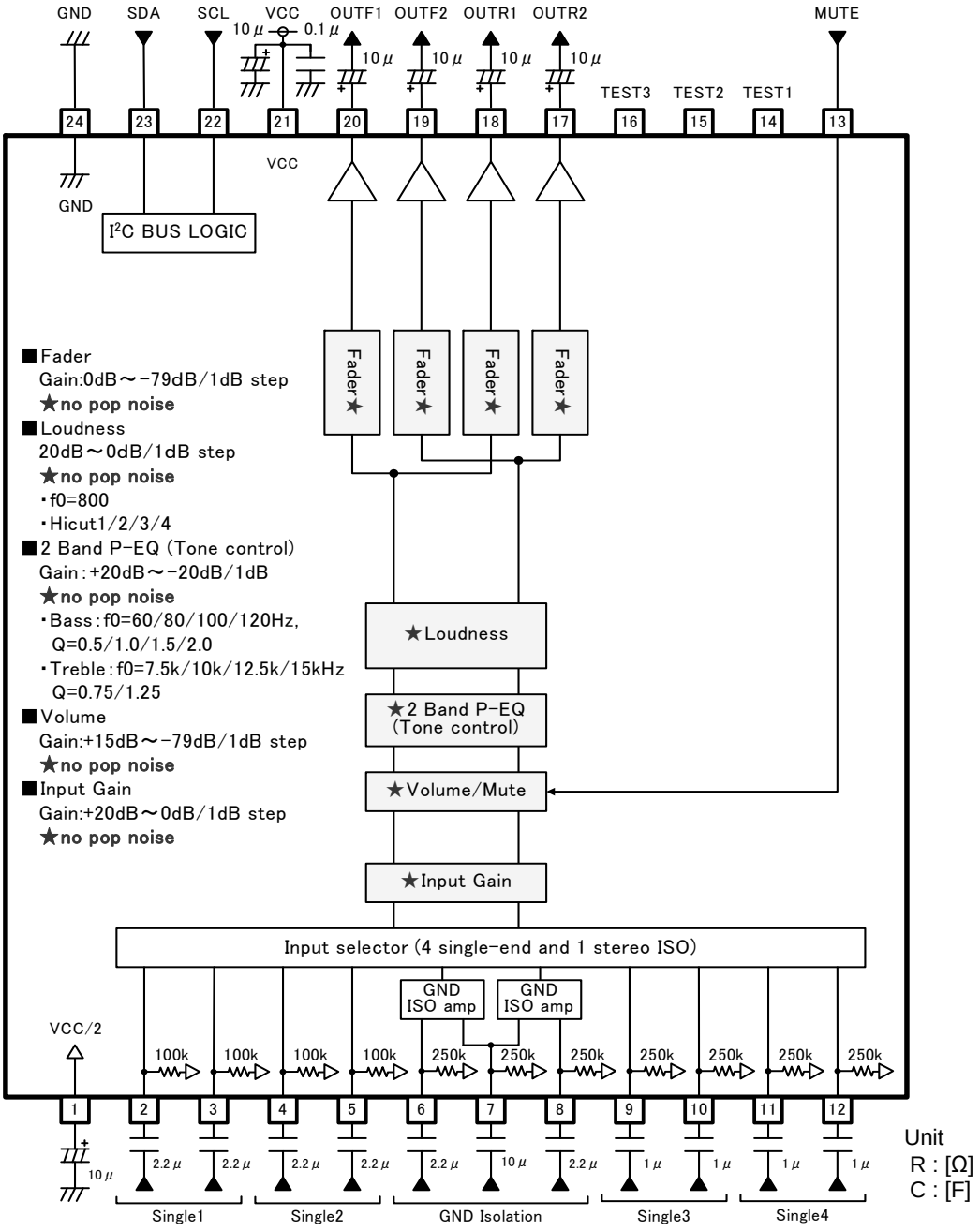


Fig.21 BD37522FS

Notes on wiring

① Please connect the decoupling capacitor of a power supply in the shortest distance as much as possible to GND.
② Lines of GND shall be one-point connected.
③ Wiring pattern of Digital shall be away from that of analog unit and cross-talk shall not be acceptable.
④ ILines of SCL and SDA of I²C BUS shall not be parallel if possible.
The lines shall be shielded, if they are adjacent to each other.
⑤ Lines of analog input shall not be parallel if possible. The lines shall be shielded, if they are adjacent to each other.
⑥ About TEST pin(14,15,16pin), please use with OPEN.

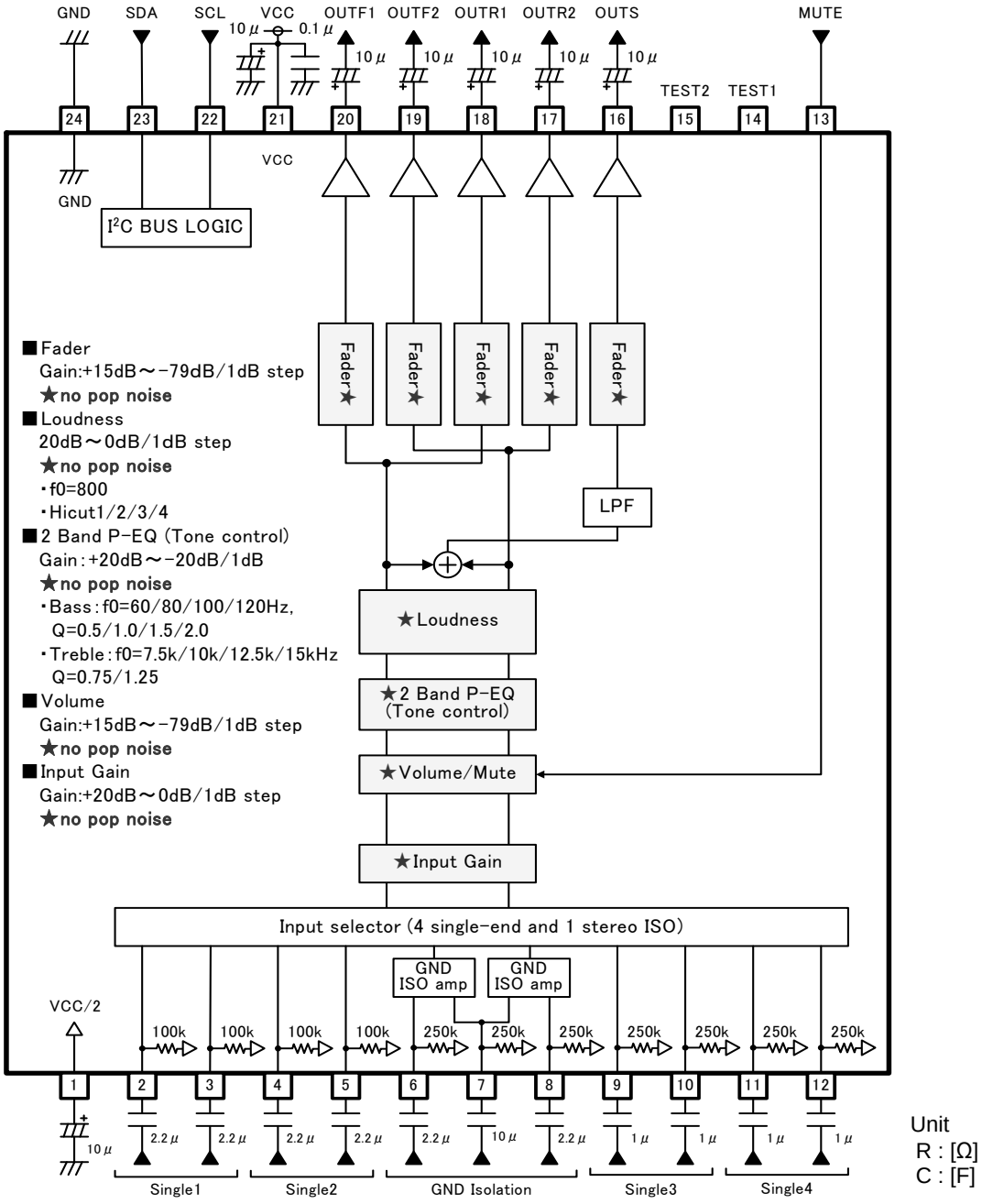


Fig.22 BD37523FS

Notes on wiring

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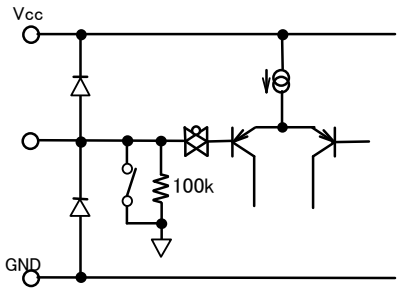
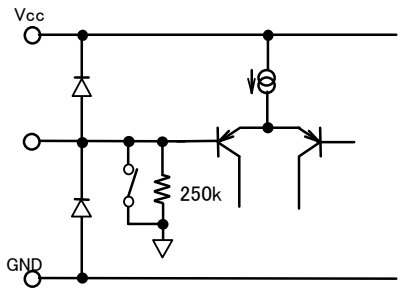
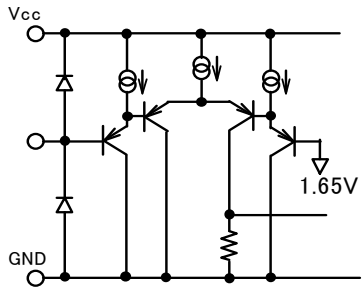
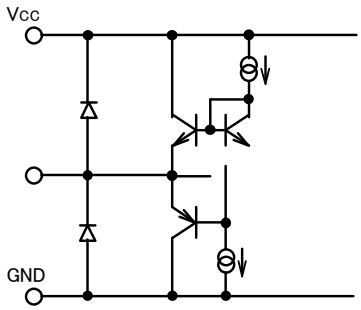
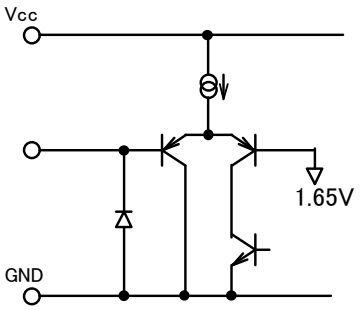
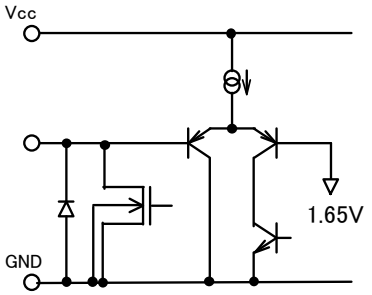
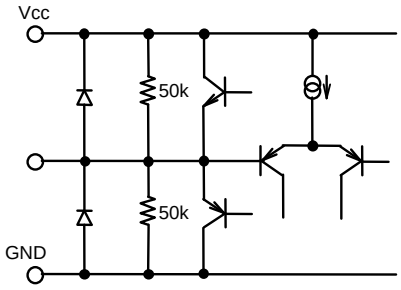
●**Interfaces**

Terminal No.	Terminal Name	Terminal Voltage	Equivalent Circuit	Terminal Description
2 3 4 5	A1 A2 B1 B2	4.25		A terminal for signal input. The input impedance is 100kΩ(typ).
6 7 8 9 10 11 12	CP1 CN CP2 D1 D2 E1 E2	4.25		A terminal for signal input. The input impedance is 250kΩ(typ).
13	MUTE	—		A terminal for external compulsory mute. If terminal voltage is High level, the mute is off. And if the terminal voltage is Low level, the mute is on.
16 17 18 19 20	OUTS OUTR2 OUTR1 OUTF2 OUTF1	4.25		A terminal for fader and Subwoofer output. (16pin:OUTS is only in BD37523FS,)

The figure in the pin explanation and input/output equivalent circuit is reference value, it doesn't guarantee the value.

Terminal No.	Terminal Name	Terminal Voltage	Equivalent Circuit	Terminal Description
21	VCC	8.5		Power supply terminal.
22	SCL	—		A terminal for clock input of I²C BUS communication.
23	SDA	—		A terminal for data input of I²C BUS communication.
24	GND	0		Ground terminal.
1	FIL	4.25		Voltage for reference bias of analog signal system. The simple precharge circuit and simple discharge circuit for an external capacitor are built in.
14 15 16	TEST	-		TEST terminal About BD37522FS, 14,15,16pin are TEST Pin. About BD37523FS, 14,15pin are TEST Pin.

The figure in the pin explanation and input/output equivalent circuit is reference value, it doesn't guarantee the value.

●Notes for use

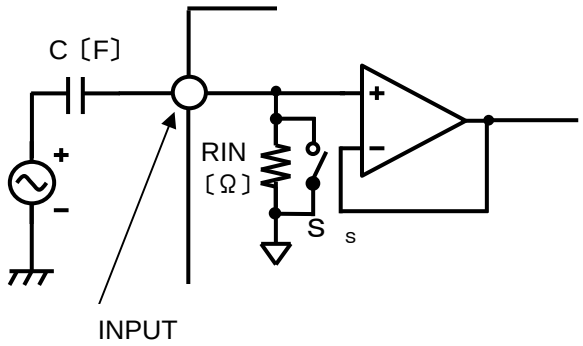
1. Absolute maximum rating voltage

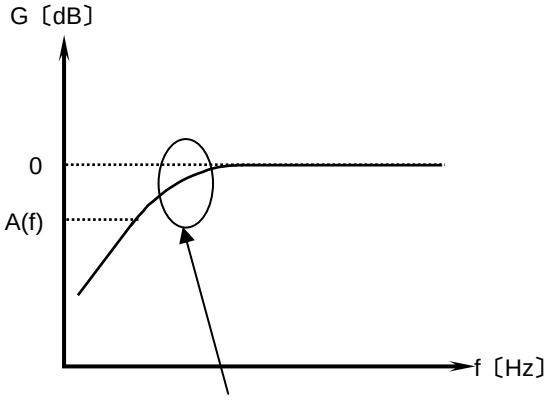
When it impressed the voltage on VCC more than the absolute maximum rating voltage, circuit currents increase rapidly, and there is absolutely a case to reach characteristic deterioration and destruction of a device. In particular in a serge examination of a set, when it is expected the impressing serge at VCC terminal (21pin), please do not impress the large and over the absolute maximum rating voltage (including a operating voltage + serge ingredient (around 14V)).

2. About a signal input part

1) About constant set up of input coupling capacitor

In the signal input terminal, the constant setting of input coupling capacitor C(F) be sufficient input impedance R_{IN}(Ω) inside IC and please decide. The first HPF characteristic of RC is composed.





$$A(f) = \sqrt{\frac{(2\pi fCR_{IN})^2}{1+(2\pi fCR_{IN})^2}}$$

2) About the input selector SHORT

SHORT mode is the command which makes switch S_{SH} =ON an input selector part and input impedance RIN of all terminals, and makes resistance small. Switch S_{SH} is OFF when not choosing a SHORT command.
A constant time becomes small at the time of this command twisting to the resistance inside the capacitor connected outside and LSI. The charge time of a capacitor becomes short. Since SHORT mode turns ON the switch of S_{SH} and makes it low impedance, please use it at the time of a non-signal.

3. About Mute terminal(13pin) when power supply is off

Any voltage shall not be supplied to Mute terminal (13pin) when power-supply is off.
Please insert a resistor (about 2.2kΩ) to Mute terminal in series, if voltage is supplied to mute terminal in case. (Please refer Application Circuit Diagram.)

4. About TEST Pin

About TEST Pin, please use with OPEN.
About BD37522FS, 14,15,16pin are TEST Pin. About BD37523FS, 14,15pin are TEST Pin.

●Thermal Derating Curve

About the thermal design by the IC

Characteristics of an IC have a great deal to do with the temperature at which it is used, and exceeding absolute maximum ratings may degrade and destroy elements. Careful consideration must be given to the heat of the IC from the two standpoints of immediate damage and long-term reliability of operation.

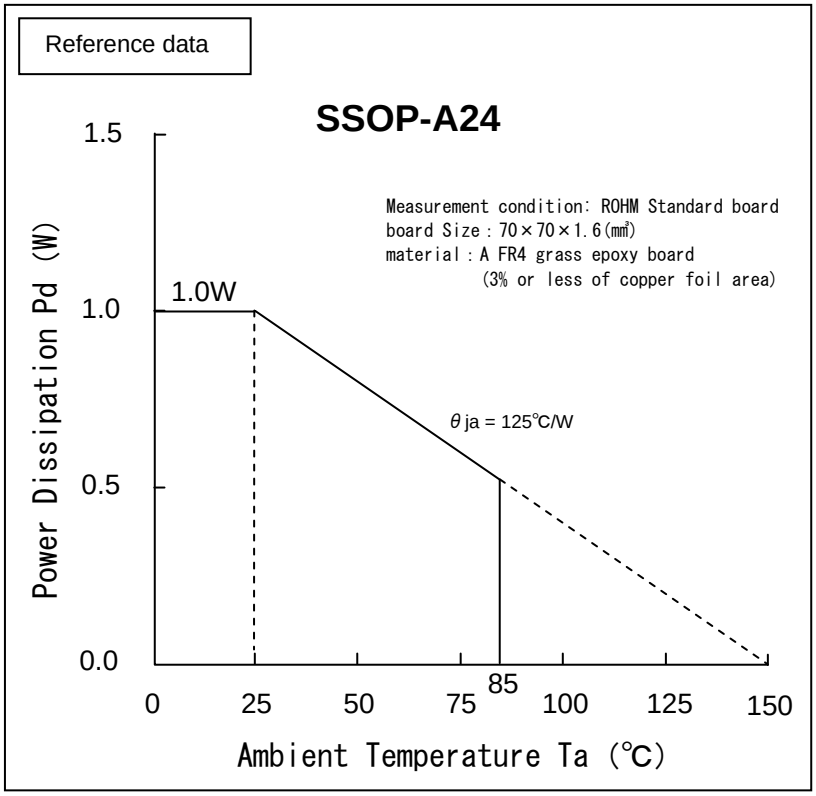


Fig.23 Temperature Derating Curve

Note) Values are actual measurements and are not guaranteed.

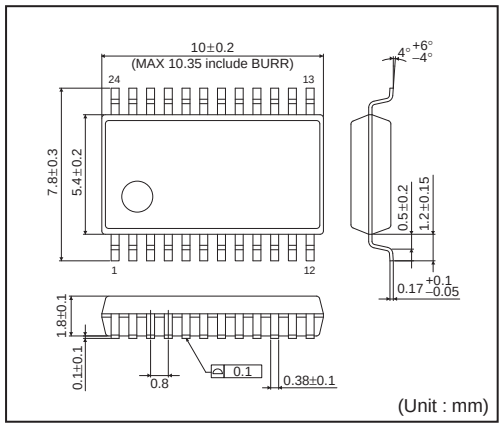
Power dissipation values vary according to the board on which the IC is mounted.

●Ordering part number

B	D	3	7	5	2	2	F	S	-	E	2

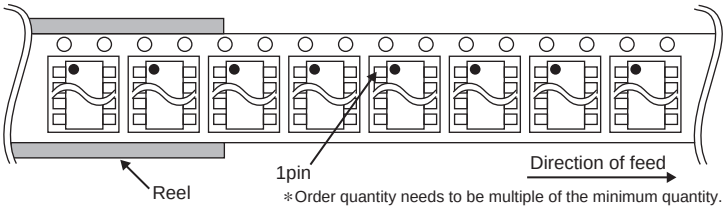
Part No.	Part No.	Package	Packaging and forming specification
	37522 37523	FS : SSOP-A24	E2: Embossed tape and reel

SSOP-A24



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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