Technical Note

Power Supply IC Series for TFT-LCD Panels

5V Input Multi-channel System Power Supply IC

BD8179MUV

No.09035EBT04

●Description

The BD8179MUV is a system power supply IC for TFT panels.
A 1-chip IC providing a total of three voltages required for TFT panels, i.e., source voltage, gate high-level, and gate low-level voltage, thus constructing a TFT panel power supply with minimal components required.

●Features

1) Step Up DC/DC Converter.
2) Incorporates 18V, 3.0A N-channel FET
3) Linear-Regulator Controllers for V_{GON} and V_{GOFF}
4) 5 channel Operational Amplifiers/±150mA Output Short-Circuit Current 40V / µs Slew Rate
5) Switching Frequency: 1200 kHz.
6) Gate Shading Function Included.
7) Protection Circuits
8) Over Current Protection
9) Timer Latch Mode Short Current Protection.
10) Thermal Shut Down.
11) Under Voltage Protection.
12) Over Voltage Protection
13) VQFN032V5050 Package

●Applications

Liquid crystal TV, PC monitor, and TFT-LCD panel

●Absolute maximum ratings (Ta = 25℃)

Parameter	Symbol	Limit	Unit
Power Supply Voltage	V_{IN}	7	V
VMAIN Voltage	V_{MAIN}	20	V
SUP Voltage	V_{SUP}	20	V
DRVP Voltage	V_{DRVP}	40	V
DRVN Voltage	V_{DRVN}	-30	V
SRC Voltage	V_{SRC}	40	V
CTL Voltage	V_{CTL}	7	V
Junction Temperature	Tjmax	150	℃
Power Dissipation	Pd	4560	mW
Operating Temperature Range	Topr	-40～85	℃
Storage Temperature Range	Tstg	-55～150	℃

* Reduced by 19.52 mW/℃ over 25℃, when mounted on a glass epoxy board.
(4-layer 74.2 mm × 74.2 mm × 1.6 mm).

●Operating Condition

Parameter	Symbol	Limit		Unit
		Min.	Max.	
Power Supply Voltage	V_{IN}	2.6	5.5	V
V_{MAIN} Voltage	V_{MAIN}	8	18	V
SUP Voltage	V_{SUP}	-	18	V
DRVP Voltage	V_{DRVP}	-	38	V
DRVN Voltage	V_{DRVN}	-	-20	V
SRC Voltage	V_{SRC}	-	38	V

●**Electrical Characteristics** (Unless otherwise specified, V_{IN} = 3.3V; V_{SUP} = 12 V; V_{GON} = 25 V; V_{GOFF} = -6V; Ta = 25℃)

1 DC/DC CONVERTER CONTROLLER BLOCK

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
[ERROR AMPLIFIER BLOCK]						
FB Input Bias Current	I_{FB}	-	0.1	-	µA	
Feed Back Voltage	V_{FB}	1.221	1.233	1.245	V	Buffer, No load
Comp Sink Current	Ioi	1	5	10	µA	V_{FB}=1.5V V_{COMP}=0.5V
Comp Source Current	Ioo	-10	-5	-1	µA	V_{FB}=1.0V V_{COMP}=0.5V
[LX BLOCK]						
LX ON-Resistance	Ron	-	200	-	mΩ	
LX Leak Current	I_{leak}	-	0	10	µA	V_{LX}=18V
MAX Duty Cycle	D_{MAX}	-	90	-	%	
LX Current Limit	I_{LX}	2.5	-	-	A	
[INTERNAL SOFT START BLOCK]						
Soft Start Delay Time	tss	-	3.25	-	ms	

2. GATE-ON LINEAR REGULATOR CONTROLLER

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
FBP Voltage	V_{FBP}	1.225	1.25	1.275	V	
FBP Input Bias Current	I_{FBP}	-	0.1	-	µA	
DRVP Current Limit	I_{DRVP}	1	5	10	mA	

3. GATE-OFF LINEAR REGULATOR CONTROLLER

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
FBN Voltage	V_{FBN}	0.235	0.25	0.265	V	
FBN Input Bias Current	I_{FBN}	-	0.1	-	µA	
DRVN Current Limit	I_{DRVN}	1	5	10	mA	

4. OPERATIONAL AMPLIFIERS

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
Input Offset Voltage	Voff	-	0	-	mV	V_{POS}1～5 = 6V
Input Range	V_{RANGE}	0		V_{SUP}	V	
DRIVE Current	Idrv	50	-	-	mA	
Slew Rate	SR	-	40	-	V/us	

5. GATE SHADING CONTROLLER BLOCK

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
DEL Start Period	tdd	-	15	-	ms	
DEL Source Current	Idls	-8	-5	-2	µA	
DEL Threshold Voltage	Vdls	1.2	1.25	1.3	V	
CTL Input Low Voltage	Vctll	-	-	V_{IN} x 0.3	V	
CTL Input High Voltage	Vchlh	V_{IN} x 0.7	-	-	V	
CTL Input Current	Ictl	8	16.5	25	µA	V_{CTL}=3.3V
SRC ON Resistance	Ron_{SRC}	-	5	-	Ω	
DRN ON Resistance	Ron_{DRV}	-	30	-	Ω	

○This product is not designed for protection against radioactive rays.

●**Electrical Characteristics** (Unless otherwise specified, V_{IN} = 3.3V; V_{SUP} = 12 V; V_{GON} = 25 V; V_{GOFF} = -6V; Ta = 25℃)

6. WHOLE DEVICE

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
[REFERENCE BLOCK]						
Reference Voltage	V_{REF}	1.231	1.25	1.269	V	
[OSCILLATION BLOCK]						
Oscillation Frequency	F_{OSC}	1020	1200	1380	kHz	
[VIN UNDER VOLTAGE LOCK OUT BLOCK]						
Detect Voltage	Vuvlo	2.25	2.4	2.55	V	
[SUP OVER VOLTAGE LOCK OUT BLOCK]						
Detect Voltage	Vovp	18	19	20	V	
[SHORT CURRENT PROTECTION BLOCK]						
Fault Delay Time	Tscp	-	150	-	ms	
[DETECTOR BLOCK]						
VFB OFF Threshold Voltage	Vthfb	0.9	1.0	1.1	V	
VFBP OFF Threshold Voltage	Vthfbp	0.9	1.0	1.1	V	
VFBN OFF Threshold Voltage	Vthfpn	0.4	0.5	0.6	V	

○This product is not designed for protection against radio active rays.

●**Reference Data** (Unless otherwise specified, Ta = 25℃, VIN=5V)

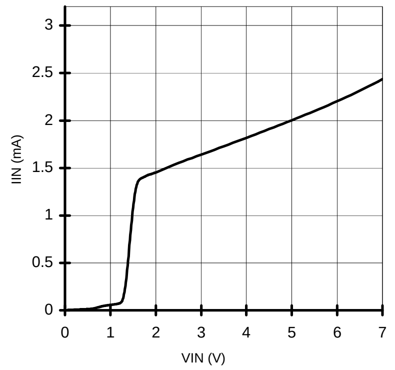


Fig.1 Supply Current
(No switching)

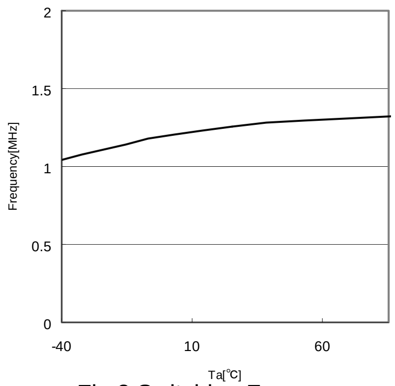


Fig.2 Switching Frequency
vs Temperature

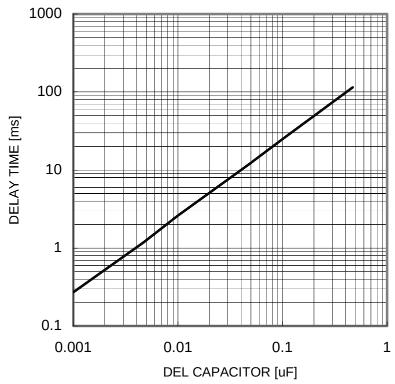


Fig.3 Delay Time
vs Capacitor

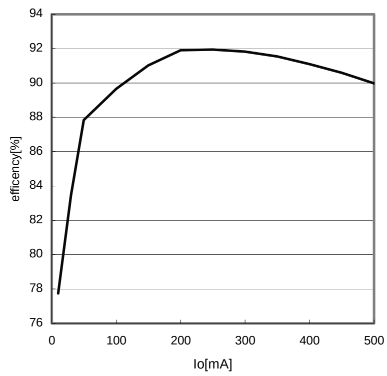


Fig.4 Efficiency vs Output Current
(VMAIN)

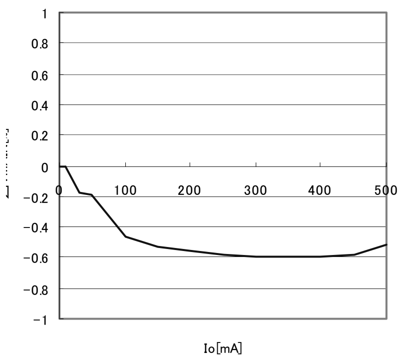


Fig.5 VMAIN Voltage
Load Regulation

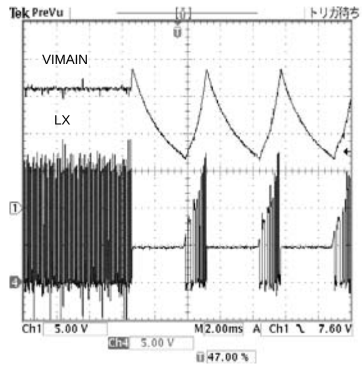


Fig.6 Over Voltage Protect
waveform

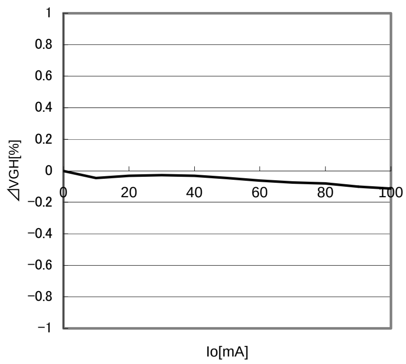


Fig.7 Gate-ON Voltage
Load Regulation

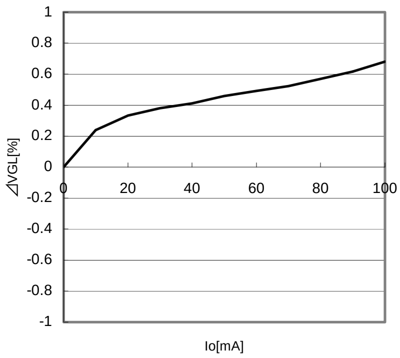


Fig.8 Gate-OFF Voltage
Load Regulation

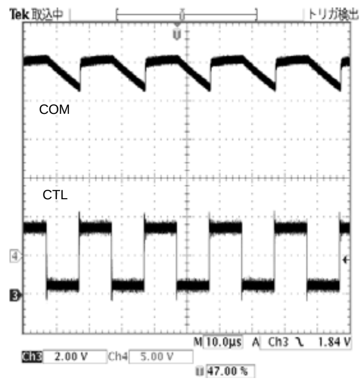


Fig.9 Gate Shading Output
waveform

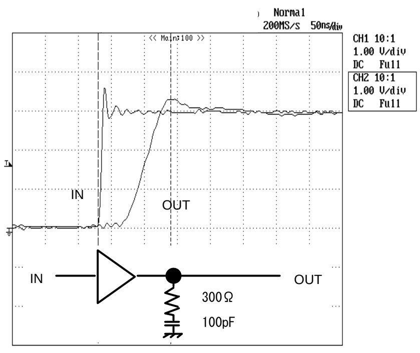


Fig.10 AMP Slew Rate
(Rise)

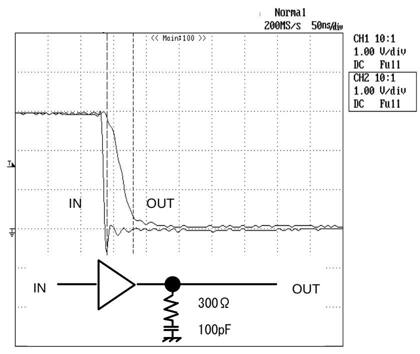


Fig.11 AMP Slew Rate
(Fall)

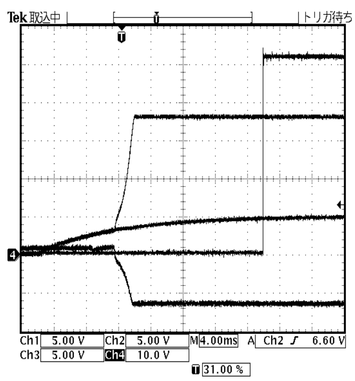
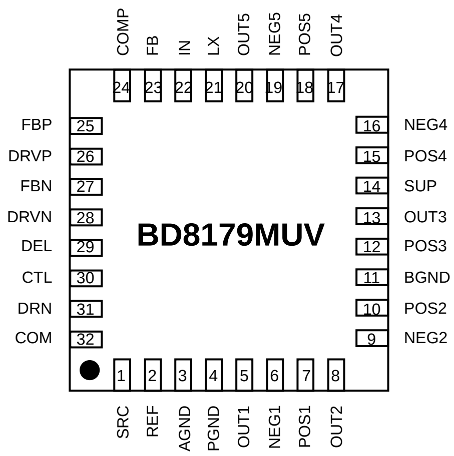
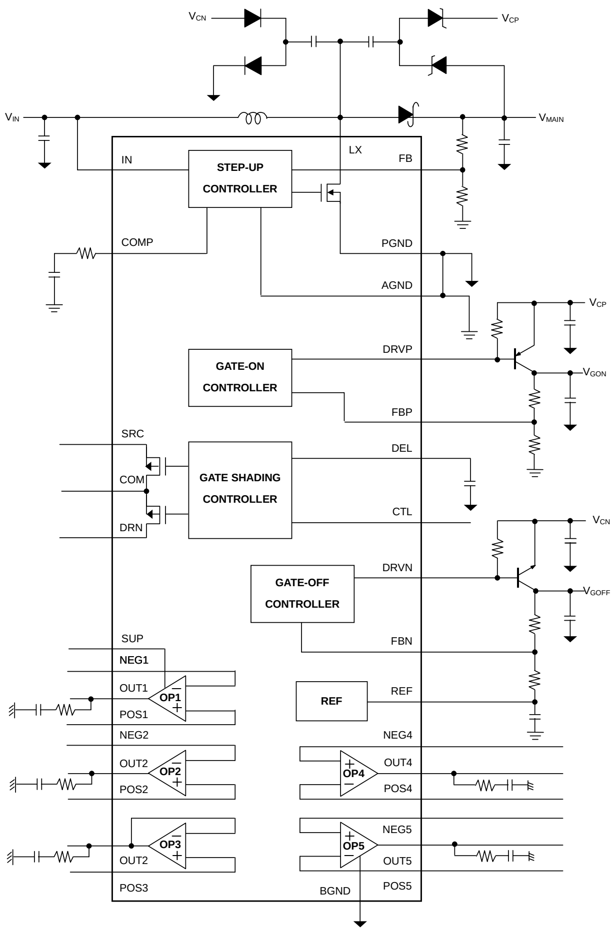


Fig.12 Start Up Sequence
waveform

●Pin Assignments Diagram



●Block Diagram



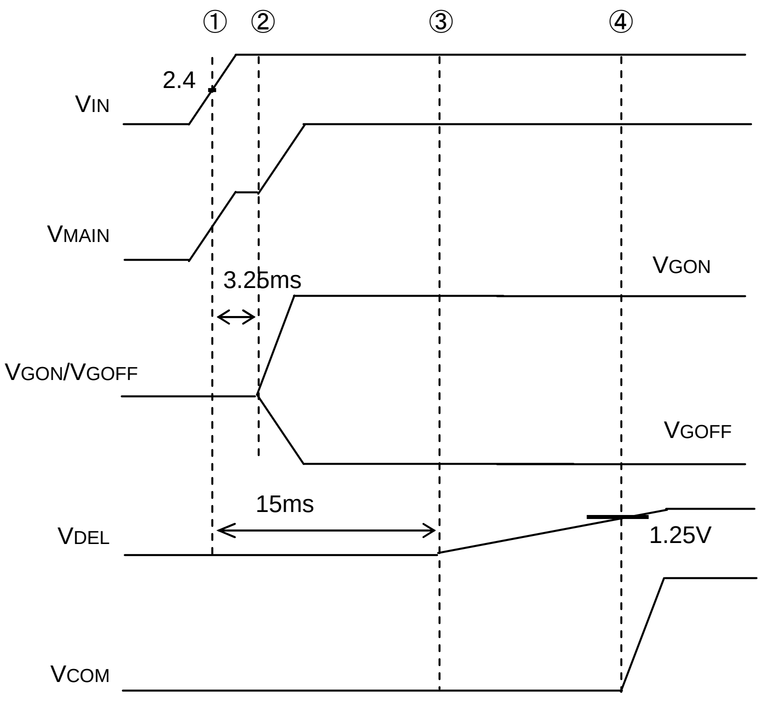
●Pin Assignments

PIN NO.	Pin Name	Function	PIN NO.	Pin Name	Function
1	SRC	Highside Input for Gate Shading switch	17	OUT4	Operational Amplifier 4 Output
2	REF	Reference for VGOFF	18	POS5	Operational Amplifier 5 Noninverting Input
3	AGND	Ground	19	NEG5	Operational Amplifier 5 Inverting Input
4	PGND	Power Ground	20	OUT5	Operational Amplifier 5 Output
5	OUT1	Operational Amplifier 1 Output	21	LX	Nch Power MOS FET Drain and Switching Node
6	NEG1	Operational Amplifier 1 Inverting Input	22	IN	Power Supply voltage Input
7	POS1	Operational Amplifier 1 Noninverting Input	23	FB	Feedback Input for step up DC/DC
8	OUT2	Operational Amplifier 2 Output	24	COMP	Error Amplifier Compensation Point for step up DC/DC
9	NEG2	Operational Amplifier 2 Inverting Input	25	FBP	Feedback Input for Gate-ON Linear-Regulator
10	POS2	Operational Amplifier 2 Noninverting Input	26	DRVP	Gate-ON Linear-Regulator Base Drive
11	BGND	Ground	27	FBN	Feedback Input for Gate-OFF Linear-Regulator
12	POS3	Operational Amplifier 3 Noninverting Input	28	DRVN	Gate-OFF Linear-Regulator Base Drive
13	OUT3	Operational Amplifier 3 Output	29	DEL	Delay Input for Gate Shading
14	SUP	Power Supply voltage Input for operational Amplifier	30	CTL	Switch Control Input for Gate Shading
15	POS4	Operational Amplifier 4 Noninverting Input	31	DRN	Lowside Input for Gate Shading switch
16	NEG4	Operational Amplifier 4 Inverting Input	32	COM	Gate Shading Output

●Block Function

- Step-up Controller
  A controller circuit for DC/DC boosting.
  The switching duty is controlled so that the feedback voltage FB is set to 1.233 V (typ.).
  A soft start operates at the time of starting.
- Gate-on Controller
  A controller circuit for the positive-side charge pump.
  The liner regulator controls so that the feedback voltage FBP will be set to 1.25 V (typ.).
- Gate-off Controller
  A controller circuit for the negative-side charge pump.
  The liner regulator controls so that the feedback voltage FBN will be set to 0.25 V (Typ.).
- Gate Shading Controller
  A controller circuit for MOS FET Switch
  The COM switching synchronize with CTL input.
- Start-up Controller
  A control circuit for the starting sequence.
  Controls to start in order of $V_{CC} \rightarrow V_{MAIN} \rightarrow V_{GOFF}/V_{GON} \rightarrow V_{COM}$
- REF
  A block that generates internal reference voltage. 1.25V (Typ.) is output.
- TSD/UVLO/OVP
  Thermal shutdown/Under-voltage lockout protection/circuit blocks.
  The thermal shutdown circuit is shut down at an IC internal temperature of 175°C and reactivate at 160°C.
  The under-voltage lockout protection circuit shuts down the IC when the VIN is 2.4 V (typ.) or below.
  The over-voltage lockout protection circuit shuts down the IC when the SUP is 19.0 V (typ.) or over.
- OP1～OP5
  Operational amplifier block

●Starting sequence



①UVLO released when V_{IN} voltage reaches 2.4V
②Step up DCDC converter starts switching, and V_{GON} and V_{GOFF} starts.
③V_{DEL} starts.
④V_{COM} ON when V_{DEL} reaches 1.25V

●Under Voltage Lock Out (UVLO)

The UVLO circuit compares the input voltage at IN with the UVLO threshold (2.4V rising, 2.2V falling, typ) to ensure the input voltage is high enough for reliable operation.
The 200mV (typ) hysteresis prevents supply transients from causing a restart. Once the input voltage exceeds the UVLO rising threshold, startup begins. When the input voltage falls below the UVLO falling threshold, the controller turns off the main step-up regulator, turns off the linear-regulator outputs, and disables the Gate Shading controller.

●Thermal Shut Down (TSD)

The TSD prevents excessive power dissipation from overheating the BD8179MUV. When the junction temperature exceeds Tj=175℃(Typ), a thermal sensor immediately activates. The fault protection, which shuts down all outputs except the reference, allowing the device to cool down. Once the device cools down by approximately 15℃ reactivate the device.

●Over Voltage Protection (OVP)

The Step up DC/DC converter has OVP circuit.
The OVP circuit compares the input Voltage at SUP with the OVP threshold (19V rising, 18.5V falling, Typ) to protect the step up DC/DC output exceed the absolute maximum voltage. Once the SUP Voltage exceeds the OVP rising threshold, turn off the main Step-up regulator.
Then, the SUP Voltage falls bellow the OVP falling threshold,reactivate the main Step-Up regulator.

●Over Current Protection (OCP)

The Step-Up DC/DC converter, linear-regulator and Operational Amplifier have OCP circuit respectively.
The OCP circuit restricts to load current, when an OCP activated, one's own output only restricted.
However, if the output continue to overload, the device is possible to activate thermal shutdown or short current protection.

●Timer Latch Mode Short Current Protection (SCP)

BD8179MUV has SCP circuit feature to prevent the large current flowing when the output is shorted to GND.
This function is monitoring VMAIN, VGON, and VGOFF Voltage and starts the timer when at least one of the outputs operating properly (when the output voltage was lower than expected).
After 150ms (Typ.) of this abnormal state, the device will shutdown the all outputs and latch the state.

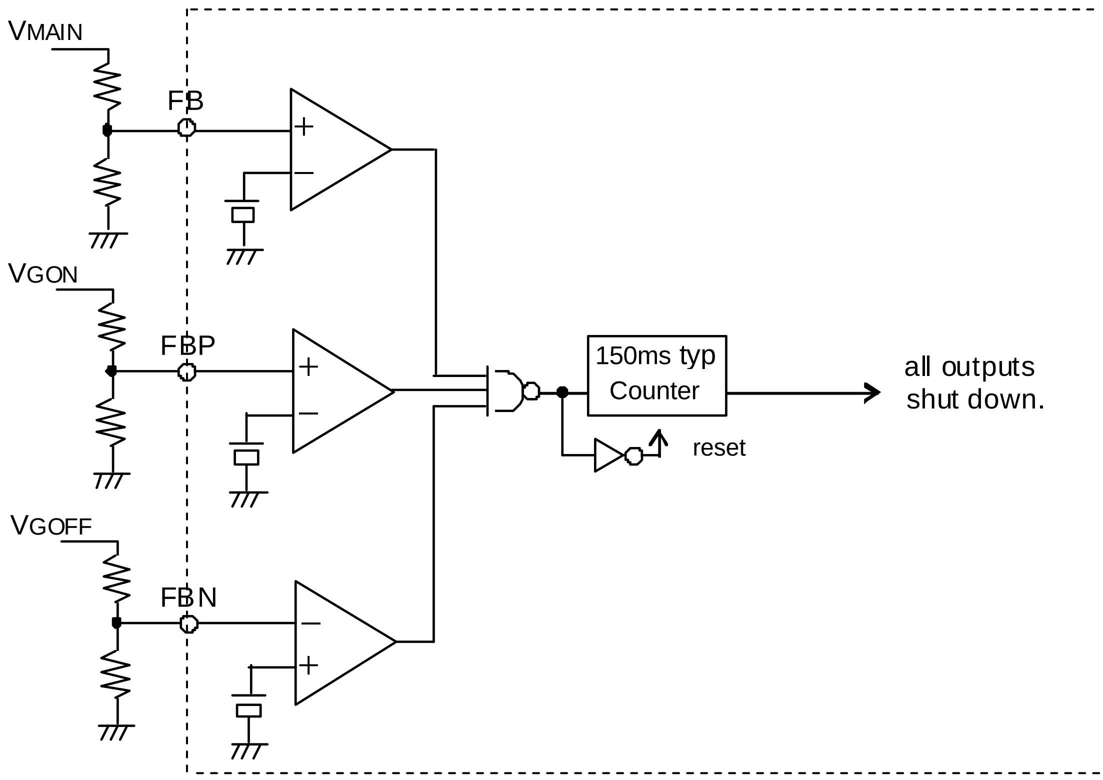


Fig.13 SCP Block Diagram

●Selecting Application Components

(1) Setting the Output L Constant

The coil to use for output is decided by the rating current ILR and input current maximum value IINMAX of the coil.

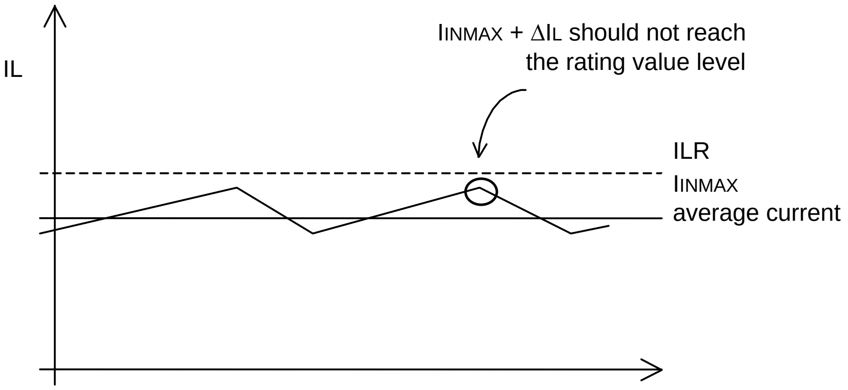


Fig.14 Coil Current Waveform

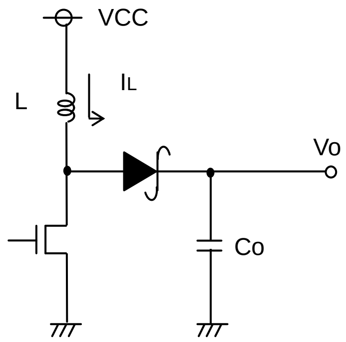


Fig. 15 Output Application Circuit Diagram

Adjust so that I_{INMAX} +ΔI_L does not reach the rating current value I_{LR}. At this time, ΔI_L can be obtained by the following equation.

$$\Delta I_L = \frac{1}{L} \times Vcc \times \frac{Vo-Vcc}{Vcc} \times \frac{1}{f} \ \text{[A]}$$ Here, f is the switching frequency.

Set with sufficient margin because the coil value may have the dispersion of ±30%. If the coil current exceeds the rating current I_{LR} of the coil, it may damage the IC internal element.

BD8179MUV uses the current mode DC/DC converter control and has the optimized design at the coil value. A coil inductance (L) of 4.7 µH to 15 µH is recommended from viewpoints of electric power efficiency, response, and stability.

(2) Output Capacity Settings

For the capacitor to use for the output, select the capacitor which has the larger value in the ripple voltage V_{PP} allowance value and the drop voltage allowance value at the time of sudden load change. Output ripple voltage is decided by the following equation.

$$⊿V_{PP} = I_{LMAX} \times R_{ESR} + \frac{1}{fCo} \times \frac{Vcc}{Vo} \times \left(I_{LMAX} - \frac{⊿I_L}{2}\right) \ \text{[V]}$$ Here, f is the switching frequency.

Perform setting so that the voltage is within the allowable ripple voltage range. For the drop voltage during sudden load change; V_{DR}, please perform the rough calculation by the following equation.

$$V_{DR} = \frac{⊿I}{Co} \times 10\ \text{us} \quad \text{[V]}$$

However, 10 µs is the rough calculation value of the DC/DC response speed. Please set the capacitance considering the sufficient margin so that these two values are within the standard value range.

(3) Selecting the Input Capacitor

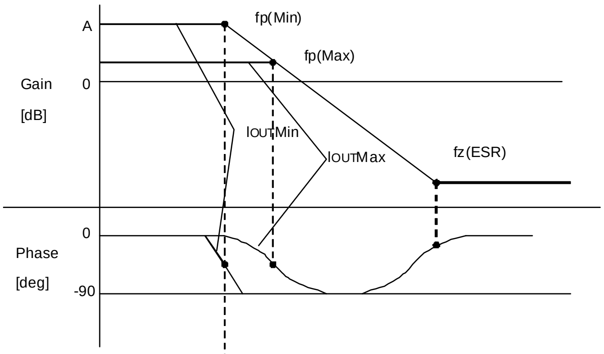
Since the peak current flows between the input and output at the DC/DC converter, a capacitor is required to install at the input side. For the reason, the low ESR capacitor is recommended as an input capacitor which has the value more than 10 µF and less than 100 mΩ. If a capacitor out of this range is selected, the excessive ripple voltage is superposed on the input voltage, accordingly it may cause the malfunction of IC.

However these conditions may vary according to the load current, input voltage, output voltage, inductance and switching frequency. Be sure to perform the margin check using the actual product.

(4) Setting R_C, C_C of the Phase Compensation Circuit

In the current mode control, since the coil current is controlled, a pole (phase lag) made by the CR filter composed of the output capacitor and load resistor will be created in the low frequency range, and a zero (phase lead) by the output capacitor and ESR of capacitor will be created in the high frequency range. In this case, to cancel the pole of the power amplifier, it is easy to compensate by adding the zero point with C_C and R_C to the output from the error amp as shown in the illustration.

Open loop gain characteristics



Error amp phase compensation characteristics

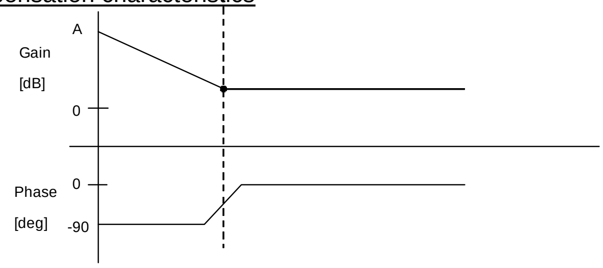


Fig. 16 Gain vs Phase

$$F_p = \frac{1}{2\pi \times R_O \times C_O} \quad [\mathrm{Hz}]$$

$$f_z(ESR) = \frac{1}{2\pi \times ESR \times C_O} \quad [\mathrm{Hz}]$$

Pole at the power amplification stage

When the output current reduces, the load resistance R_O increases and the pole frequency lowers.

$$f_p(Min) = \frac{1}{2\pi \times R_{OMax} \times C_O} \quad [\mathrm{Hz}] \leftarrow \text{at light load}$$

$$f_z(Max) = \frac{1}{2\pi \times R_{OMin} \times C_O} \quad [\mathrm{Hz}] \leftarrow \text{at heavy load}$$

Zero at the power amplification stage

When the output capacitor is set larger, the pole frequency lowers but the zero frequency will not change. (This is because the capacitor ESR becomes 1/2 when the capacitor becomes 2 times.)

$$f_p(Amp.) = \frac{1}{2\pi \times R_C \times C_C} \quad [\mathrm{Hz}]$$

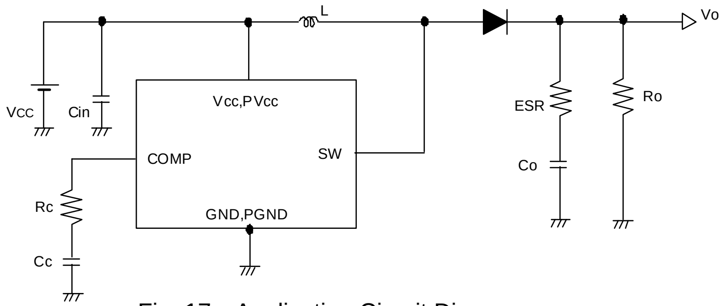


Fig. 17 Application Circuit Diagram

It is possible to realize the stable feedback loop by canceling the pole fp(Min.), which is created by the output capacitor and load resistor, with CR zero compensation of the error amp as shown below.

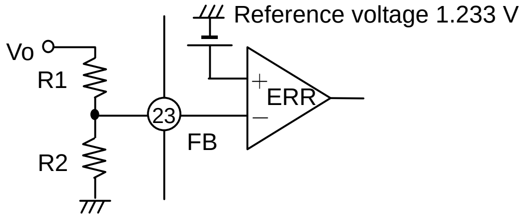
fz(Amp.) = fp(Min.)

$$\longrightarrow \quad \frac{1}{2\pi \times R_c \times C_c} - \frac{1}{2\pi \times R_{omax} \times C} \quad [\mathrm{Hz}]$$

(5) Design of the Feedback Resistor Constant

Refer to the following equation to set the feedback resistor. As the setting range, 10 kΩ to 330 kΩ is recommended. If the resistor is set lower than a 10 kΩ, it causes the reduction of power efficiency. If it is set more than 330 kΩ, the offset voltage becomes larger by the input bias current 0.4 µA(Typ.) in the internal error amplifier.

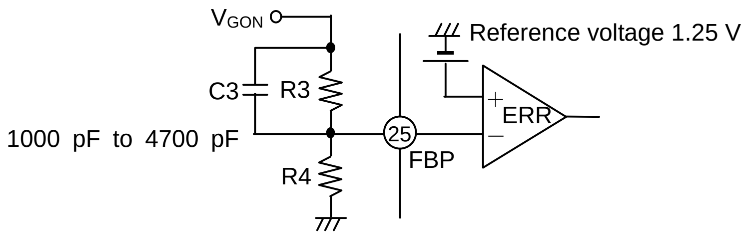
$$V_{MAIN} = \frac{R1 + R2}{R2} \times 1.233 \quad [V]$$



(6) Positive-side Charge Pump Settings

BD8179MUV incorporates a charge pump controller, thus making it possible to generate stable gate voltage.
The output voltage is determined by the following formula. As the setting range, 10 kΩ to 330 kΩ is recommended. If the resistor is set lower than a 10kΩ, it causes the reduction of power efficiency. If it is set more than 330 kΩ, the offset voltage becomes larger by the input bias current 0.4 µA (Typ.) in the internal error amp.

$$V_{GON} = \frac{R3 + R4}{R4} \times 1.25 \quad [V]$$



In order to prevent output voltage overshooting, add capacitor C3 in parallel with R3. The recommended capacitance is 1000 pF to 4700 pF. If a capacitor outside this range is inserted, the output voltage may oscillate.
By connecting capacitance to the DEL, a rising delay time can be set for the positive-side charge pump.
The delay time is determined by the following formula.

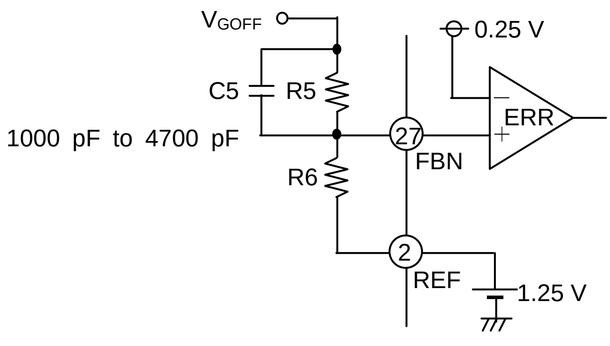
- Delay time of charge pump block t_{DELAY}

t_{DELAY} = (C_{DEL} × 1.25)/5 µA [s]
Where, C_{DEL} is the external capacitance.

(7) Negative-side Charge Pump Settings

BD8179MUV incorporates a charge pump controller for negative voltage, thus making it possible to generate stable gate voltage.
The output voltage is determined by the following formula. As the setting range, 10 kΩ to 330 kΩ is recommended. If the resistor is set lower than a 10 kΩ, it causes the reduction of power efficiency. If it is set more than 330 kΩ, the offset voltage becomes larger by the input bias current 0.4 µA (Typ.) in the internal error amp.

$$V_{GOFF} = -\frac{R5}{R6} \times 1.0 + 0.25\ V \quad [V]$$



The delay time is internally fixed at 200 us.
In order to prevent output voltage overshooting, insert capacitor C5 in parallel with R5. The recommended capacitance is 1000 pF to 4700 pF. If a capacitor outside this range is inserted, the output voltage may oscillate.

●Notes for use

1) Absolute maximum ratings
Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2) GND potential
Ensure a minimum GND pin potential in all operating conditions.

3) Setting of heat
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4) Pin short and mistake fitting
Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pins caused by the presence of a foreign object may result in damage to the IC.

5) Actions in strong magnetic field
Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.

6) Testing on application boards
When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process.

7) Ground wiring patterns
When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring patterns of any external components.

8) This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements.For example, when the resistors and transistors are connected to the pins as shown in Fig. 18, a parasitic diode or a transistor operates by inversing the pin voltage and GND voltage.
The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements, such as the application of voltages lower than the GND (P board) voltage to input and output pins.

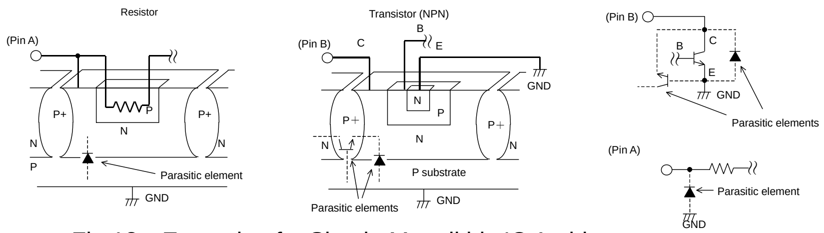


Fig.18 Example of a Simple Monolithic IC Architecture

9) Overcurrent protection circuits
An overcurrent protection circuit designed according to the output current is incorporated for the prevention of IC destruction that may result in the event of load shorting. This protection circuit is effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous operation or transitioning of the protection circuits. At the time of thermal designing, keep in mind that the current capability has negative characteristics to temperatures.

10) Thermal shutdown circuit
This IC incorporates a built-in thermal shutdown circuit for the protection from thermal destruction. The IC should be used within the specified power dissipation range. However, in the event that the IC continues to be operated in excess of its power dissipation limits, the attendant rise in the chip's temperature Tj will trigger the thermal shutdown circuit to turn off all output power elements. The circuit automatically resets once the chip's temperature Tj drops.
Operation of the thermal shutdown circuit presumes that the IC's absolute maximum ratings have been exceeded. Application designs should never make use of the thermal shutdown circuit.

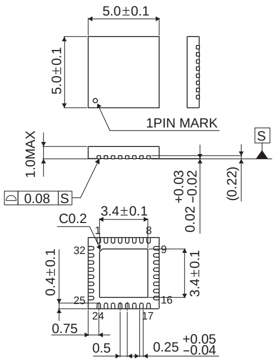
11) Testing on application boards
At the time of inspection of the installation boards, when the capacitor is connected to the pin with low impedance, be sure to discharge electricity per process because it may load stresses to the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC.

●Ordering part number

B	D	8	1	7	9	M	U	V	-	E	2

- B D: Part No.
- 8 1 7 9: Part No.
- M U V: Package MUV:VQFN032V5050
- E 2: Packaging and forming specification E2: Embossed tape and reel

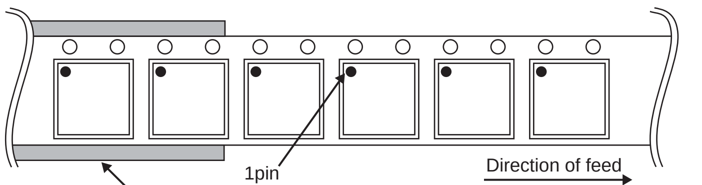
VQFN032V5050



(Unit : mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※Order quantity needs to be multiple of the minimum quantity.

Notes

No copying or reproduction of this document, in part or in whole, is permitted without the consent of ROHM Co.,Ltd.

The content specified herein is subject to change for improvement without notice.

The content specified herein is for the purpose of introducing ROHM's products (hereinafter "Products"). If you wish to use any such Product, please be sure to refer to the specifications, which can be obtained from ROHM upon request.

Examples of application circuits, circuit constants and any other information contained herein illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.

Great care was taken in ensuring the accuracy of the information specified in this document. However, should you incur any damage arising from any inaccuracy or misprint of such information, ROHM shall bear no responsibility for such damage.

The technical information specified herein is intended only to show the typical functions of and examples of application circuits for the Products. ROHM does not grant you, explicitly or implicitly, any license to use or exercise intellectual property or other rights held by ROHM and other parties. ROHM shall bear no responsibility whatsoever for any dispute arising from the use of such technical information.

The Products specified in this document are intended to be used with general-use electronic equipment or devices (such as audio visual equipment, office-automation equipment, communication devices, electronic appliances and amusement devices).

The Products specified in this document are not designed to be radiation tolerant.

While ROHM always makes efforts to enhance the quality and reliability of its Products, a Product may fail or malfunction for a variety of reasons.

Please be sure to implement in your equipment using the Products safety measures to guard against the possibility of physical injury, fire or any other damage caused in the event of the failure of any Product, such as derating, redundancy, fire control and fail-safe designs. ROHM shall bear no responsibility whatsoever for your use of any Product outside of the prescribed scope or not in accordance with the instruction manual.

The Products are not designed or manufactured to be used with any equipment, device or system which requires an extremely high level of reliability the failure or malfunction of which may result in a direct threat to human life or create a risk of human injury (such as a medical instrument, transportation equipment, aerospace machinery, nuclear-reactor controller, fuel-controller or other safety device). ROHM shall bear no responsibility in any way for use of any of the Products for the above special purposes. If a Product is intended to be used for any such special purpose, please contact a ROHM sales representative before purchasing.

If you intend to export or ship overseas any Product or technology specified herein that may be controlled under the Foreign Exchange and the Foreign Trade Law, you will be required to obtain a license or permit under the Law.

ROHM SEMICONDUCTOR

Thank you for your accessing to ROHM product informations.
More detail product informations and catalogs are available, please contact us.

ROHM Customer Support System

http://www.rohm.com/contact/