# Overvoltage and Overcurrent Protection IC and Li+ Charger Front-End Protection IC

**Check for Samples :bq24308**

## FEATURES

- **Provides Protection for Three Variables:**
  - **Input Overvoltage**
  - **Input Overcurrent with Current Limiting**
  - **Battery Overvoltage**
- **30V Maximum Input Voltage**
- **Supports Up to 1.5A Input Current**
- **Robust Against False Triggering Due to Current Transients**
- **Thermal Shutdown**
- **LDO Mode Voltage Regulation of 5V**
- **Small 2 mm × 2 mm 8-Pin SON Package**

## APPLICATIONS

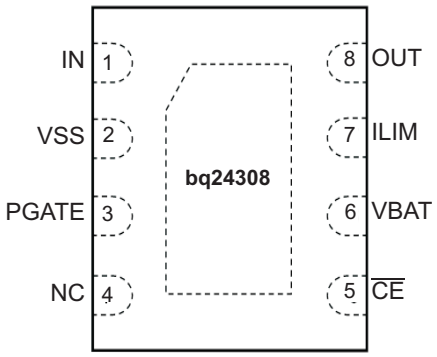
- **Mobile and Smart Phones**
- **PDAs**
- **MP3 Players**
- **Low-Power Handheld Devices**
- **Bluetooth Headsets**

## DESCRIPTION

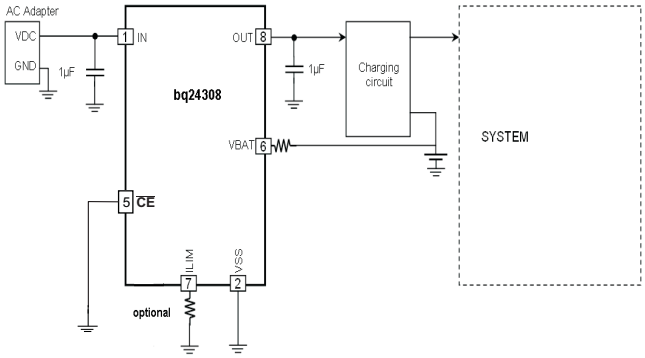
The bq24308 is a highly integrated circuit designed to provide protection to Li-ion batteries from failures of the charging circuit. The IC continuously monitors the input voltage, the input current and the battery voltage. In case of an input over-voltage condition, the IC immediately removes power from the charging circuit by turning off an internal switch. In the case of an over-current condition, it limits the current to a safe value for a blanking duration before turning the switch off. Battery voltage may also be monitored and if the battery voltage exceeds the specified value the internal switch is turned off. Additionally, the IC also monitors its own die temperature and switches off if it becomes too hot.

The input over-current threshold can be increased using an external resistor. The IC also offers optional protection against reverse voltage at the input using an external P-channel FET.

## PINOUT




## TYPICAL APPLICATION CIRCUIT

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PowerPAD is a trademark of Texas Instruments.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE DISSIPATION RATINGS

| PACKAGE | $R_{\theta JC}$ | $R_{\theta JA}$ (1) |
|---|---|---|
| DSG | 5°C/W | 75°C/W |

(1) This data is based on using the JEDEC High-K board and the exposed die pad is connected to a Cu pad on the board. The pad is connected to the ground plane by a 2x3 via matrix.

## ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

| | | VALUE | UNIT |
|---|---|---|---|
| Input voltage | IN, PGATE (with respect to VSS) | –0.3 to 30 | V |
| | OUT (with respect to VSS) | –0.3 to 12 | V |
| | ILIM, $\overline{CE}$, VBAT (with respect to VSS) | –0.3 to 7 | V |
| Input current | IN | 2.0 | A |
| Output current | OUT | 2.0 | A |
| | PGATE | 5 | mA |
| ESD Withstand voltages | All (Human body Model per JESD22-A114-E) | 2000 | V |
| | All (Machine Model per JESD22-A115-A) | 200 | V |
| | All (Charged Device Model per JESD22-C101-C) | 500 | V |
| | IN (IEC 61000-4-2) (with IN pin bypassed to VSS with 1.0-µF low-ESR ceramic capacitor) | 15 (Air discharge)<br>8 (Contact) | kV |
| Junction temperature, $T_J$ | | –40 to 150 | °C |
| Storage temperature, $T_{STG}$ | | –65 to 150 | °C |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN}$ | Input voltage range | 3.3 | 26 | V |
| $I_{IN}$ | Input current, IN pin | | 1.5 | A |
| $I_{OUT}$ | Current, OUT pin | | 1.5 | A |
| $R_{ILIM}$ | OCP programming resistor | 31 | | kΩ |
| $T_J$ | Junction temperature | –40 | 125 | °C |

## ORDERING INFORMATION

| PART NUMBER | MARKING | MEDIUM | QUANTITY | PACKAGE |
|---|---|---|---|---|
| bq24308DSGR | DAS | Tape and Reel | 3000 | 2mm × 2mm SON |
| bq24308DSGT | DAS | Tape and Reel | 250 | 2mm × 2mm SON |

## ELECTRICAL CHARACTERISTICS

over junction temperature range –40°C ≤ $T_J$ ≤ 125°C and recommended supply voltage (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **IN** | | | | | | |
| $V_{UVLO}$ | Under-voltage lock-out, input power detected threshold | $\overline{CE}$= Low, $V_{IN}$: 0 V → 3 V | 2.5 | 2.7 | 2.8 | V |
| $V_{HYS-UVLO}$ | Hysteresis on UVLO | $\overline{CE}$= Low, $V_{IN}$: 3 V → 0 V | 200 | 260 | 300 | mV |
| $t_{DGL(PGOOD)}$ | Deglitch time, input power detected status | $\overline{CE}$ = Low. Time measured from $V_{IN}$ 0V → 4V 1 µs rise-time, to output turning ON | | 8 | | ms |
| $I_{DD}$ | Operating current | $\overline{CE}$= Low, $V_{IN}$ = 5 V, no load on OUT pin | | 410 | 500 | µA |
| $I_{STDBY}$ | Standby current | $\overline{CE}$= High, $V_{IN}$ = 5 V | | 65 | 95 | µA |
| **INPUT TO OUTPUT CHARACTERISTICS** | | | | | | |
| $V_{DO}$ | Drop-out voltage IN to OUT | $\overline{CE}$ = Low, $V_{IN}$ = 4 V, $I_{OUT}$ = 250 mA | | 45 | 75 | mV |
| **INPUT OVER-VOLTAGE PROTECTION** | | | | | | |
| $V_{OVP}$ | Input over-voltage protection threshold | $\overline{CE}$= Low, $V_{IN}$: 4 V → 10 V | 6.1 | 6.3 | 6.5 | V |
| $V_{HYS-OVP}$ | Hysteresis on OVP | $\overline{CE}$= Low, $V_{IN}$: 10 V → 4 V | 20 | 60 | 110 | mV |
| $t_{PD(OVP)}$ | Input OVP propagation delay(1) | $\overline{CE}$= Low, Time measured from $V_{IN}$ 4 V → 10 V, 1µs rising time, to output turning OFF | | 0.2 | 1 | µs |
| $t_{ON(OVP)}$ | Recovery time from input overvoltage condition | $\overline{CE}$ = Low, Time measured from $V_{IN}$ 10 V → 4V, 1 µs fall-time, to output turning ON | | 8 | | ms |
| **OUTPUT VOLTAGE REGULATION** | | | | | | |
| $V_{O(REG)}$ | Output voltage | $\overline{CE}$ = Low, $V_{IN}$= 6 V, $I_{OUT}$ = 250 mA | 4.85 | 5.0 | 5.15 | V |
| **INPUT OVER-CURRENT PROTECTION** | | | | | | |
| $I_{OCP}$ | Internal input over-current protection threshold | $\overline{CE}$= Low, $V_{IN}$ = 5V, ILIM floating; $T_J$ = 0°C to 125°C | 630 | 700 | 770 | mA |
| | Input over-current protection range | $\overline{CE}$ = Low, $V_{IN}$ = 5V; $T_J$ = 0°C to 125°C | 630 | | 1500 | mA |
| $\Delta I_{OCP}$ | OCP threshold accuracy | $T_J$ = 0°C to 125°C | | ±10% | | |
| | | $T_J$ = –40°C to 125°C | | ±13% | | |
| $K_{ILIM}$ | Current limit programming: IOCP(program) = IOCP + KILIM ÷ $R_{ILIM}$ | | | 25000 | | AΩ |
| $t_{BLANK(OCP)}$ | Blanking time, input over-current detected | $\overline{CE}$= Low | | 5 | | ms |
| $t_{REC(OCP)}$ | Recovery time from input over-current condition | $\overline{CE}$ = Low | | 64 | | ms |
| **BATTERY OVER-VOLTAGE PROTECTION** | | | | | | |
| $BV_{OVP}$ | Battery overvoltage protection threshold | $\overline{CE}$ = Low, $V_{IN}$ > 4.4 V, $V_{VBAT}$: 4.2 V → 4.5 V | 4.30 | 4.35 | 4.40 | V |
| $V_{HYS-BOVP}$ | Hysteresis on $BV_{OVP}$ | $\overline{CE}$= Low, $V_{IN}$ > 4.4 V, $V_{VBAT}$: 4.5 V → 3.9 V | 200 | 275 | 320 | mV |
| $I_{VBAT}$ | Input bias current on VBAT pin | $V_{VBAT}$ = 4.4 V, $T_J$ = 25°C | | | 10 | nA |
| $t_{DGL(BOVP)}$ | Deglitch time, battery overvoltage detected | $\overline{CE}$= Low, $V_{IN}$ > 4.4 V, time measured from $V_{VBAT}$ 4.2 V → 4.5 V, 1µs rising time, to output turning OFF | | 176 | | µs |
| **THERMAL PROTECTION** | | | | | | |
| $T_{J(OFF)}$ | Thermal shutdown temperature | | | 140 | 150 | °C |
| $T_{J(OFF-HYS)}$ | Thermal shutdown hysteresis | | | 20 | | °C |
| **P-FET Gate Driver** | | | | | | |
| $V_{GCLMP}$ | Gate driver clamp voltage | $V_{IN}$ >17V | 13 | 15 | 17 | V |

(1) Not tested in production. Specified by design.

## ELECTRICAL CHARACTERISTICS (continued)

over junction temperature range –40°C ≤ $T_J$ ≤ 125°C and recommended supply voltage (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **LOGIC LEVELS ON $\overline{CE}$** | | | | | | |
| $V_{IL}$ | Low-level input voltage | | 0 | | 0.4 | V |
| $V_{IH}$ | High-level input voltage | | 1.4 | | | V |
| $I_{IL}$ | Low-level input current | | | | 1 | µA |
| $I_{IH}$ | High-level input current | $V_{CE}$ = 1.8 V | | | 15 | µA |

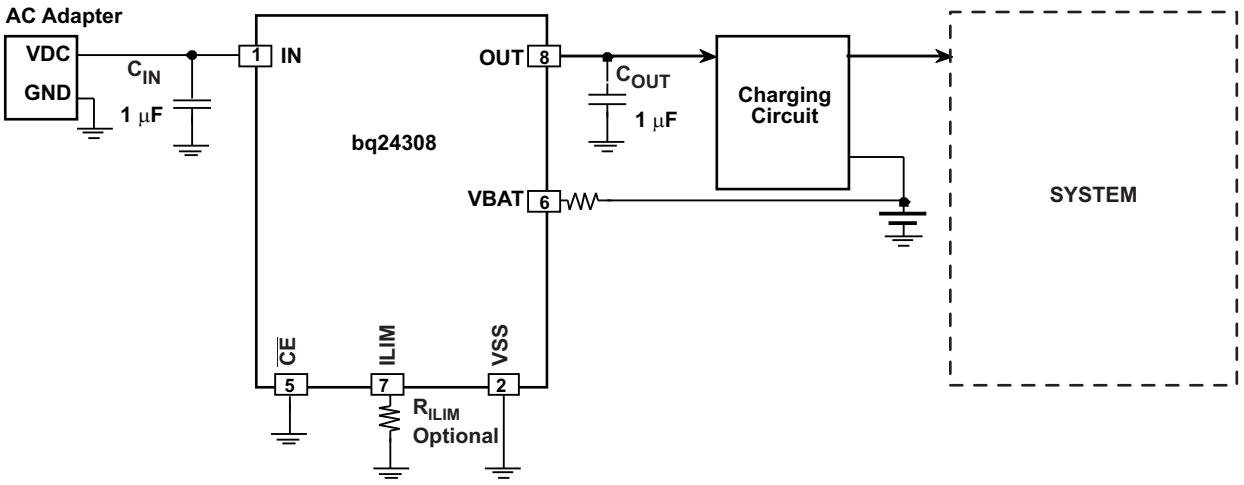



**Figure 1. Overvoltage, Overcurrent, and Battery Overvoltage Protection**

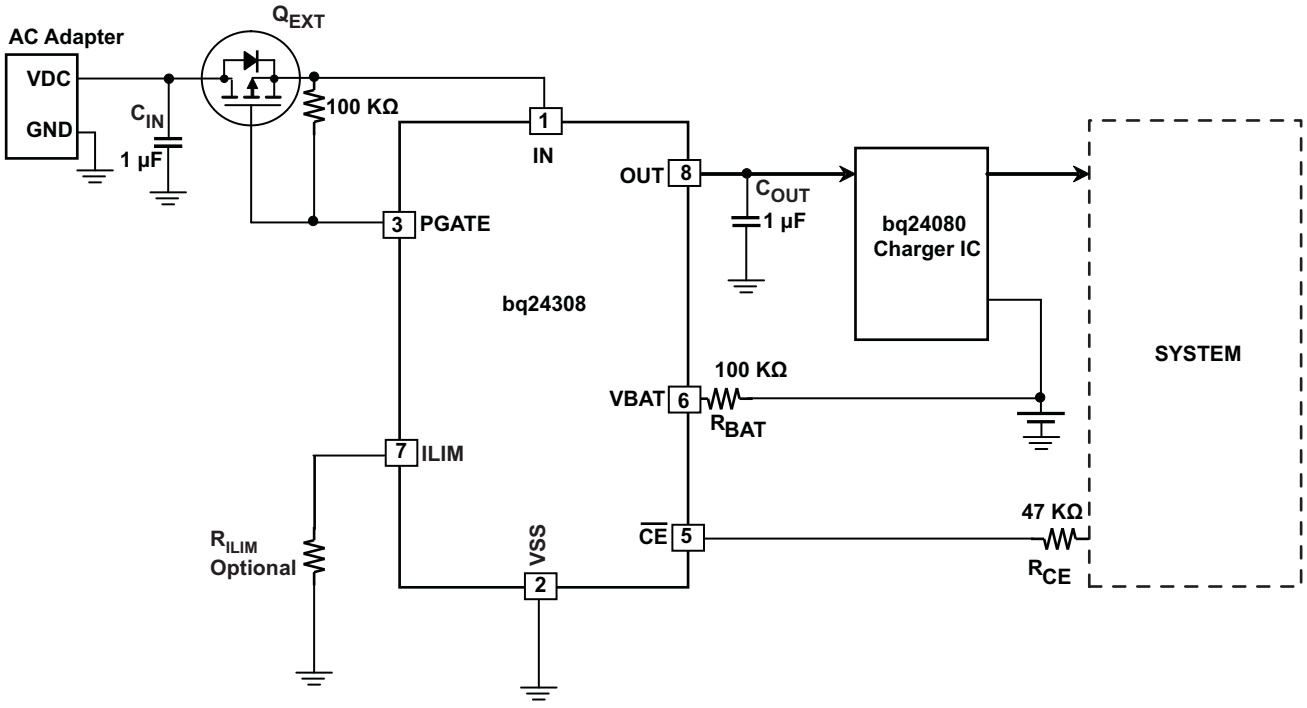



**Figure 2. OVP, OCP, BATOVP With Input Reverse-Polarity Protection**

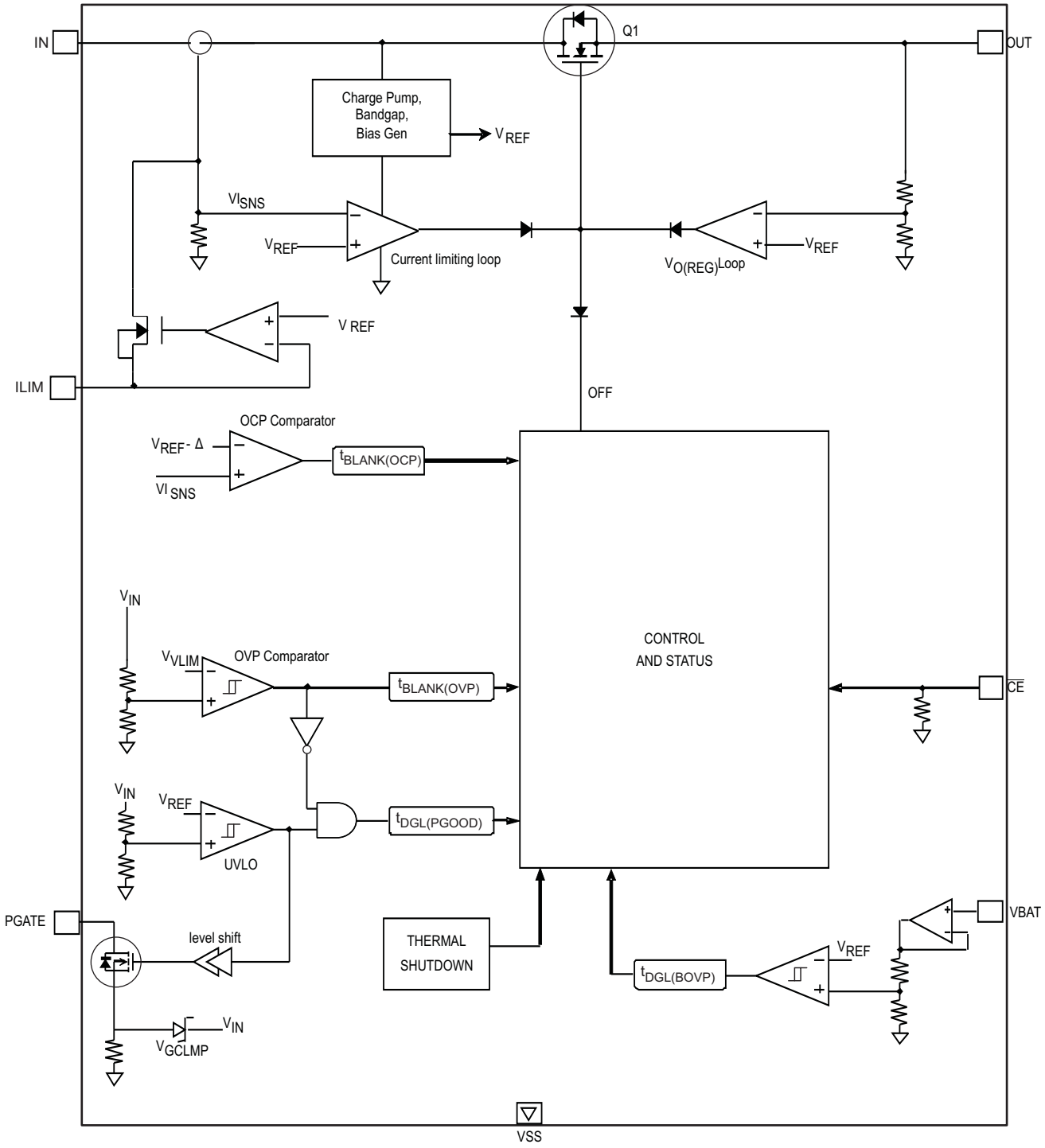



**Figure 3. Simplified Block Diagram**

## PIN FUNCTIONS

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| IN | 1 | I | Input power, connect to external DC supply. Connect external 0.1µF (minimum) ceramic capacitor to VSS |
| OUT | 8 | O | Output terminal to the charging system. Connect external 1µF capacitor (minimum) ceramic capacitor to VSS |
| VBAT | 6 | I | Battery voltage sense input. Connect to pack positive terminal through a resistor. |
| NC | 4 | – | Do not connect to any external circuit. This pin may have internal connections used for test purpose. |
| ILIM | 7 | I | Input over-current threshold programming. An optional external resistor can be used to increase input over-current threshold. Connect a resistor to VSS to increase the OCP threshold. |
| VSS | 2 | – | Ground terminal |
| PGATE | 3 | O | Gate drive for optional external P-FET |
| $\overline{CE}$ | 5 | I | Chip enable input. Active low. When $\overline{CE}$= High, the input FET is off. Internally pulled down. |
| ThermalPAD | | - | There is an internal electrical connection between the exposed thermal pad and the VSS pin of the device. The thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. VSS pin must be connected to ground at all times. |

## TYPICAL OPERATING PERFORMANCE

Test conditions (unless otherwise noted) for typical operating performance are: $V_{IN}$ = 5 V, $C_{IN}$ = 1 µF, $C_{OUT}$ = 1µF, $R_{BAT}$ = 100 kΩ, $R_{OUT}$ = 16Ω, $T_A$ = 25°C (see Figure 1 - Typical Application Circuit)

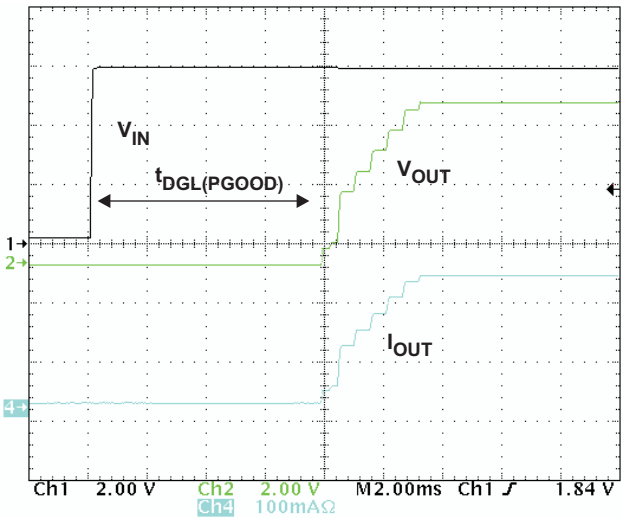



**Figure 4. Normal Power-On Showing Soft-Start. $V_{IN}$ 0 V to 6.0 V, $t_R$ = 20µs**

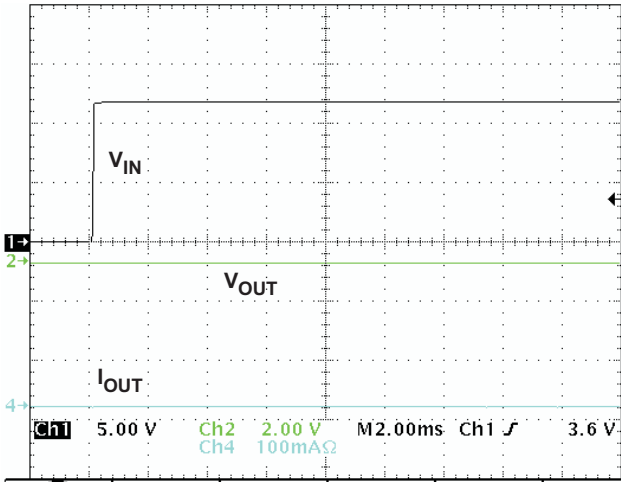



**Figure 5. Power-On with Input Overvoltage. $V_{IN}$ 0 V to 12.0 V, $t_R$ = 50 µs**

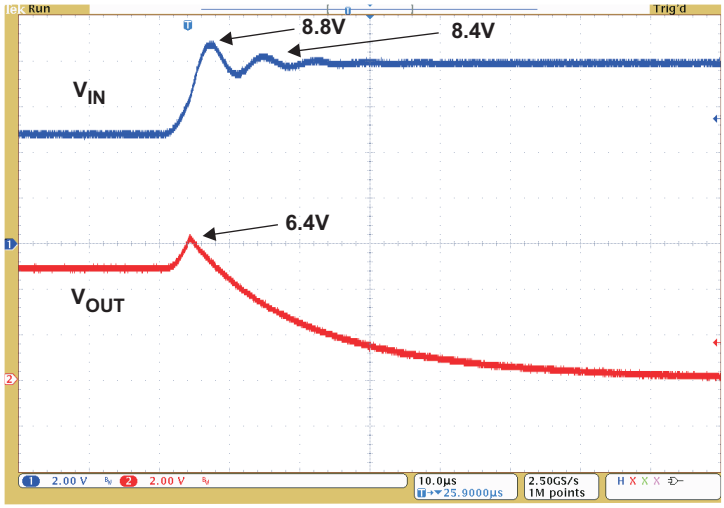



**Figure 6. bq24308 OVP Response for Input Step. $V_{IN}$ 5 V to 8 V, $t_R$ = 3µs.**

## TYPICAL OPERATING PERFORMANCE

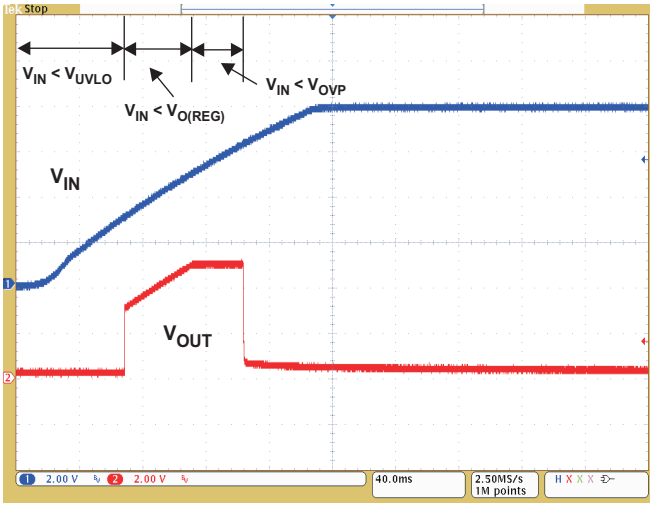



**Figure 7. OUT Pin Response to Slow Input Ramp.**

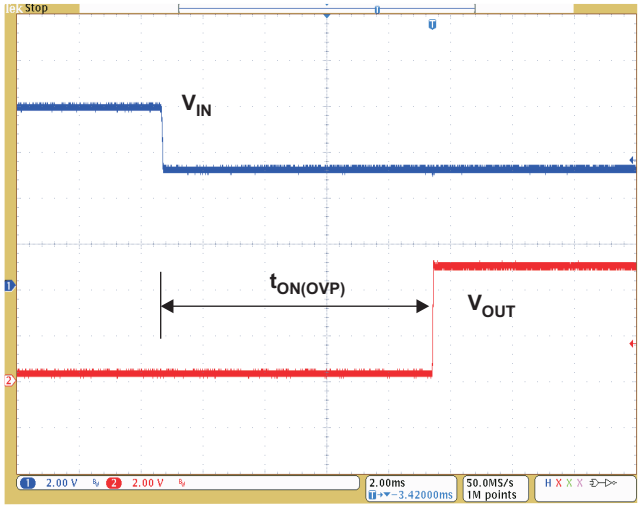



**Figure 8. bq24308 Recovery from Input OVP. $V_{IN}$ 8 V to 5 V, $t_F$ = 100 µs**

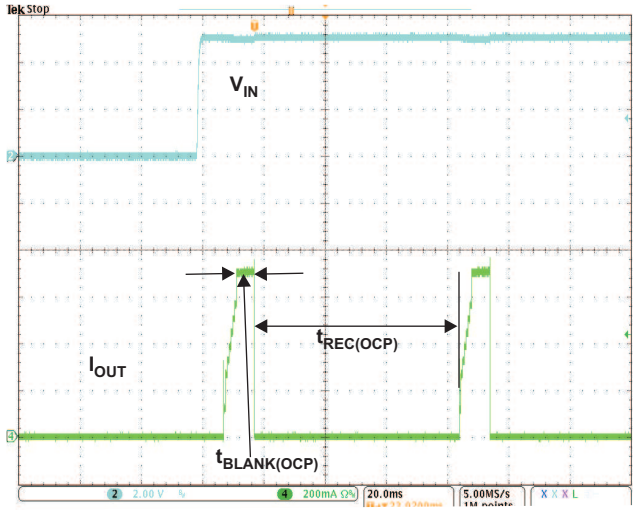



**Figure 9. OCP, Powering up with OUT Pin Shorted to VSS**

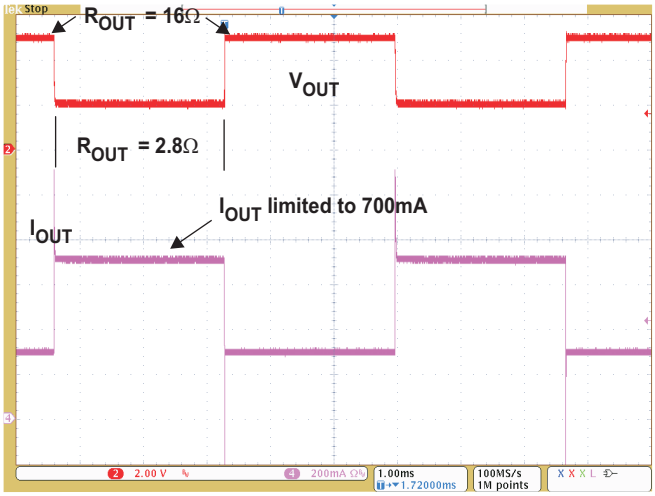



**Figure 10. OCP, Showing Current Limiting, $R_{OUT}$ 16 Ω to 2.8 Ω**

## TYPICAL OPERATING PERFORMANCE (continued)

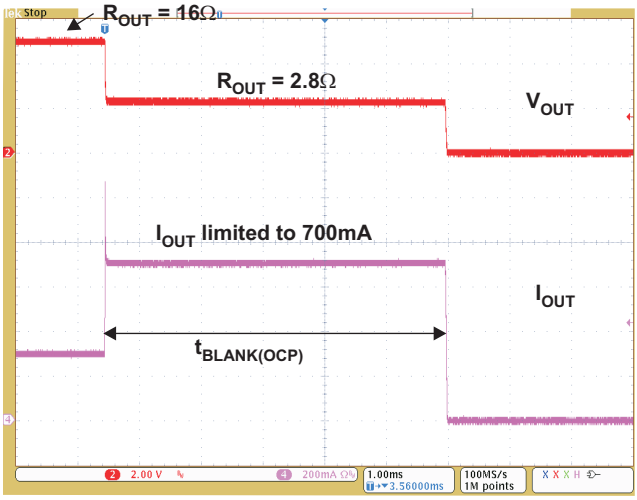



**Figure 11. OCP, Showing Current Limiting and OCP Blanking. $R_{OUT}$ 16 Ω to 2.8 Ω**

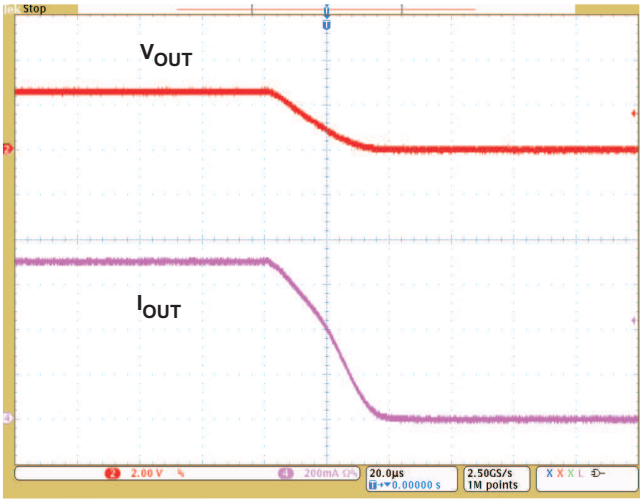



**Figure 12. Zoom-in on Turn-off Region of Figure 11, Showing Soft-Stop**

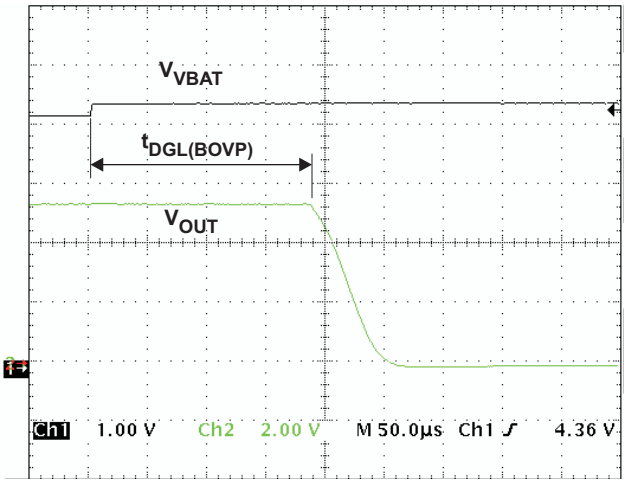



**Figure 13. Battery OVP. $V_{VBAT}$ Steps from 4.3 V to 4.5 V. Shows $t_{DGL(BOVP)}$ and Soft-Stop**

## TYPICAL OPERATING PERFORMANCE (continued)

**UNDERVOLTAGE LOCKOUT vs FREE-AIR TEMPERATURE**

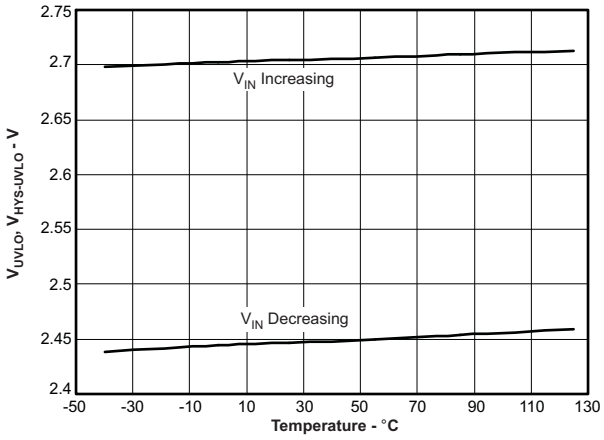



**Figure 14.**

**DROPOUT VOLTAGE (IN to OUT) vs FREE-AIR TEMPERATURE**

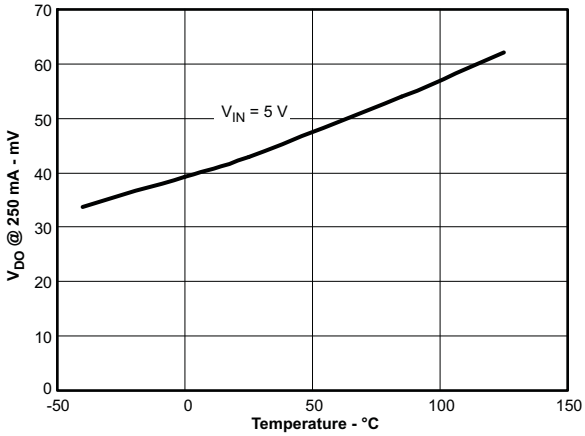



**Figure 15.**

**REGULATION VOLTAGE (OUT pin) vs FREE-AIR TEMPERATURE**

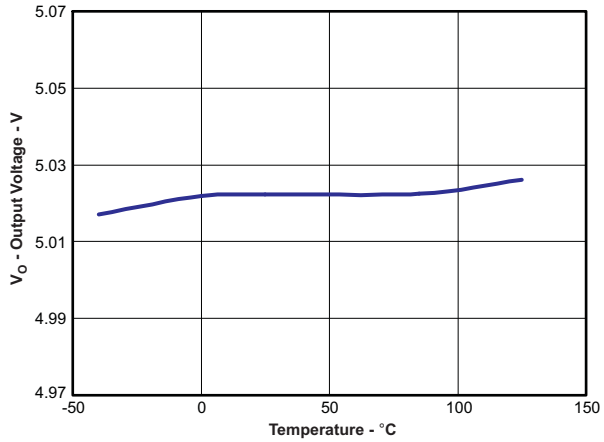



**Figure 16.**

**OVP THRESHOLD vs FREE-AIR TEMPERATURE**

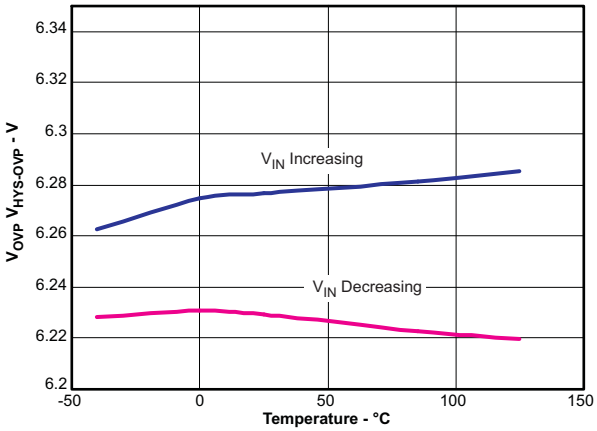



**Figure 17.**

## TYPICAL OPERATING PERFORMANCE (continued)

**OCP THRESHOLD vs FREE-AIR TEMPERATURE**

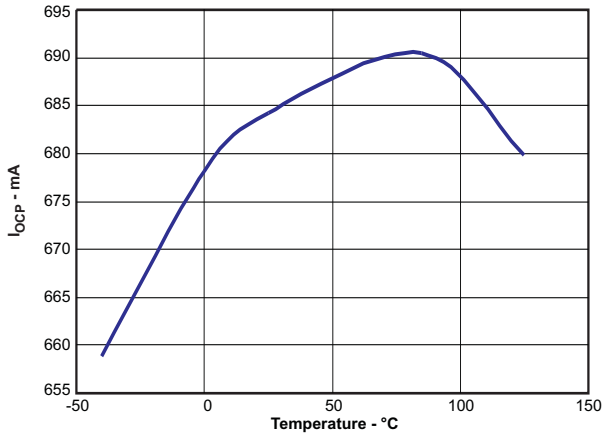



**Figure 18.**

**BATTERY OVP THRESHOLDS vs FREE-AIR TEMPERATURE**

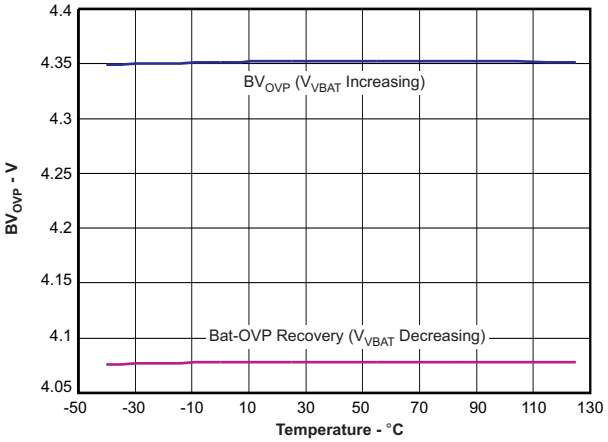



**Figure 19.**

**LEAKAGE CURRENT (BAT pin) vs FREE-AIR TEMPERATURE**

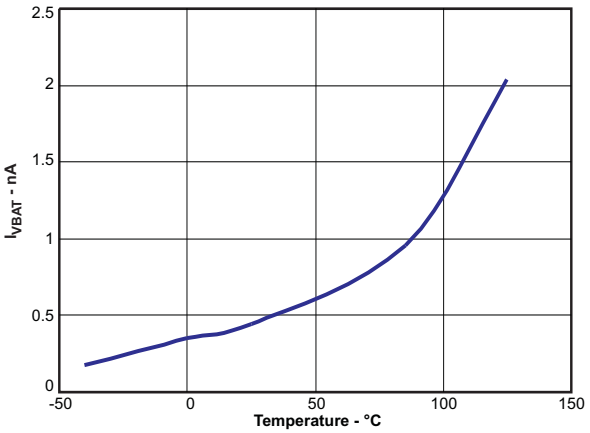



**Figure 20.**

**SUPPLY CURRENT vs INPUT VOLTAGE**

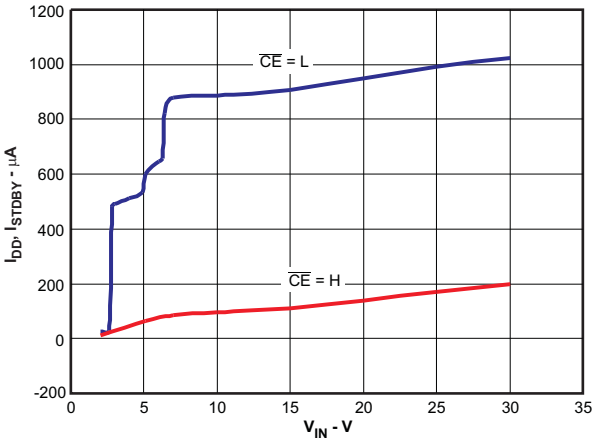



**Figure 21.**

## TYPICAL OPERATING PERFORMANCE (continued)

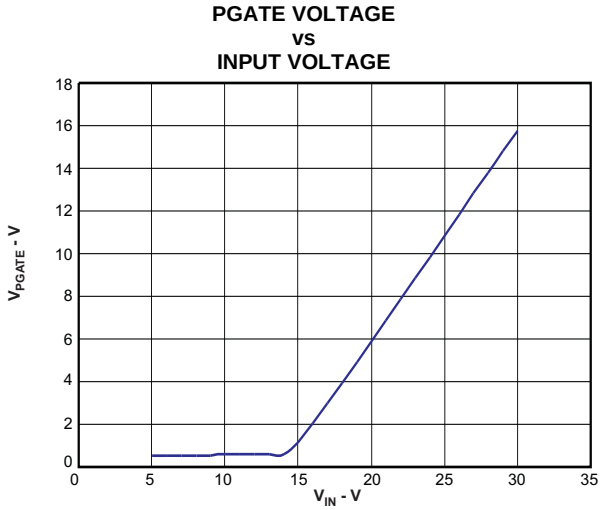



**Figure 22.**

## DETAILED FUNCTIONAL DESCRIPTION

The bq24308 is a highly integrated circuit designed to provide protection to Li-ion batteries from failures of the charging circuit. The IC continuously monitors the input voltage, the input current and the battery voltage. In case of an input over-voltage condition, the IC immediately removes power from the charging circuit by turning off an internal switch. In the case of an over-current condition, it limits the current to a safe value for a blanking duration before turning the switch off. Additionally, the IC also monitors its own die temperature and switches off if it becomes too hot.

The input and over-current threshold is user-programmable. The IC can be controlled by a processor using the CE pin.

### POWER DOWN

The device remains in power down mode when the input voltage at the IN pin is below the under-voltage lock-out threshold, VUVLO. The FET Q1 (see **Figure 3**) connected between IN and OUT pins is off.

### POWER-ON RESET

The device resets all internal timers when the input voltage at the IN pin exceeds the UVLO threshold. The gate driver for the external P-FET is enabled. The IC then waits for duration $t_{DGL(PGOOD)}$ for the input voltage to stabilize. If, after $t_{DGL(PGOOD)}$, the input voltage and battery voltage are safe, FET Q1 is turned ON. The IC has a soft-start feature to control the inrush current. This soft-start minimizes voltage ringing at the input (the ringing occurs because the parasitic inductance of the adapter cable and the input bypass capacitor form a resonant circuit). **Figure 4** shows the power-up behavior of the device. Because of the deglitch time at power-on, if the input voltage rises rapidly to beyond the OVP threshold, the device will not switch on at all, as shown in **Figure 5**.

### OPERATION

The device continuously monitors the input voltage, the input current and the battery voltage as described in detail in the following sections.

#### Input Overvoltage Protection

If the input voltage rises above VOVP, the internal FET Q1 is turned off, removing power from the circuit. As shown in **Figure 6** to **Figure 7**, the response is very rapid, with the FET turning off in less than a microsecond. When the input voltage returns below $V_{OVP} – V_{hys(OVP)}$ (but is still above UVLO), the FET Q1 is turned on again after a deglitch time of $t_{ON(OVP)}$ to ensure that the input supply has stabilized. **Figure 8** shows the recovery from input OVP.

#### Input Overcurrent Protection

The device can supply load current up to $I_{OCP}$ continuously. If the load current tries to exceed this threshold, the current is limited to $I_{OCP}$ for a maximum duration of $t_{BLANK(OCP)}$. If the load current returns to less than $I_{OCP}$ before $t_{BLANK(OCP)}$ times out, the device continues to operate (see **Figure 9**). However, if the overcurrent situation persists for $t_{BLANK(OCP)}$, FET Q1 is turned off for a duration of $t_{REC(OCP)}$. It is then turned on again and the current is monitored all over again (see **Figure 10** and **Figure 11**).

To prevent the input voltage from spiking up due to the inductance of the input cable, Q1 is not turned off rapidly in an overcurrent fault condition. Instead, the gate drive of Q1 is reduced slowly, resulting in a "soft-stop", as shown in **Figure 12**. The over-current threshold can be programmed to level greater than $I_{OCP}$ by connecting a resistor $R_{(ILIM)}$ from the $I_{LIM}$ pin to $V_{SS}$. The programmed over-current threshold is given by $I_{OCP(program)} = I_{OCP} + K_{ILIM} \div R_{(ILIM)}$.

#### Battery Overvoltage Protection

The battery overvoltage threshold $B_{VOVP}$ is internally set to 4.35V. If the battery voltage exceeds the $B_{VOVP}$ threshold for longer than $t_{DGL(BOVP)}$, FET Q1 is turned off (see **Figure 13**). This switch-off is also a soft-stop. Q1 is turned ON (soft-start) once the battery voltage drops to $B_{VOVP} – V_{HYS-BOVP}$.

### Thermal Protection

If the junction temperature of the device exceeds $T_{J(OFF)}$, FET Q1 is turned off. The FET is turned back on when the junction temperature falls below $T_{J(OFF)} - T_{J(OFF-HYS)}$.

### Enable Function

The IC has an enable pin which can be used to enable or disable the device. When the $\overline{CE}$ pin is driven high, the internal FET is turned off. When the $\overline{CE}$ pin is low, the FET is turned on if other conditions are safe. The $\overline{CE}$ pin has an internal pull-down resistor of 200 kΩ (typical) and can be left floating.

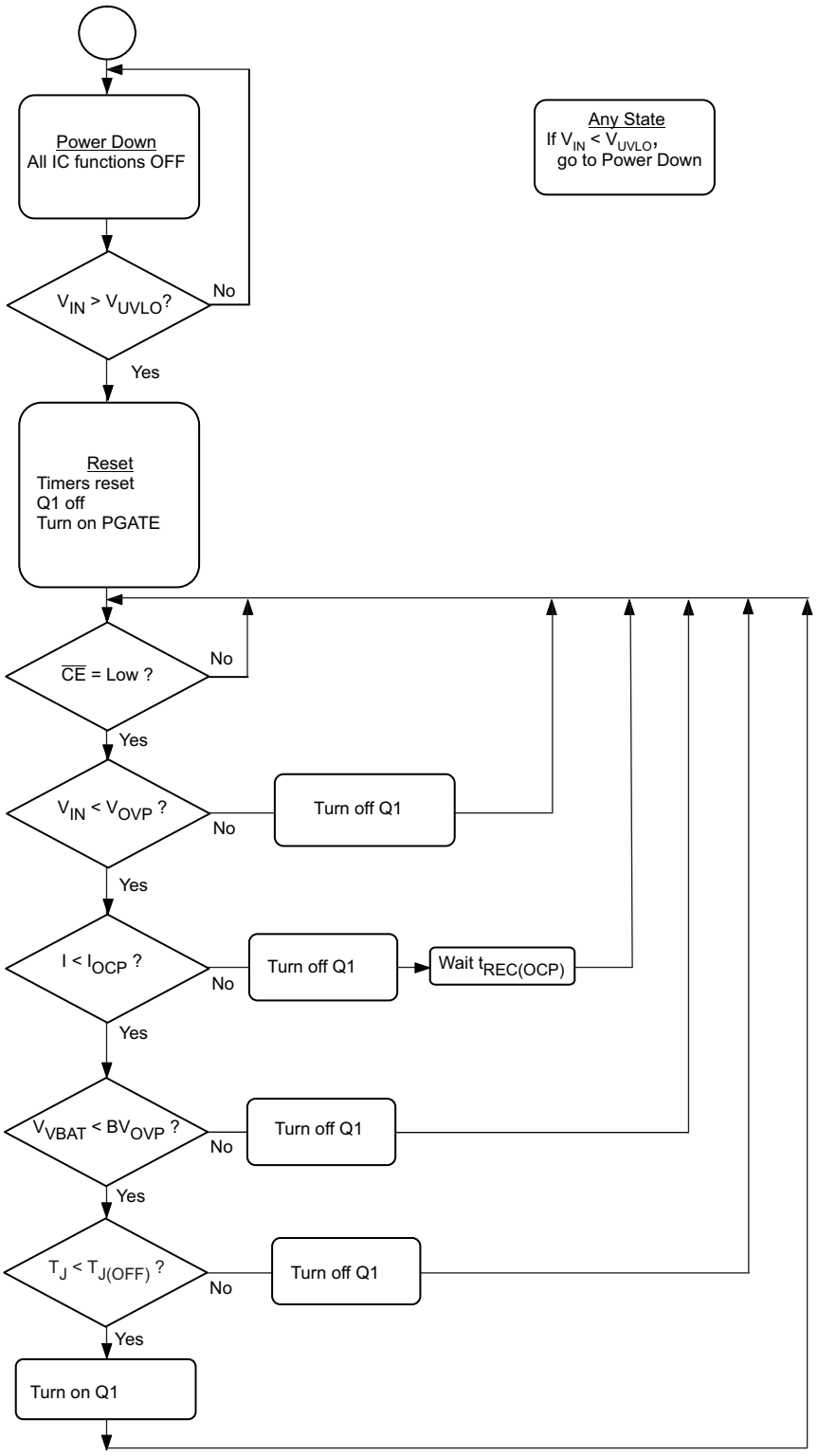



**Figure 23. State Diagram**

## APPLICATION INFORMATION

### Selection of $R_{BAT}$:

It is strongly recommended that the battery not be tied directly to the VBAT pin of the device, as under some failure modes of the IC, the voltage at the IN pin may appear on the VBAT pin. This voltage can be as high as 30V, and applying 30V to the battery in case of the failure of the device can be hazardous. Connecting the VBAT pin through $R_{BAT}$ prevents a large current from flowing into the battery in case of failure of the IC. In the interests of safety, $R_{BAT}$ should have a very high value. The problem with a large $R_{BAT}$ is that the voltage drop across this resistor because of the VBAT bias current $I_{VBAT}$ causes an error in the $BV_{OVP}$ threshold. This error is over and above the tolerance on the nominal 4.35V $BV_{OVP}$ threshold.

Choosing $R_{BAT}$ in the range 100KΩ to 470kΩ is a good compromise. In the case of IC failure, with $R_{BAT}$ equal to 100kΩ, the maximum current flowing into the battery would be (30V – 3V) ÷ 100kΩ = 270µA, which is low enough to be absorbed by the bias currents of the system components. $R_{BAT}$ equal to 100kΩ would result in a worst-case voltage drop of $R_{BAT}$ X $I_{VBAT}$ ≈ 1mV. This is negligible compared to the internal tolerance of 50mV on the $BV_{OVP}$ threshold.

If the Bat-OVP function is not required, the VBAT pin should be connected to VSS.

### Selection of $R_{CE}$:

The $\overline{CE}$ pin can be used to enable and disable the IC. If host control is not required, the $\overline{CE}$ pin can be tied to ground or left un-connected, permanently enabling the device.

In applications where external control is required, the $\overline{CE}$ pin can be controlled by a host processor. As in the case of the VBAT pin (see above), the $\overline{CE}$ pin should be connected to the host GPIO pin through a resistor as large as possible. The limitation on the resistor value is that the minimum $V_{OH}$ of the host GPIO pin less the drop across the resistor should be greater than $V_{IH}$ of the bq24308 $\overline{CE}$ pin. The drop across the resistor is given by $R_{CE}$ X $I_{IH}$.

### Selection of Input and Output Bypass Capacitors:

The input capacitor $C_{IN}$ in **Figure 1** and **Figure 2** is for decoupling, and serves an important purpose. Whenever there is a step change downwards in the system load current, the inductance of the input cable causes the input voltage to spike up. $C_{IN}$ prevents the input voltage from overshooting to dangerous levels. It is strongly recommended that a ceramic capacitor of at least 1µF be used at the input of the device. It should be located in close proximity to the IN pin.

$C_{OUT}$ in **Figure 1** and **Figure 2** is also important: If a very fast (< 1µs rise-time) overvoltage transient occurs at the input, the current that charges $C_{OUT}$ causes the device's current-limiting loop to kick in, reducing the gate-drive to FET Q1. This results in improved performance for input overvoltage protection. $C_{OUT}$ should also be a ceramic capacitor of at least 1µF, located close to the OUT pin. $C_{OUT}$ also serves as the input decoupling capacitor for the charging circuit downstream of the protection IC.

### PCB Layout Guidelines:

1. This device is a protection device, and is meant to protect down-stream circuitry from hazardous voltages. Potentially, high voltages may be applied to this IC. It has to be ensured that the edge-to-edge clearances of PCB traces satisfy the design rules for the maximum voltages expected to be seen in the system.
2. The device uses SON packages with a PowerPAD™. For good thermal performance, the PowerPAD should be thermally coupled with the PCB ground plane. In most applications, this will require a copper pad directly under the IC. This copper pad should be connected to the ground plane with an array of thermal vias.
3. $C_{IN}$ and $C_{OUT}$ should be located close to the IC. Other components like $R_{BAT}$ should also be located close to the IC.

## REVISION HISTORY

NOTE: Page numbers of current version may differ from previous versions.

| Changes from Original (September 2009) to Revision A | Page |
|---|---|
| • Changed Units from V to A for Input and Output Current spec in Absolute Maximum Ratings table. | 2 |
| • Added ESD Withstand voltage specifications to Absolute Maximum Ratings table. | 2 |
| • Changed $V_{O(REG)}$ test condition, $I_{OUT}$ value from 50 mA to 250 mA | 3 |
| • Added $T_J$ = 0°C to 125°C to test conditions for $I_{OCP}$ spec. | 3 |
| • Changed $Q_{EXT}$ device symbol in the Input Reverse-Polarity Protection schematic. | 4 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| BQ24308DSGR | ACTIVE | WSON | DSG | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 125 | DAS | Samples |
| BQ24308DSGT | ACTIVE | WSON | DSG | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 125 | DAS | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

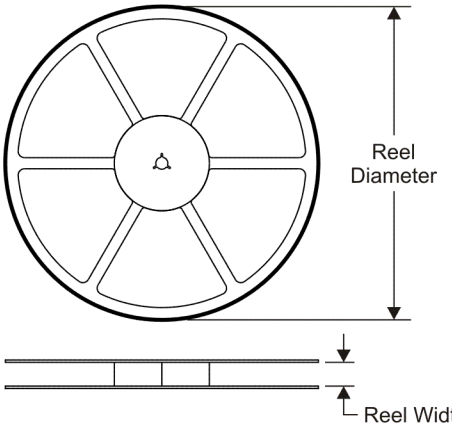
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

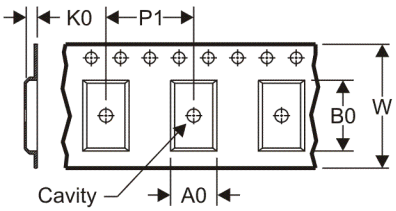
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

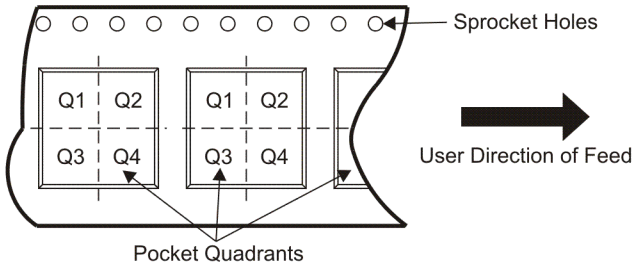



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

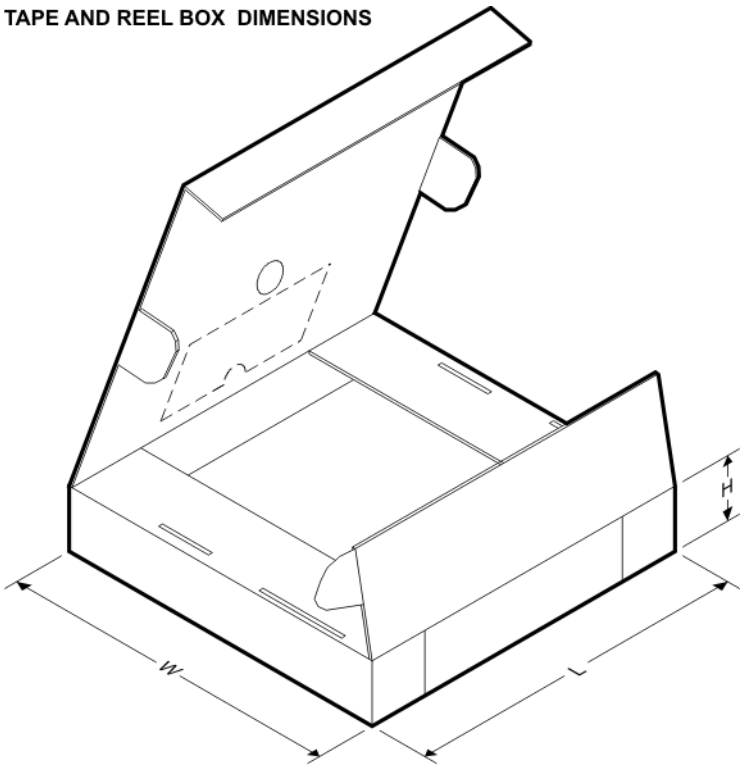
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BQ24308DSGR | WSON | DSG | 8 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| BQ24308DSGT | WSON | DSG | 8 | 250 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |

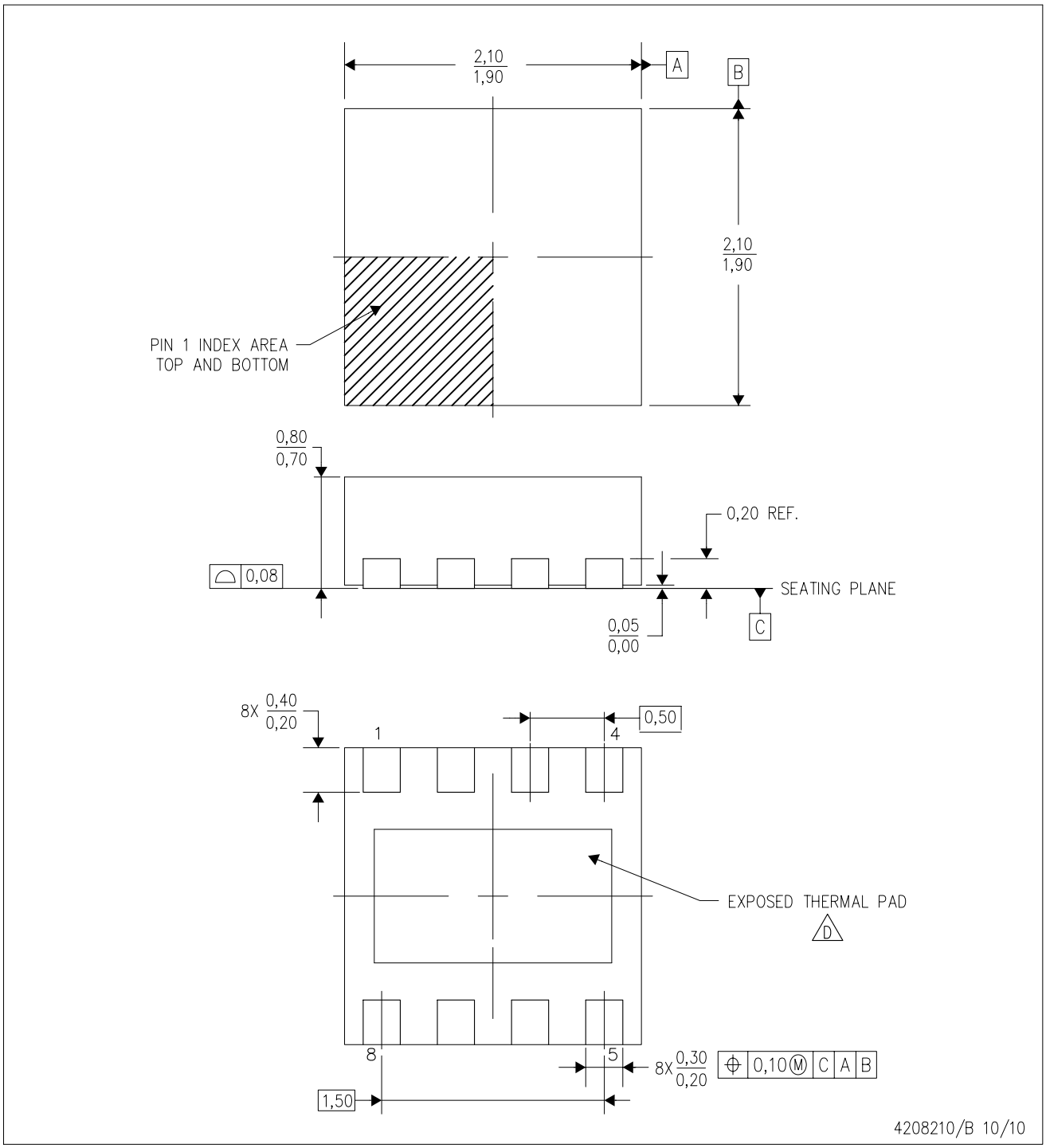
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| BQ24308DSGR | WSON | DSG | 8 | 3000 | 195.0 | 200.0 | 45.0 |
| BQ24308DSGT | WSON | DSG | 8 | 250 | 195.0 | 200.0 | 45.0 |

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–229.

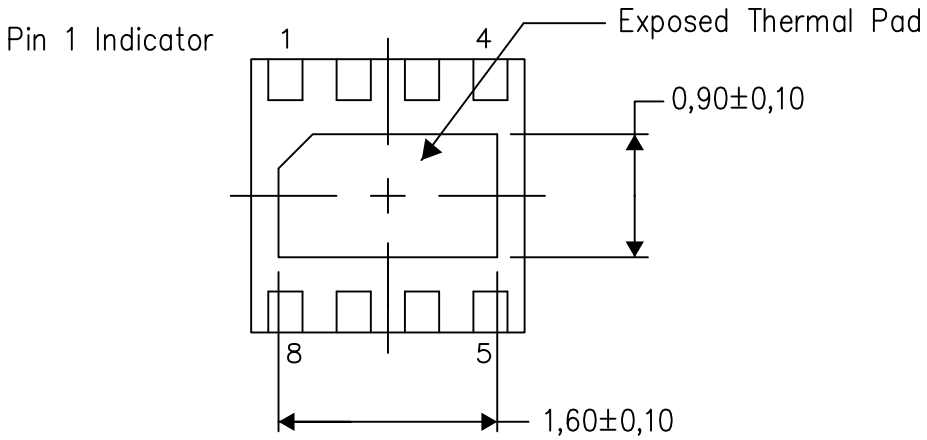
DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



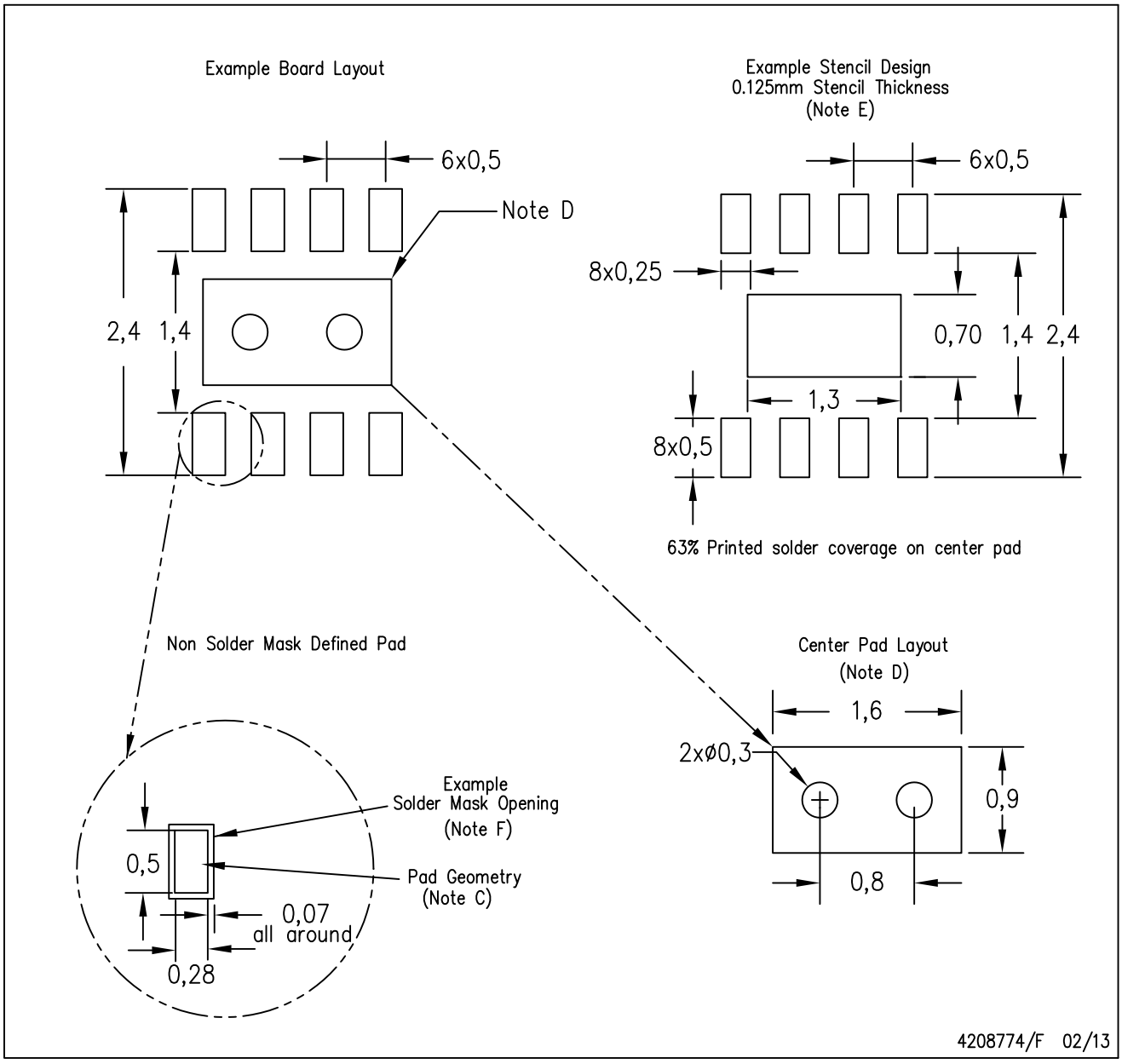

Bottom View

Exposed Thermal Pad Dimensions

4208347/G 08/13

NOTE: All linear dimensions are in millimeters

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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