Charger Detection Device with High Speed USB Switch Battery Charger Specification v1.2

Check for Samples: bq24392

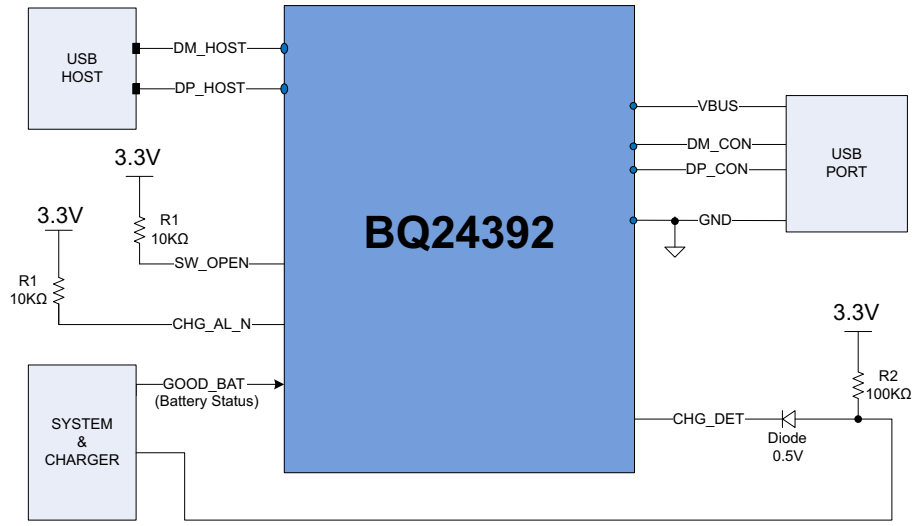
FEATURES

- Charger Detection Device
  - USB BCv1.2 Compliant
  - VBUS Detection
  - Data Contact Detection
  - Primary & Secondary Detection
  - Dead Battery Provision (DBP) 32-min Timer
- Switch
  - USB 2.0 High Speed Switch
- Compatible Accessories
  - Dedicated Charging Port
  - Standard Charging Port
  - Charging Port
- Other Chargers Detected
  - Apple™ Charger
  - TomTom™ Charger
  - Non Compliant USB Charger
- VBUS Voltage Range
  - –2V to 28V Tolerance on VBUS
- ESD Performance Tested per JESD 22
  - 4000-V Human-Body Model (A114-B, Class II)
  - 1500-V Charged-Device Model (C101)
- ESD Performance DP_CON/DM_CON to GND
  - ±8kV Contact Discharge (IEC 61000-4-2)

APPLICATIONS

- Cell Phones
- Smart-Phones
- Tablets
- Camera & GPS Systems

TYPICAL APPLICATION DIAGRAM



ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	µQFN 0.5-mm pitch – RSE	Tape and Reel	BQ24392RSER	APH

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

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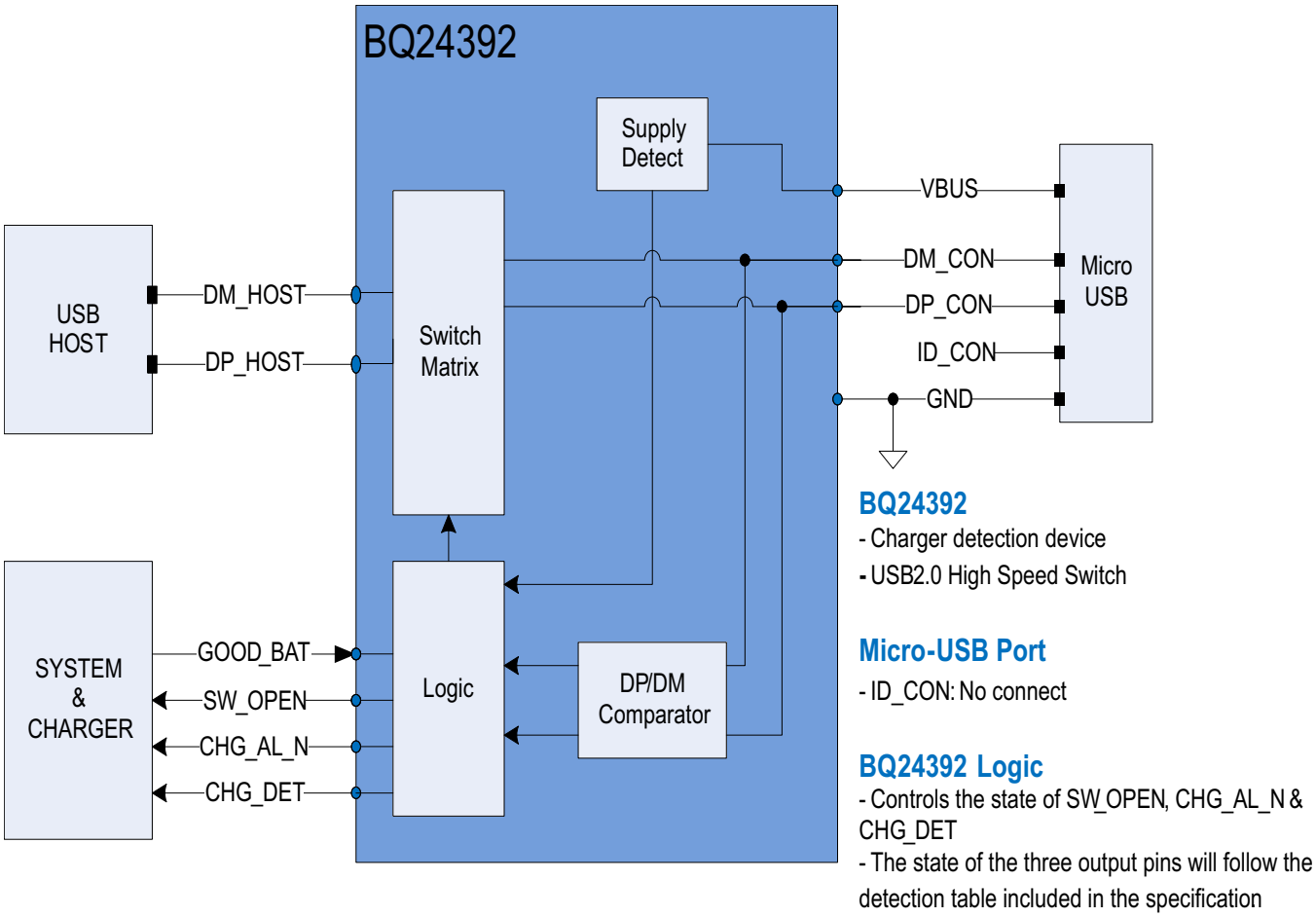
DESCRIPTION

The bq24392 is a charger detection device with an integrated isolation switch for use with a micro/mini USB port. The device is compliant with USB Battery Charging specification v1.2. This device allows cell phones and tablets to be charged from different adapters including USB BCv1.2 compliant and non-standard USB chargers. These non-standard chargers include Apple, TomTom, and non-compliant USB chargers. The bq24392 conforms to Dead Battery Provision (DBP) specified in BCv1.2. This includes a 32-min timer that cannot exceed 45 mins.

The bq24392 has a USB 2.0 switch that supports high speed. In addition to a USB connector and host pins, bq24392 has one input and three output pins. This results in a minimum software workload for the system to interact with the device.

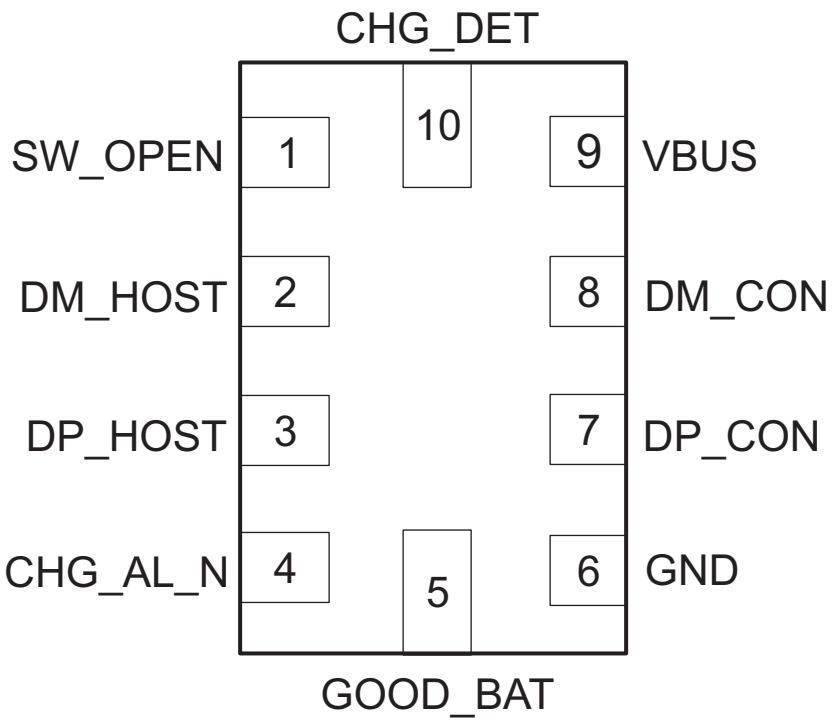
V_{BUS} has 28V tolerance to avoid external protection. Power for this device is supplied through VBUS when accessory is attached.

BLOCK DIAGRAM



PINOUT DIAGRAM

(TOP VIEW)



PIN DESCRIPTION

PIN		I/O	DESCRIPTION
NO.	NAME		
1	SW_OPEN	O	Open-drain output. 10kΩ external pull-up resistor. This pin indicates the status of the USB switch. SW_OPEN = LOW then switch is connected SW_OPEN = HIGH-Z then switch is not connected
2	DM_HOST	I/O	D– signal to transceiver
3	DP_HOST	I/O	D+ signal to transceiver
4	CHG_AL_N	O	Open-drain output add 10kΩ external pull-up resistor. This pin indicates when charging is allowed. CHG_AL_N = LOW then charging allowed CHG_AL_N = HIGH-Z then no charging
5	GOOD_BAT	I	Input from the system This pin indicates the status of the battery GOOD_BAT = LOW indicates a dead battery GOOD_BAT = HIGH indicates a good battery
6	GND		USB DM connected to USB receptacle
7	DP_CON	I/O	D+ signal from USB connector
8	DM_CON	I/O	D– signal from USB connector
9	VBUS	I	Supply pin from USB connector
10	CHG_DET	O	Push-pull output to the system This pin indicates if a charger is detected by the device CHG_DET = LOW indicates a charger is not detected CHG_DET = HIGH indicates a charger detected

SUMMARY OF TYPICAL CHARACTERISTICS

T_A = 25°C	USB Path (DP_CON and DM_CON)
ON-state resistance (r_{on})	8 Ω
ON-state resistance match (Δr_{on})	0.5 Ω
ON-state resistance flatness ($r_{on(flat)}$)	0.5 Ω
Bandwidth (BW)	920 MHz
OFF isolation (O_{ISO})	–26 dB at 250 MHz
Crosstalk (X_{TALK})	–32 dB at 250 MHz
Leakage current ($I_{IO(ON)}$)	50 nA

ABSOLUTE MAXIMUM RATINGS

over –40℃ to 85℃ temperature range (unless otherwise noted)

		ABSOLUTE MAX	UNIT
Pin voltage range	VBUS	–2 to 28	V
	CHG_AL_N	–2 to 28	V
	All Others	–0.3 to 7	V
ESD	HBM	4000	V
	CDM	1500	V
	IEC Contact Discharge (DP_CON, DM_CON to GND)	8000	V

RECOMMENDED OPERATING CONDITIONS

	MIN	MAX	UNIT
VBUS	4.75	5.25	V

THERMAL IMPEDANCE RATINGS

		RSE PACKAGE	UNIT
θ_{JA}	Package thermal impedance	184	°C/W

GENERAL ELECTRICAL SPECIFICATION

over –40℃ to 85℃ temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BUS_VALID}	VBUS Valid threshold	Rising VBUS threshold		3.5		V
V_{OH}	CHG_DET	I_{OH} = –2 mA	3.5		VBUS (1)	V
V_{OL}	CHG_DET, SW_OPEN, CHG_AL_N	I_{OL} = 2 mA			0.4	V
V_{IH}	GOOD_BAT		1.1			V
V_{IL}					0.5	V
R_{PD}		Internal pull-down resistor		950		kΩ
$I_{Q\text{-}SWON}$	Current consumption	VBUS = 5V; USB Switch ON; GOOD_BAT VIH Min = 1.1 V		250		µA
$I_{Q\text{-}SWON}$		VBUS = 5 V; USB Switch ON; GOOD_BAT VIH Min = 2.5 V		80		µA
$I_{Q\text{-}SWOFF}$		VBUS = 5 V; USB Switch OFF		45		µA
t_{DBP}	Dead battery provision timer			32	45	Mins

(1) CHG_DET Max value will be clamped at 7V when VBUS > 7V.

USB SWITCHING ELECTRICAL CHARACTERISTICS

V_{BUS} = 4.5V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
VUSBIO	Analog signal range			0		3.6	V
r_{ON}	ON-state resistance	DM_CON, DP_CON, DM_HOST, DP_HOST	VI = 0 V to 3.6 V, IO = –2 mA		8		Ω
Δr_{ON}	ON-state resistance match between channels	DM_CON, DP_CON, DM_HOST, DP_HOST	VI = 0.4 V, O = –2 mA		0.5		Ω
r_{ON}(flat)	ON-state resistance flatness	DM_CON, DP_CON, DM_HOST, DP_HOST	VI = 0 V to 3.6 V, IO = –2 mA		1.1		Ω
$I_{IO(OFF)}$	VI or VO OFF leakage current		VI = 0.3 V, VO = 2.7 V or VI = 2.7 V, VO = 0.3 V, Switch OFF		45		nA
$I_{IO(ON)}$	VO ON leakage current		VI = OPEN, VO = 0.3 V or 2.7 V, Switch ON		50		nA
DYNAMIC							
$C_{I(OFF)}$	VI OFF capacitance		DC bias = 0 V or 3.6 V, f = 10 MHz, Switch OFF		2		pF
$C_{O(OFF)}$	VO OFF capacitance		DC bias = 0 V or 3.6 V, f = 10 MHz, Switch OFF		10		pF
$C_{I(ON)}$, $C_{O(ON)}$	VI, VO ON capacitance		DC bias = 0 V or 3.6 V, f = 10 MHz, Switch ON		11		pF
BW	Bandwidth		R_L = 50 Ω, Switch ON		920		MHz
O_{ISO}	OFF Isolation		f = 240 MHz, R_L = 50 Ω, Switch OFF		–26		dB
X_{TALK}	Crosstalk		f = 240 MHz, R_L = 50 Ω		–30.5		dB

(1) V_O is equal to the asserted voltage on DP_CON, DM_CON pins.
V_I is equal to the asserted voltage on DP_HOST and DM_HOST pins.
I_O is equal to the current on the DP_CON, DM_CON.
I_I is equal to the current on the DP_HOST and DM_HOST pins.

GENERAL OPERATION

The bq24392 is designed to interface a micro/mini USB connector to external peripherals.

The device will automatically detect different types of chargers through the mini/micro USB pin connector. The bq24392 has a high speed USB 2.0 switch that can be automatically opened and closed based on the accessory detected.

DETECTION SEQUENCE

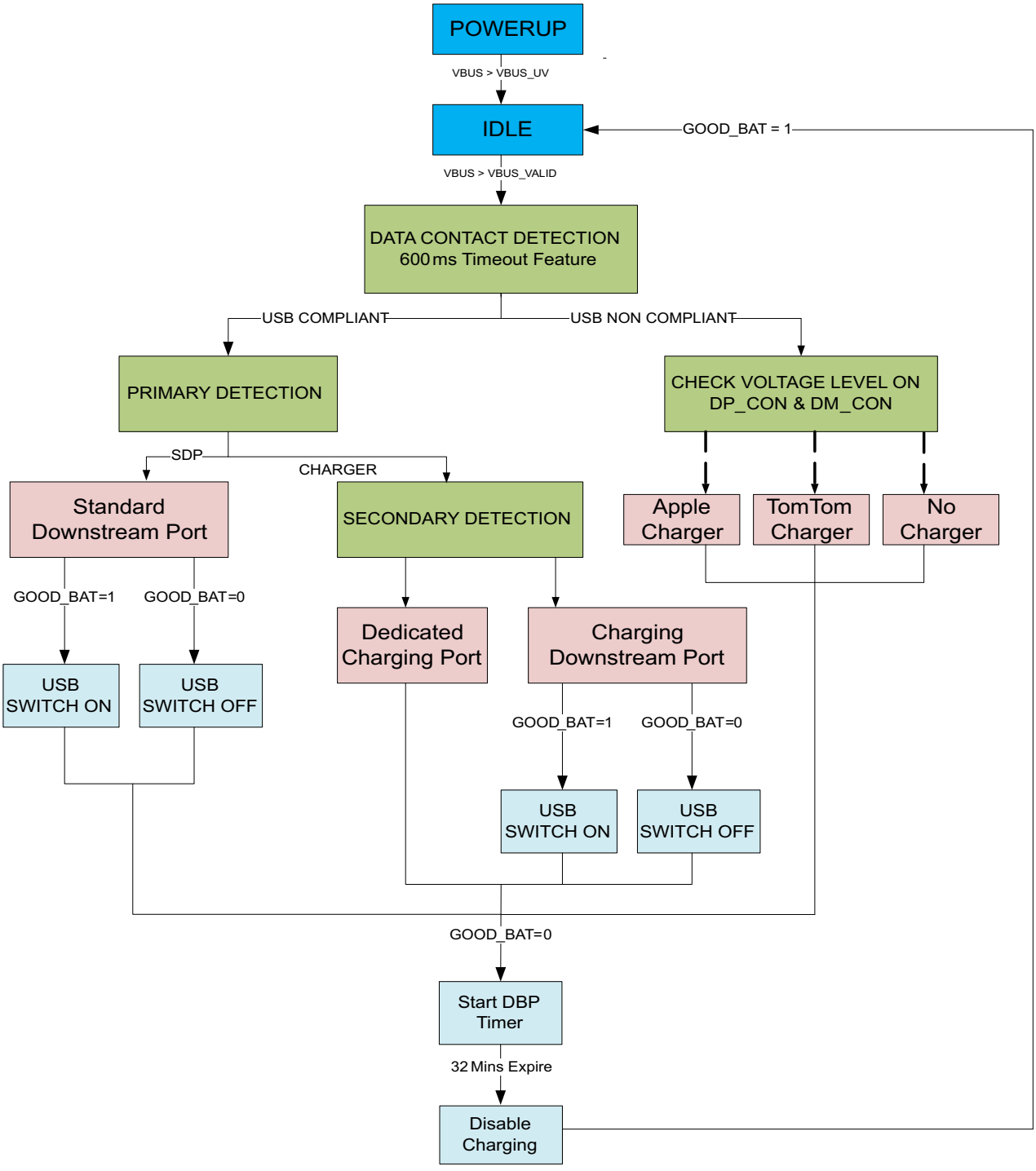
After accessory insertion, once VBUS voltage is greater than V_{BUS_VALID} threshold, the device proceeds onto data contact detection. This state has a 600ms timeout feature specified in BCDv1.2. Depending on the result, the next step is primary detection or non-compatible USB charger detection. In the case of former, the next step is detecting a Standard Downstream Port (SDP), Dedicated Charging Port (DCP), or Charging Downstream Port (CDP). In the case of latter, the next step is detecting an Apple, TomTom, or Non-compliant Charger.

The USB 2.0 switches are automatically closed to enable data transfer if either SDP or CDP is detected and the GOOD_BAT input is HIGH.

Once a charger has been detected, and if the GOOD_BAT input is LOW, a Dead Battery timer is initiated. If the GOOD_BAT continues to be LOW for 30 minutes (maximum of 45 minutes), charging is disabled. Toggling GOOD_BAT HIGH after DBP timer expires will re-start detection.

The following flow-chart shows the detection sequence used in the bq24392.

Flow Chart of Detection Sequence



Detection Table

The table below lists the configurations of the DP_CON (D+) and DM_CON (D–) that are internal to the various device types.

Device Type	VBUS	DP_CON (D+)	DM_CON (D–)	GOOD_BAT (Input)	CHG_AL_N (Output)	CHG_DET (Output)	SW_OPEN (Output)	Switch Status
Standard Downstream Port	>3.5V	Pull-down R to GND	Pull-down R to GND	HIGH	LOW	LOW	LOW	Connected
				LOW	LOW	LOW	Hi-Z	Not Connected
Charging Downstream Port	>3.5V	Pull-down R to GND	V_{DM_SRC}	HIGH	LOW	HIGH	LOW	Connected
				LOW	LOW	HIGH	Hi-Z	Not Connected
Dedicated Charging Port	>3.5V	Short to D–	Short to D+	HIGH	LOW	HIGH	Hi-Z	Not Connected
				LOW	LOW	HIGH	Hi-Z	Not Connected
Apple Charger	>3.5V	$2.0 < V_{DP} < 2.8$	$2.0 < V_{DM} < 2.8$	HIGH	LOW	HIGH	Hi-Z	Not Connected
				LOW	LOW	HIGH	Hi-Z	Not Connected
TomTom Charger	>3.5V	$2.0 < V_{DP} < 3.1$	$2.0 < V_{DM} < 3.1$	HIGH	LOW	HIGH	Hi-Z	Not Connected
				LOW	LOW	HIGH	Hi-Z	Not Connected
PS/2 Charger	>3.5V	Pull-up R to VBUS	Pull-up R to VBUS	X	LOW	LOW	Hi-Z	Not Connected
Non-compliant USB Charger	>3.5V	Open	Open	X	LOW	LOW	Hi-Z	Not Connected
Any Device	<3.5V	Open	Open	X	Hi-Z	LOW	Hi-Z	Not Connected
Any Device DBP Timer Expired	>3.5V	X	X	LOW	Hi-Z	LOW	Hi-Z	Not Connected

USB 2.0 EYE DIAGRAM

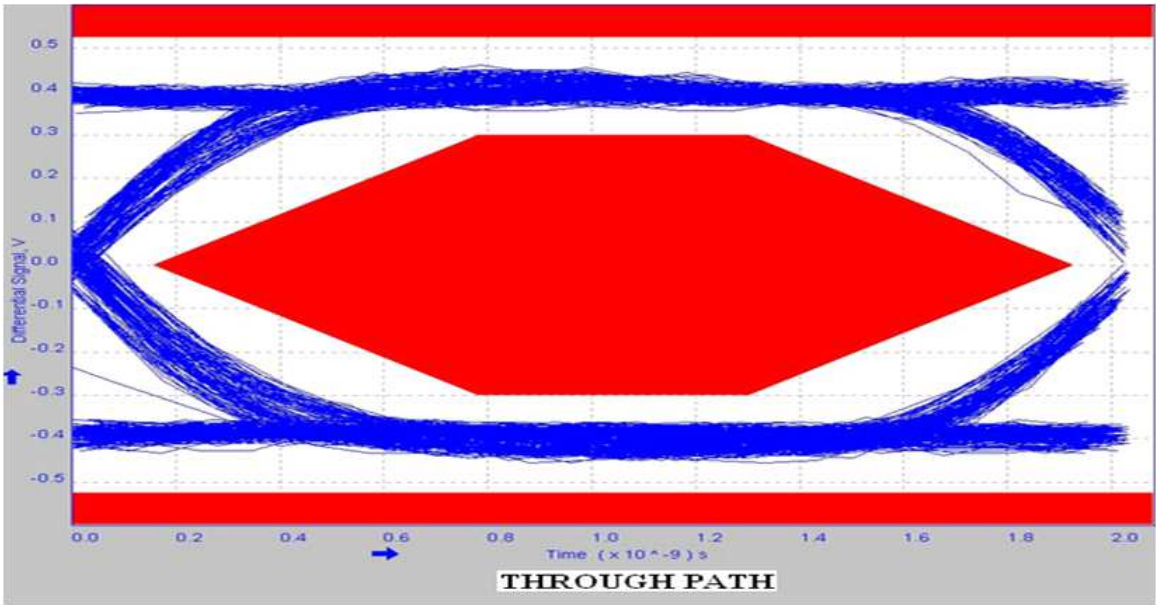


Figure 1. 480-Mbps USB 2.0 Eye Diagram with No Device

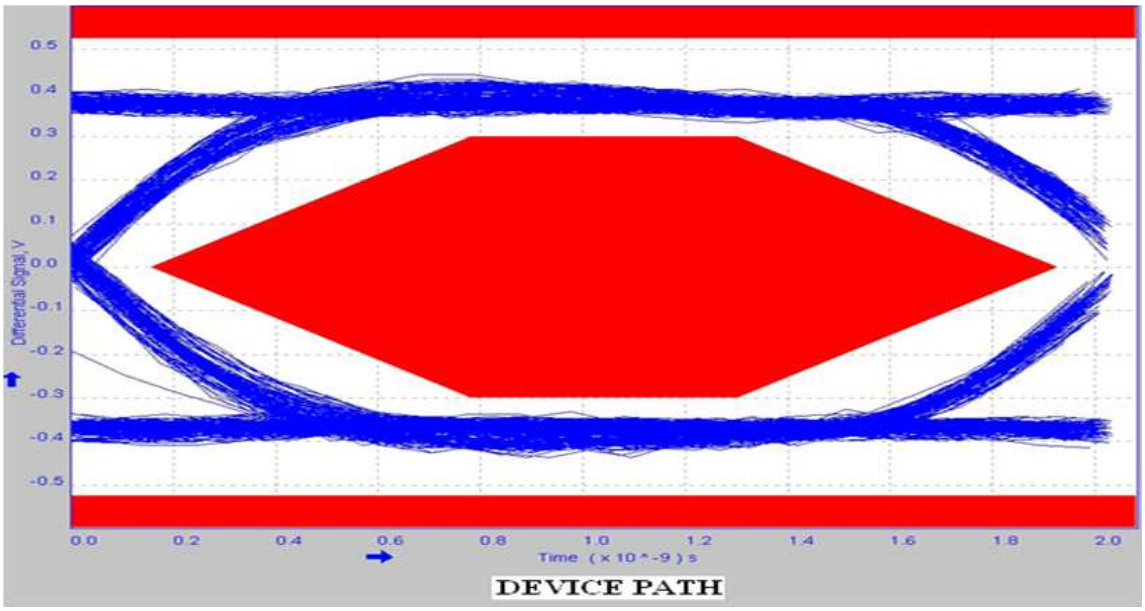


Figure 2. 480-Mbps USB 2.0 Eye Diagram with USB Switch

REFERENCE SCHEMATIC

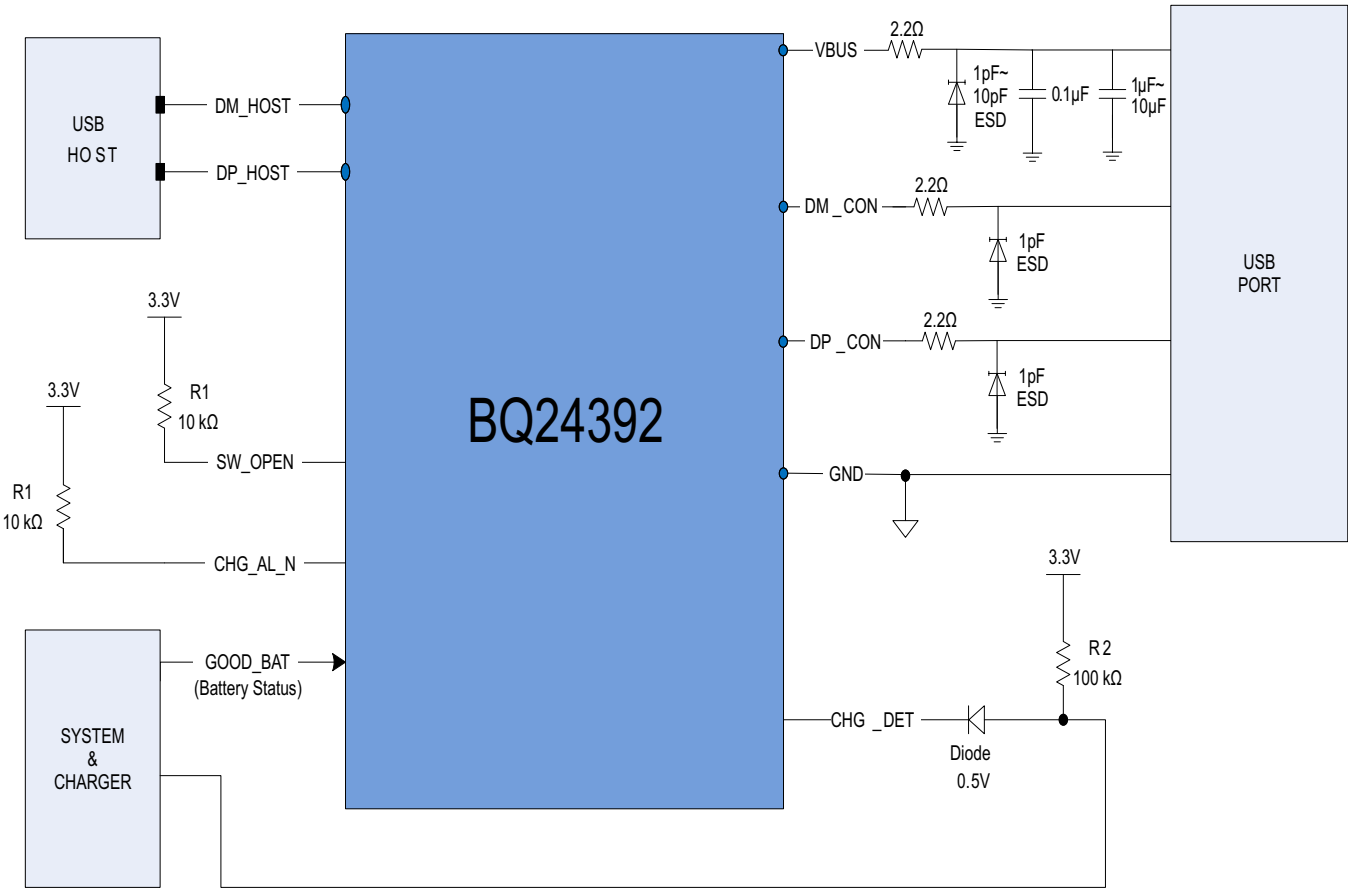


Table 1. Critical Components

PIN		
NAME	**NUMBER**	**CRITICAL COMPONENT**
V_{BUS}	9	1µF~10µF
		2.2Ω
		ESD Protection Diode
		0.1µF
SW_OPEN	1	10kΩ
CHG_AL_N	4	10kΩ
DM_CON	14	2.2Ω
		ESD Protection Diode
DP_CON	15	2.2Ω
		ESD Protection Diode

Schematic Guidelines

1. V_{BUS} requires 1µF~10µF and 0.1µF decoupling capacitors to reduce noise from circuit elements. The capacitors act as a shunt to block off the noise. The 0.1µF capacitor smooths out high frequencies and has a lower series inductance. The 1µF~10µF capacitor smooths out the lower frequencies and has a much higher series inductance. Using both capacitors will provide better load regulation across the frequency spectrum.
2. SW_OPEN and CHG_AL_N are open-drain outputs that require a 10kΩ pull-up resistor to VDDIO.
3. V_{BUS}, DM_CON, and DP_CON are recommended to have an external resistor of 2.2Ω to provide extra ballasting to protect the chip and internal circuitry.
4. DM_CON and DP_CON are recommended to have a 1pF external ESD Protection Diode rated for 8kV IEC protection to prevent failure in case of an 8kV IEC contact discharge.
5. V_{BUS_IN} is recommended to have a 1pF ~ 10pF external ESD Protection Diode rated for 8kV IEC protection to prevent failure in case of an 8kV IEC contact discharge.
6. CHG_DET is a push-pull output pin. An external pull-up and Diode are shown to depict a typical 3.3V system. The pull-up resistor and diode are optional. The pull-up range on the CHG_DET pin is from 3.5V to VBUS. When VBUS > 7V, CHG_DET will be clamped to 7V.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ24392RSER	ACTIVE	UQFN	RSE	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	APH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

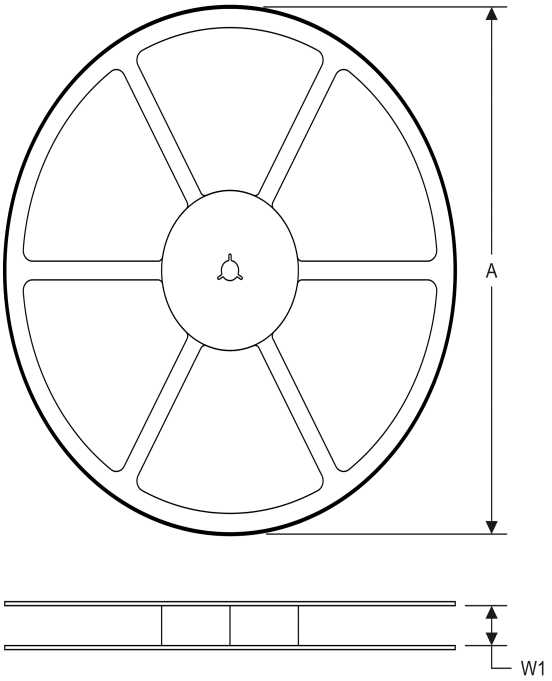
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

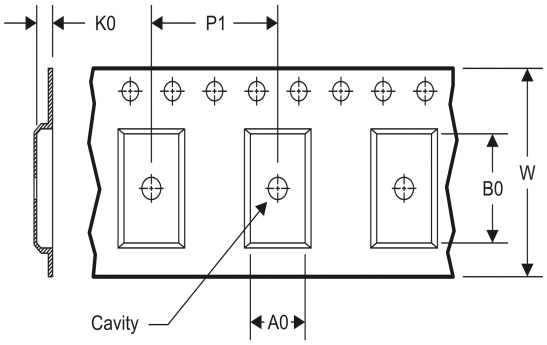
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



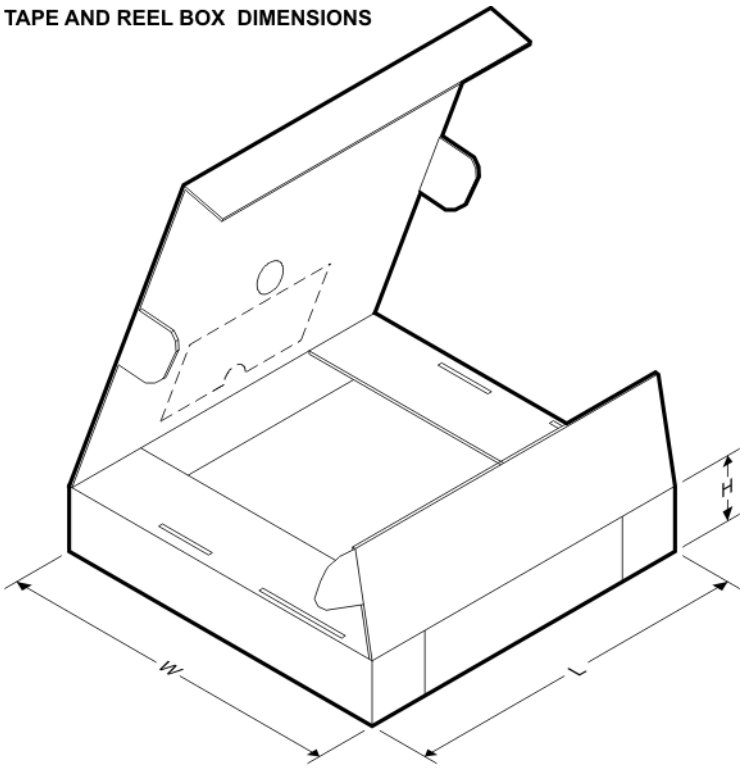
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24392RSER	UQFN	RSE	10	3000	180.0	8.4	1.68	2.13	0.76	4.0	8.0	Q1

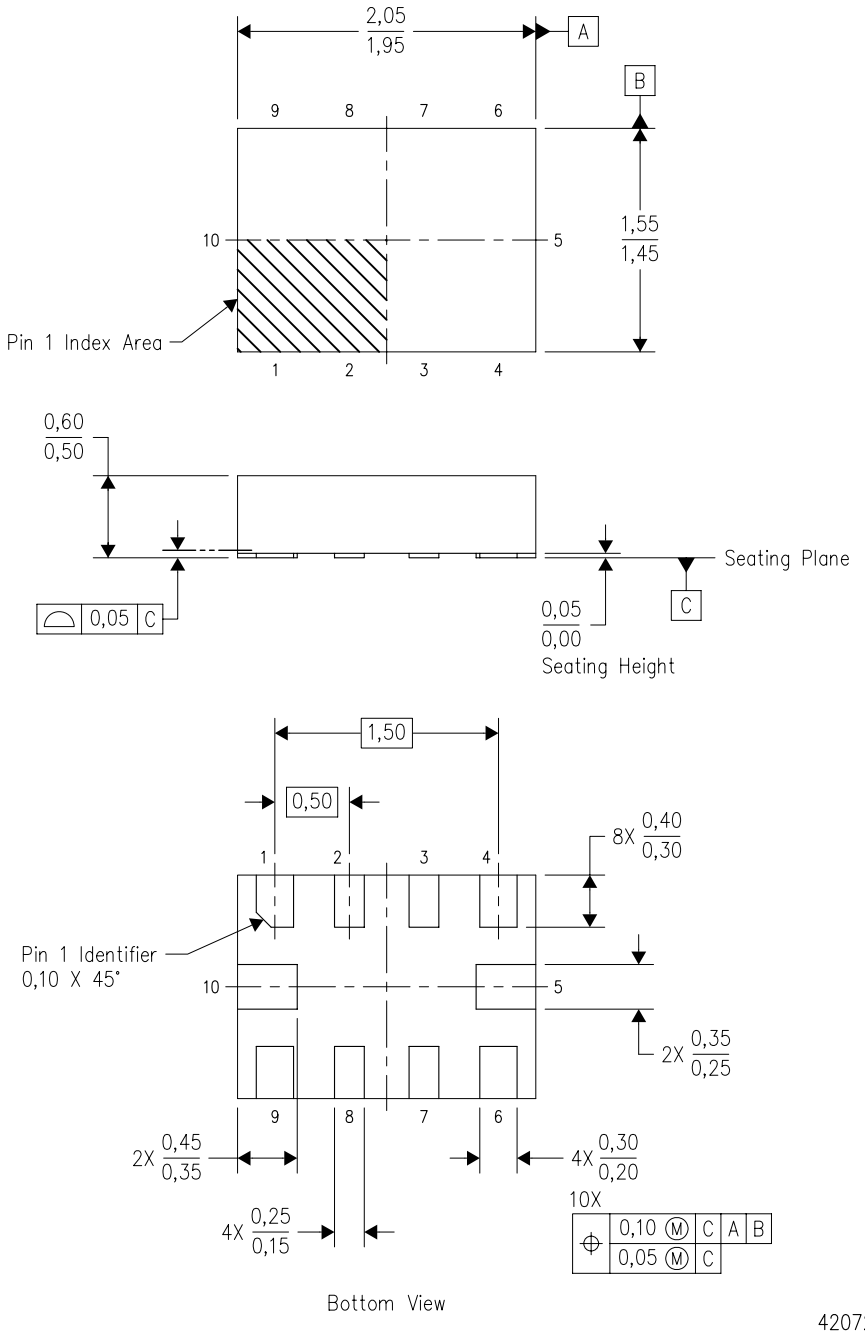
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24392RSER	UQFN	RSE	10	3000	202.0	201.0	28.0

RSE (R–PUQFN–N10) PLASTIC QUAD FLATPACK NO–LEAD



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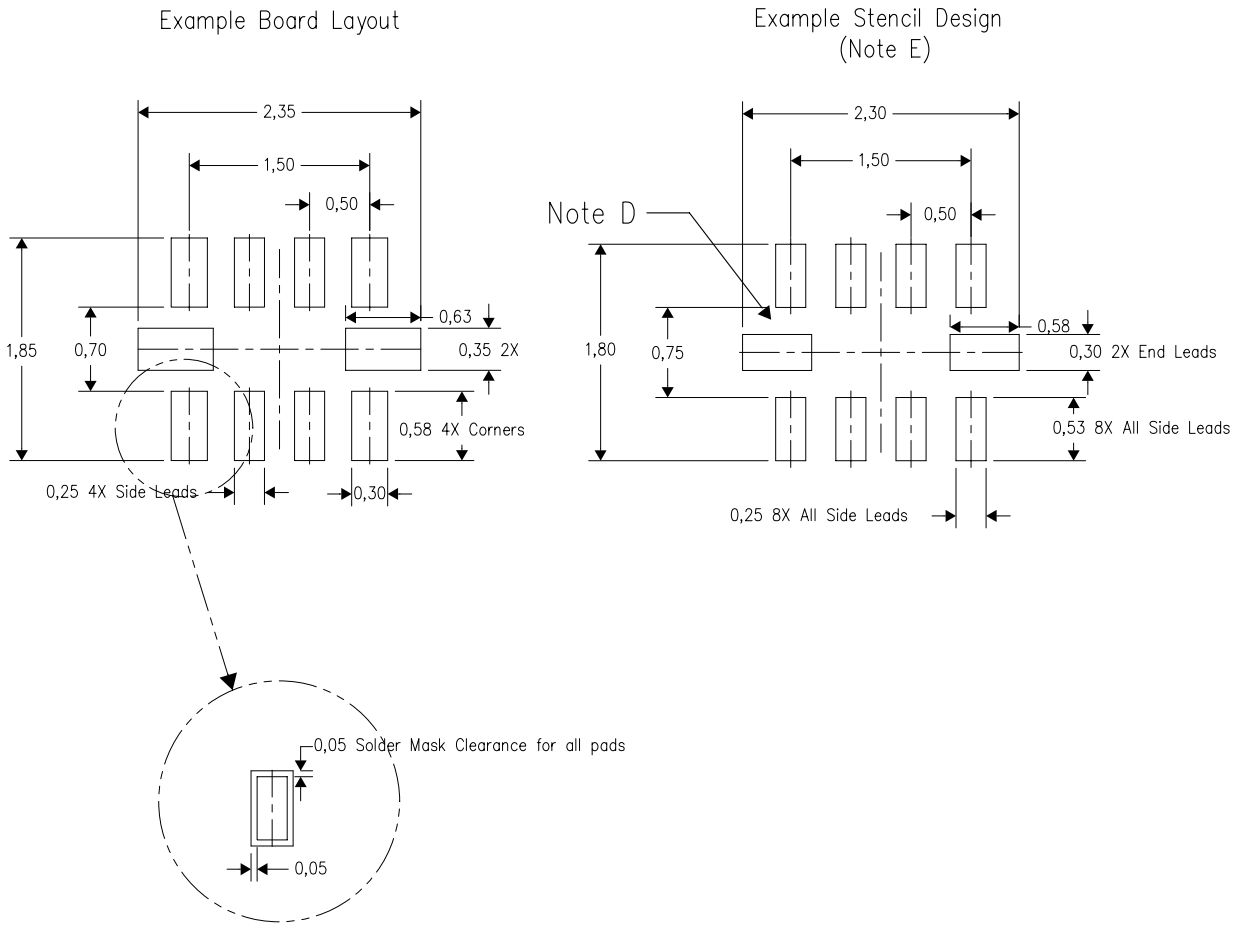
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation UEFD.

RSE (R–PUQFN–N10) PLASTIC QUAD FLATPACK NO–LEAD



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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