Ultra Low Power Boost Converter with Battery Management for Energy Harvester Applications

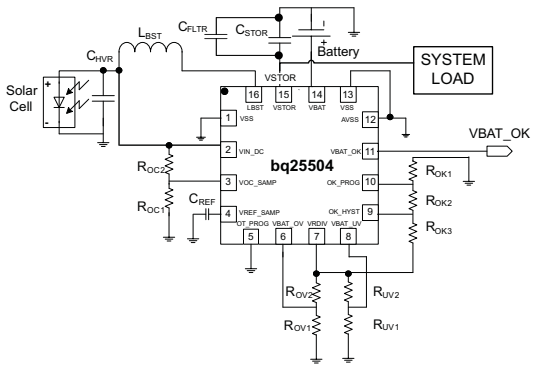
Check for Samples: bq25504

FEATURES

- Ultra Low Power With High Efficiency DC/DC Boost Converter/Charger
  - Continuous Energy Harvesting From Low Input Sources: V_{IN} ≥ 80 mV(Typical)
  - Ultra Low Quiescent Current: I_Q < 330 nA (Typical)
  - Cold-Start Voltage: V_{IN} ≥ 330 mV (Typical)
- Programmable Dynamic Maximum Power Point Tracking (MPPT)
  - Integrated Dynamic Maximum Power Point Tracking for Optimal Energy Extraction From a Variety of Energy Generation Sources
  - Input Voltage Regulation Prevents Collapsing Input Source
- Energy Storage
  - Energy can be Stored to Re-Chargeable Li-ion Batteries, Thin-film Batteries, Super-Capacitors, or Conventional Capacitors
- Battery Charging and Protection
  - User Programmable Undervoltage and Overvoltage Levels
  - On-Chip Temperature Sensor with Programmable Overtemperature Shutoff
- Battery Status Output
  - Battery Good Output Pin
  - Programmable Threshold and Hysteresis
  - Warn Attached Microcontrollers of Pending Loss of Power
  - Can be Used to Enable/Disable System Loads

APPLICATIONS

- Energy Harvesting
- Solar Charger
- Thermal Electric Generator (TEG) Harvesting
- Wireless Sensor Networks (WSN)
- Industrial Monitoring
- Environmental Monitoring
- Bridge and Structural Health Monitoring (SHM)
- Smart Building Controls
- Portable and Wearable Health Devices
- Entertainment System Remote Controls



DESCRIPTION

The bq25504 is the first of a new family of intelligent integrated energy harvesting Nano-Power management solutions that are well suited for meeting the special needs of ultra low power applications. The product is specifically designed to efficiently acquire and manage the microwatts (µW) to miliwatts (mW) of power generated from a variety of DC sources like photovoltaic (solar) or thermal electric generators. The bq25504 is the first device of its kind to implement a highly efficient boost converter/charger targeted toward products and systems, such as wireless sensor networks (WSN) which have stringent power and operational demands. The design of the bq25504 starts with a DCDC boost converter/charger that requires only microwatts of power to begin operating.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION CONTINUED

Once started, the boost converter/charger can effectively extract power from low voltage output harvesters such as thermoelectric generators (TEGs) or single or dual cell solar panels. The boost converter can be started with VIN as low as 330 mV, and once started, can continue to harvest energy down to V_{IN} = 80 mV.

The bq25504 also implements a programmable maximum power point tracking sampling network to optimize the transfer of power into the device. Sampling the VIN_DC open circuit voltage is programmed using external resistors, and held with an external capacitor (CREF).

For example solar cells that operate at maximum power point (MPP) of 80% of their open circuit voltage, the resistor divider can be set to 80% of the VIN_DC voltage and the network will control the VIN_DC to operate near that sampled reference voltage. Alternatively, an external reference voltage can be provide by a MCU to produce a more complex MPPT algorithm.

The bq25504 was designed with the flexibility to support a variety of energy storage elements. The availability of the sources from which harvesters extract their energy can often be sporadic or time-varying. Systems will typically need some type of energy storage element, such as a re-chargeable battery, super capacitor, or conventional capacitor. The storage element will make certain constant power is available when needed for the systems. The storage element also allows the system to handle any peak currents that can not directly come from the input source.

To prevent damage to a customer's storage element, both maximum and minimum voltages are monitored against the user programmed undervoltage (UV) and overvoltage (OV) levels.

To further assist users in the strict management of their energy budgets, the bq25504 toggles the battery good flag to signal an attached microprocessor when the voltage on an energy storage battery or capacitor has dropped below a pre-set critical level. This should trigger the shedding of load currents to prevent the system from entering an undervoltage condition. The OV, UV and battery good thresholds are programmed independently.

All the capabilities of bq25504 are packed into a small foot-print 16-lead 3 mm x 3 mm QFN package.

ORDERING INFORMATION

PART NO.	PACKAGE	ORDERING NUMBER (TAPE AND REEL)(1)	PACKAGE MARKING	QUANTITY
bq25504	QFN 16 pin 3 mm x 3 mm	BQ25504RGTR	B5504	3000
		BQ25504RGTT	B5504	250

(1) The RGW package is available in tape on reel. Add R suffix to order quantities of 3000 parts per reel, T suffix for 250 parts per reel.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Input voltage	VIN_DC, VOC_SAMP, VREF_SAMP, VBAT_OV, VBAT_UV, VRDIV, OK_HYST, OK_PROG, VBAT_OK, VBAT, VSTOR, LBST(2)	–0.3	5.5	V
Peak Input Power, P_{IN_PK}			400	mW
Operating junction temperature range, T_J		–40	125	°C
Storage temperature range, T_{STG}		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}/ground terminal.

THERMAL INFORMATION

THERMAL METRIC(1)(2)		bq25504 RGT (16 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	48.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	63.9	
θ_{JB}	Junction-to-board thermal resistance	22	
ψ_{JT}	Junction-to-top characterization parameter	1.8	
ψ_{JB}	Junction-to-board characterization parameter	22	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	6.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
$V_{IN\ (DC)}$	DC input voltage into VIN_DC(1)	0.13		3	V
VBAT	Battery voltage range(2)	2.5		5.25	V
C_{HVR}	Input capacitance	4.23	4.7	5.17	µF
C_{STOR}	Storage capacitance	4.23	4.7	5.17	µF
C_{BAT}	Battery pin capacitance or equivalent battery capacity	100			µF
C_{REF}	Sampled reference storage capacitance	9	10	11	nF
$R_{OC1} + R_{OC2}$	Total resistance for setting for MPPT reference.	18	20	22	MΩ
$R_{OK}1 + R_{OK}2 + R_{OK3}$	Total resistance for setting reference voltage.	9	10	11	MΩ
$R_{UV1} + R_{UV2}$	Total resistance for setting reference voltage.	9	10	11	MΩ
$R_{OV1} + R_{OV2}$	Total resistance for setting reference voltage.	9	10	11	MΩ
L_{BST}	Input inductance	19.8	22	24.2	µH
T_A	Operating free air ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		105	°C

(1) Maximum input power ≤ 300 mW. Cold start has been completed
(2) VBAT_OV setting must be higher than VIN_DC

ELECTRICAL CHARACTERISTICS

Over recommended temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for conditions of VIN_DC = 1.2V, VBAT = VSTOR = 3V. External components L_{BST} = 22 µH, C_{HVR} = 4.7 µF C_{STOR}= 4.7 µF.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BOOST CONVERTER \ CHARGER STAGE						
$V_{IN(DC)}$	DC input voltage into VIN_DC	Cold-start completed	130		3000	mV
$I_{IN(DC)}$	Peak Current flowing from V_{IN} into VIN_DC input	0.5V < V_{IN} < 3 V; VSTOR = 4.2 V		200	300	mA
P_{IN}	Input power range for normal charging	VBAT > VIN_DC; VIN_DC = 0.5 V	0.01		300	mW
$V_{IN(CS)}$	Cold-start Voltage. Input voltage that will start charging of VSTOR	VBAT < VBAT_UV; VSTOR = 0 V; 0°C < T_A < 85°C		330	450	mV
$P_{IN(CS)}$	Minimum cold-start input power to start normal charging	VBAT < VBAT_UV; VSTOR = 0 V; Input source impedance 0 Ω		10	50	µW
V_{STOR_CHGEN}	Voltage on VSTOR when cold start operation ends and normal charger operation begins		1.6	1.77	1.95	V
$R_{BAT(on)}$	Resistance of switch between VBAT and VSTOR when turned on.	VBAT = 4.2 V; VSTOR load = 50 mA			2	Ω
$R_{DS(on)}$	Charger Low Side switch ON resistance	VBAT = 2.1 V			2	Ω
		VBAT = 4.2 V			2	
	Charger rectifier High Side switch ON resistance	VBAT = 2.1 V			5	Ω
		VBAT = 4.2 V			5	
f_{SW_BST}	Boost converter mode switching frequency				1	MHz

ELECTRICAL CHARACTERISTICS (continued)

Over recommended temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for conditions of VIN_DC = 1.2V, VBAT = VSTOR = 3V. External components L_{BST} = 22 µH, C_{HVR} = 4.7 µF C_{STOR}= 4.7 µF.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BATTERY MANAGEMENT						
I_{VBAT}	Leakage on VBAT pin	VBAT = 2.1 V; VBAT_UV = 2.3 V, T_J = 25°C VSTOR = 0 V		1	5	nA
		VBAT = 2.1 V; VBAT_UV = 2.3 V, –40°C < T_J < 65°C, VSTOR = 0 V			80	nA
I_{VSTOR}	VSTOR Quiescent current Charger Shutdown in UV Condition	VIN_DC = 0V; VBAT < VBAT_UV = 2.4V; VSTOR = 2.2V, No load on VBAT		330	750	nA
	VSTOR Quiescent current Charger Shutdown in OV Condition	VIN_DC = 0V, VBAT > VBAT_OV, VSTOR = 4.25, No load on VBAT		570	1400	nA
V_{BAT_OV}	Programmable voltage range for overvoltage threshold (Battery voltage is rising)	VBAT increasing	2.5		5.25	V
$V_{BAT\_OV\_HYST}$	Battery voltage overvoltage hysteresis threshold (Battery voltage is falling), internal threshold	VBAT decreasing	18	35	89	mV
V_{BAT_UV}	Programmable voltage range for under voltage threshold (Battery voltage is falling)	VBAT decreasing; VBAT_UV > V_{Bias}	2.2		VBAT_OV	V
$V_{BAT\_UV\_HYST}$	Battery under voltage threshold hysteresis, internal thershold	VBAT increasing	40	80	125	mV
V_{BAT_OK}	Programmable voltage range for threshold voltage for high to low transition of digital signal indicating battery is OK,	VBAT decreasing	VBAT_UV		VBAT_OV	V
$V_{BAT\_OK\_HYST}$	Programmable voltage range for threshold voltage for low to high transition of digital signal indicating battery is OK,	VBAT increasing	50		VBAT_OV-VBAT_UV	mV
$V_{BAT\_ACCURACY}$	Overall Accuracy for threshold values, UV, OV, VBAT_OK	Selected resistors are 0.1% tolerance	–5%		5%	
V_{BAT_OKH}	VBAT OK (High) threshold voltage	Load = 10 µA			VSTOR-200mV	V
V_{BAT_OKL}	VBAT OK (Low) threshold voltage	Load = 10 µA			100	mV
TSD_PROTL	The temperature at which the boost converter is disabled and the switch between VBAT and VSTOR is disconnected to protect the battery	OT_Prog = LO		65		°C
TSD_PROTH		OT_Prog = HI		120		
OT_Prog	Voltage for OT_PROG High setting		2			V
	Voltage for OT_PROG Low setting				0.3	V
BIAS and MPPT CONTROL STAGE						
VOC_sample	Sampling period of VIN_DC open circuit voltage			16		s
VOC_Settling	Sampling period of VIN_DC open circuit voltage			256		ms
VIN_Reg	Regulation of VIN_DC during charging	0.5 V <V_{IN} < 3 V; I_{IN} (DC) = 10 mA	–10%		10%	
VIN_shutoff	DC input voltage into VIN_DC when charger is turned off		40	80	130	mV
MPPT_Disable	Threshold on VOC_SAMP to disable MPPT functionality		VSTOR-15 mV			V
VBIAS	Voltage node which is used as reference for the programmable voltage thresholds	VIN_DC ≥ 0.5V; VSTOR ≥ 1.8 V	1.21	1.25	1.27	V

DEVICE INFORMATION

RGT PACKAGE
(TOP VIEW)

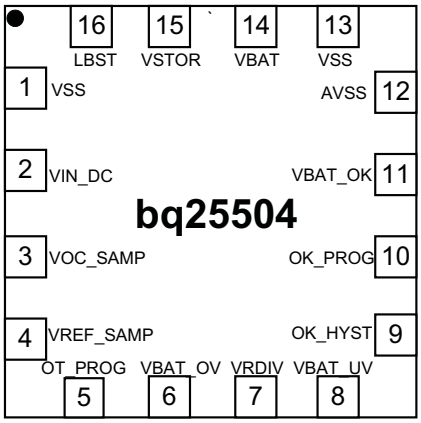


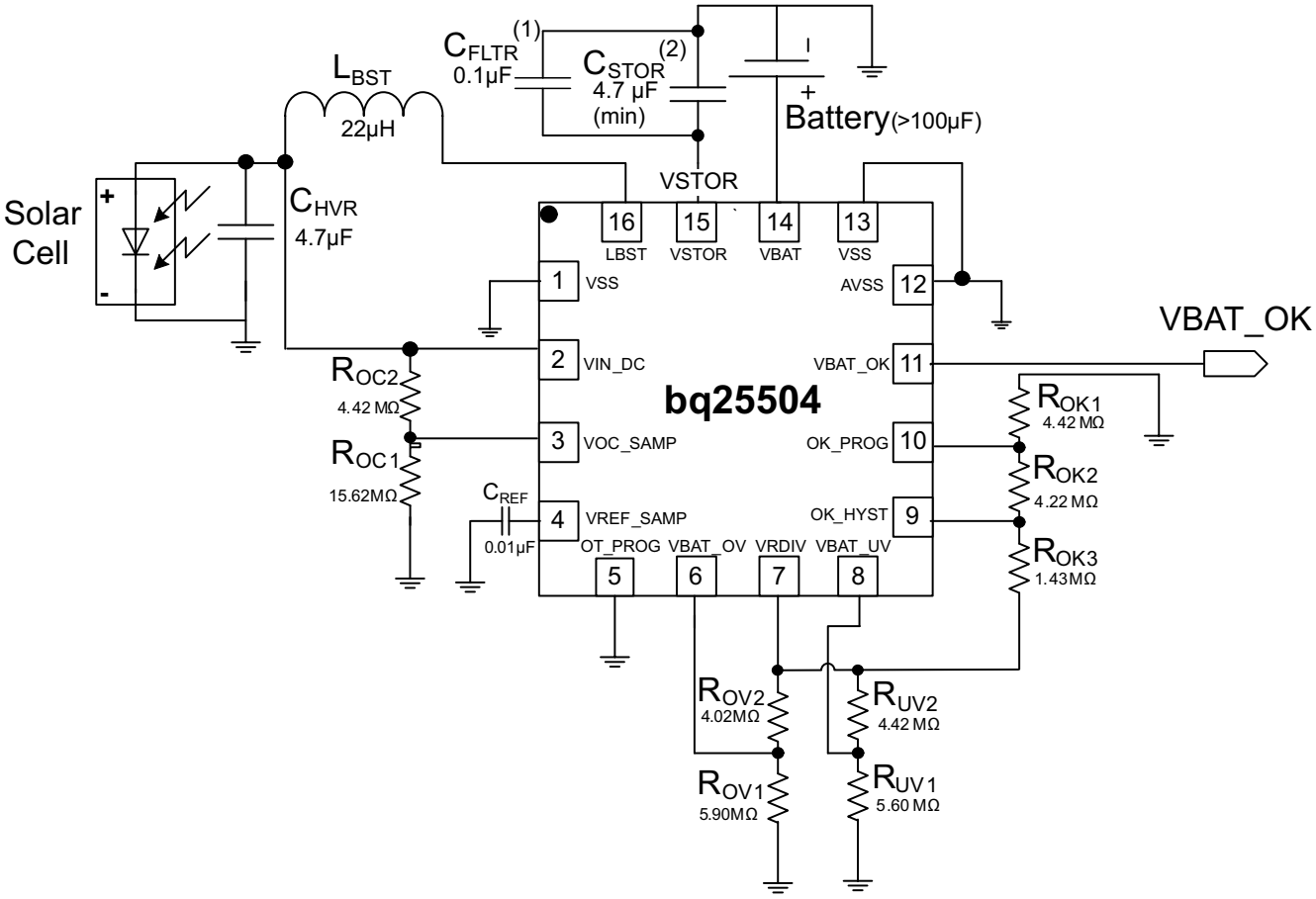
Figure 1. bq25504 3mm x 3mm QFN-16 Package

PIN FUNCTIONS

PIN		I/O TYPE	DESCRIPTION
NO.	NAME		
1	VSS	Input	General ground connection for the device
2	VIN_DC	Input	DC voltage input from energy harvesters
3	VOC_SAMP	Input	Sampling pin for MPPT network. To disable MPPT, connect to VSTOR
4	VREF_SAMP	Input	Switched node for holding the reference set by resistors on VOC_SAMP for MPPT. When MPPT is disabled, VREF_SAMP should not be left floating but either either be tied to an external reference voltage or tied to GND.
5	OT_PROG	Input	Digital Programming input for overtemperature threshold
6	VBAT_OV	Input	Resistor divider input for over voltage threshold
7	VRDIV	Output	Resistor divider biasing voltage.
8	VBAT_UV	Input	Resistor divider input for under voltage threshold
9	OK_HYST	Input	Resistor divider input for VBAT_OK hysteresis threshold
10	OK_PROG	Input	Resistor divider input for VBAT_OK threshold
11	VBAT_OK	Output	Digital battery good indicator referenced to VSTOR pin
12	AVSS	Supply	Signal ground connection for the device
13	VSS	Supply	General ground connection for the device
14	VBAT	I/O	Connection for storage elements
15	VSTOR	Output	Connection for the system load, output of the boost converter
16	LBST	Input	Inductor connection for the boost converter switching node

TYPICAL APPLICATION CIRCUITS

VIN_DC = 1.2 V, C_{STOR}= 4.7 µF, L_{BST}= 22 µH, C_{HVR}= 4.7 µF, C_{REF}= 10 nF, TSD_PROTL (65°C), MPPT (V_{OC}) = 80% VBAT_OV = 3.1 V, VBAT_UV = 2.2 V, VBAT_OK = 2.4 V, VBAT_OK_HYST = 2.8 V, R_{OK1} = 4.42 MΩ, R_{OK2} = 4.22 MΩ, R_{OK3} = 1.43 MΩ, R_{OV1} = 5.9 MΩ, R_{OV2} = 4.02 MΩ, R_{UV1}= 5.6 MΩ, R_{UV2} = 4.42 MΩ, R_{OC1}= 15.62 MΩ, R_{OC2} = 4.42 MΩ

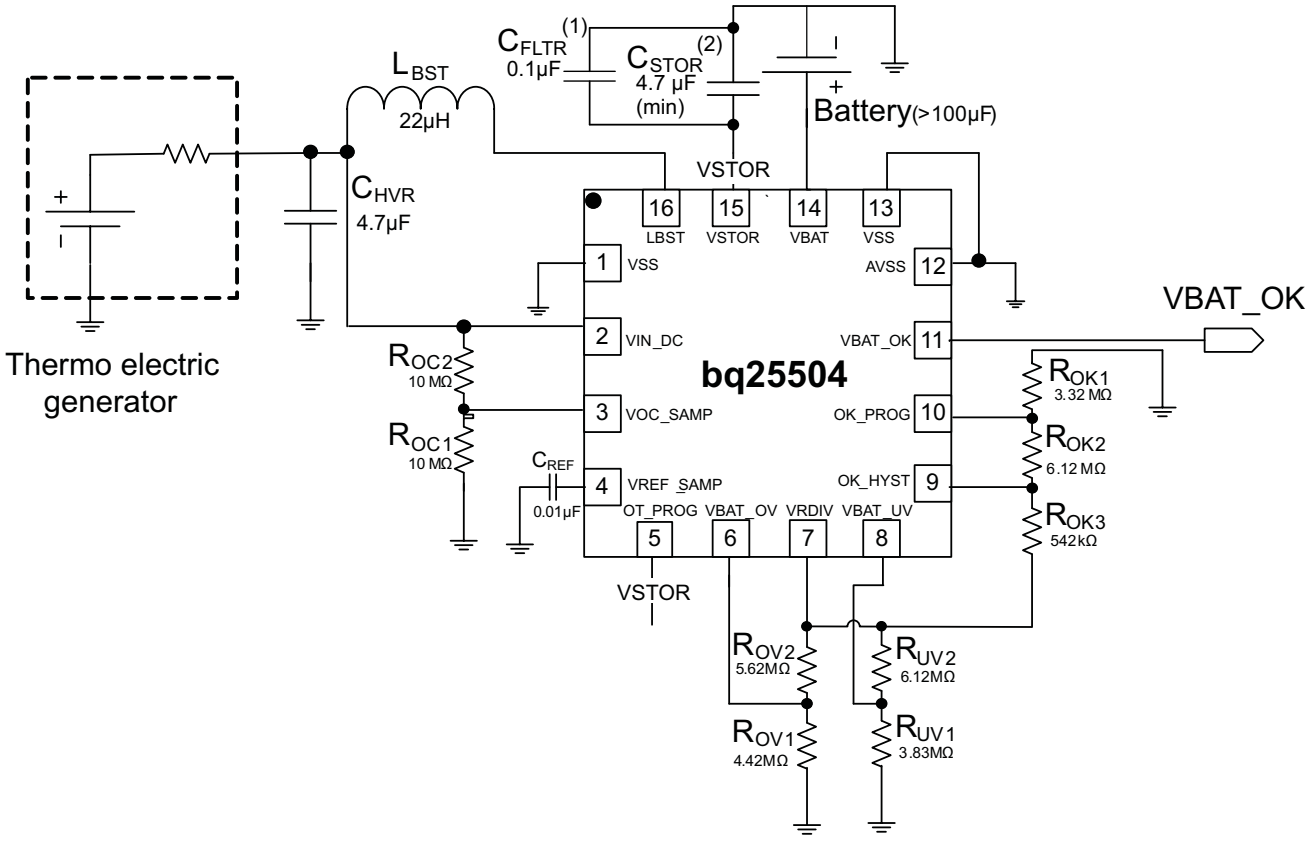


(1) Place close as possible to IC pin 15 (VSTOR) and pin 13 (VSS)

(2) See the Capacitor Selection section for guidance on sizing C_{STOR}

Figure 2. Typical Solar Application Circuit

VIN_DC = 0.5 V, C_{STOR} = 4.7 µF, L_{BST} = 22 µH, C_{HVR} = 4.7 µF, C_{REF} = 10 nF, TSD_PROTH (120°C), MPPT (V_{OC}) = 50% VBAT_OV = 4.2 V, VBAT_UV = 3.2 V, VBAT_OK = 3.5 V, VBAT_OK_HYST = 3.7 V, R_{OK1} = 3.32 MΩ, R_{OK2} = 6.12 MΩ, R_{OK3} = 0.542 MΩ, R_{OV1} = 4.42 MΩ, R_{OV2} = 5.62 MΩ, R_{UV1} = 3.83 MΩ, R_{UV2} = 6.12 MΩ, R_{OC1} = 10 MΩ, R_{OC2} = 10 MΩ

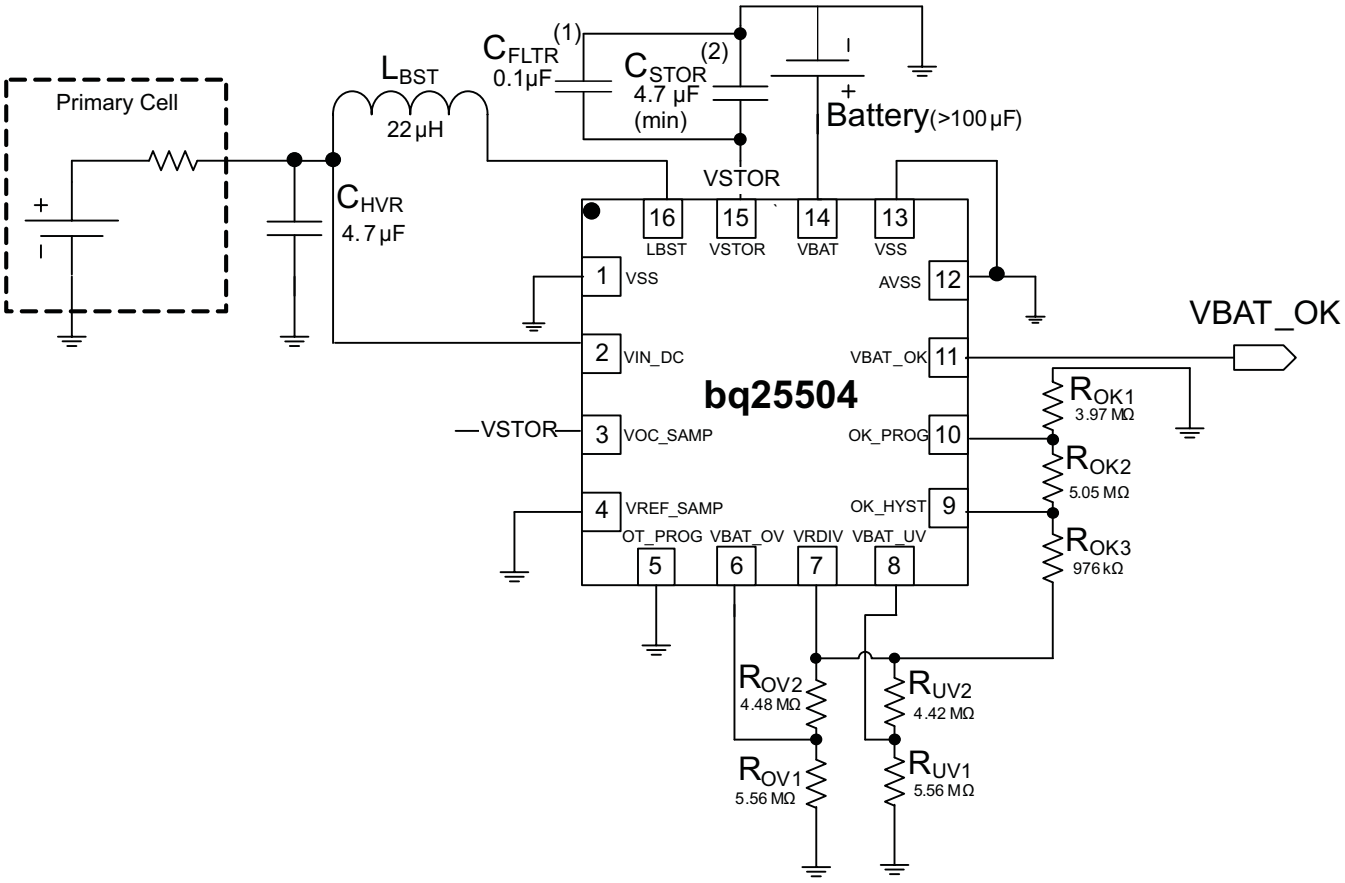


(1) Place close as possible to IC pin 15 (VSTOR) and pin 13 (VSS)

(2) See the Capacitor Selection section for guidance on sizing C_{STOR}

Figure 3. Typical TEG Application Circuit

VIN_DC = 1.2 V, C_{STOR} = 4.7 µF, L_{BST} = 22 µH, C_{HVR} = 4.7 µF, TSD_PROTL (65°C),
MPPT (V_{OC}) = Disabled VBAT_OV = 3.3 V, VBAT_UV = 2.2 V, VBAT_OK = 2.8 V, VBAT_OK_HYST = 3.1 V,
R_{OK1} = 3.97 MΩ, R_{OK2} = 5.05 MΩ, R_{OK3} = 0.976 MΩ, R_{OV1} = 5.56 MΩ,
R_{OV2} = 4.48 MΩ, R_{UV1} = 5.56 MΩ, R_{UV2} = 4.42 MΩ



(1) Place close as possible to IC pin 15 (VSTOR) and pin 13 (VSS)
(2) See the Capacitor Selection section for guidance on sizing C_{STOR}

Figure 4. Typical MPPT Disabled Application Circuit

HIGH-LEVEL FUNCTIONAL BLOCK DIAGRAM

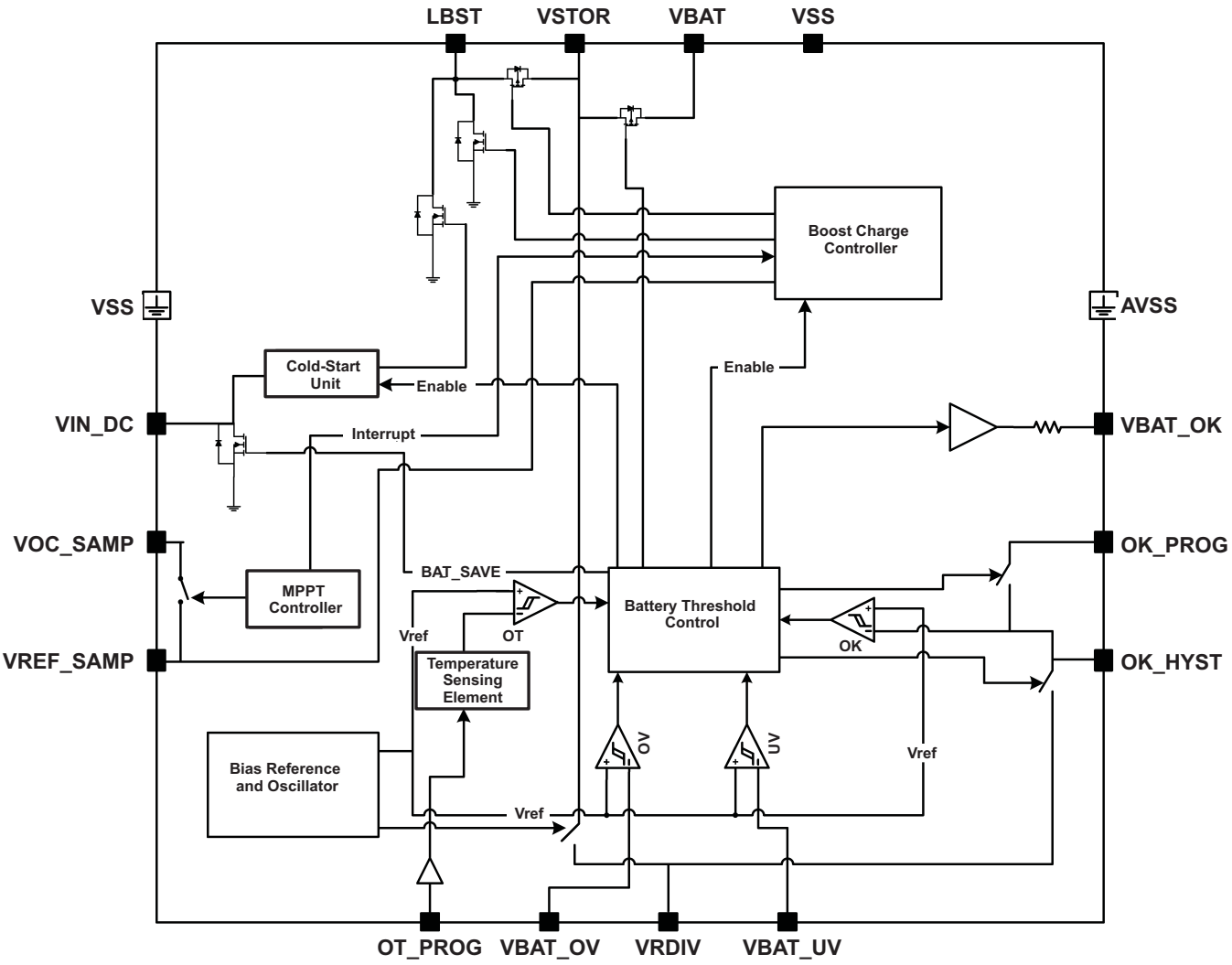


Figure 5. High-level Functional Diagram

TYPICAL CHARACTERISTICS

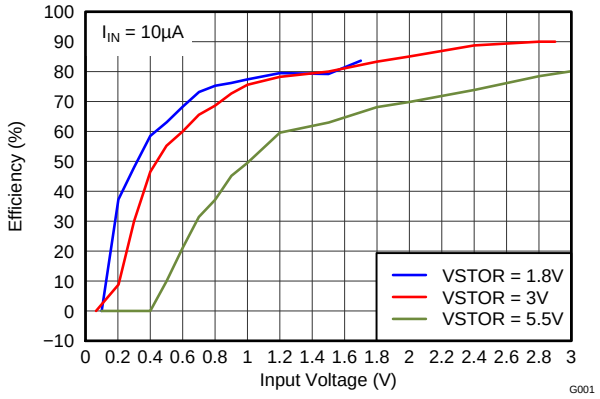


Figure 6. Efficiency vs Input Voltage

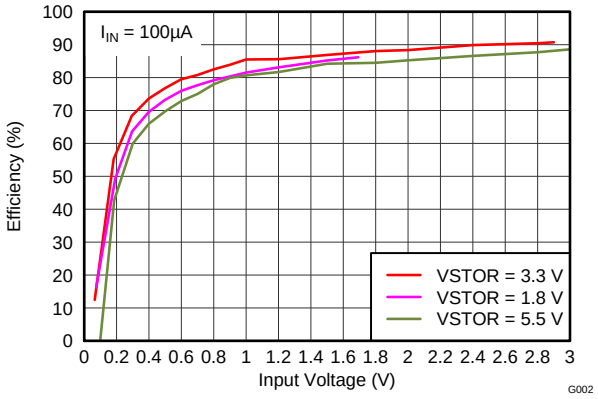


Figure 7. Efficiency vs Input Voltage

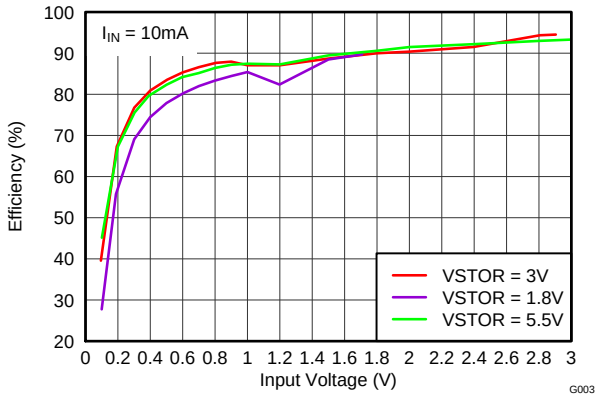


Figure 8. Efficiency vs Input Voltage

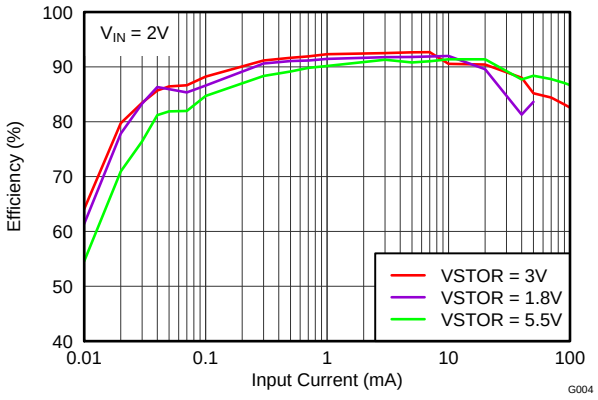


Figure 9. Efficiency vs Input Current

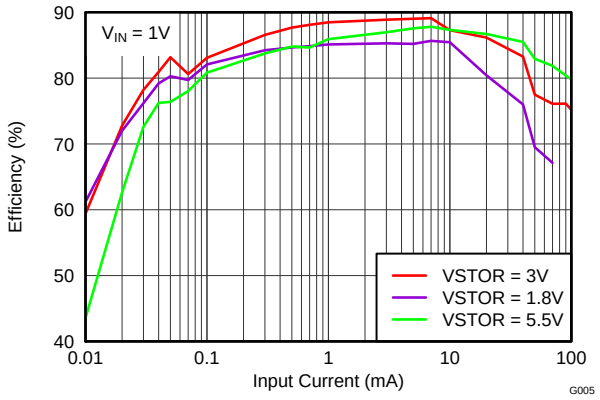


Figure 10. Efficiency vs Input Current

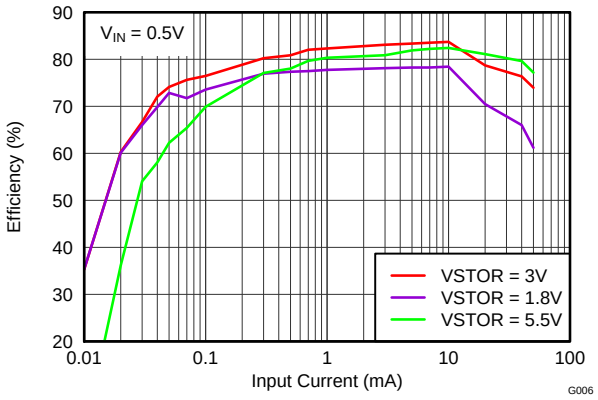


Figure 11. Efficiency vs Input Current

TYPICAL CHARACTERISTICS (continued)

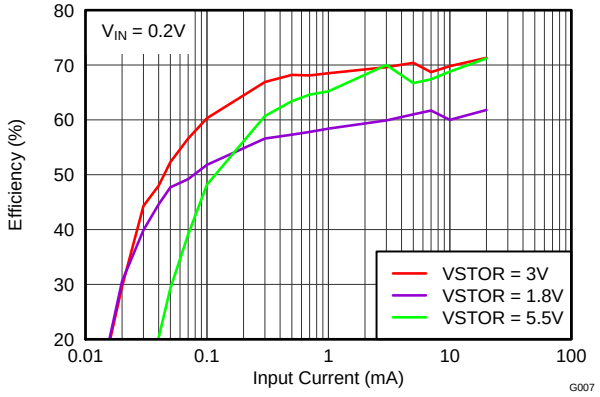


Figure 12. Efficiency vs Input Current

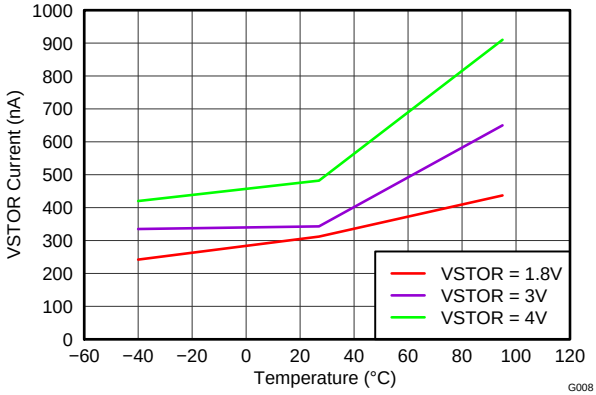


Figure 13. VSTOR Quiescent Current vs Temperature

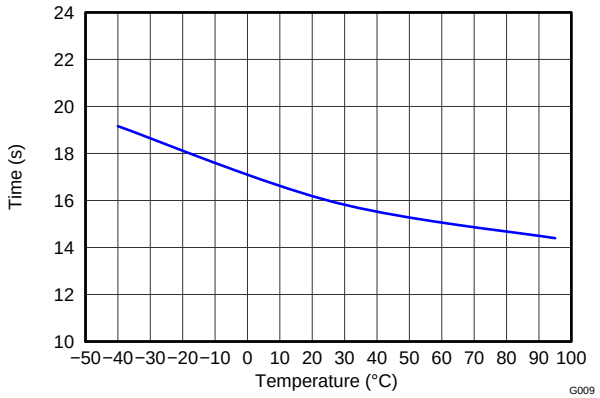


Figure 14. Sample Period vs Temperature

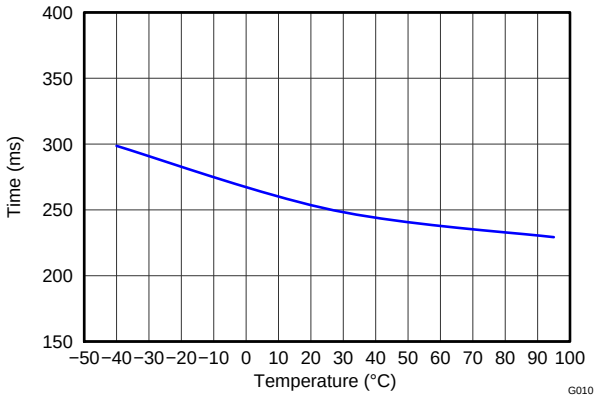


Figure 15. Settling Period vs Temperature

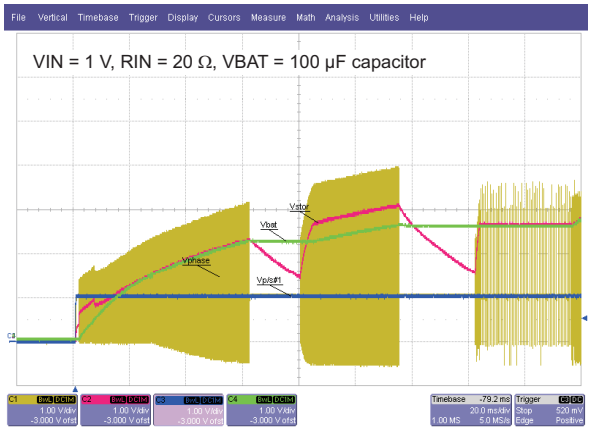


Figure 16. Example of Startup with no Battery and 10 KΩ Load

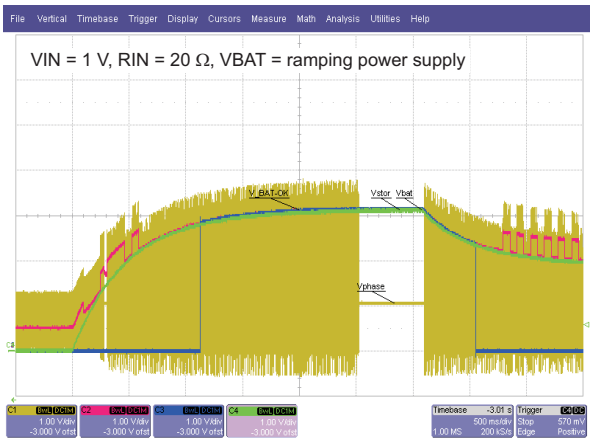


Figure 17. Example of VBAT_OK Operation, Ramping Battery From 0 V to 3.1 V

TYPICAL CHARACTERISTICS (continued)

Figure 18. Example of PFM Switching Converter Waveform

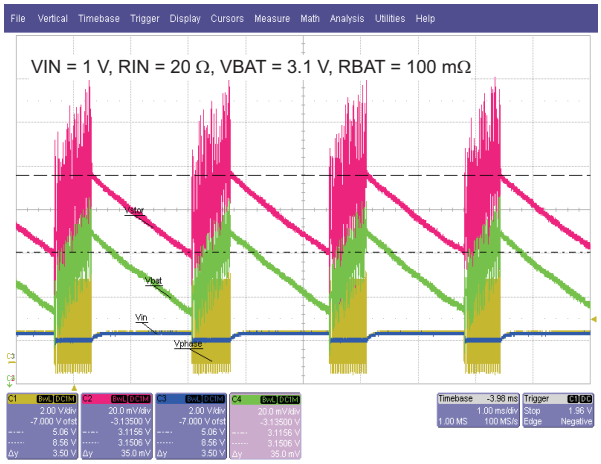


Figure 19. Example of Output Ripple Voltage During Operation at O V Setting

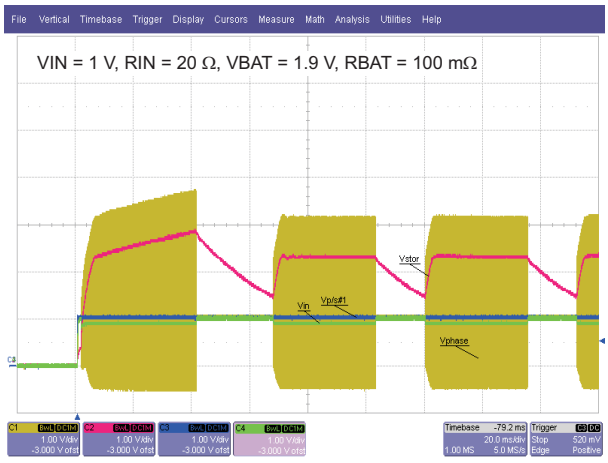


Figure 20. Example of Startup When VBAT is Held Below UV Setting

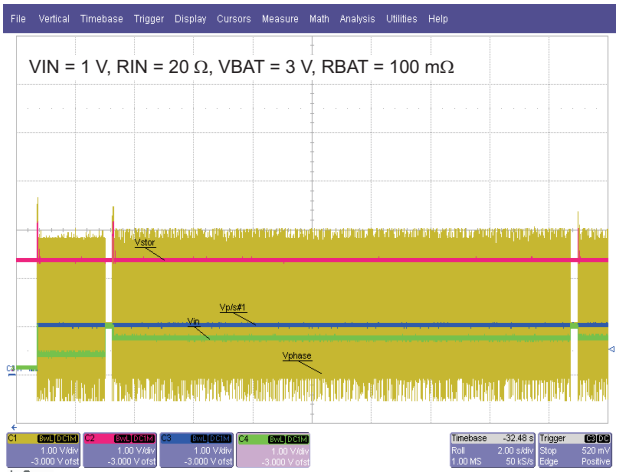


Figure 21. Example of Sampling Time for MPPT Operation

DETAILED PRINCIPLE OF OPERATION

OVERVIEW

The bq25504 is an ultra low quiescent current, efficient synchronous boost converter/charger. The boost converter is based on a switching regulator architecture which maximizes efficiency while minimizing start-up and operation power. The bq25504 uses pulse frequency modulation (PFM) to maintain efficiency, even under light load conditions. In addition, bq25504 also implements battery protection features so that either rechargeable batteries or capacitors can be used as energy storage elements. Figure 5 is a high-level functional block diagram which highlights most of the major functional blocks inside the bq25504.

Intended Operation

The bq25504's priority is to charge up the VSTOR capacitor, CSTOR, then power additional internal circuitry from VSTOR. When a storage element is attached (i.e. hot-plugged), the bq25504 will first attempt to charge up CSTOR from the storage element by turning on the internal PFET between the VSTOR and VBAT pins for approximately 45ms. See Storage Element section for guidance on selecting the storage element. If a system load tied to VSTOR prevent the storage element from charging VSTOR within 45 ms typical, it is recommended to add an external PFET between the system load and VSTOR. An inverted VBAT_OK signal can be used to drive the gate of the PFET. Once the VSTOR pin voltage reaches the user set under voltage threshold (VBAT_UV), the internal PFET stays on and the boost converter / charger begins to charge the storage element if there is sufficient power available at the VIN_DC pin, as explained below.If VSTOR does not reach VBAT_UV within 45 ms typical, then the PFET turns off and the Cold-Start subsystem turns on, also as explained below.

When no input source is attached, the VSTOR node should be discharged to ground before attaching a storage element. Hot-plugging a storage element that is charged (e.g., the battery protector is closed) and with VSTOR above ground results in the PFET between VSTOR and VBAT remaining off until a input source is attached and charging resumes. In addition, if a system load attached to VSTOR has fast transients that could pull VSTOR below VBAT_UV, the internal PFET switch will turn off in order to recharge the CSTOR capacitor. See the application section for guidance on sizing the VSTOR and/or VBAT capacitance to account for transients. If the voltage applied at VIN_DC is greater than VSTOR or VBAT then current may flow until the voltage at the input is reduced or the voltage at VSTOR and VBAT rise. This is considered an abnormal condition and the boost converter/charger does not operate.

Cold -Start Operation (VSTOR < V_{STOR_CHGN} and VIN_DC > $V_{IN(CS)}$)

When the voltage at pin VIN_DC exceeds the minimum input voltage with sufficient power, the cold-start subsystem turns on. The cold-start subsystem is essentially an unregulated boost converter. When the storage capacitor, CSTOR, voltage reaches V_{STOR_CHGEN} (1.8V typical), the main boost regulator starts up. The VSTOR voltage from the main boost regulator is now compared against battery undervoltage threshold (VBAT_UV). When the VBAT_UV threshold is reached, the PMOS switch between VSTOR and VBAT is turned on, which allows the energy storage element attached to VBAT to charge up. Cold start is not as efficient as the main boost regulator. If there is not sufficient power available it is possible that the cold start continuously runs and the VSTOR output does not increase to 1.8 V and start the main boost regulator.

Figure 22 shows the key threshold voltages. The battery management thresholds are explained later is this section.

Boost Converter, Charger Operation (VSTOR > V_{STOR_CHGN} and VIN_DC > $V_{IN(DC)-MIN}$)

The boost converter in bq25504 is used to charge the storage element attached at VBAT with the energy available from the DC input source. For the first 32 ms (typical) after the main converter is turned ON, the charger is disabled to let the input go up to its open-circuit voltage. This is needed to get the reference voltage which will be used for the remainder of the charger operation till the next MPPT sampling cycle turns ON. The boost converter employs pulse frequency modulation (PFM) mode of control to regulate the input voltage (VIN_DC) close to the desired reference voltage. The reference voltage is set by the MPPT control scheme as described in the next section. Input voltage regulation is obtained by transferring charge from the input to VSTOR only when the input voltage is higher than the voltage on pin VREF_SAMP. The current through the inductor is controlled through internal current sense circuitry. The peak current in the inductor is dithered internally to set levels to maintain high efficiency of the converter across a wide input current range. The converter nominally transfers up to a average of 100 mA of input current. The boost converter is disabled when the voltage on VSTOR reaches the OV condition to protect the battery connected at VBAT from overcharging.

Maximum Power Point Tracking

Maximum power point tracking (MPPT) is implemented in bq25504 in order to maximize the power extracted from an energy harvester source. MPPT is performed by periodically sampling a ratio of the open-circuit voltage of the energy harvester and using that as the reference voltage (VREF_SAMP) to the boost converter. The sampling ratio can be externally programmed using the resistors R_{OC1} and R_{OC2}. For solar harvesters, the resistive division ratio can be typically set between 0.7-0.8 and for thermoelectric harvesters; a resistive division ratio of 0.5 is typically used. The exact ratio for MPPT can be optimized to meet the needs of the input source being used.

Internally, the boost converter modulates the effective impedance of the energy transfer circuitry to regulate the input voltage (VIN_DC) to the sampled reference voltage (VREF_SAMP). A new reference voltage is obtained every 16s by periodically disabling the charger for 256ms and sampling a ratio of the open-circuit voltage. The reference voltage is set by the following expression:

$$VREF\_SAMP = VIN\_DC(OpenCircuit)\left(\frac{R_{OC1}}{R_{OC1} + R_{OC2}}\right) \quad (1)$$

The internal MPPT circuitry and the periodic sampling of VIN_DC can be disabled by tying the VOC_SAMP pin to VSTOR. When disabled an external reference voltage can be fed to the VREF_SAMP pin. The boost converter will then regulate VIN_DC to the externally provided reference. If input regulation is not desired, VREF_SAMP can be tied to GND.

Storage Element

When operating as a charger, the main storage elements must be connected to VBAT pin. Many types of elements can be used, such as capacitors, super capacitors or various battery chemistries. A storage element with 100uF equivalent capacitance is required to filter the pulse currents of the PFM switching converter. The equivalent capacitance of a battery can be computed as computed as C_{EQ} = 2 x $mAHr_{BAT(CHRGD)}$ x 3600 s/Hr / $V_{BAT(CHRGD)}$. In order for the storage element to be able to charge VSTOR capacitor (CSTOR) with in the 45ms window at hot-plug; therefore preventing the IC from entering cold start. The time constant created by he storage element's series resistance (plus the resistance of the internal PFET switch) and equivalent capacitance must be less than 45 ms (typical). For example, a battery's resistance can be computed as $R_{BAT} = V_{BAT} / I_{BAT(CONTIUOUS)}$ from the battery specifications. To take full advantage of the battery management, the load is normally tied to the VSTOR pin and not the VBAT pin. Also, if there are large load transients or the storage element has significant impedance then it may be necessary to increase the CSTOR capacitor from the 4.7uF minimum or add additional capacitance to VBAT in order to prevent a droop in the VSTOR voltage. See Capacitor Selection section in Application Information section for guidance on sizing the capacitor.

Battery Management

In this section the battery management functionality of the bq25504 integrated circuit (IC) is presented. The IC has internal circuitry to manage the voltage across the storage element and to optimize the charging of the storage element. For successfully extracting energy from the source, three different threshold voltages must be programmed using external resistors, namely the under voltage (UV) threshold, battery good threshold (VBAT_OK) and over voltage (OV) threshold. The three threshold voltages determine the region of operation of the IC. Figure 22 shows a plot of the voltage at the VSTOR pin and the various threshold voltages. For the best operation of the system, the VBAT_OK should be used to determine when a load can be applied or removed. A detailed description of the three voltage thresholds and the procedure for designing the external resistors for setting the three voltage thresholds are described next.

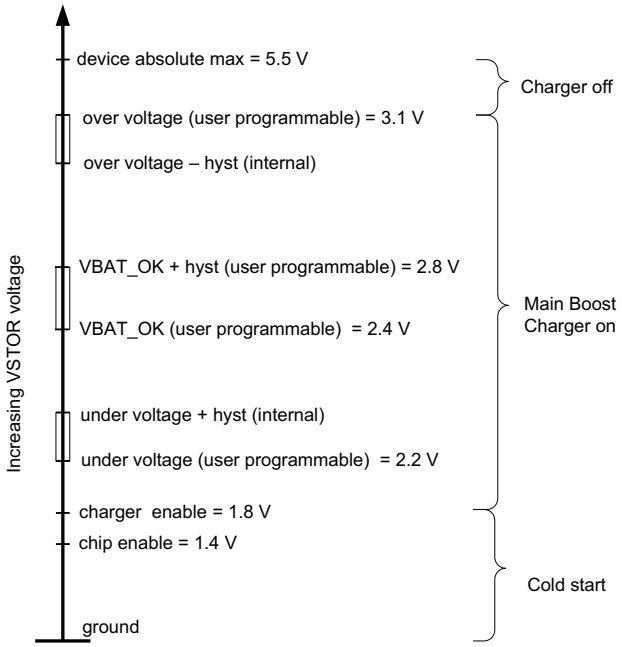


Figure 22. Figure Shows the Relative Position of Various Threshold Voltages (Threshold Voltages are From Typical Solar Application Circuit in Figure 2)

Battery Undervoltage Protection

To prevent rechargeable batteries from being deeply discharged and damaged, and to prevent completely depleting charge from a capacitive storage element, the undervoltage (VBAT_UV) threshold must be set using external resistors. The VBAT_UV threshold voltage when the battery voltage is decreasing is given by Equation 2:

$$VBAT\_UV = VBIAS\left(1 + \frac{R_{UV2}}{R_{UV1}}\right) \quad (2)$$

The sum of the resistors should be approximately, 10 MΩ that is, R_{UV1} + R_{UV2} = 10 MΩ. The undervoltage threshold when battery voltage is increasing is given by UV_HYST. It is internal set to the under voltage threshold plus an internal hysteresis voltage denoted by VBAT_UV_HYST. For proper functioning of the IC and the overall system, the load must be connected to the VSTOR pin while the storage element must be connected to the VBAT pin. Once the VSTOR pin voltage goes above the UV_HYST threshold, the VSTOR pin and the VBAT pins are shorted. The switch remains closed until the VSTOR pin voltage falls below the under voltage threshold. The VBAT_UV threshold should be considered a fail safe to the system and the system load should be removed or reduced based on the VBAT_OK signal.

Battery Overvoltage Protection

To prevent rechargeable batteries from being exposed to excessive charging voltages and to prevent over charging a capacitive storage element, the over-voltage (VBAT_OV) threshold level must be set using external resistors. This is also the voltage value to which the charger will regulate the VSTOR/VBAT pin when the input has sufficient power. The VBAT_OV threshold when the battery voltage is rising is given by Equation 3:

$$VBAT\_OV = \frac{3}{2}VBIAS\left(1 + \frac{R_{OV2}}{R_{OV1}}\right) \quad (3)$$

The sum of the resistors should be approximately 10 MΩ that is, R_{OV1} + R_{OV2} = 10 MΩ. The overvoltage threshold when battery voltage is decreasing is given by OV_HYST. It is internal set to the over voltage threshold minus an internal hysteresis voltage denoted by VBAT_OV_HYST. Once the voltage at the battery exceeds VBAT_OV threshold, the boost converter is disabled. The charger will start again once the battery voltage falls below the VBAT_OV_HYST level. When there is excessive input energy, the VBAT pin voltage will ripple between the VBAT_OV and the VBAT_OV_HYST levels.

CAUTION

If VIN_DC is higher than VSTOR and VSTOR is higher than VBAT_OV, the input VIN_DC is pulled to ground through a small resistance to stop further charging of the attached battery or capacitor. It is critical that if this case is expected, the impedance of the source attached to VIN_DC be higher than 20 Ω and not a low impedance source.

Battery Voltage in Operating Range (VBAT_OK Output)

The IC allows the user to set a programmable voltage independent of the overvoltage and undervoltage settings to indicate whether the VSTOR voltage (and therefore the VBAT voltage when the PFET between the two pins is turned on) is at an acceptable level. When the battery voltage is decreasing the threshold is set by Equation 4

$$VBAT\_OK\_PROG = VBIAS\left(1 + \frac{R_{OK2}}{R_{OK1}}\right) \quad (4)$$

When the battery voltage is increasing, the threshold is set by Equation 5

$$VBAT\_OK\_HYST = VBIAS\left(1 + \frac{R_{OK2} + R_{OK3}}{R_{OK1}}\right) \quad (5)$$

The sum of the resistors should be approximately 10 MΩ i.e., R_{OK1} + R_{OK2} + R_{OK3}= 10 MΩ. The logic high level of this signal is equal to the VSTOR voltage and the logic low level is ground. The logic high level has ~20 KΩ internally in series to limit the available current to prevent MCU damage until it is fully powered. The VBAT_OK_PROG threshold must be greater than or equal to the UV threshold. For the best operation of the system, the VBAT_OK should be setup to drive an external PFET between VSTOR and the system load in order to determine when the load can be applied or removed to optimize the storage element capacity.

Thermal Shutdown

Rechargeable Li-ion batteries need protection from damage due to operation at elevated temperatures. The application should provide this battery protection and ensure that the ambient temperature is never elevated greater than the expected operational range of 85°C.

The bq25504 uses an integrated temperature sensor to monitor the junction temperature of the device. If the OT_PROG pin is tied low, then the temperature threshold for thermal protection is set to TSD_ProtL which is 65°C typically. If the OT_PROG is tied high, then the temperature is set to TSD_ProtH which is 120°C typically. Once the temperature threshold is exceeded, the boost converter/charger is disabled and charging ceases. Once the temperature of the device drops below this threshold, the boost converter and or charger can resume operation. To avoid unstable operation near the overtemp threshold, a built-in hysteresis of approximately 5°C has been implemented. Care should be taken to not over discharge the battery in this condition since the boost converter/charger is disabled. However, if the supply voltage drops to the VBAT_UV setting, then the switch between VBAT and VSTOR will open and protect the battery even if the device is in thermal shutdown.

APPLICATION INFORMATION

INDUCTOR SELECTION

For the bq25504 to operate properly, an inductor of appropriate value must be connected between Pin 16 (LBST) and Pin 2 (VIN_DC) for the boost converter.

For the boost converter and or charger, the inductor must have an inductance = 22 µH and have a peak current capability of ≥250 mA with the minimum series resistance to keep high efficiency.

CAPACITOR SELECTION

In general, all the capacitors need to be low leakage. Any leakage the capacitors have will reduce efficiency, increase the quiescent current and diminish the effectiveness of the IC for energy harvesting.

VREF_SAMP Capacitance:

The MPPT operation depends on the sampled value of the open circuit voltage and the input regulation follows the voltage stored on the CREF capacitor. This capacitor is sensitive to leakage since the holding period is around 16 seconds. As the capacitor voltage drops due to any leakage, the input regulation voltage also drops preventing proper operation from extraction the maximum power from the input source. Therefore, it is recommended that the leakage be less than 2 nA at 3 V bias.

VIN_DC Capacitance:

Energy from the energy harvester input source is initially stored on a capacitor CHVR tied to Pin 2 (VIN_DC) and ground (VSS, Pin 1). For energy harvesters which have a source impedance which is dominated by a capacitive behavior, the value of the harvester capacitor should scaled according to the value of the output capacitance of the energy source, but an initial value of 4.7 µF is recommended.

:VSTOR Capacitance

Operation of the BQ25504 requires a two capacitors to be connected between Pin 15 (VSTOR) and ground. A high frequency bypass capacitor of at 0.01 µF should be placed as close as possible between VSTOR and GND. In addition, a bulk capacitor of at least 4.7 µF should be connected between Pin 15 and ground to assure stability of the boost converter, especially when the battery is fully charged and the converter in output voltage limiting mode.

Additional Capacitance on VSTOR or VBAT:

If there are large, fast system load transients and, or the storage element has high resistance, then the CSTOR capacitors may momentarily discharge below the VBAT_UV threshold in response to the transient. This causes the bq25504 to turn off the PFET switch between VSTOR and VBAT and turn on the boost converter. Of, the CSTOR capacitors may further discharge below the VSTOR_CHGEN threshold and cause the bq25504 to enter Cold Start. For instance, some Li-ion batteries or thin-film batteries may not have the current capacity to meet the surge current requirements of an attached low power radio. To prevent VSTOR from drooping, either increase the CSTOR capacitance or add additional capacitance in parallel with the storage element is recommended. For example, if the bq25504 is configured to charge the storage element to 4.2 V and a 500 mA load transient of 50 µs duration infrequently occurs, then, solving I = C x dv/dt for CSTOR gives :

$$\text{CSTOR} \geq 500\ \text{mA} \times 50\ \mu\text{s}/(4.2\ \text{V} - 1.8\ \text{V}) = 10.5\ \mu\text{F} \quad (6)$$

Note that increasing CSTOR is the recommended solution but will cause the bq25504 to operate in the less efficient Cold Start mode for a longer period at startup compared to using CSTOR = 4.7 µF. If longer Cold Start run times are not desired, then place the additional capacitance in parallel with the storage element.

For a recommended list of standard components, see the EVM User's guide (SLUU654).

LAYOUT CONSIDERATIONS

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the boost converter/charger could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground paths. The input and output capacitor, as well as the inductor should be placed as close as possible to the IC.

The resistors that program the thresholds should be placed as close as possible to the input pins of the IC to minimize parasitic capacitance to less than 2 pF.

To layout the ground, it is recommended to use short traces as well, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current. Assure that the ground traces are connected close to the device GND pin.

THERMAL CONSIDERATIONS

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below.

- Improving the power-dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

For more details on how to use the thermal parameters in the Thermal Table, check the Thermal Characteristics Application Note (SZZA017) and the IC Package Thermal Metrics Application Note (SPRA953).

REVISION HISTORY

Changes from Original (October 2011) to Revision A **Page**

- Added C_{FLTR} and Notes 1 and 2 to Figure 2 6
- Added C_{FLTR} and Notes 1 and 2 to Figure 3 7
- Added C_{FLTR} and Notes 1 and 2 to Figure 4 8
- Added the INTENDED OPERATION section 13
- Changed the Cold -Start Operation section 13
- Changed the Boost Converter, Charger Operation section 13
- Changed the Storage Element section 14
- Changed the CAPACITOR SELECTION section 17

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
BQ25504RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B5504	Samples
BQ25504RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	B5504	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

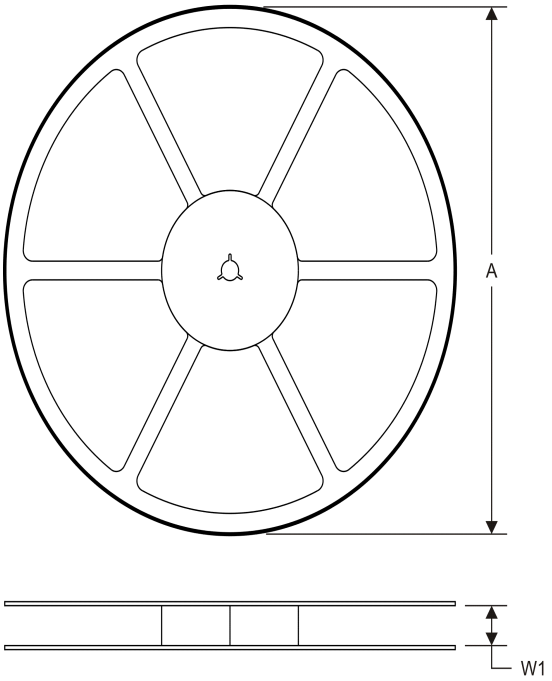
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

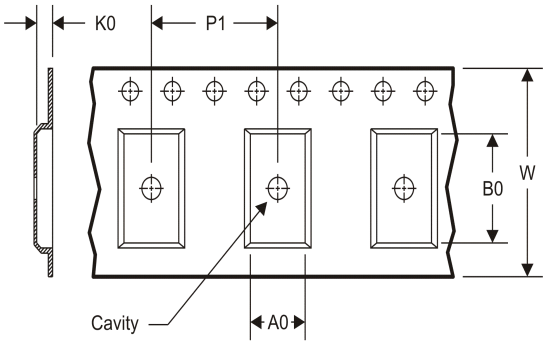
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



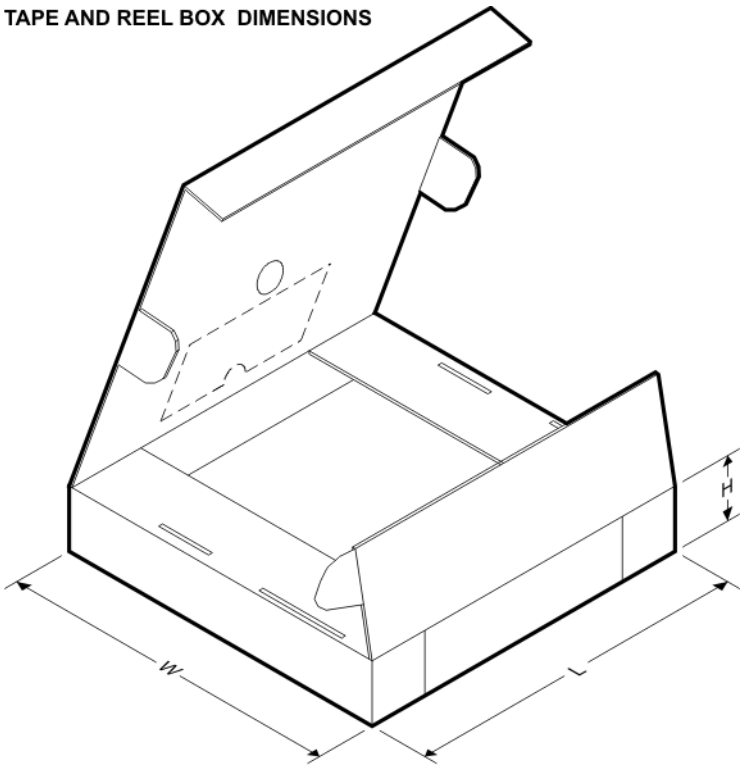
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25504RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ25504RGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

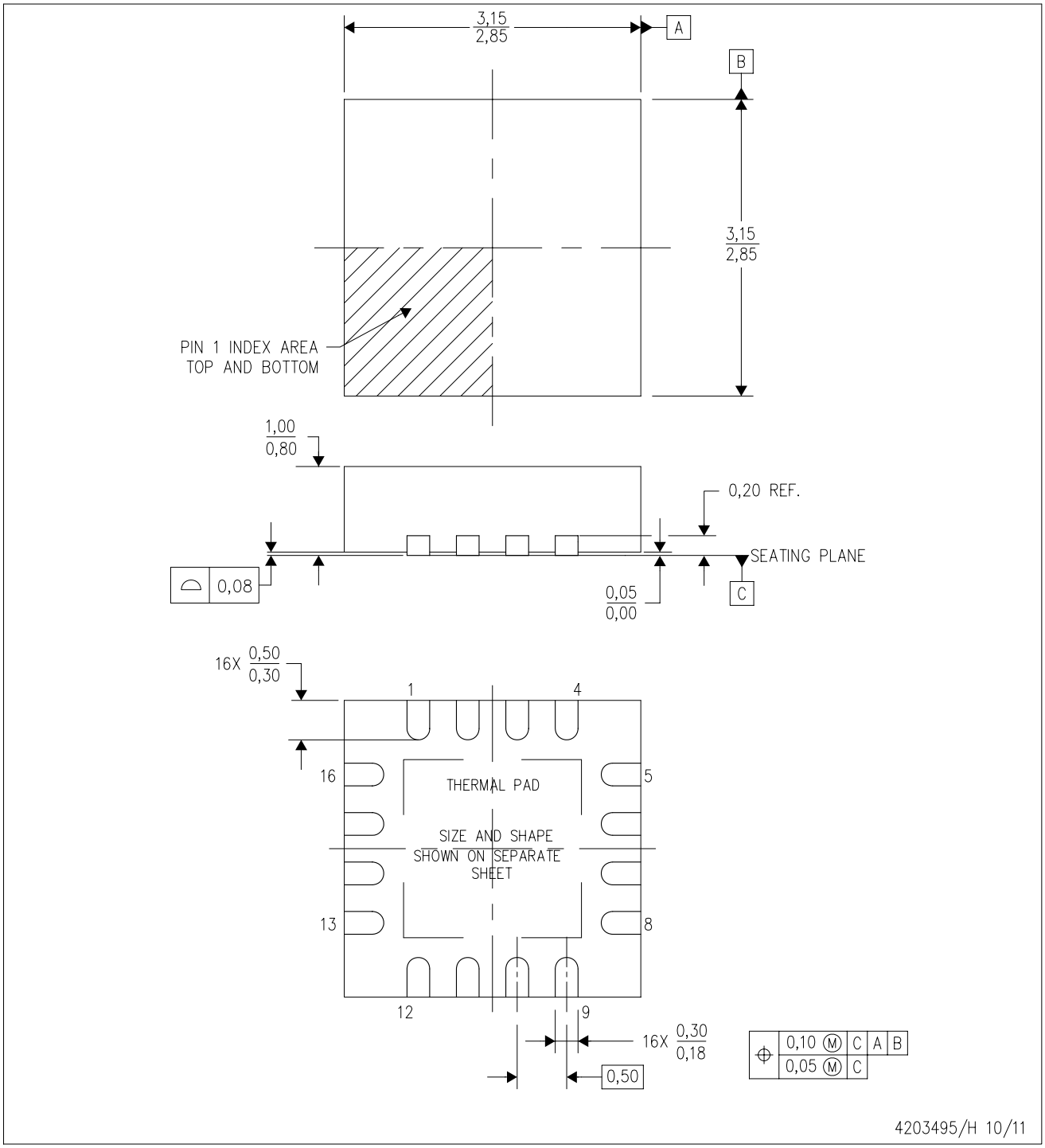
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25504RGTR	QFN	RGT	16	3000	367.0	367.0	35.0
BQ25504RGTT	QFN	RGT	16	250	210.0	185.0	35.0

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

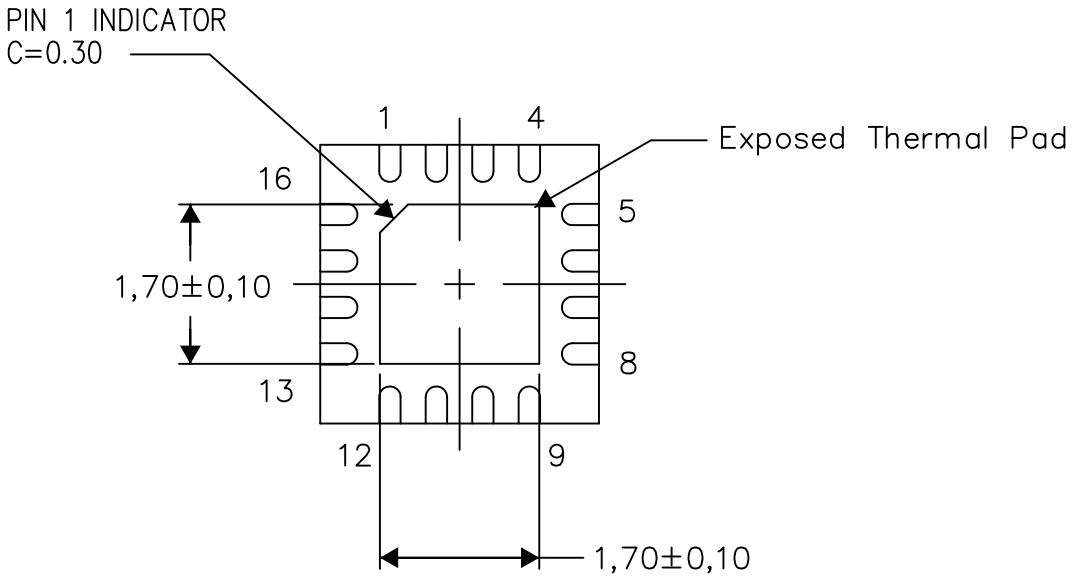
RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



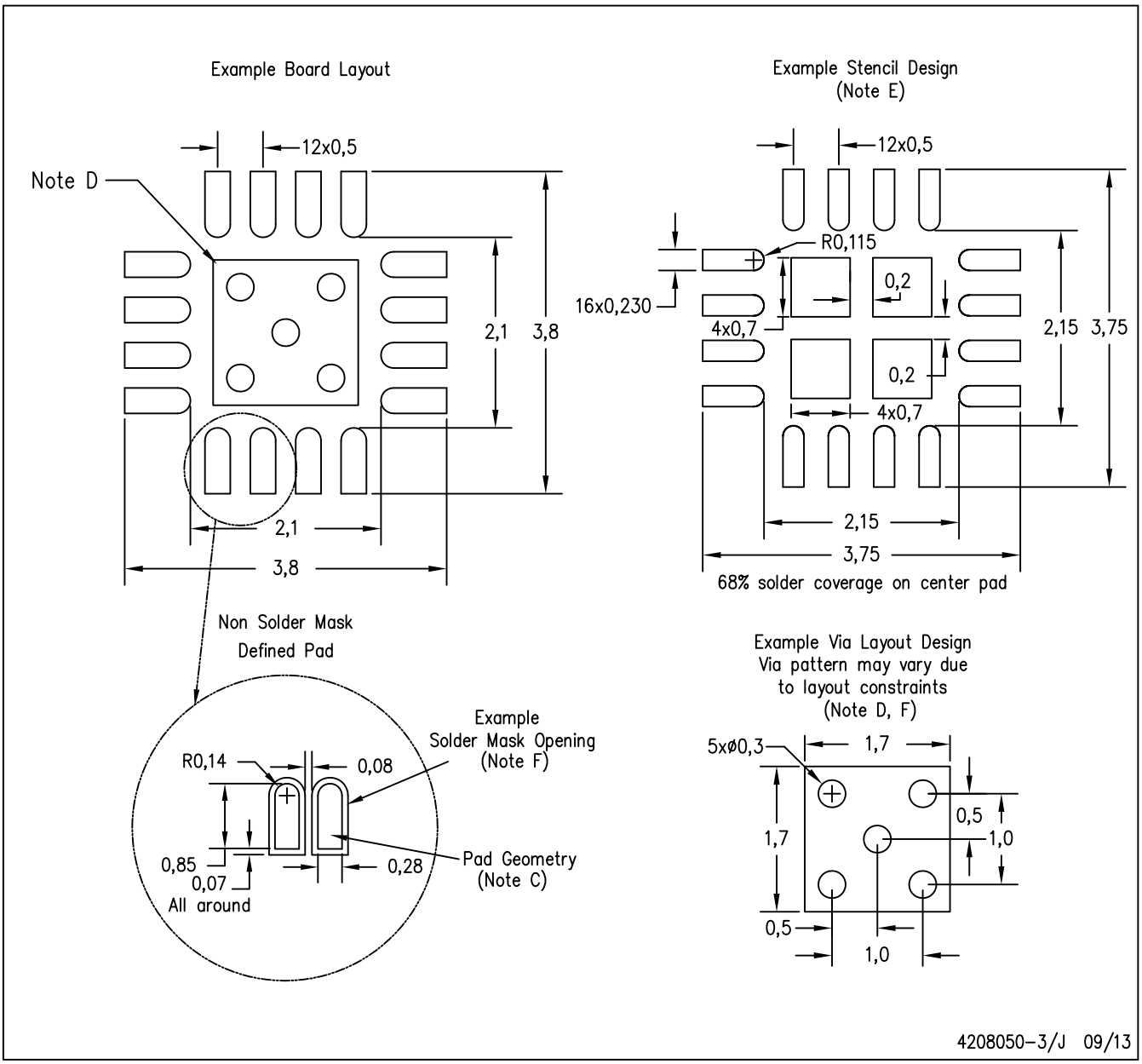
Bottom View

Exposed Thermal Pad Dimensions

4206349–4/U 09/13

NOTE: All linear dimensions are in millimeters

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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