2-Series, 3-Series, and 4-Series Li-Ion Battery Pack Manager

Check for Samples: bq3055

FEATURES

- **Fully Integrated 2-Series, 3-Series, and 4-Series Li-Ion or Li-Polymer Cell Battery Pack Manager and Protection**
- **Advanced Compensated End-of-Discharge Voltage (CEDV) Gauging**
- **High Side N-CH Protection FET Drive**
- **Integrated Cell Balancing**
- **Low Power Modes**
  - **Low Power: < 180 µA**
  - **Sleep < 76 µA**
- **Full Array of Programmable Protection Features**
  - **Voltage**
  - **Current**
  - **Temperature**
- **Sophisticated Charge Algorithms**
  - **JEITA**
  - **Enhanced Charging**
  - **Adaptive Charging**
- **Supports Two-Wire SMBus v1.1 Interface**
- **SHA-1 Authentication**
- **Compact Package: 30-Lead TSSOP**

APPLICATIONS

- **Notebook/Netbook PCs**
- **Medical and Test Equipment**
- **Portable Instrumentation**

DESCRIPTION

The bq3055 device is a fully integrated, single-chip, pack-based solution that provides a rich array of features for gas gauging, protection, and authentication for 2-series, 3-series, and 4-series cell Li-Ion and Li-Polymer battery packs.

Using its integrated high-performance analog peripherals, the bq3055 device measures and maintains an accurate record of available capacity, voltage, current, temperature, and other critical parameters in Li-Ion or Li-Polymer batteries, and reports this information to the system host controller over an SMBus v1.1 compatible interface.

The bq3055 provides software-based 1st-level and 2nd-level safety protection for overvoltage, undervoltage, overtemperature, and overcharge conditions, as well as hardware-based protection for overcurrent in discharge and short circuit in charge and discharge conditions.

SHA-1 authentication with secure memory for authentication keys enables identification of genuine battery packs beyond any doubt.

The compact 30-lead TSSOP package minimizes solution cost and size for smart batteries while providing maximum functionality and safety for battery gauging applications.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PART NUMBER	PACKAGE	PACKAGE DESIGNATOR	PACKAGE MARKING	ORDERING INFORMATION(1)	
					TUBE(2)	TAPE AND REEL(3)
–40°C to 85°C	bq3055	TSSOP-30	DBT	bq3055	bq3055DBT	bq3055DBTR

(1) For the most current package and ordering information, see the Package Option Addendum at the end of the document, or see the TI website at www.ti.com.
(2) A single tube quantity is 50 units.
(3) A single reel quantity is 2000 units.

THERMAL INFORMATION

THERMAL METRIC(1)		bq3055 TSSOP 30 PINS	UNITS
$\theta_{JA, High K}$	Junction-to-ambient thermal resistance(2)	73.1	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance (3)	17.5	
θ_{JB}	Junction-to-board thermal resistance (4)	34.5	
ψ_{JT}	Junction-to-top characterization parameter (5)	0.3	
ψ_{JB}	Junction-to-board characterization parameter (6)	30.3	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance (7)	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

TYPICAL IMPLEMENTATION

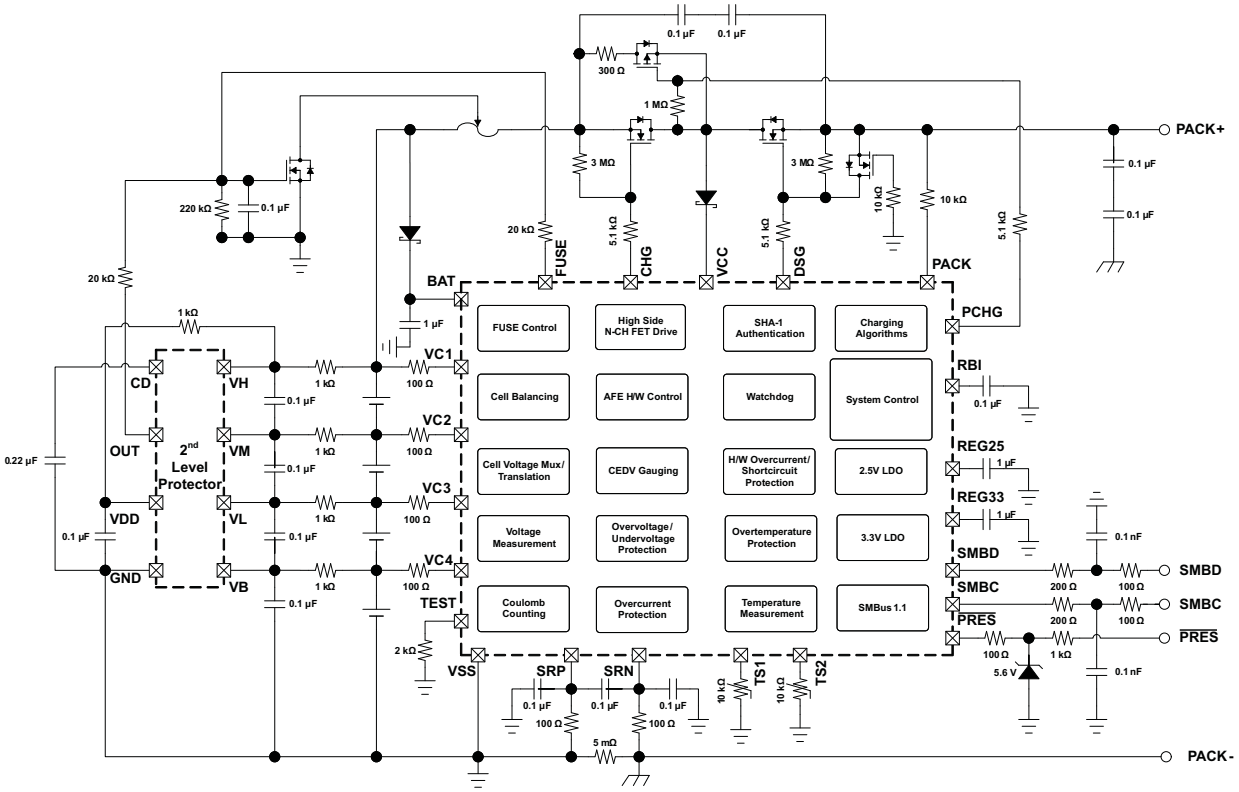


Figure 1. bq3055 Implementation

Pin-Out Diagram

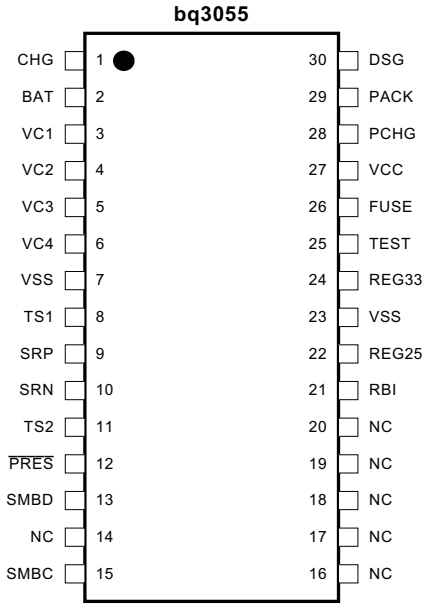


Figure 2. bq3055 Pin-Out Diagram

PIN FUNCTIONS

PIN NAME	PIN NUMBER	TYPE(1)	DESCRIPTION
	bq3055-DBT		
CHG	1	O	Charge N-FET gate drive
BAT	2	P	Alternate power source
VC1	3	I	Sense input for positive voltage of top most cell in stack and cell balancing input for top most cell in stack
VC2	4	I	Sense input for positive voltage of third lowest cell in stack and cell balancing input for third lowest cell in stack
VC3	5	I	Sense input for positive voltage of second lowest cell in stack and cell balancing input for second lowest cell in stack
VC4	6	I	Sense input for positive voltage of lowest cell in stack and cell balancing input for lowest cell in stack
VSS	7	P	Device ground
TS1	8	AI	Temperature sensor 1 thermistor input
SRP	9	AI	Differential Coulomb Counter input
SRN	10	AI	Differential Coulomb Counter input
TS2	11	AI	Temperature sensor 2 thermistor input
$\overline{\text{PRES}}$	12	I	Host system present input
SMBD	13	I/OD	SMBus v1.1 data line
NC	14	—	Not internally connected, connect to VSS
SMBC	15	I/OD	SMBus v1.1 clock line
NC	16	—	Not internally connected, connect to VSS
NC	17	—	Not internally connected, connect to VSS
NC	18	—	Not internally connected, connect to VSS
NC	19	—	Not internally connected, connect to VSS
NC	20	—	Not internally connected, connect to VSS
RBI	21	P	RAM backup

(1) P = Power Connection, O = Digital Output, AI = Analog Input, I = Digital Input, I/OD = Digital Input/Output

PIN FUNCTIONS (continued)

PIN NAME	PIN NUMBER	TYPE(1)	DESCRIPTION
	bq3055-DBT		
REG25	22	P	2.5-V regulator output
VSS	23	P	Device ground
REG33	24	P	3.3-V regulator output
TEST	25	—	Test pin, connect to VSS through 2-kΩ resistor
FUSE	26	O	Fuse drive
VCC	27	P	Power supply voltage
PCHG	28	I/OD	Pre-charge P-FET gate drive
PACK	29	P	Alternate power source
DSG	30	O	Discharge N-FET gate drive

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)(1)

DESCRIPTION	PINS	VALUE
Supply voltage range, V_{MAX}	VCC, TEST, PACK w.r.t. Vss	–0.3 V to 34 V
Input voltage range, V_{IN}	VC1, BAT	V_{VC2} – 0.3 V to V_{VC2} + 8.5 V or 34 V, whichever is lower
	VC2	V_{VC3} – 0.3 V to V_{VC3} + 8.5 V
	VC3	V_{VC4} – 0.3 V to V_{VC4} + 8.5 V
	VC4	V_{SRP} – 0.3 V to V_{SRP} + 8.5 V
	SRP, SRN	–0.3 V to 0.3 V
	SMBC, SMBD	V_{SS} – 0.3 V to 6.0 V
	TS1, TS2, $\overline{PRES}$	–0.3 V to V_{REG25} + 0.3 V
Output voltage range, V_O	DSG	–0.3 V to V_{PACK} + 20 V or V_{SS} + 34 V, whichever is lower
	CHG	–0.3 V to V_{BAT} + 20 V or V_{SS} + 34 V, whichever is lower
	FUSE	–0.3 V to 34 V
	RBI, REG25	–0.3 V to 2.75 V
	REG33	–0.3 V to 5.0 V
Maximum VSS current, I_{SS}		50 mA
Current for cell balancing, I_{CB}		10 mA
ESD Rating	HBM, VCx Only	1 kV
Functional Temperature, T_{FUNC}		–40 to 110°C
Storage temperature range, T_{STG}		–65 to 150°C
Lead temperature (soldering, 10 s), T_{SOLDER}		300°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

		MIN	TYP	MAX	UNIT
Supply voltage	VCC, PACK			25	V
	BAT	3.8		V_{VC2} + 5.0	
$V_{STARTUP}$	Start up voltage at PACK	3.0		5.5	V

RECOMMENDED OPERATING CONDITIONS (continued)

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	VC1, BAT	V_{VC2}		V_{VC2} + 5.0	V
		VC2	V_{VC3}		V_{VC3} + 5.0	
		VC3	V_{VC4}		V_{VC4} + 5.0	
		VC4	V_{SRP}		V_{SRP} + 5.0	
		VCn – VC(n+1), (n=1, 2, 3, 4)	0		5.0	
		PACK			25	
		SRP to SRN	–0.2		0.2	V
C_{REG33}	External 3.3V REG capacitor		1			µF
C_{REG25}	External 2.5V REG capacitor		1			µF
T_{OPR}	Operating temperature		–40		85	°C

ELECTRICAL CHARACTERISTICS: Supply Current

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Normal	CHG on, DSG on, no Flash write		410		µA
	Sleep	CHG on, DSG on, no SBS communication		160		µA
		CHG off, DSG off, no SBS communication		80		µA
	Shutdown				3.7	µA

ELECTRICAL CHARACTERISTICS: Power On Reset (POR)

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT–}$	Negative-going voltage input	At REG25	1.9	2.0	2.1	V
V_{HYS}	POR Hysteresis	At REG25	65	125	165	mV

ELECTRICAL CHARACTERISTICS: WAKE FROM SLEEP

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{WAKE}	V_{WAKE} Threshold	V_{WAKE} = 1.2 mV	0.2	1.2	2.0	mV
		V_{WAKE} = 2.4 mV	0.4	2.4	3.6	
		V_{WAKE} = 5 mV	2.0	5.0	6.8	
		V_{WAKE} = 10 mV	5.3	10	13	
V_{WAKE_TCO}	Temperature drift of VWAKE accuracy			0.5		%/°C
t_{WAKE}	Time from application of current and wake of bq3055			0.2	1	ms

ELECTRICAL CHARACTERISTICS: RBI RAM Backup

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(RBI)}$	RBI data-retention input current	VRBI > $V_{(RBI)MIN}$, VCC < VIT		20	1100	nA
		VRBI > $V_{(RBI)MIN}$, VCC < VIT, T_A= 0°C to 70°C			500	
$V_{(RBI)}$	RBI data-retention voltage		1			V

ELECTRICAL CHARACTERISTICS: 3.3V Regulator

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REG33}	Regulator output voltage	3.8 V < VCC or BAT ≤ 5 V, I_{CC} ≤4 mA	2.4		3.5	V
		5V < VCC or BAT ≤ 6.8 V, I_{CC} ≤13 mA	3.1	3.3	3.5	V
		6.8 V < VCC or BAT ≤ 20 V, I_{CC} ≤ 30 mA	3.1	3.3	3.5	V
I_{REG33}	Regulator output current		2			mA
$\Delta V_{(VDDTEMP)}$	Regulator output change with temperature	VCC or BAT = 14.4 V, I_{REG33} = 2 mA		0.2		%
$\Delta V_{(VDDLINE)}$	Line regulation	VCC or BAT = 14.4 V, I_{REG33} = 2 mA		1	13	mV
$\Delta V_{(VDDLOAD)}$	Load regulation	VCC or BAT = 14.4 V, I_{REG33} = 2 mA		5	18	mV
$I_{(REG33MAX)}$	Current limit	VCC or BAT = 14.4 V, V_{REG33} = 3 V			70	mA
		VCC or BAT = 14.4 V, V_{REG33} = 0 V			33	

ELECTRICAL CHARACTERISTICS: 2.5V Regulator

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REG25}	Regulator output voltage	I_{REG25} = 10 mA	2.35	2.5	2.55	V
I_{REG25}	Regulator Output Current		3			mA
$\Delta V_{(VDDTEMP)}$	Regulator output change with temperature	VCC or BAT = 14.4 V, I_{REG25} = 2 mA		0.25		%
$\Delta V_{(VDDLINE)}$	Line regulation	VCC or BAT = 14.4 V, I_{REG25} = 2 mA		1	4	mV
$\Delta V_{(VDDLOAD)}$	Load regulation	VCC or BAT = 14.4 V, I_{REG25} = 2 mA		20	40	mV
$I_{(REG33MAX)}$	Current limit	VCC or BAT = 14.4 V, V_{REG25} = 2.3 V			65	mA
		VCC or BAT = 14.4 V, V_{REG25} = 0 V			23	

ELECTRICAL CHARACTERISTICS: $\overline{PRES}$, SMBD, SMBC

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input	$\overline{PRES}$, SMBD, SMBC	2.0			V
V_{IL}	Low-level input	$\overline{PRES}$, SMBD, SMBC			0.8	V
V_{OL}	Low-level output voltage	SMBD, SMBC			0.4	V
C_{IN}	Input capacitance	$\overline{PRES}$, SMBD, SMBC		5		pF
I_{LKG}	Input leakage current	$\overline{PRES}$, SMBD, SMBC			1	µA
I_{WPU}	Weak Pull Up Current	$\overline{PRES}$, V_{OH} = V_{REG25} – 0.5 V	60		120	µA
$R_{PD(SMBx)}$	SMBC, SMBD Pull-Down	T_A = –40 to 100˚C	550	775	1000	kΩ

ELECTRICAL CHARACTERISTICS: CHG, DSG FET Drive

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(FETON)}$	Output voltage, charge, and discharge FETs on	$V_{O(FETONDSG)} = V_{(DSG)} – V_{PACK}$, V_{GS} connect 10 MΩ, VCC 3.8 V to 8.4 V	8.0	9.7	12	V
		$V_{O(FETONDSG)} = V_{(DSG)} – V_{PACK}$, V_{GS} connect 10 MΩ, VCC > 8.4 V	9.0	11	12	V
		$V_{O(FETONCHG)} = V_{(CHG)} – V_{BAT}$, V_{GS} connect 10 MΩ, VCC 3.8 V to 8.4 V	8.0	9.7	12	V
		$V_{O(FETONCHG)} = V_{(CHG)} – V_{BAT}$, V_{GS} connect 10 MΩ, VCC > 8.4 V	9.0	11	12	V
$V_{(FETOFF)}$	Output voltage, charge and discharge FETs off	$VO_{(FETOFFDSG)} = V_{(DSG)} – V_{PACK}$	–0.4		0.4	V
		$V_{O(FETOFFCHG)} = V_{(CHG)} – V_{BAT}$	–0.4		0.4	V
t_r	Rise time	C_L= 4700 pF R_G= 5.1 kΩ VCC < 8.4 V_{DSG}: V_{BAT} to V_{BAT} + 4 V V_{CHG}: V_{PACK} to V_{PACK} + 4 V		800	1400	µs
		C_L = 4700 pF R_G = 5.1 kΩ VCC > 8.4 V_{DSG}: V_{BAT} to V_{BAT} + 4 V V_{CHG}: V_{PACK} to V_{PACK} + 4 V		200	500	µs
t_f	Fall time	C_L = 4700 pF R_G = 5.1 kΩ V_{DSG}: V_{BAT} + $V_{O(FETONDSG)}$ to V_{BAT} + 1 V V_{CHG}: V_{PACK} + $V_{O(FETONCHG)}$ to V_{PACK} + 1 V		80	200	µs

ELECTRICAL CHARACTERISTICS: PCHG FET Drive

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{PU_PCHG}	PCHG Pull-Up Voltage				V_{CC}	V
V_{OL_PCHG}	PCHG Output Voltage Low	I_{OL} = 1 mA	0.3			V

ELECTRICAL CHARACTERISTICS: FUSE

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH(FUSE)}$	High Level FUSE Output	VCC = 3.8 V to 9 V	2.4		8.5	V
		VCC = 9 V to 25 V	7	8	9	V
$V_{IH(FUSE)}$	Weak pull-up current in off state(1)		2.8			V
				100		nA
$t_{R(FUSE)}$	FUSE Output Rise Time	C_L = 1 nF, VCC = 9 V to 25 V, $V_{OH(FUSE)}$ = 0 V to 5 V		5	20	µs
$Z_{O(FUSE)}$	FUSE Output Impedance			2	5	kΩ

(1) Verified by design. Not production tested.

ELECTRICAL CHARACTERISTICS: COULOMB COUNTER

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	SRP – SRN	–0.20		0.25	V
	Conversion time	Single conversion		250		ms
	Resolution (no missing codes)		16			Bits
	Effective resolution	Single conversion, signed	15			Bits
	Offset error	Post calibrated		10		µV
	Offset error drift			0.3	0.5	µV/°C
	Full-scale error		–0.8%	0.2%	0.8%	
	Full-scale error drift				150	PPM/°C
	Effective input resistance		2.5			mΩ

ELECTRICAL CHARACTERISTICS: VC1, VC2, VC3, VC4

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	VC4 – VC3, VC3 – VC2, VC2 – VC1, VC1 – VSS	–0.20		8	V
	Conversion time	Single conversion		32		ms
	Resolution (no missing codes)		16			Bits
	Effective resolution	Single conversion, signed	15			Bits
$R_{(BAL)}$	$R_{DS(ON)}$ for internal FET at V_{DS} > 2 V	V_{DS} = VC4 – VC3, VC3 – VC2, VC2 – VC1, VC1 – VSS	200	310	430	Ω
	$R_{DS(ON)}$ for internal FET at V_{DS} > 4 V	V_{DS} = VC4 – VC3, VC3 – VC2, VC2 – VC1, VC1 – VSS	60	125	230	Ω

ELECTRICAL CHARACTERISTICS: TS1, TS2

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R	Internal Pull Up Resistor		16.5	17.5	19.0	KΩ
R_{DRIFT}	Internal Pull Up Resistor Drift From 25°C				200	PPM/°C
R_{PAD}	Internal Pin Pad resistance			84		Ω
V_{IN}	Input voltage range	TS1 – VSS, TS2 – VSS	–0.20		0.8 × V_{REG25}	V
	Conversion Time			16		ms
	Resolution (no missing codes)		16			Bits
	Effective resolution		11	12		Bits

ELECTRICAL CHARACTERISTICS: Internal Temperature Sensor

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(TEMP)}$	Temperature sensor voltage		–1.9	–2.0	–2.1	mV/°C
	Conversion Time			16		ms
	Resolution (no missing codes)		16			Bits
	Effective resolution		11	12		Bits

ELECTRICAL CHARACTERISTICS: Internal Thermal Shutdown

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{MAX2}	Maximum REG33 temperature		125		175	
$T_{RECOVER}$	Recovery hysteresis temperature			10		°C
$t_{PROTECT}$	Protection time			5		µs

ELECTRICAL CHARACTERISTICS: High Frequency Oscillator

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(OSC)}$	Operating frequency of CPU Clock			4.194		MHz
$f_{(EIO)}$	Frequency error(1)(2)	T_A = –20°C to 70°C	–2%	±0.25%	2%	
		T_A = –40°C to 85°C	–3%	±0.25%	3%	
$t_{(SXO)}$	Start-up time(3)	T_A = –25°C to 85°C		3	6	ms

(1) The frequency error is measured from 4.194 MHz.
(2) The frequency drift is included and measured from the trimmed frequency at V_{REG25} = 2.5V, T_A = 25°C.
(3) The startup time is defined as the time it takes for the oscillator output frequency to be ±3% when the device is already powered.

ELECTRICAL CHARACTERISTICS: Low Frequency Oscillator

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(LOSC)}$	Operating frequency			32.768		kHz
$f_{(LEIO)}$	Frequency error(1)(2)	T_A = –20°C to 70°C	–1.5%	±0.25%	1.5%	
		T_A = –40°C to 85°C	–2.5%	±0.25%	2.5%	
$t_{(LSXO)}$	Start-up time(3)	T_A = –25°C to 85°C			100	µs

(1) The frequency drift is included and measured from the trimmed frequency at VCC = 2.5V, T_A = 25°C.
(2) The frequency error is measured from 32.768 kHz.
(3) The startup time is defined as the time it takes for the oscillator output frequency to be ±3%.

ELECTRICAL CHARACTERISTICS: Internal Voltage Reference

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	Internal Reference Voltage		1.215	1.225	1.230	V
V_{REF_DRIFT}	Internal Reference Voltage Drift	T_A = –25°C to 85°C		±80		PPM/°C
		T_A = 0°C to 60°C		±50		PPM/°C

ELECTRICAL CHARACTERISTICS: Flash

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER(1)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Data retention		10			Years
	Flash programming write-cycles	Data Flash	20k			Cycles
		Instruction Flash	1k			Cycles
$I_{CC(PROG\_DF)}$	Data Flash-write supply current	T_A = –40°C to 85°C		3	4	mA
$I_{CC(ERASE\_DF)}$	Data Flash-erase supply current	T_A = –40°C to 85°C		3	18	mA

(1) Verified by design. Not production tested.

ELECTRICAL CHARACTERISTICS: OCD Current Protection

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(OCD)}$	OCD detection threshold voltage range, typical	RSNS = 0	50		200	mV
		RSNS = 1	25		100	mV
$\Delta V_{(OCDT)}$	OCD detection threshold voltage program step	RSNS = 0		10		mV
		RSNS = 1		5		mV
$V_{(OFFSET)}$	OCD offset		–10		10	mV
$V_{(Scale\_Err)}$	OCD scale error		–10		10	%
$t_{(OCDD)}$	Over Current in Discharge Delay		1		31	ms
$t_{(OCDD\_STEP)}$	OCDD Step options			2		ms
$t_{(DETECT)}$	Current fault detect time	VSRP – SRN = VTHRESH + 12.5 mV			160	µs
t_{ACC}	Over Current and Short Circuit delay time accuracy	Accuracy of typical delay time	–20		20	%

ELECTRICAL CHARACTERISTICS: SCD1 Current Protection

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(SDC1)}$	SCD1 detection threshold voltage range, typical	RSNS = 0	100		450	mV
		RSNS = 1	50		225	mV
$\Delta V_{(SCD1T)}$	SCD1 detection threshold voltage program step	RSNS = 0		50		mV
		RSNS = 1		25		mV
$V_{(OFFSET)}$	SCD1 offset		–10		10	mV
$V_{(Scale\_Err)}$	SCD1 scale error		–10		10	%
$t_{(SCD1D)}$	Short Circuit in Discharge Delay	AFE.STATE_CNTL[SCDDx2] = 0	0		915	µs
		AFE.STATE_CNTL[SCDDx2] = 1	0		1830	µs
$t_{(SCD1D\_STEP)}$	SCD1D Step options	AFE.STATE_CNTL[SCDDx2] = 0		61		µs
		AFE.STATE_CNTL[SCDDx2] = 1		122		µs
$t_{(DETECT)}$	Current fault detect time	VSRP – SRN = VTHRESH + 12.5 mV			160	µs
t_{ACC}	Over Current and Short Circuit delay time accuracy	Accuracy of typical delay time	–20		20	%

ELECTRICAL CHARACTERISTICS: SCD2 Current Protection

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(SDC2)}$	SCD2 detection threshold voltage range, typical	RSNS = 0	100		450	mV
		RSNS = 1	50		225	mV
$\Delta V_{(SCD2T)}$	SCD2 detection threshold voltage program step	RSNS = 0		50		mV
		RSNS = 1		25		mV
$V_{(OFFSET)}$	SCD2 offset		–10		10	mV
$V_{(Scale\_Err)}$	SCD2 scale error		–10		10	%
$t_{(SCD1D)}$	Short Circuit in Discharge Delay	AFE.STATE_CNTL[SCDDx2] = 0	0		458	µs
		AFE.STATE_CNTL[SCDDx2] = 1	0		915	µs
$t_{(SCD2D\_STEP)}$	SCD2D Step options	AFE.STATE_CNTL[SCDDx2] = 0		30.5		µs
		AFE.STATE_CNTL[SCDDx2] = 1		61		µs
$t_{(DETECT)}$	Current fault detect time	VSRP – SRN = VTHRESH + 12.5 mV			160	µs
t_{ACC}	Over Current and Short Circuit delay time accuracy	Accuracy of typical delay time	–20		20	%

ELECTRICAL CHARACTERISTICS: SCC Current Protection

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(SCCT)}$	SCC detection threshold voltage range, typical	RSNS = 0	–100		–300	mV
		RSNS = 1	–50		–225	mV
$\Delta V_{(SCCDT)}$	SCC detection threshold voltage program step	RSNS = 0		–50		mV
		RSNS = 1		–25		mV
$V_{(OFFSET)}$	SCC offset		–10		10	mV
$V_{(Scale\_Err)}$	SCC scale error		–10		10	%
$t_{(SCCD)}$	Short Circuit in Charge Delay		0		915	ms
$t_{(SCCD\_STEP)}$	SCCD Step options			61		ms
$t_{(DETECT)}$	Current fault detect time	VSRP – SRN = VTHRESH + 12.5 mV			160	µs
t_{ACC}	Over Current and Short Circuit delay time accuracy	Accuracy of typical delay time	–20		20	%

ELECTRICAL CHARACTERISTICS: SBS Timing Characteristics

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SMB}	SMBus operating frequency	Slave mode, SMBC 50% duty cycle	10		100	kHz
f_{MAS}	SMBus master clock frequency	Master mode, no clock low slave extend		51.2		kHz
t_{BUF}	Bus free time between start and stop		4.7			µs
$t_{HD:STA}$	Hold time after (repeated) start		4.0			µs
$t_{SU:STA}$	Repeated start setup time		4.7			µs
$t_{SU:STO}$	Stop setup time		4.0			µs
$t_{HD:DAT}$	Data hold time		300			ns
$t_{SU:DAT}$	Data setup time		250			ns
$t_{TIMEOUT}$	Error signal/detect	See (1)	25		35	ms
t_{LOW}	Clock low period		4.7			µs
t_{HIGH}	Clock high period	See (2)			Disabled	
t_{HIGH}	Clock high period	See (2)	4.0		50	µs
$t_{LOW:SEXT}$	Cumulative clock low slave extend time	See (3)			25	ms
$t_{LOW:MEXT}$	Cumulative clock low master extend time	See (4)			10	ms
t_F	Clock/data fall time	See (5)			300	ns
t_R	Clock/data rise time	See (6)			1000	ns

(1) The bq3055 times out when any clock low exceeds $t_{TIMEOUT}$.
(2) t_{HIGH}, Max, is the minimum bus idle time. SMBC = 1 for t > 50 µs causes reset of any transaction involving bq3055 that is in progress. This specification is valid when the THIGH_VAL=0. If THIGH_VAL = 1, then the value of THIGH is set by THIGH_1,2 and the timeout is not SMBus standard.
(3) $t_{LOW:SEXT}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop.
(4) $t_{LOW:MEXT}$ is the cumulative time a master device is allowed to extend the clock cycles in one message from initial start to the stop.
(5) Rise time tR = V_{ILMAX} – 0.15) to (V_{IHMIN} + 0.15)
(6) Fall time tF = 0.9 V_{DD} to (V_{ILMAX} – 0.15)

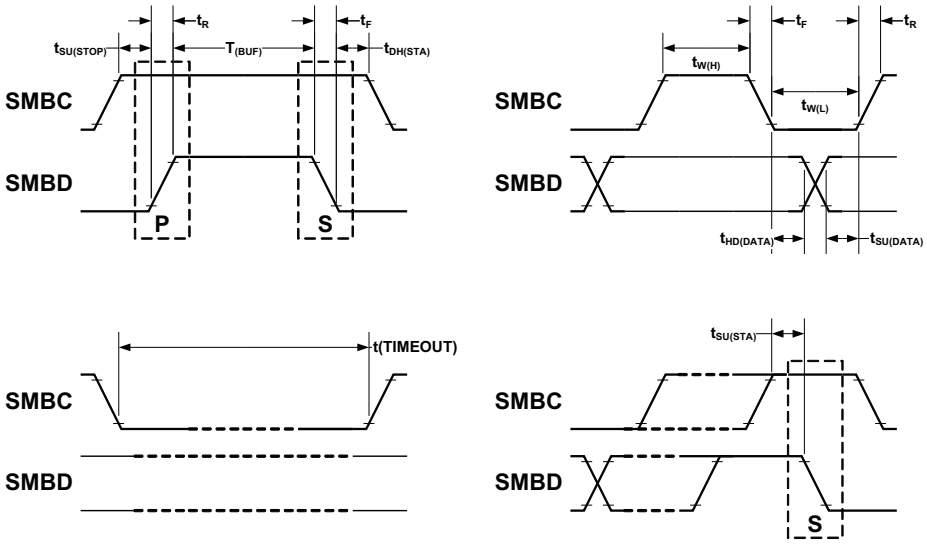


Figure 3. SMBus Timing Diagram

FEATURE SET

Primary (1st Level) Safety Features

The bq3055 supports a wide range of battery and system protection features that can easily be configured. The primary safety features include:

- Cell Overvoltage/Undervoltage Protection
- Charge and Discharge Overcurrent
- Short-Circuit
- Charge and Discharge Over-Temperature
- AFE Watchdog

Secondary (2nd Level) Safety Features

The secondary safety features of the bq3055 can be used to indicate more serious faults via the FUSE pin. This pin can be used to blow an in-line fuse to permanently disable the battery pack from charging or discharging. The secondary safety protection features include:

- Safety Overvoltage
- Safety Overcurrent in Charge and Discharge
- Safety Over-Temperature in Charge and Discharge
- Charge FET, Discharge FET, and Pre-Charge FET Faults
- Cell Imbalance Detection
- Fuse Blow by Secondary Voltage Protection IC
- AFE Register Integrity Fault (AFE_P)
- AFE Communication Fault (AFE_C)

Charge Control Features

The bq3055 charge control features include:

- Supports JEITA temperature ranges. Reports charging voltage and charging current according to the active temperature range
- Handles more complex charging profiles. Allows for splitting the standard temperature range into two sub-ranges and allows for varying the charging current according to the cell voltage
- Reports the appropriate charging current needed for constant current charging and the appropriate charging voltage needed for constant voltage charging to a smart charger using SMBus broadcasts
- Reduce the charge difference of the battery cells in fully charged state of the battery pack gradually using a voltage-based cell balancing algorithm during charging. A voltage threshold can be set up for cell balancing to be active. This prevents fully charged cells from overcharging and causing excessive degradation and also increases the usable pack energy by preventing premature charge termination.
- Supports pre-charging/zero-volt charging
- Supports charge inhibit and charge suspend if battery pack temperature is out of temperature range
- Reports charging fault and also indicate charge status via charge and discharge alarms

Gas Gauging

The bq3055 uses the CEDV algorithm to measure and calculate the available capacity in battery cells. The bq3055 accumulates a measure of charge and discharge currents and compensates the charge current measurement for the temperature and state-of-charge of the battery. The bq3055 estimates self-discharge of the battery and also adjusts the self-discharge estimation based on temperature. See the *bq3055 Technical Reference Manual* (SLUU440) for further details.

Lifetime Data Logging Features

The bq3055 offers limited lifetime data logging for the following critical battery parameters:

- Lifetime Maximum Temperature
- Lifetime Minimum Temperature

- Lifetime Maximum Battery Cell Voltage
- Lifetime Minimum Battery Cell Voltage

Authentication

- The bq3055 supports authentication by the host using SHA-1.
- SHA-1 authentication by the gas gauge is required for unsealing and full access.

Power Modes

The bq3055 supports three power modes to reduce power consumption:

- In Normal Mode, the bq3055 performs measurements, calculations, protection decisions, and data updates in 0.25-second intervals. Between these intervals, the bq3055 is in a reduced power stage.
- In Sleep Mode, the bq3055 performs measurements, calculations, protection decisions, and data updates in adjustable time intervals. Between these intervals, the bq3055 is in a reduced power stage. The bq3055 has a wake function that enables exit from Sleep mode when current flow or failure is detected.
- In Shutdown Mode, the bq3055 is completely disabled.

Configuration

Oscillator Function

The bq3055 fully integrates the system oscillators and does not require any external components to support this feature.

System Present Operation

The bq3055 checks the $\overline{\text{PRES}}$ pin periodically (1s). If $\overline{\text{PRES}}$ input is pulled to ground by the external system, the bq3055 detects this as system present.

2-, 3-, or 4-Cell Configuration

In a 2-cell configuration, VC1 is shorted to VC2 and VC3. In a 3-cell configuration, VC1 is shorted to VC2.

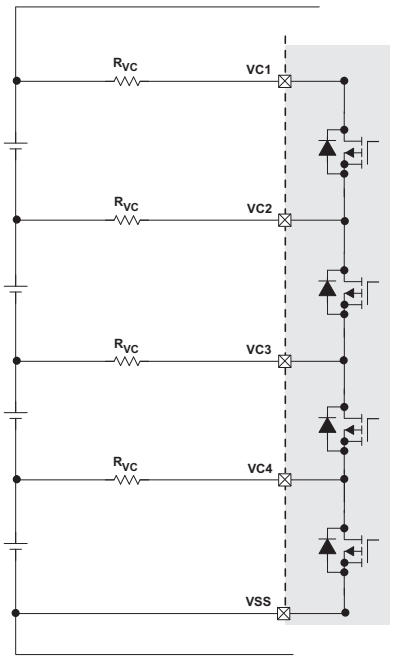
Cell Balancing

The device supports cell balancing by bypassing the current of each cell during charging or at rest. If the device's internal bypass is used, up to 10 mA can be bypassed and multiple cells can be bypassed at the same time. Higher cell balance current can be achieved by using an external cell balancing circuit. In external cell balancing mode, only one cell at a time can be balanced.

The cell balancing algorithm determines the amount of charge needed to be bypassed to balance the capacity of all cells.

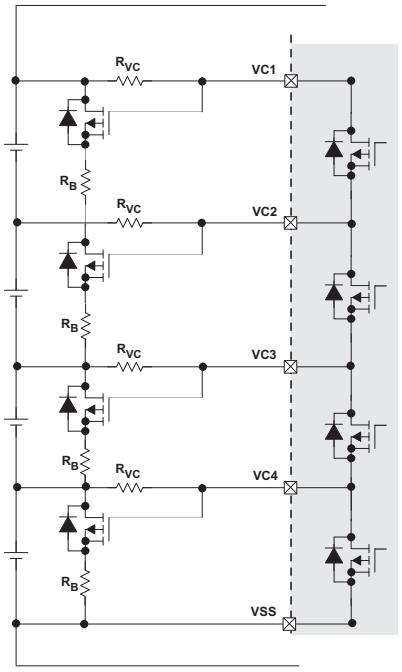
Internal Cell Balancing

When internal cell balancing is configured, the cell balance current is defined by the external resistor R_{VC} at the VCx input.



External Cell Balancing

When external cell balancing is configured, the cell balance current is defined by R_B. Only one cell at a time can be balanced.



BATTERY PARAMETER MEASUREMENTS

Charge and Discharge Counting

The bq3055 uses an integrating delta-sigma analog-to-digital converter (ADC) for current measurement, and a second delta-sigma ADC for individual cell and battery voltage and temperature measurement.

The integrating delta-sigma ADC measures the charge/discharge flow of the battery by measuring the voltage drop across a small-value sense resistor between the SR1 and SR2 pins. The integrating ADC measures bipolar signals from –0.25 V to 0.25 V. The bq3055 detects charge activity when $V_{SR} = V_{(SRP)} – V_{(SRN)}$ is positive, and discharge activity when $V_{SR} = V_{(SRP)} – V_{(SRN)}$ is negative. The bq3055 continuously integrates the signal over time, using an internal counter. The fundamental rate of the counter is 0.65 nVh.

Voltage

The bq3055 updates the individual series cell voltages at 0.25-second intervals. The internal ADC of the bq3055 measures the voltage, and scales and calibrates it appropriately. This data is also used to calculate the impedance of the cell for the CEDV gas-gauging.

Current

The bq3055 uses the SRP and SRN inputs to measure and calculate the battery charge and discharge current using a 5-mΩ to 20-mΩ typ. sense resistor.

Auto Calibration

The bq3055 provides an auto-calibration feature to cancel the voltage offset error across SRN and SRP for maximum charge measurement accuracy. The bq3055 performs auto-calibration when the SMBus lines stay low continuously for a minimum of 5 s.

Temperature

The bq3055 has an internal temperature sensor and inputs for two external temperature sensors. All three temperature sensor options are individually enabled and configured for cell or FET temperature. Two configurable thermistor models are provided to allow the monitoring of cell temperature in addition to FET temperature, which may be of a higher temperature type.

Communications

The bq3055 uses SMBus v1.1 with Master Mode and packet error checking (PEC) options per the SBS specification.

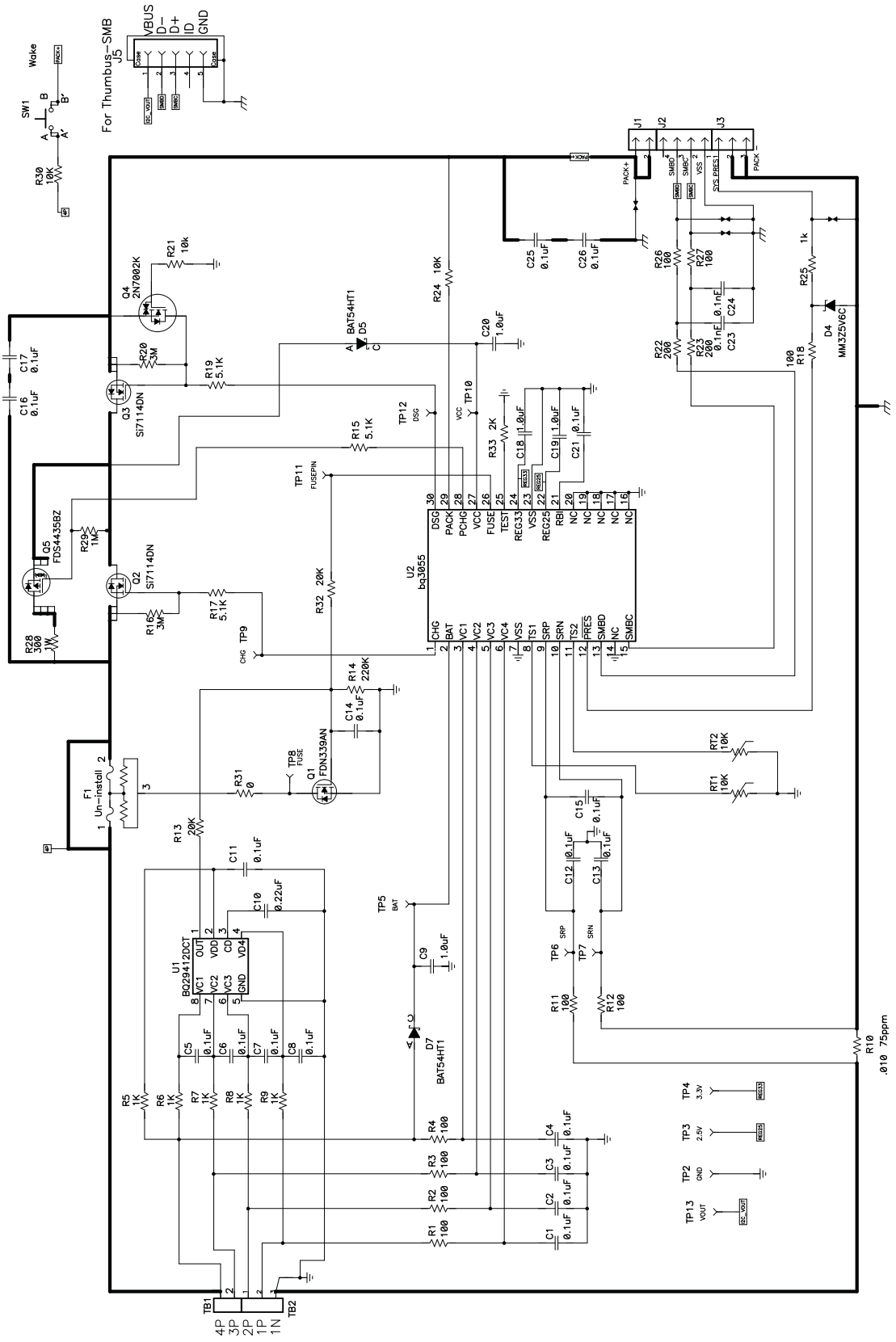
SMBus On and Off State

The bq3055 detects an SMBus off state when SMBC and SMBD are low for two or more seconds. Clearing this state requires that either SMBC or SMBD transition high. The communication bus will resume activity within 1 ms.

SBS Commands

See the *bq3055 Technical Reference Manual* (SLUU440) for further details.

APPLICATION SCHEMATIC

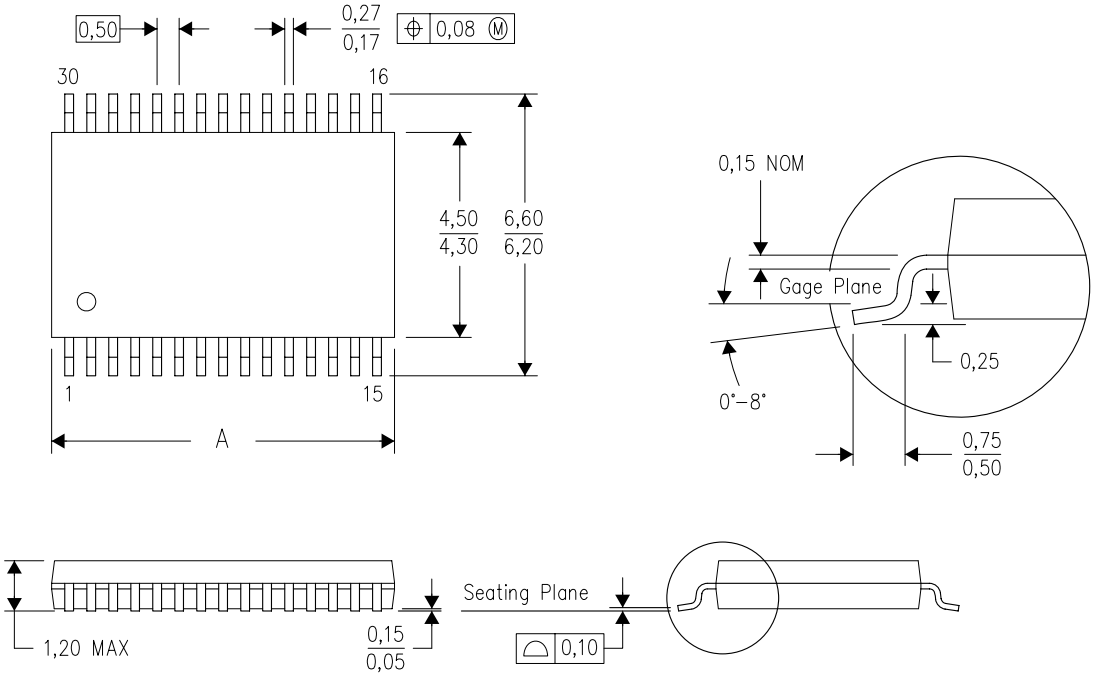


REVISION HISTORY

Changes from Revision A (June 2011) to Revision B	Page
• Changed Electrical Characteristic for I_{CC} Shutdown	6

DBT (R–PDSO–G**) PLASTIC SMALL–OUTLINE PACKAGE

30 PINS SHOWN



DIM \ PINS **	20	24	28	30	38	44	50
A MAX	5,10	6,60	7,90	7,90	9,80	See Sheet 3	12,60
A MIN	4,90	6,40	7,70	7,70	9,60	See Sheet 3	12,40

4073252–2/H 10/09

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–153 except 44 pin package length.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ3055DBT	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ3055	Samples
BQ3055DBTR	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ3055	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

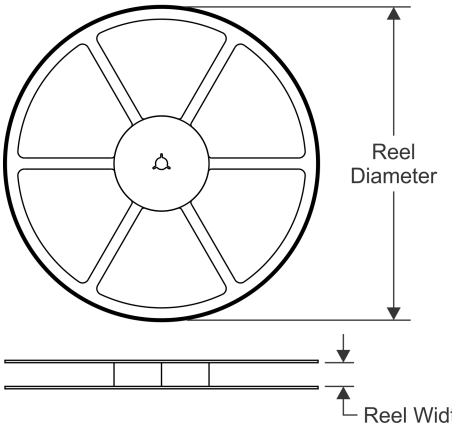
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

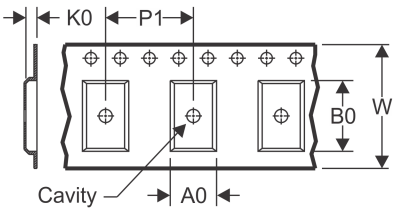
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

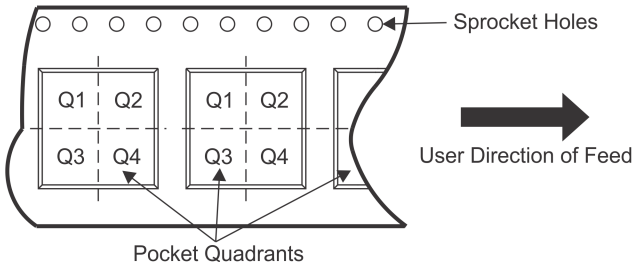


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

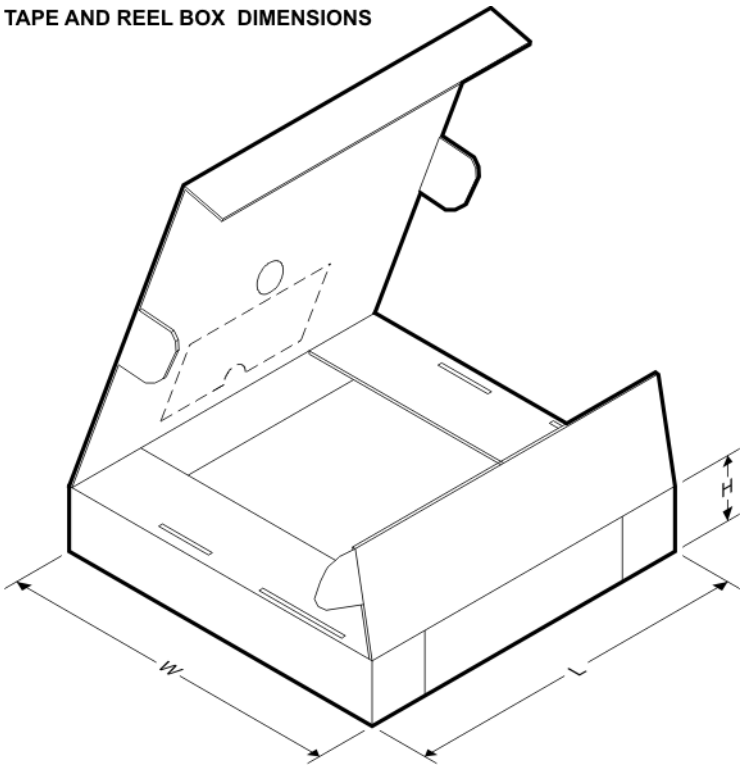
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ3055DBTR	TSSOP	DBT	30	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

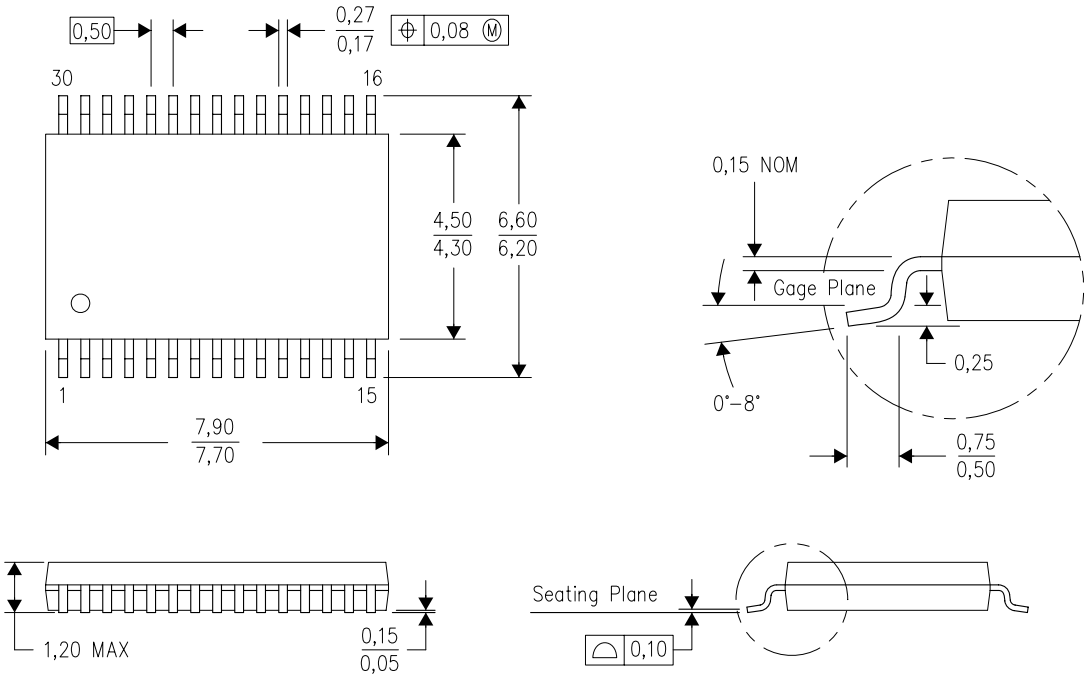
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ3055DBTR	TSSOP	DBT	30	2000	367.0	367.0	38.0

DBT (R–PDSO–G30) PLASTIC SMALL OUTLINE



4073252–5/I 03/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–153.

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DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
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