Overvoltage Protection for 2-Series to 5-Series Cell Li-Ion Batteries with Internal Delay Timer

Check for Samples: bq771800, bq771801, bq771802, bq771803, bq771808, bq771809

FEATURES

- 2-, 3-, 4-, and 5-Series Cell Overvoltage Protection
- Internal Delay Timer
- Fixed OVP Threshold
- High-Accuracy Overvoltage Protection: ± 10 mV
- Low Power Consumption $I_{CC} \approx 1\ \mu A$ ($V_{CELL(ALL)} < V_{PROTECT}$)
- Low Leakage Current Per Cell Input < 100 nA
- Small Package Footprint
  - 8-pin QFN (3 mm × 4 mm)

APPLICATIONS

- Protection in Li-Ion Battery Packs in:
  - Power Tools
  - UPS Battery Backup
  - Light Electric Vehicles (eBike, eScooter, Pedal Assist Bicycles)

DESCRIPTION

The bq7718xy family of products is an overvoltage monitor and protector for Li-Ion battery pack systems. Each cell is monitored independently for an overvoltage condition.

In the bq7718xy device, an internal delay timer is initiated upon detection of an overvoltage condition on any cell. Upon expiration of the delay timer, the output is triggered into its active state (either high or low depending on the configuration). For quicker production-line testing, the bq7718xy device provides a Customer Test Mode with greatly reduced delay time.

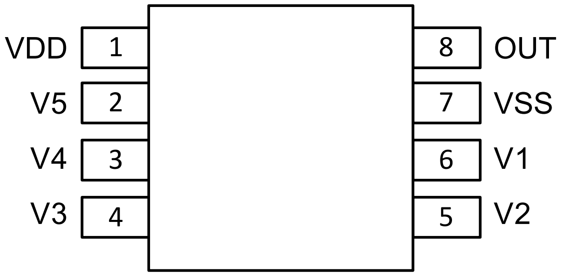


Figure 1. bq771800 Pinout

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	Part Number	Package	Package Designator	OVP (V)	OV Hysteresis (V)	Output Delay	Output Drive	Tape and Reel (Large)	Tape and Reel (Small)
–40°C to 110°C	bq771800	8-Pin QFN	DPJ	4.300	0.300	4 s	CMOS Active High	bq771800DPJR	bq771800DPJT
	bq771801			4.275	0.050	3 s	NCH Active Low, Open Drain	bq771801DPJR	bq771801DPJT
	bq771802			4.225	0.300	1 s	NCH Active Low, Open Drain	bq771802DPJR	bq771802DPJT
	bq771803			4.275	0.050	1 s	NCH Active Low, Open Drain	bq771803DPJR	bq771803DPJT
	bq771804(1)			4.225	0.300	3 s	CMOS Active High	bq771804DPJR	bq771804DPJT
	bq771805(1)			4.325	0.300	3 s	CMOS Active High	bq771805DPJR	bq771805DPJT
	bq771806(1)			4.350	0.300	3 s	CMOS Active High	bq771806DPJR	bq771806DPJT
	bq771807(1)			4.450	0.300	3 s	CMOS Active High	bq771807DPJR	bq771807DPJT
	bq771808			4.200	0.050	1 s	NCH Active Low	bq771808DPJR	bq771808DPJT
	bq771809			4.200	0.050	1 s	CMOS Active High	bq771809DPJR	bq771809DPJT
	bq771810(1)			4.200	0.250	1 s	CMOS Active High	bq771810DPJR	bq771810DPJT
	bq771811(1)			4.225	0.050	1 s	CMOS Active High	bq771811DPJR	bq771811DPJT
	bq771812(1)			4.250	0.050	1 s	CMOS Active High	bq771812DPJR	bq771812DPJT
	bq771813(1)			4.250	0.050	1 s	CMOS Active High	bq771813DPJR	bq771813DPJT
	bq771814(1)			3.900	0.300	3 s	CMOS Active High	bq771814DPJR	bq771814DPJT
	bq771815(1)			4.225	0.050	1 s	NCH Active Low	bq771815DPJR	bq771815DPJT
	bq771816(1)			4.250	0.050	1 s	NCH Active Low	bq771816DPJR	bq771816DPJT
	bq7718xy(2)			3.850–4.650	0–0.300	1 s	NCH, Active Low, Open Drain	bq7718xyDPJR	bq7718xyDPJT

(1) Product Preview only.
(2) Future option, contact TI.

THERMAL INFORMATION

THERMAL METRIC(1)		bq7718xy	UNITS
		8 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	56.6	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	56.4	
θ_{JB}	Junction-to-board thermal resistance	30.6	
ψ_{JT}	Junction-to-top characterization parameter	1.0	
ψ_{JB}	Junction-to-board characterization parameter	37.8	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	11.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

PIN FUNCTIONS

bq7718xy	Pin Name	Type I/O	Description
1	VDD	P	Power supply
2	V5	I	Sense input for positive voltage of the fifth cell from the bottom of the stack
3	V4	I	Sense input for positive voltage of the fourth cell from the bottom of the stack
4	V3	I	Sense input for positive voltage of the third cell from the bottom of the stack
5	V2	I	Sense input for positive voltage of the second cell from the bottom of the stack
6	V1	I	Sense input for positive voltage of the lowest cell in the stack
7	VSS	P	Electrically connected to IC ground and negative terminal of the lowest cell in the stack
8	OUT	O	Output drive for overvoltage fault signal

PIN DETAILS

In the bq7718xy device, each cell is monitored independently. Overvoltage is detected by comparing the actual cell voltage to a protection voltage reference, V_{OV}. If any cell voltage exceeds the programmed OV value, a timer circuit is activated. When the timer expires, the OUT terminal goes from inactive to active state.

For NCH Open Drain Active Low configurations, the OUT pin pulls down to VSS when active (OV present) and is high impedance when inactive (no OV).

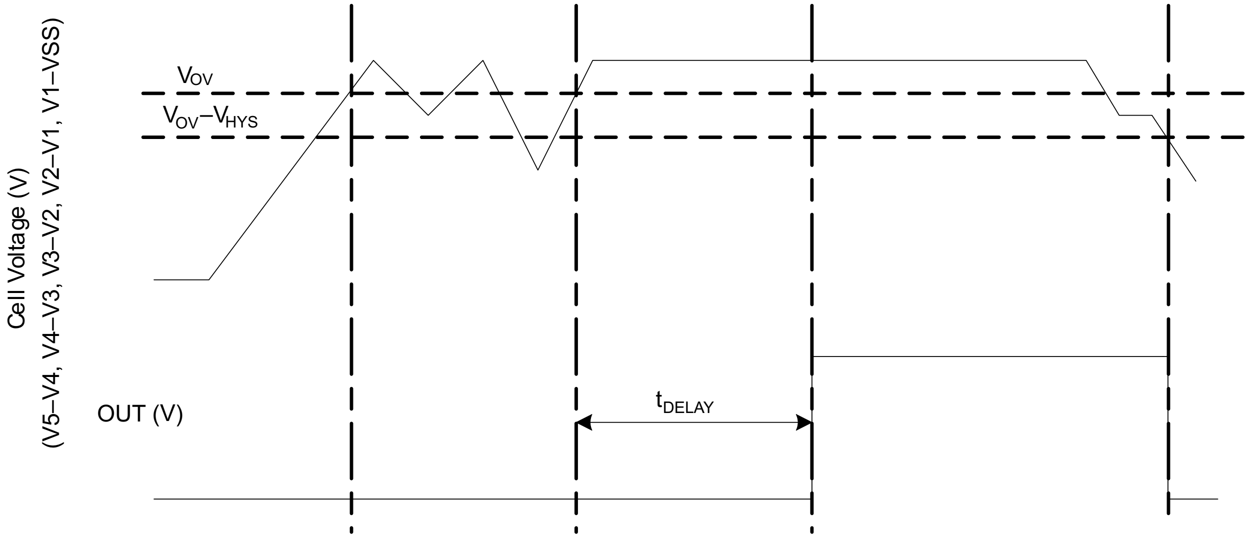


Figure 2. Timing for Overvoltage Sensing

Sense Positive Input for Vx

This is an input to sense each single battery cell voltage. A series resistor and a capacitor across the cell for each input is required for noise filtering and stable voltage monitoring.

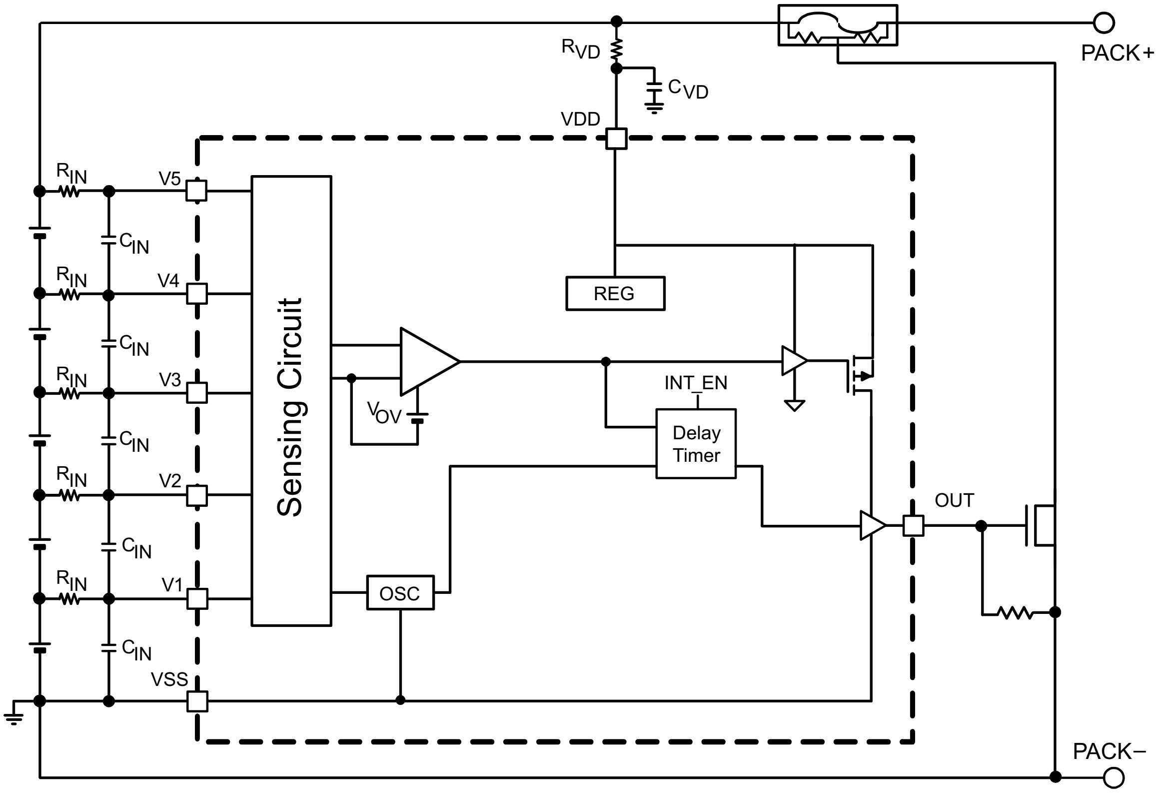
Output Drive, OUT

This terminal serves as the fault signal output, and may be ordered in either active HIGH or LOW options.

Supply Input, VDD

This terminal is the unregulated input power source for the IC. A series resistor is connected to limit the current, and a capacitor is connected to ground for noise filtering.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER	CONDITION	VALUE/UNIT
Supply voltage range	VDD–VSS	–0.3 to 30 V
Input voltage range	V5–VSS or V4–VSS or V3–VSS or V2–VSS or V1–VSS	–0.3 to 30 V
Output voltage range	OUT–VSS	–0.3 to 30 V
Continuous total power dissipation, P_{TOT}		See package dissipation rating.
Functional temperature		–40 to 110°C
Storage temperature range, T_{STG}		–65 to 150°C
Lead temperature (soldering, 10 s), T_{SOLDER}		300°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum–rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (1)		3		25	V
Input voltage range	V5–V4 or V4–V3 or V3–V2 or V2–V1 or V1–VSS	0		5	V
Operating ambient temperature range, T_A		–40		110	°C

(1) See APPLICATION SCHEMATIC.

DC CHARACTERISTICS

Typical values stated where T_A = 25°C and VDD = 18 V, MIN/MAX values stated where T_A = –40°C to 110°C and V_{DD} = 3 V to 25 V (unless otherwise noted).

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Voltage Protection Threshold VCx						
V_{OV}	$V_{(PROTECT)}$ Overvoltage Detection	bq771800		4.300		V
		bq771801		4.275		V
		bq771803		4.275		V
		bq771802		4.225		V
		bq771804(1)		4.225		V
		bq771805(1)		4.325		V
		bq771806(1)		4.350		V
		bq771807(1)		4.450		V
		bq771808		4.200		V
		bq771809		4.200		V
		bq771810(1)		4.200		V
		bq771811(1)		4.225		V
		bq771812(1)		4.250		V
		bq771813(1)		4.250		V
		bq771814(1)		3.900		V
		bq771815(1)		4.225		V
		bq771816(1)		4.250		V
V_{HYS}	OV Detection Hysteresis	bq771800	250	300	400	mV
		bq771801	0	50	100	V
		bq771802	250	300	400	mV
		bq771803	0	50	100	V
		bq771804(1)	250	300	400	mV
		bq771805(1)	250	300	400	mV
		bq771806(1)	250	300	400	mV
		bq771807(1)	250	300	400	mV
		bq771808	0	50	100	V
		bq771809	0	50	100	V
		bq771810(1)	200	250	250	mV
		bq771811(1)	0	50	100	V
		bq771812(1)	0	50	100	V
		bq771813(1)	0	50	100	V
		bq771814(1)	250	300	400	mV
		bq771815(1)	0	50	100	V
		bq771816(1)	0	50	100	V
V_{OA}	OV Detection Accuracy	T_A = 25°C	–10		10	mV
$V_{OADRIFT}$	OV Detection Accuracy Across Temperature	T_A = –40°C	–40		44	mV
		T_A = 0°C	–20		20	mV
		T_A = 60°C	–24		24	mV
		T_A = 110°C	–54		54	mV
Supply and Leakage Current						
I_{CC}	Supply Current	(V5–V4) = (V4–V3) = (V3–V2) = (V2–V1) = (V1–VSS) = 4.0 V (See Figure 13.)		1	2	µA
I_{IN}	Input Current at Vx Pins	(V5–V4) = (V4–V3) = (V3–V2) = (V2–V1) = (V1–VSS) = 4.0 V (See Figure 13.)	–0.1		0.1	µA

(1) Product Preview only.

DC CHARACTERISTICS (continued)

Typical values stated where T_A = 25°C and VDD = 18 V, MIN/MAX values stated where T_A = –40°C to 110°C and V_{DD} = 3 V to 25 V (unless otherwise noted).

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Output Drive OUT, CMOS Active HIGH Versions Only						
V_{OUT1}	Output Drive Voltage, Active High	(V5–V4), (V4–V3), (V3–V2), (V2–V1), or (V1–VSS) > V_{OV}, VDD = 18 V, I_{OH} = 100 µA	6			V
		If three of four cells are short circuited and only one cell remains powered and > V_{OV}, VDD = Vx (cell voltage), I_{OH} = 100 µA		VDD – 0.3		V
		(V5–V4), (V4–V3), (V3–V2), (V2–V1), and (V1–VSS) < V_{OV}, VDD = 18 V, I_{OL} = 100 µA measured into pin		250	400	mV
I_{OUTH1}	OUT Source Current (during OV)	(V5–V4), (V4–V3), (V3–V2), (V2–V1), or (V1–VSS) > V_{OV}, VDD = 18 V. OUT = 0 V. Measured out of OUT pin			4.5	mA
I_{OUTL1}	OUT Sink Current (no OV)	(V5–V4), (V4–V3), (V3–V2), (V2–V1), and (V1–VSS) < V_{OV}, VDD = 18 V, OUT = VDD. Measured into OUT pin	0.5		14	mA
Output Drive OUT, NCH Open Drain Active LOW Versions Only						
V_{OUT2}	Output Drive Voltage, Active Low	(V5–V4), (V4–V3), (V3–V2), (V2–V1), or (V1–VSS) > V_{OV}, VDD = 18 V, I_{OL} = 100 µA measured into OUT pin		250	400	mV
I_{OUTH2}	OUT Sink Current (during OV)	(V5–V4), (V4–V3), (V3–V2), (V2–V1), or (V1–VSS) > V_{OV}, VDD = 18 V. OUT = VDD. Measured into OUT pin	0.5		14	mA
I_{OUTL2}	OUT Source Current (no OV)	(V5–V4), (V4–V3), (V3–V2), (V2–V1), and (V1–VSS) < V_{OV}, VDD = 18 V. OUT = VDD. Measured out of OUT pin			100	nA
Delay Timer						
t_{DELAY}	OV Delay Time	bq771800	3.2	4	4.8	s
		bq771801	2.4	3	3.6	s
		bq771802, bq771803	0.8	1	1.2	s
		Preview option only. Contact TI.	4.4	5.5	6.6	s
$X_{CTMDELAY}$	Fault Detection Delay Time during Customer Test Mode	See CUSTOMER TEST MODE.		15		ms

TYPICAL CHARACTERISTICS

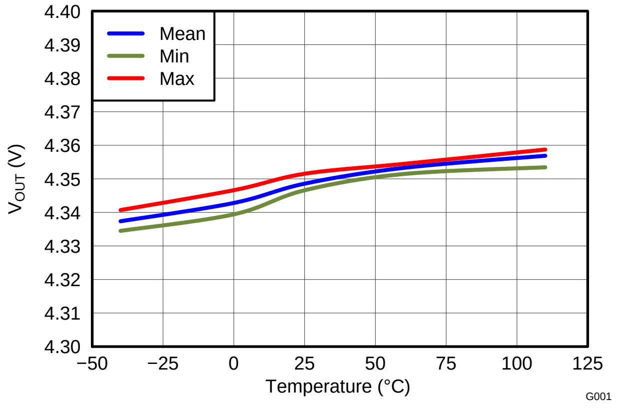


Figure 3. Overvoltage Threshold (OVT) vs. Temperature

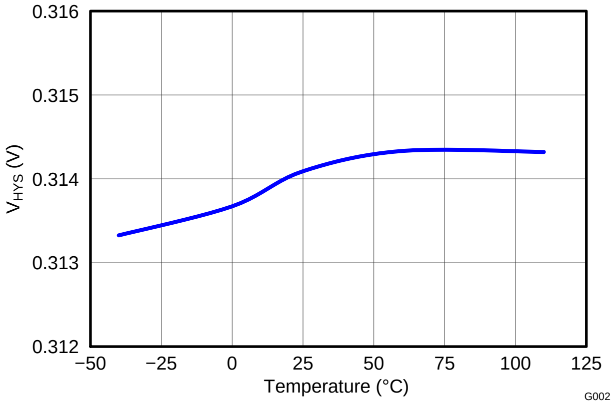


Figure 4. Hysteresis V_{HYS} vs. Temperature

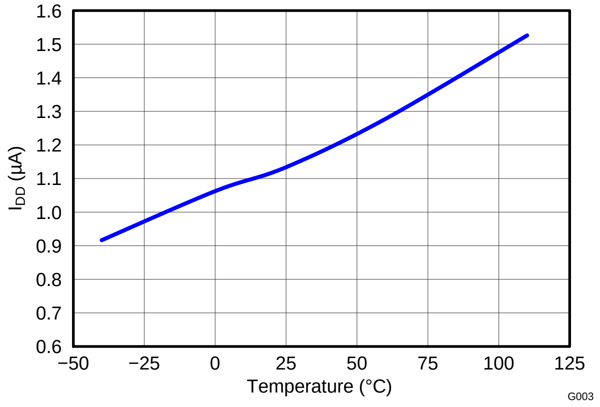


Figure 5. I_{DD} Current Consumption vs. Temperature at VDD = 16 V

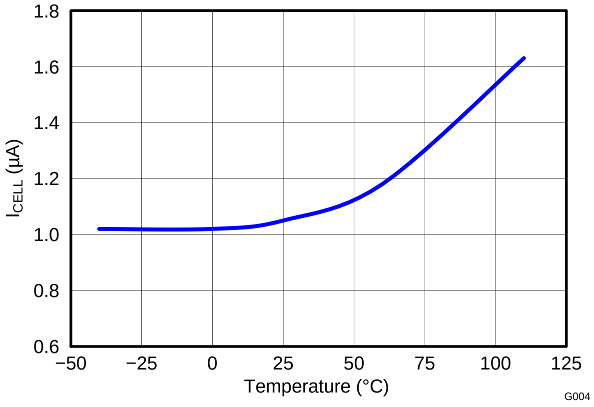


Figure 6. I_{CELL} vs. Temperature at V_{CELL}= 9.2 V

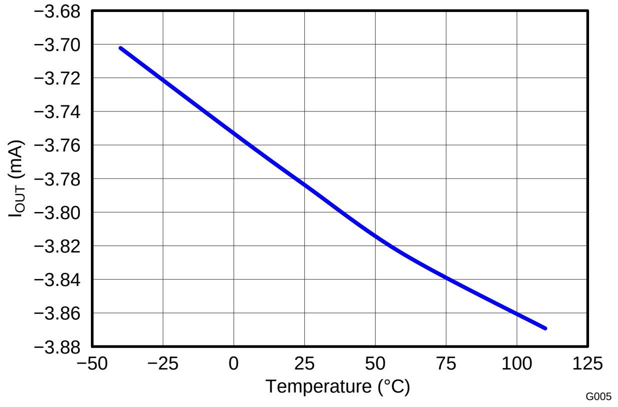


Figure 7. Output Current I_{OUT} vs. Temperature

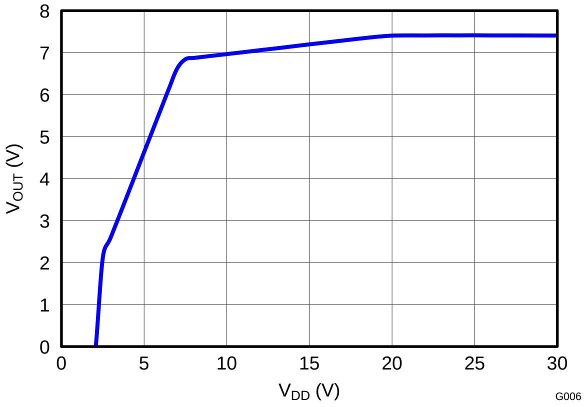


Figure 8. V_{OUT} vs. V_{DD}

APPLICATION INFORMATION

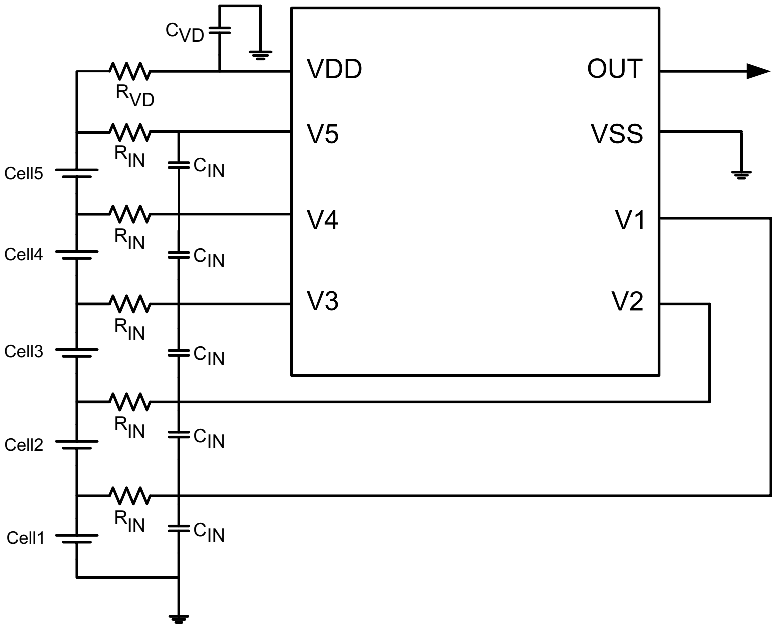


Figure 9. Application Configuration

NOTE

In the case of an Open Drain Active Low configuration, an external pull-up resistor is required on the OUT terminal.

Changes to the ranges stated in Table 1 will impact the accuracy of the cell measurements.

Changes to the ranges stated in Table 1 will impact the accuracy of the cell measurements. Figure 9 shows each external component.

Table 1. Parameters

PARAMETER	EXTERNAL COMPONENT	MIN	NOM	MAX	UNIT
Voltage monitor filter resistance	RIN	900	1000	1100	Ω
Voltage monitor filter capacitance	CIN	0.01		0.1	µF
Supply voltage filter resistance	RVD	100		1K	Ω
Supply voltage filter capacitance	CVD		0.1		µF
CD external delay capacitance			0.1	1	µF
OUT Open drain version pull-up resistance to PACK+			100		kΩ

NOTE

The device is calibrated using an R_{IN} value = 1 kΩ. Using a value other than this recommended value changes the accuracy of the cell voltage measurements and V_{OV} trigger level.

APPLICATION SCHEMATIC

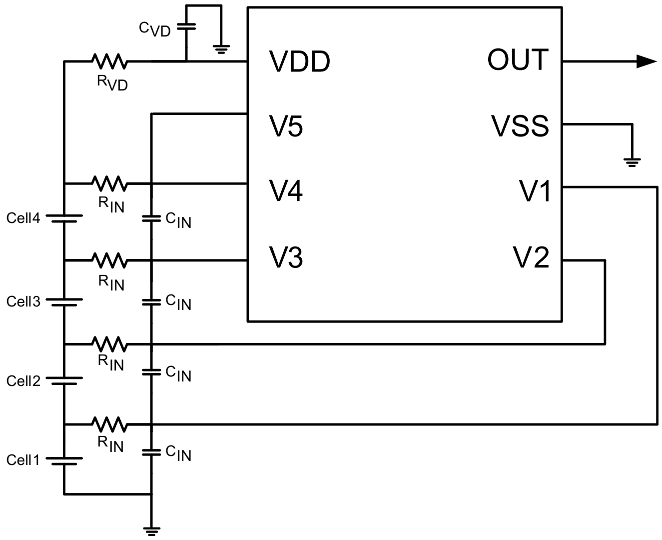


Figure 10. 4-Series Cell Configuration

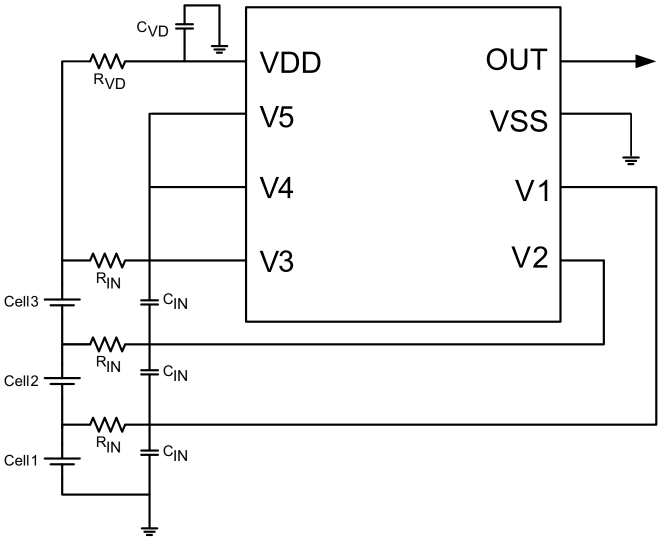


Figure 11. 3-Series Cell Configuration with Fixed Delay

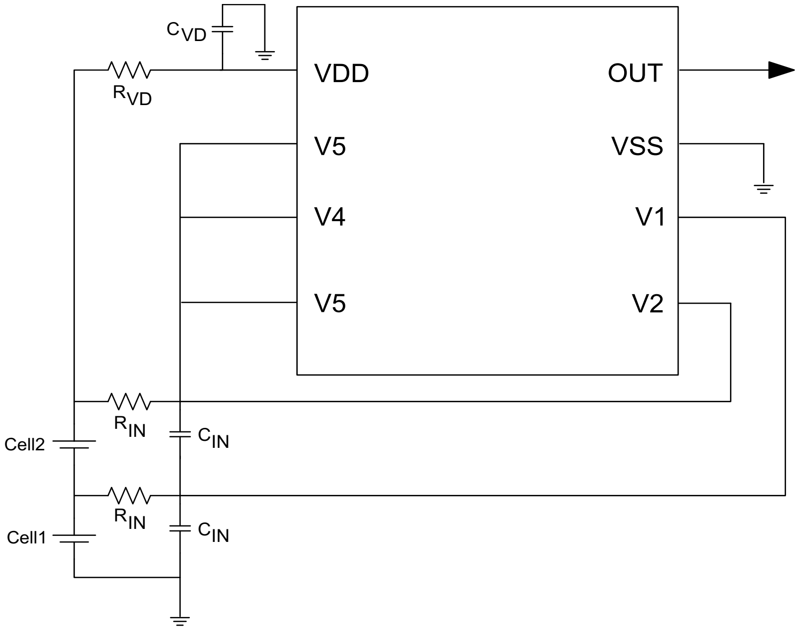


Figure 12. 2-Series Cell Configuration with Internal Fixed Delay

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NOTE

In these application examples, an external pull-up resistor is required on the OUT terminal to configure for an Open Drain Active Low operation.

CUSTOMER TEST MODE

Customer Test Mode (CTM) helps to reduce test time for checking the overvoltage delay timer parameter once the circuit is implemented in the battery pack. To enter CTM, VDD should be set to at least 10 V higher than V5 (see Figure 13). The delay timer is greater than 10 ms, but considerably shorter than the timer delay in normal operation. To exit Customer Test Mode, remove the VDD to V5 voltage differential of 10 V so that the decrease in this value automatically causes an exit.

CAUTION

Avoid exceeding any Absolute Maximum Voltages on any pins when placing the part into Customer Test Mode. Also avoid exceeding Absolute Maximum Voltages for the individual cell voltages (V5–V4), (V4–V3), (V4–V3), (V3–V2), (V2–V1), and (V1–VSS). Stressing the pins beyond the rated limits may cause permanent damage to the device.

Figure 13 shows the timing for the Customer Test Mode.

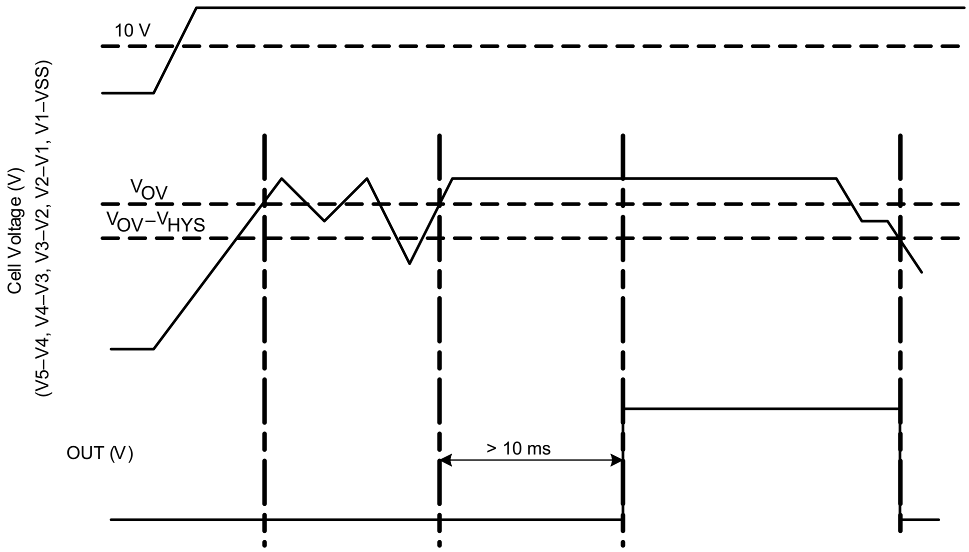

Figure 13. Timing for Customer Test Mode

Figure 14 shows the measurement for current consumption for the product for both VDD and Vx.

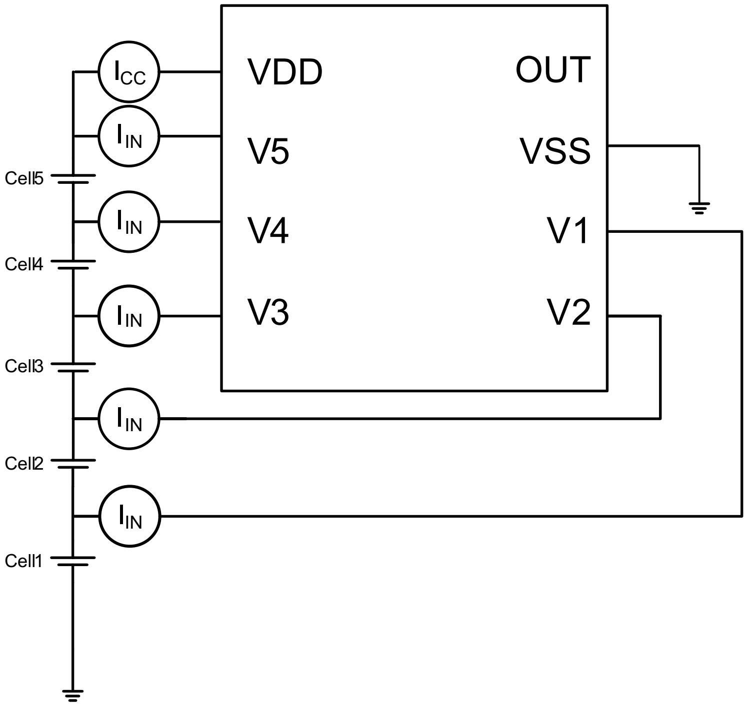

Figure 14. Configuration for IC Current Consumption Test

REVISION HISTORY

Changes from Original (December 2012) to Revision A	Page
• Added bq771808 device to Production Data	2

Changes from Revision A (September 2013) to Revision B	Page
• Added bq771809 device to Production Data	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ771800DPJR	ACTIVE	WSON	DPJ	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		771800	Samples
BQ771800DPJT	ACTIVE	WSON	DPJ	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		771800	Samples
BQ771801DPJR	ACTIVE	WSON	DPJ	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		771801	Samples
BQ771801DPJT	ACTIVE	WSON	DPJ	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		771801	Samples
BQ771802DPJR	ACTIVE	WSON	DPJ	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		771802	Samples
BQ771802DPJT	ACTIVE	WSON	DPJ	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		771802	Samples
BQ771803DPJR	ACTIVE	WSON	DPJ	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		771803	Samples
BQ771803DPJT	ACTIVE	WSON	DPJ	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		771803	Samples
BQ771808DPJR	ACTIVE	WSON	DPJ	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	771808	Samples
BQ771808DPJT	ACTIVE	WSON	DPJ	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	771808	Samples
BQ771809DPJR	ACTIVE	WSON	DPJ	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	771809	Samples
BQ771809DPJT	ACTIVE	WSON	DPJ	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	771809	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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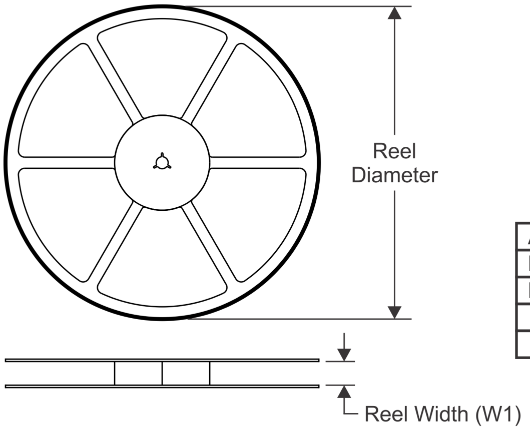
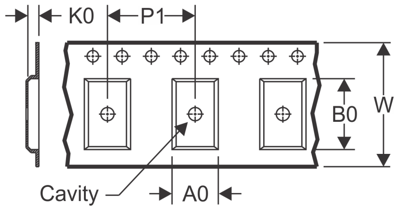
TAPE AND REEL INFORMATION

REEL DIMENSIONS

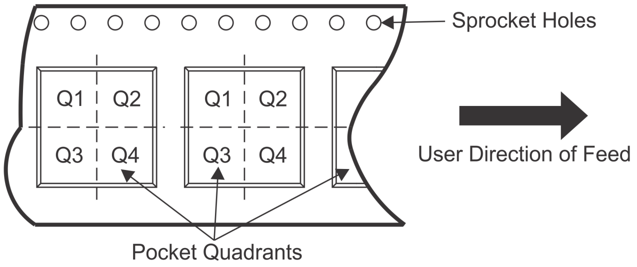


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

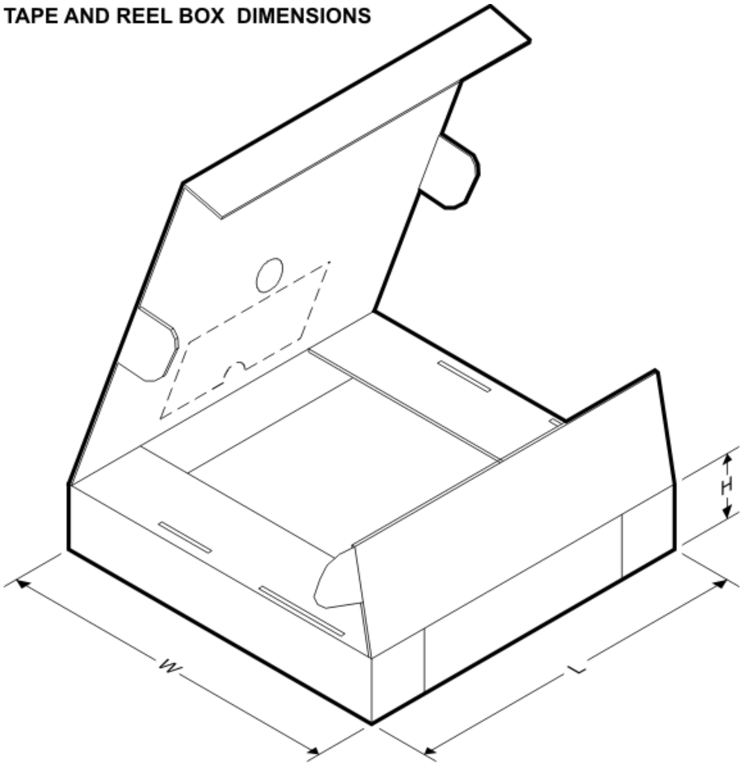
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ771800DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771800DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771801DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771801DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771802DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771802DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771803DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771803DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771808DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771808DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771809DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771809DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2

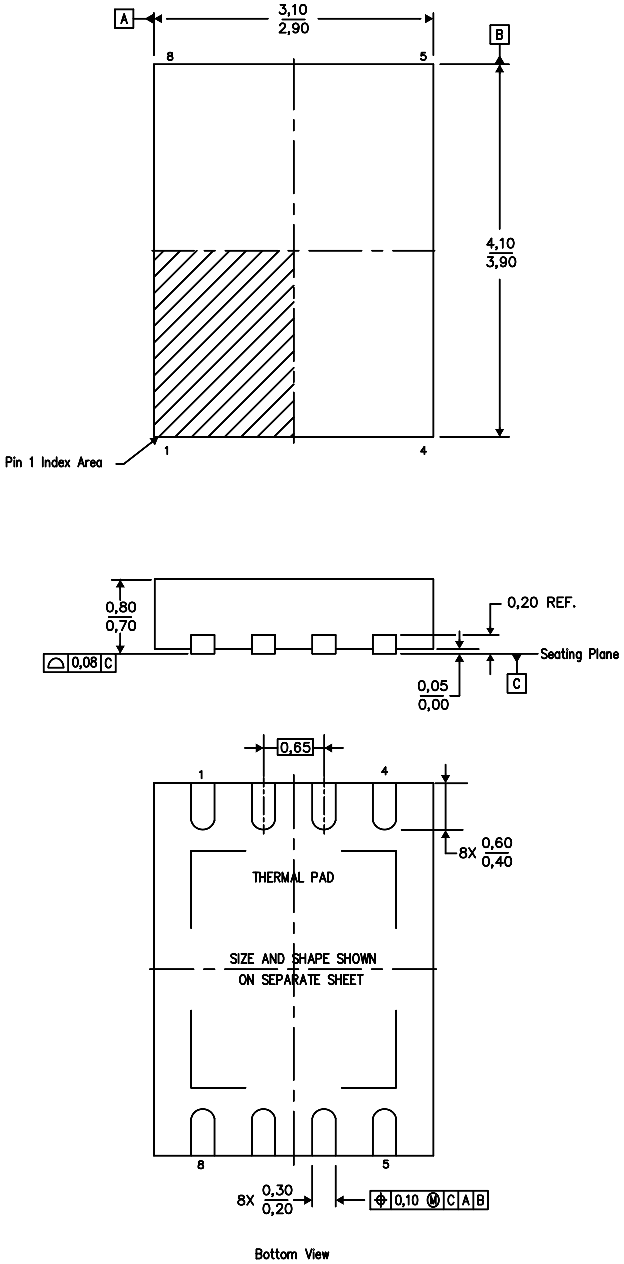
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ771800DPJR	WSON	DPJ	8	3000	367.0	367.0	35.0
BQ771800DPJT	WSON	DPJ	8	250	210.0	185.0	35.0
BQ771801DPJR	WSON	DPJ	8	3000	367.0	367.0	35.0
BQ771801DPJT	WSON	DPJ	8	250	210.0	185.0	35.0
BQ771802DPJR	WSON	DPJ	8	3000	367.0	367.0	35.0
BQ771802DPJT	WSON	DPJ	8	250	210.0	185.0	35.0
BQ771803DPJR	WSON	DPJ	8	3000	367.0	367.0	35.0
BQ771803DPJT	WSON	DPJ	8	250	210.0	185.0	35.0
BQ771808DPJR	WSON	DPJ	8	3000	367.0	367.0	35.0
BQ771808DPJT	WSON	DPJ	8	250	210.0	185.0	35.0
BQ771809DPJR	WSON	DPJ	8	3000	367.0	367.0	35.0
BQ771809DPJT	WSON	DPJ	8	250	210.0	185.0	35.0

DPJ (R–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



4212590/B 04/12

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Small Outline No–Lead (SON) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

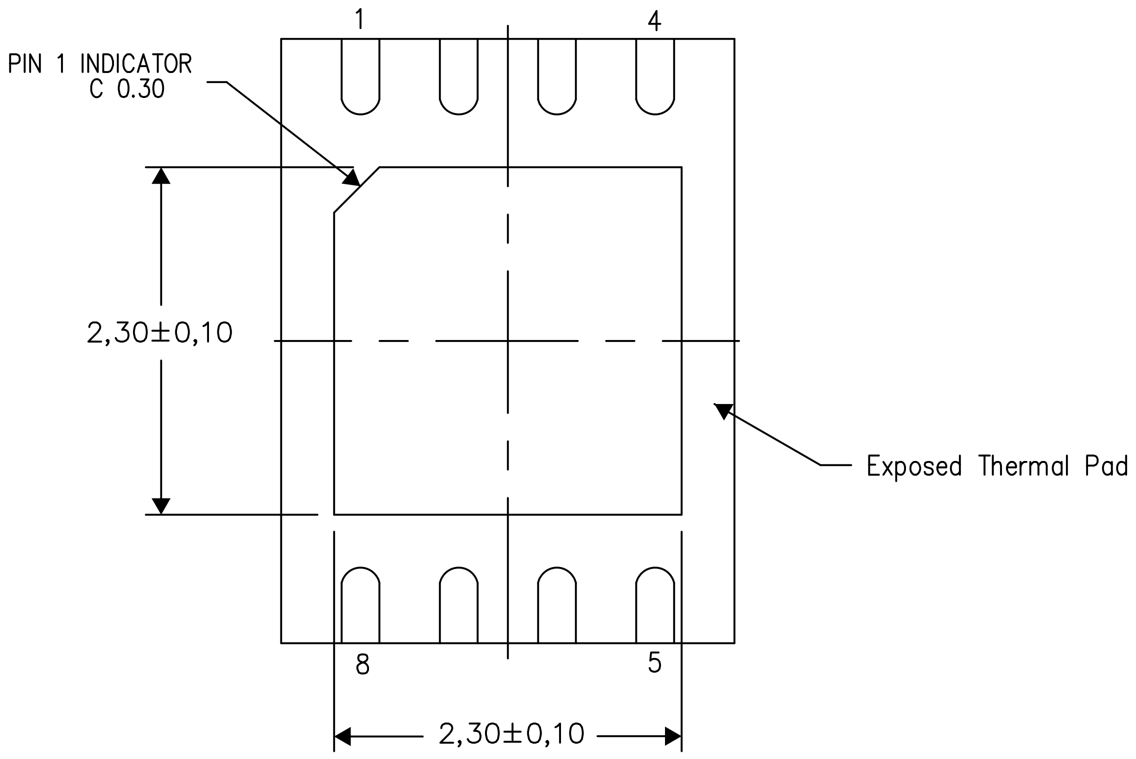
DPJ (R-PWSON-N8) PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

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NOTE: All linear dimensions are in millimeters

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