High-performance Clock Generator Series

Clock Generator with Built-in VCXO for A/V Equipments

BU2365FV

No.09005EAT05

●Description

The ROHM Clock Generator is an IC allowing for the generation of multiple clocks by a single chip through the connection of a single crystal oscillator. The BU2365FV incorporates the ROHM's unique PLL technology to provide the generation of multiple high C/N clocks necessary for the DVD recorder system. This Clock Generator has the built-in high-precision VCXO function and allows for high-precision synchronization with DVD Video clocks. It also has a built-in buffer having high driving force and allows the supply of multiple 27MHz Video clocks for the system, thus providing the reduced number of the system components.

●Features

1) The ROHM's unique PLL technology allows for the generation of high C/N clocks.
2) Built-in high precision VCXO, which is essential for the DVD recorder system
3) Built-in buffer having high driving force (Load capacity/output CL=50pF, 27MHz drive, 1×input / 2×outputs)
4) Built-in half pulse clock protection [HPC]
5) Built-in power down function, Icc=0 uA(typ.)
6) SSOP-B24 package
7) Single power supply of 3.3 V

●Application

DVD recorder

●Absolute Maximum Ratings（Ta=25℃）

Parameter	Symbol	Limits	Unit
Supply voltage	VDD	-0.3~7.0	V
Input voltage	VIN	-0.3~VDD+0.3	V
Storage temperature range	Tstg	-30~125	℃
Power dissipation	PD	820	mW

*1 Operation is not guaranteed.
*2 In the case of exceeding Ta = 25℃, 8.2mW should be reduced per 1℃.
*3 The radiation-resistance design is not carried out.
*4 Power dissipation is measured when the IC is mounted to the printed circuit board.

●Recommended Operating Range

Parameter	Symbol	Limit	Unit
Supply voltage	VDD	3.0~3.6	V
Input H voltage	VINH	0.8VDD~VDD	V
Input L voltage	VINL	0.0~0.2VDD	V
Operating temperature	Topr	-10~70	℃
22Pin / 19Pin	CL_CLK768FS/384FS	32(MAX)	pF
13Pin , 14Pin	CL_BUFOUT	50(MAX)	pF
18Pin / 24Pin	CL_CLK512FS/54M	15(MAX)	pF

●**Electrical characteristics**

VDD=3.3V, Ta=25℃, Crystal frequency (XTAL_IN)=27.000000MHz, at no load, unless otherwise specified.

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
【Consumption circuit current】	IDD	−	55	71.5	mA	At no output loads
【Output H voltage】	VOH	2.4	−	−	V	When current load = -4.0mA
【Output L voltage】	VOL	−	−	0.4	V	When current load =4.0mA
【Pull-Up resistance value】 FSEL,OE	Pull-Up R	168	260	578	kΩ	Specified by a current value running when a voltage of 0V is applied to a measuring pin. (R=DD/I)
【Pull-Down resistance value】 TEST	Pull-downR	31	48	106	kΩ	Specified by a current value running when a VDD is applied to a measuring pin. (R=VDD/I)
【Output frequency】						
CLK768FS : FSEL=L	CLK768 FS_L	−	33.868800	−	MHz	XTAL_IN × (3136/625)/4
CLK768FS : FSEL=H	CLK768 FS_H	−	36.864000	−	MHz	XTAL_IN × (2048/375)/4
CLK384FS	CLK384 FS	−	18.432000	−	MHz	XTAL_IN × (2048/375)/8
CLK512FS	CLK512 FS	−	24.576000	−	MHz	XTAL_IN × (2048/375)/6
CLK54M	CLK54M	−	54.000000	−	MHz	XTAL_IN × (32/4)/4
【Output waveform】						
Duty	Duty1	45	50	55	%	Measured at a voltage of 1/2 of VDD
Rise time	Tr	−	2.5	−	nsec	Period of time required for the output to reach 80% from 20% of VDD
Fall time	Tf	−	2.5	−	nsec	Period of time required for the output to reach 20% from 80% of VDD
【Jitter】						
Period-Jitter 1σ	P-J1σ	−	50	−	psec	※1
Period-Jitter MIN-MAX	P-J MIN-MAX	−	300	−	psec	※2
【Output Lock-Time】	Tlock	−	−	1	msec	※3
【Frequency stability】	ΔF/F0	−15	−	15	ppm	T=-10~70℃,VDD=3.3V±0.15V ※4
【Frequency sensitivity】	ΔF/Fc	±30	±45	±60	ppm	※5
【Frequency sensitivity linearity】	Linearity	−10		10	ppm	※5
【Buffer skew】	Tskew_BUF	−500	−	500	psec	Phase difference between BUF_OUT1 and BUF_OUT2∗6
【Buffer delay】	Td_BUF	−	4	8	nsec	Phase difference between BUF_IN and BUF_OUT

Note) The output frequency is determined by the arithmetic (frequency division) expression of a frequency input to XTAL_IN.

※1 Period-Jitter 1σ

This parameter represents standard deviation (=1σ) on cycle distribution data at the time when the output clock cycles are sampled 1000 times consecutively with the TDS7104 Digital Phosphor Oscilloscope of Tektronix Japan, Ltd.

※2 Period-Jitter MIN-MAX

This parameter represents a maximum distribution width on cycle distribution data at the time when the output clock cycles are sampled 1000 times consecutively with the TDS7104 Digital Phosphor Oscilloscope of Tektronix Japan, Ltd.

※3 Output Lock-Time

This parameter represents elapsed time after power supply turns ON to reach a voltage of 3.0 V, after the system is switched from Power-Down state to normal operation state, or after the output frequency is switched, until it is stabilized at a specified frequency, respectively.

※4 Frequency stability

f0 : This parameter means an optimum frequency at T=25℃(27.000000 MHz), which represents a value of a single piece of IC. Since no consideration is given to the stability of the crystal oscillator, it should be separately studied according to the system in use.

※5 Frequency sensitivity/Frequency sensitivity linearity

These parameters represents that the frequency falls within the area shown in Fig. 2 in the control circuit of control voltage shown in Fig. 1. It shows the value of IC itself. Since no consideration is given to the stability of the crystal oscillator, it should be separately studied according to the system in use.

※Common – Recommended crystal oscillators

The electrical characteristics shown above have been all evaluated with the use of the crystal oscillator NX5032GA (Spec. No. EXS00A-00278) manufactured by NIHON DEMPA KOGYO CO., LTD., under the conditions of Limiting resistance Rd=30Ω and Crystal oscillator load CL=10pF. Consequently, in order to use the BU2365FV, the said crystal oscillator is recommended.

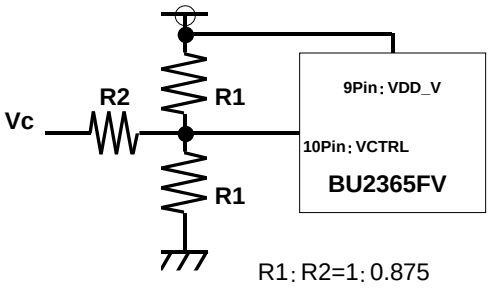
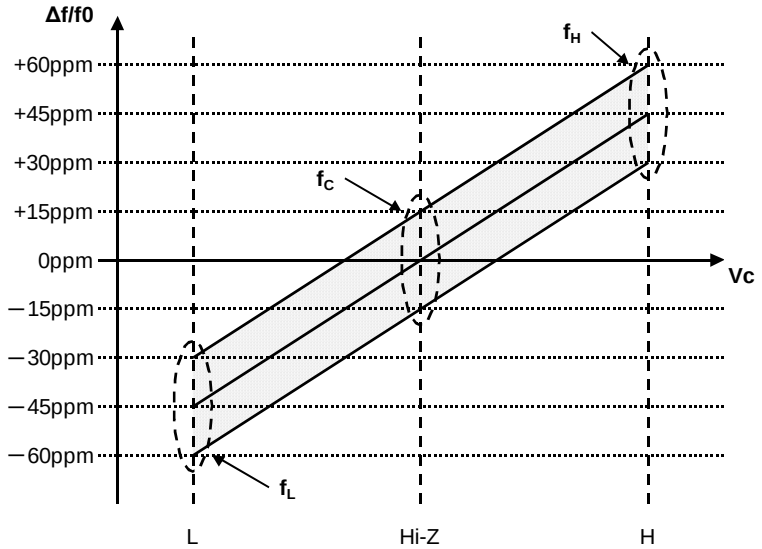


Fig.1 Control Circuit of Control Voltage



Frequency sensitivity dispersion range : f_L = -45±15ppm, f_C = 0±15ppm, f_H = 45±15ppm

However, frequency sensitivity linearity : -10ppm≦(f_H - f_C) -(f_C - f_L) ≦+10ppm

Fig. 2 Frequency Sensitivity Dispersion Range

※6 Buffer skew

This parameter is only functional when the BUF_OUT1 and the BUF_OUT2 are driven at the same load capacitance.

●Reference data (Basic data)

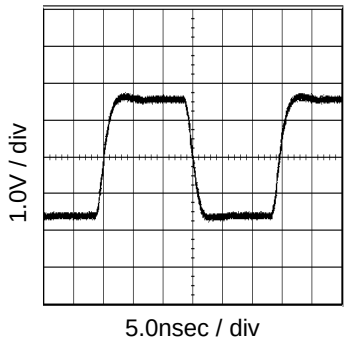


Fig.3 33.8688MHz output waveform
VDD=3.3V,CL=32pF

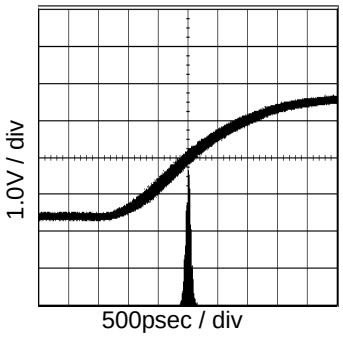


Fig.4 33.8688MHz Period-Jitter
VDD=3.3V,CL=32pF

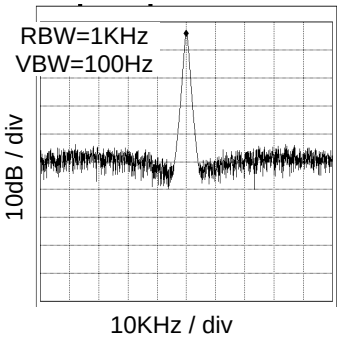


Fig.5 33.8688MHz spectrum
VDD=3.3V,CL=32pF

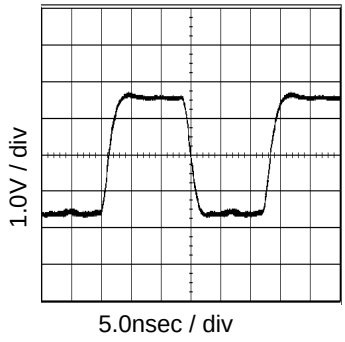


Fig.6 36.864MHz output waveform
VDD=3.3V,CL=32pF

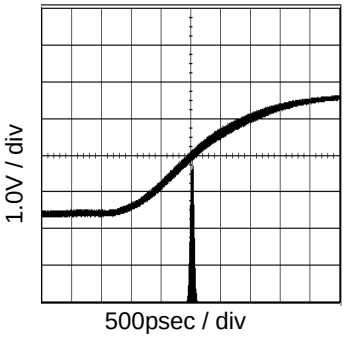


Fig.7 36.864MHz Period-Jitter
VDD=3.3V,CL=32pF

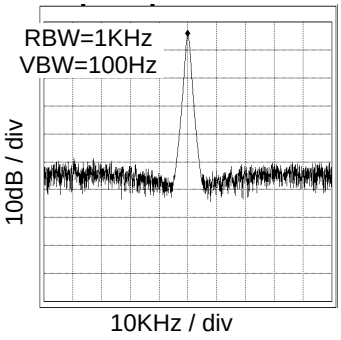


Fig.8 36.864MHz spectrum
VDD=3.3V,CL=32pF

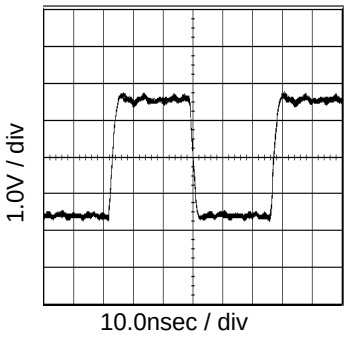


Fig.9 18.432MHz output waveform
VDD=3.3V,CL=32pF

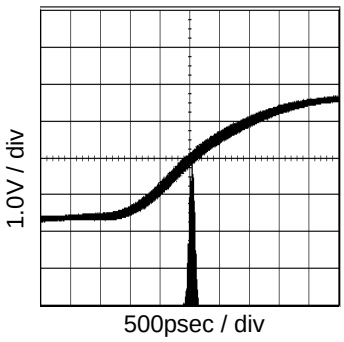


Fig.10 18.432MHz Period-Jitter
VDD=3.3V,CL=32pF

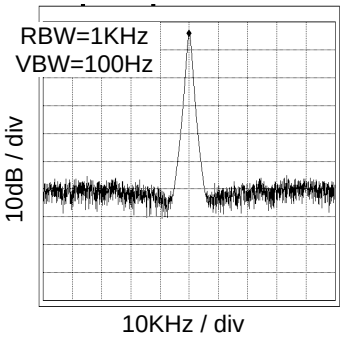


Fig.11 18.432MHz spectrum
VDD=3.3V,CL=32pF

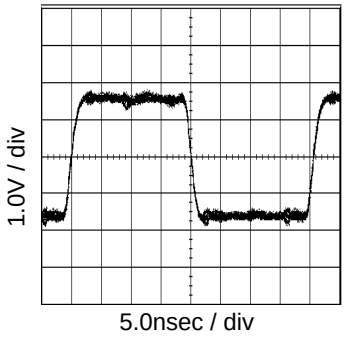


Fig.12 24.576MHz output waveform
VDD=3.3V,CL=15pF

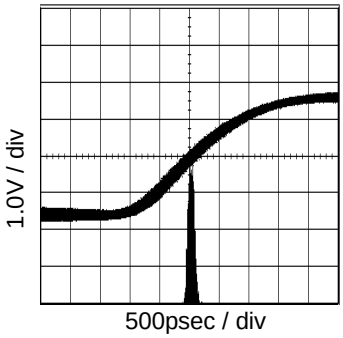


Fig.13 24.576MHz Period-Jitter
VDD=3.3V,CL=15pF

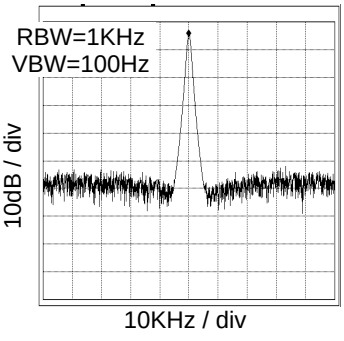


Fig.14 24.576MHz spectrum
VDD=3.3V,CL=15pF

●Reference data (Basic data)

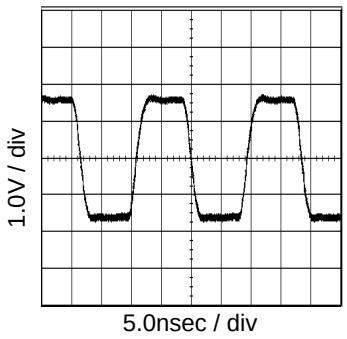


Fig.15 54MHz output waveform
VDD=3.3V,CL=15pF

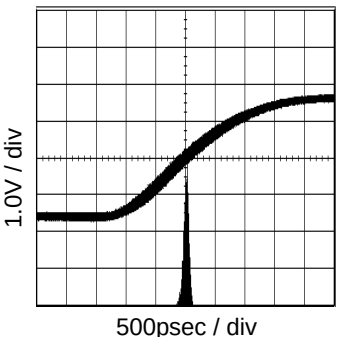


Fig.16 54MHz Period-Jitter
VDD=3.3V,CL=15pF

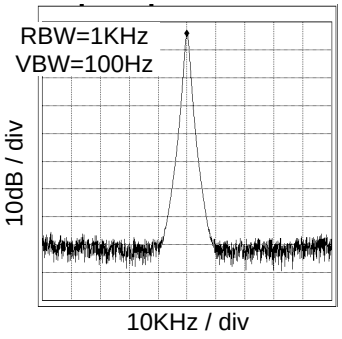


Fig.17 54MHz spectrum
VDD=3.3V,CL=15pF

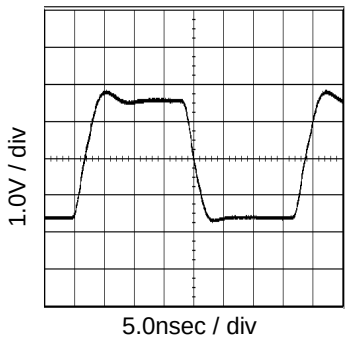


Fig.18 BUF_OUT (27MHz)
output waveform
VDD=3.3V,CL=50pF

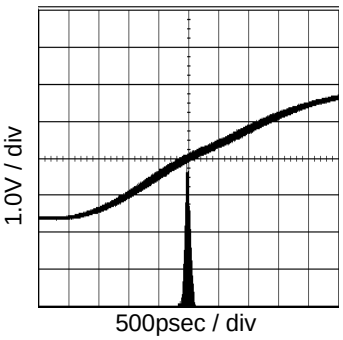


Fig.19 BUF_OUT(27MHz) Period-Jitter
VDD=3.3V,CL=50pF

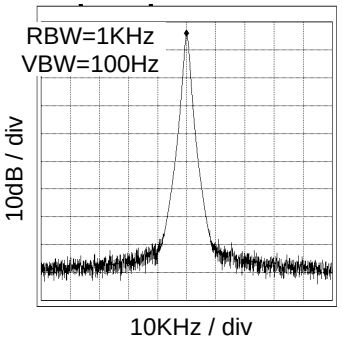


Fig.20 BUF_OUT(27MHz) spectrum
VDD=3.3V,CL=50pF

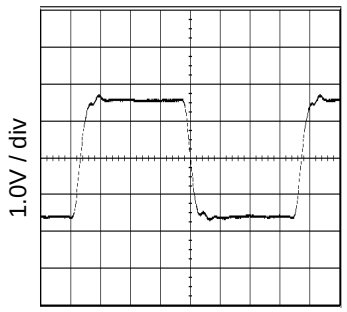


Fig.21 VCXO_OUT(27MHz)
output waveform
VDD=3.3V,CL=4pF

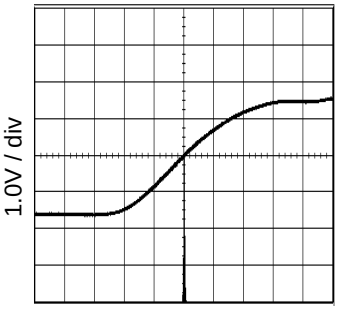


Fig.22 VCXO_OUT(27MHz) Period-Jitter
VDD=3.3V,CL=4pF

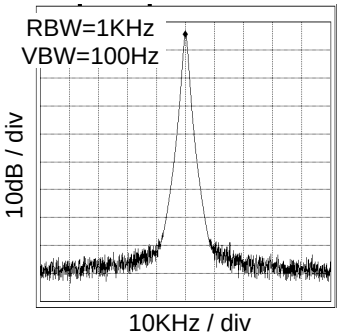


Fig.23 VCXO_OUT(27MHz) spectrum
VDD=3.3V,CL=4pF

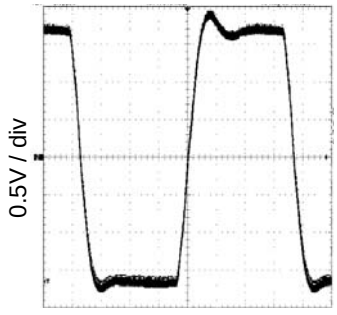


Fig.24 Buffer skew
output waveform
VDD=3.3V,CL=50pF

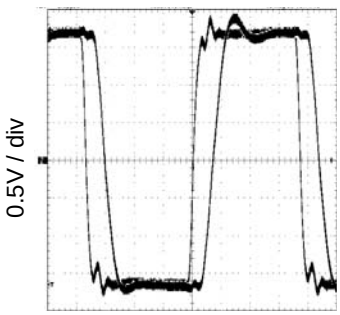


Fig.25 Buffer delay(IN→OUT1)
VDD=3.3V,CL=50pF

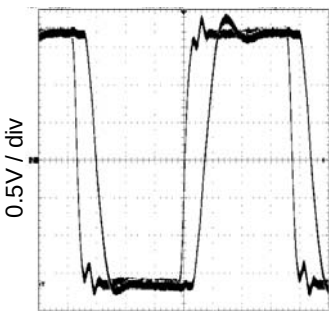


Fig.26 Buffer delay(IN→OUT2)
VDD=3.3V,CL=50pF

●Reference data (PLL: 33.8688MHz output Temperature and Supply voltage variations data)

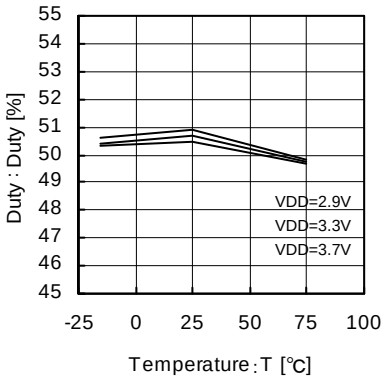


Fig.27 33.8688MHz
Temperature－Duty

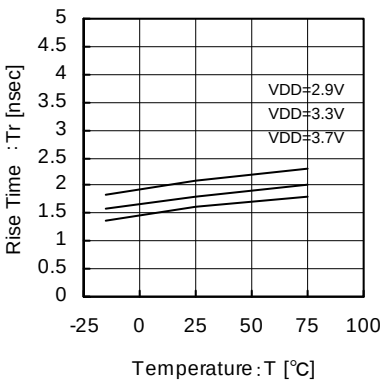


Fig.28 33.8688MHz
Temperature－rise-time

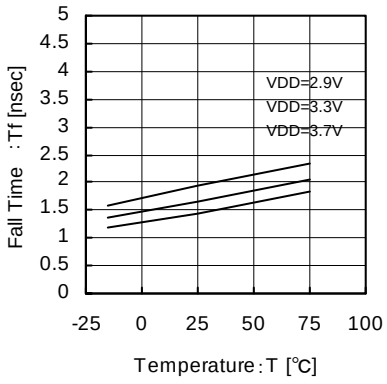


Fig.29 33.8688MHz
Temperature－fall-time

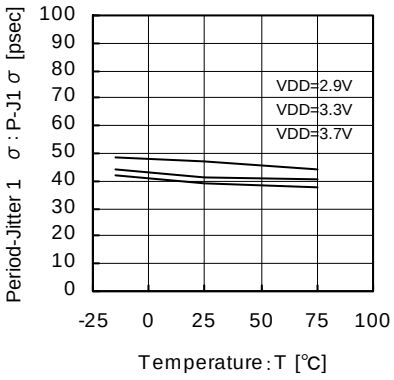


Fig.30 33.8688MHz
Temperature－Period-Jitter 1σ

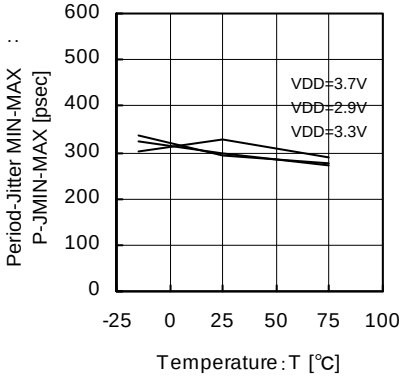


Fig.31 33.8688MHz
Temperature－Period-Jitter MIN-MAX

●Reference data (PLL: 36.864MHz output Temperature and Supply voltage variations data)

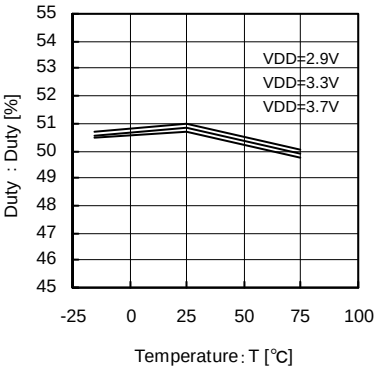


Fig.32 36.864MHz
Temperature－Duty

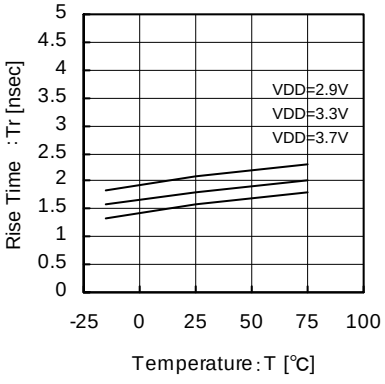


Fig.33 36.864MHz
Temperature－rise-time

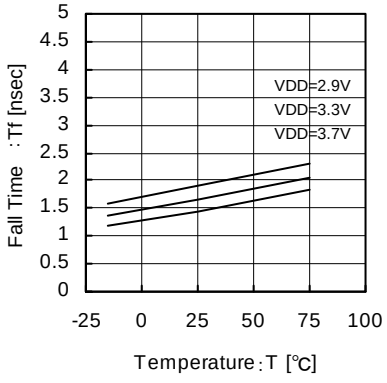


Fig.34 36.864MHz
Temperature－fall-time

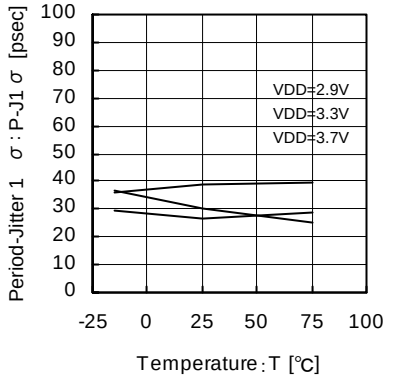


Fig.35 36.864MHz
Temperature－Period-Jitter 1σ

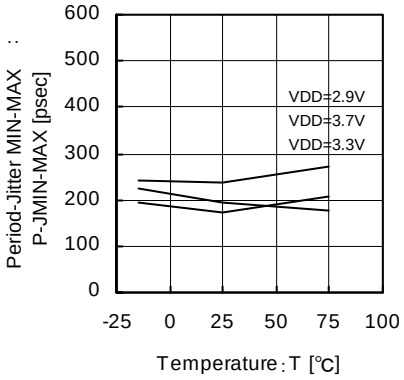


Fig.36 36.864MHz
Temperature－Period-Jitter MIN-MAX

●Reference data (PLL: 18.432MHz output Temperature and Supply voltage variations data)

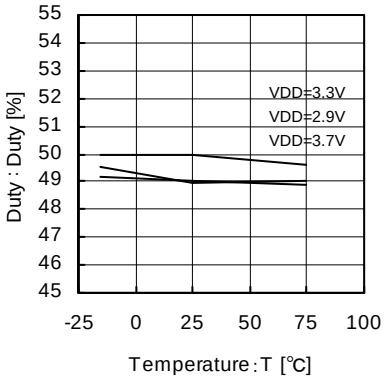


Fig.37 18.432MHz
Temperature－Duty

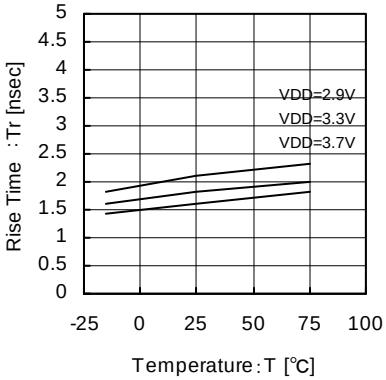


Fig.38 18.432MHz
Temperature－rise-time

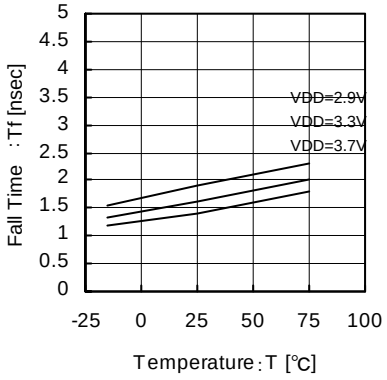


Fig.39 18.432MHz
Temperature－fall-time

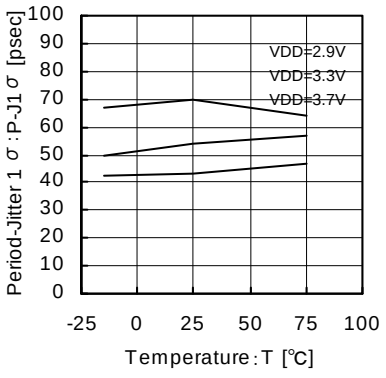


Fig.40 18.432MHz
Temperature－Period-Jitter 1σ

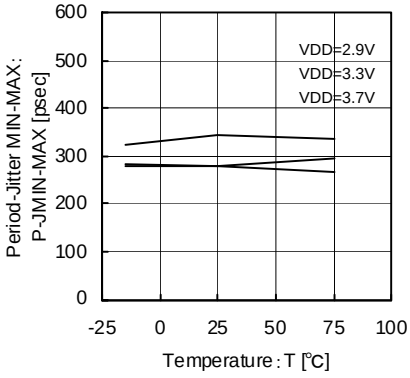


Fig.41 18.432MHz
Temperature－Period-Jitter MIN-MAX

●Reference data (PLL: 24.576MHz output Temperature and Supply voltage variations data)

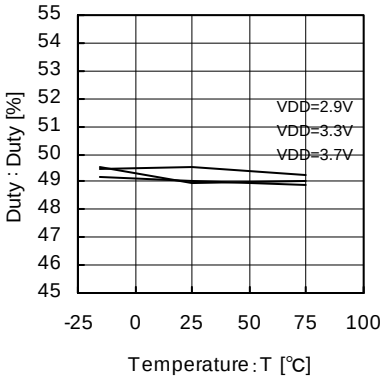


Fig.42 24.576MHz
Temperature－Duty

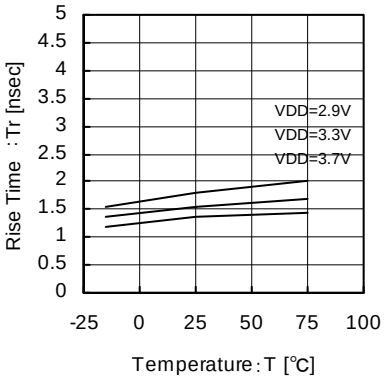


Fig.43 24.576MHz
Temperature－rise-time

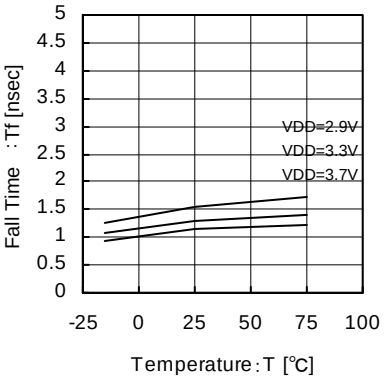


Fig.44 24.576MHz
Temperature－fall-time

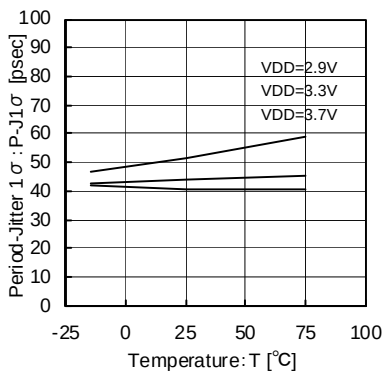


Fig.45 24.576MHz
Temperature－Period-Jitter 1σ

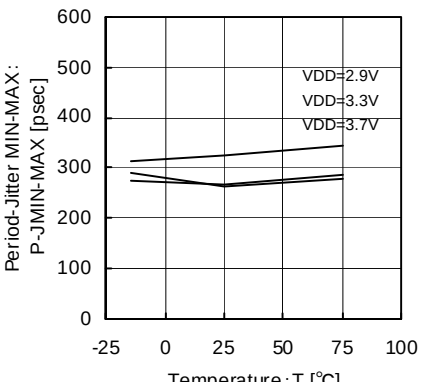


Fig.46 24.576MHz
Temperature－Period-Jitter MIN-MAX

●Reference data (PLL: 54MHz output Temperature and Supply voltage variations data)

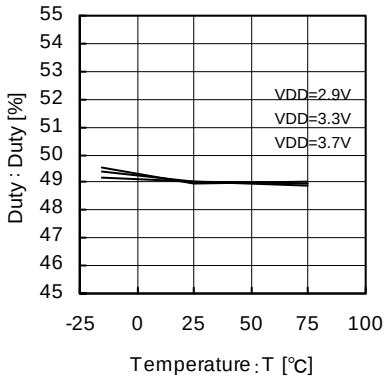


Fig.47 54MHz
Temperature－Duty

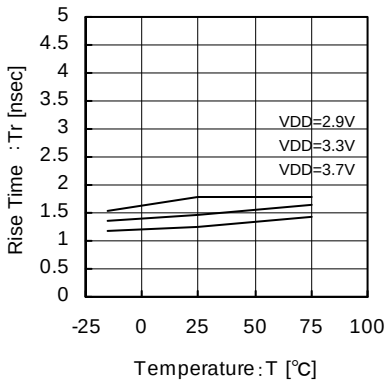


Fig.48 54MHz
Temperature－rise-time

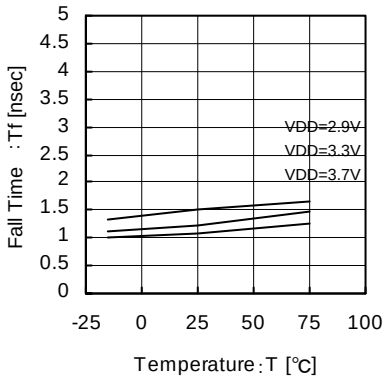


Fig.49 54MHz
Temperature－fall-time

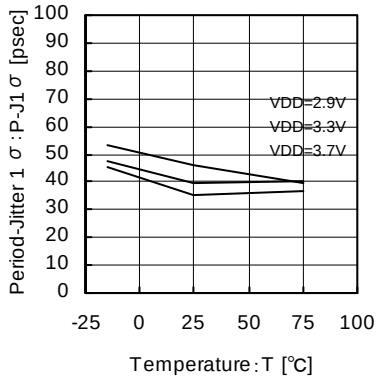


Fig.50 54MHz
Temperature－Period-Jitter 1 σ

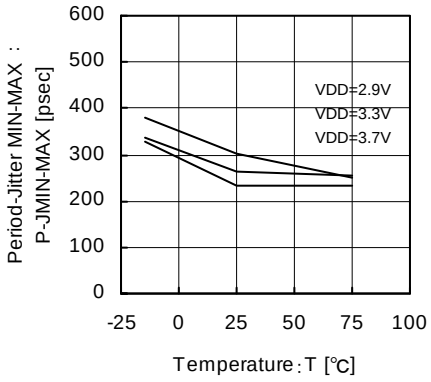


Fig.51 54MHz
Temperature－Period-Jitter MIN-MAX

●Reference data (CLOCK-BUFFER : 27MHz output Temperature and Supply voltage variations data)

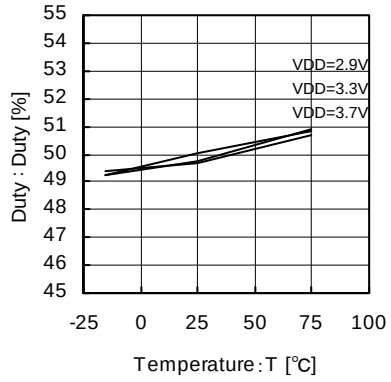


Fig.52 27MHz BUFFER
Temperature－Duty

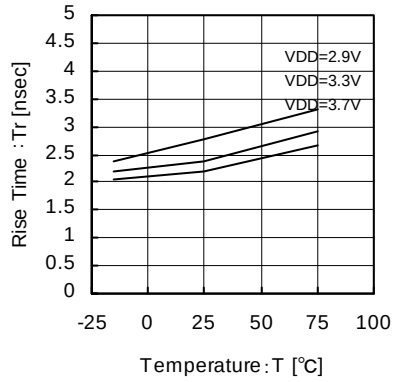


Fig.53 27MHz BUFFER
Temperature－rise-time

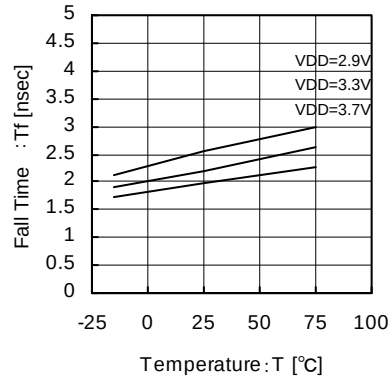


Fig.54 27MHz BUFFER
Temperature－fall-time

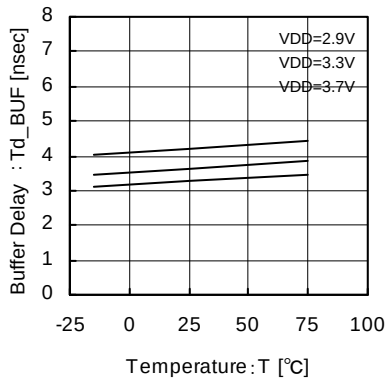


Fig.55 27MHz BUFFER
Temperature－Delay

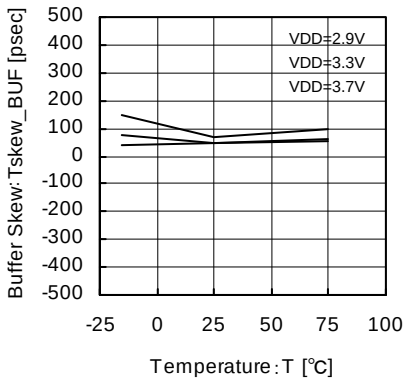


Fig.56 27MHz BUFFER
Temperature – Skew
(BUF_OUT2 Phase Lead)

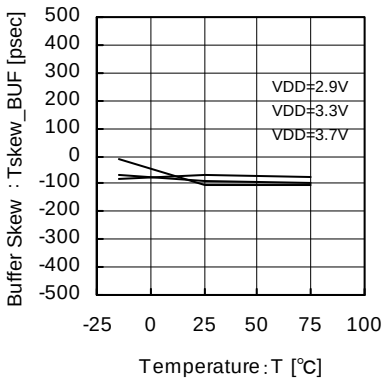


Fig.57 27MHz BUFFER
Temperature – Skew
(BUF_OUT2 Phase Delay)

●Reference data (VCXO:27MHz output Temperature and Supply voltage variations data)

This data represents the central frequency as a deviation to the optimum frequency of 27.000000MHz.

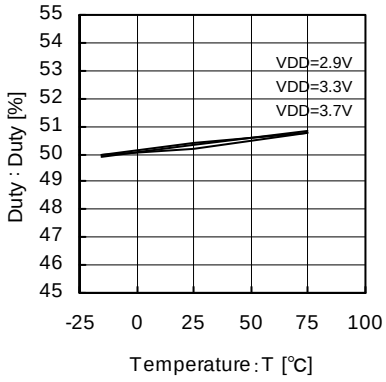


Fig.58 27MHz VCXO
Temperature－Duty

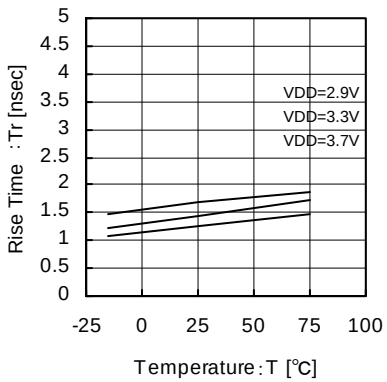


Fig.59 27MHz VCXO
Temperature－rise-time

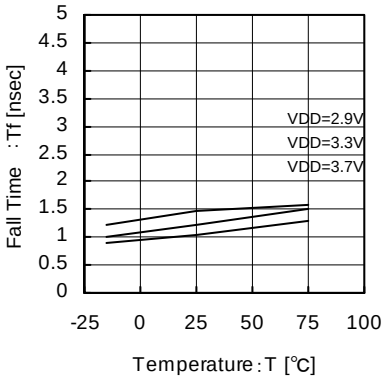


Fig.60 27MHz VCXO
Temperature－fall-time

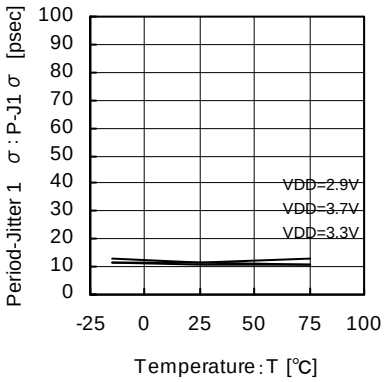


Fig.61 27MHz VCXO
Temperature－Period-Jitter 1σ

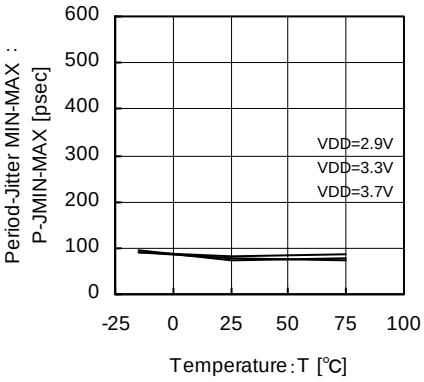


Fig.62 27MHz VCXO
Temperature－Period-Jitter MIN-MAX

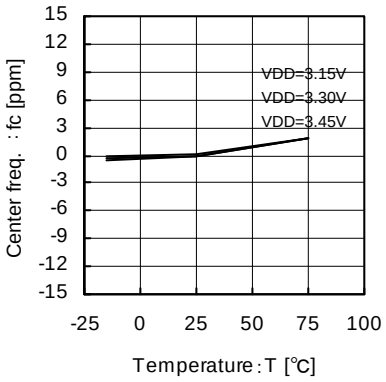


Fig.63 27MHz VCXO
Temperature – Central frequency fc

●Reference data (VCXO : 27MHz output Control voltage – Frequency data)

This data represents the central frequency as a deviation to the optimum frequency of 27.000000MHz.

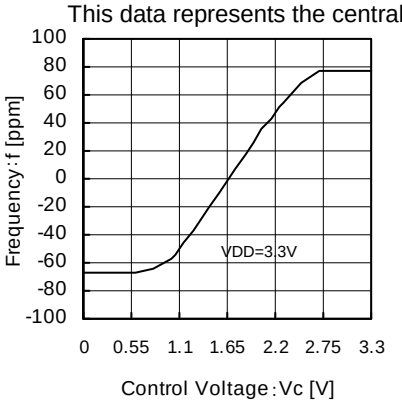


Fig.64 27MHz VCXO
Control voltage – Frequency data

●Reference data (BU2365FV consumption current Temperature and Supply voltage variations data)

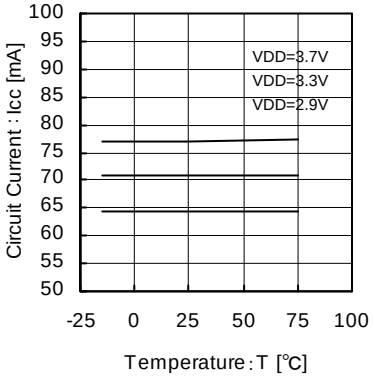


Fig.65 Maximum Load
Operating Circuit Current

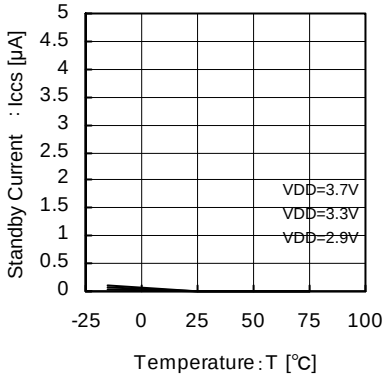


Fig.66 Power-down
Standby Current

●Reference data (PLL : Long Term Jitter data)

This data represents Period-Jitter at the 1000th cycle.

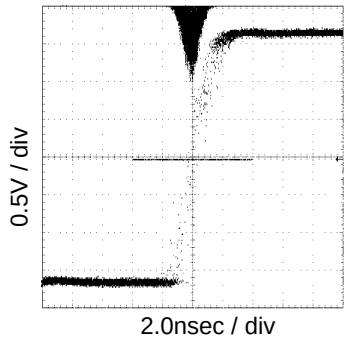


Fig.67 33.8688MHz
Long Term Jitter

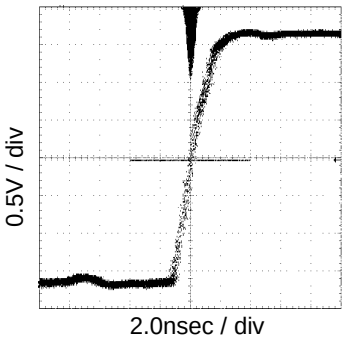


Fig.68 36.864MHz
Long Term Jitter

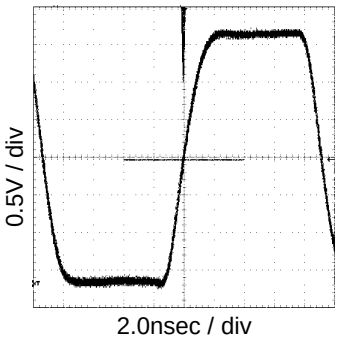


Fig.69 54MHz
Long Term Jitter

●Reference data (Period-Jitter MIN-MAX Output load CL dependence data)

This data represents the output load up to two times as high as the maximum load of each output.

Since the 27-MHz buffer is dependent on the jitter of a clock input, the output is represented by the ratio to the jitter at 50pF.

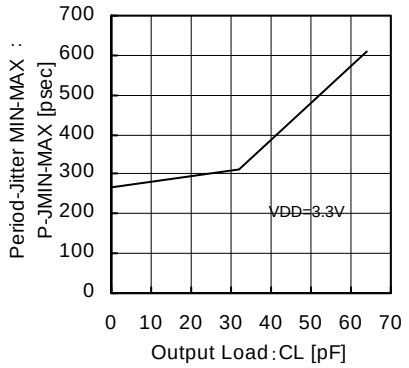


Fig.70 33.8688MHz
CL－Period-Jitter MIN-MAX

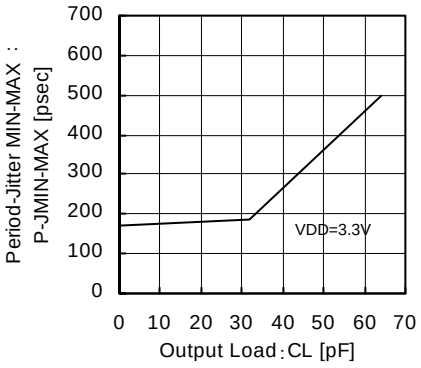


Fig.71 36.864MHz
CL－Period-Jitter MIN-MAX

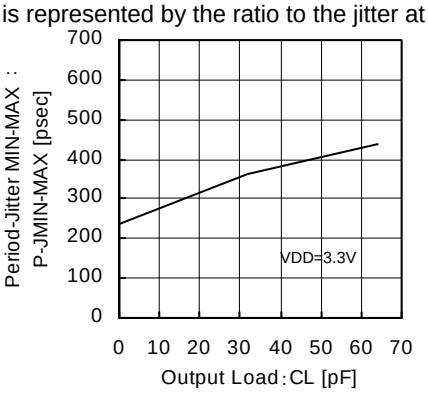


Fig.72 18.432MHz
CL－Period-Jitter MIN-MAX

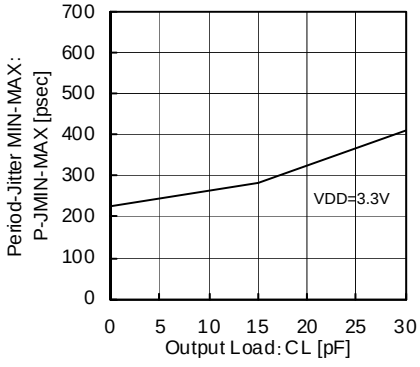


Fig.73 24.576MHz
CL－Period-Jitter MIN-MAX

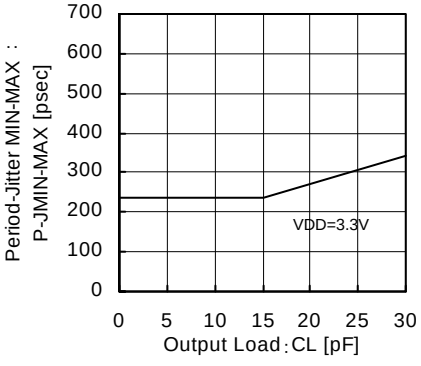


Fig.74 54MHz
CL－Period-Jitter MIN-MAX

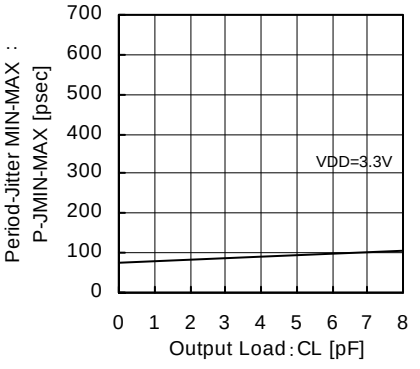


Fig.75 27MHz VCXO
CL－Period-Jitter MIN-MAX

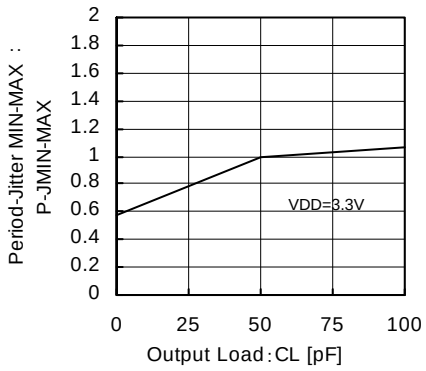


Fig.76 27MHz BUFFER
CL－Period-Jitter MIN-MAX

●Block diagram, Pin assignment

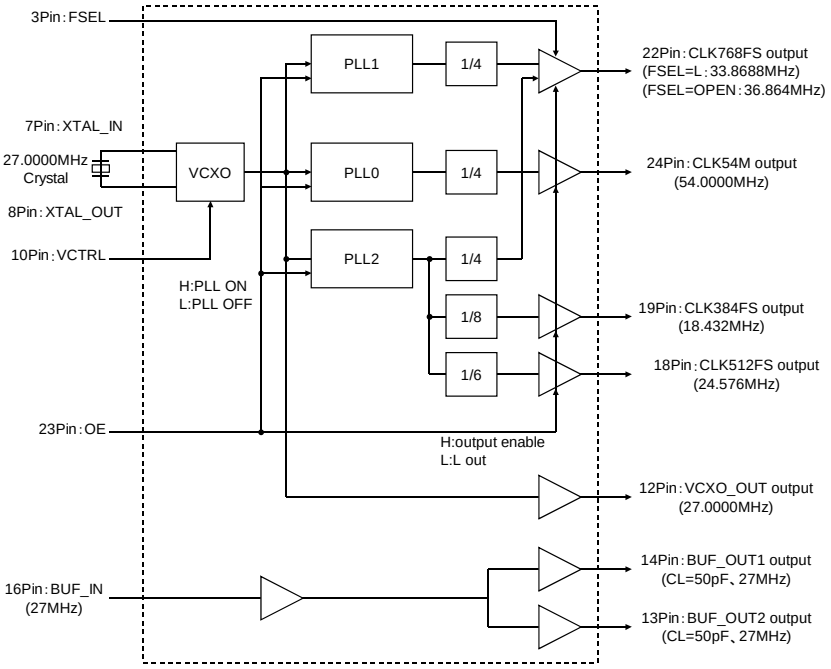


Fig.77 Block diagram

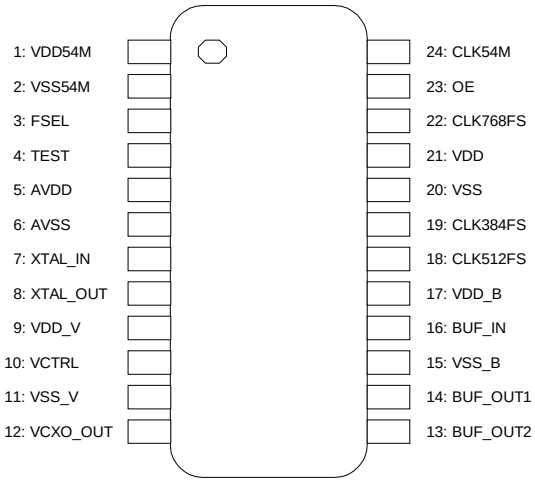


Fig.78 Pin assignment

●Pin function

Pin No.	Pin Name	Function
1	VDD54M	Power supply for CLK54M output
2	VSS54M	GND for CLK54M output
3	FSEL	FS select (CLK768FS selection) (FSEL=L: 44.1 kHz, FSEL=OPEN: 48 kHz, equipped with pull-up resistor)
4	TEST	TEST pin, normally “OPEN”, equipped with pull-down resistor)
5	AVDD	Power supply for PLL Analog
6	AVSS	GND for PLL Analog
7	XTAL_IN	Crystal oscillator input pin
8	XTAL_OUT	Crystal oscillator output pin
9	VDD_V	Power supply for VCXO
10	VCTRL	VCXO control input pin
11	VSS_V	GND for VCXO
12	VCXO_OUT	Monitor pin for VCXO output
13	BUF_OUT2	BUFFER output pin
14	BUF_OUT1	BUFFER output pin
15	VSS_B	GND for BUFFER
16	BUF_IN	BUFFER input pin
17	VDD_B	Power supply for BUFFER
18	CLK512FS	24.576 MHz output
19	CLK384FS	18.432MHz output
20	VSS	GND for PLL Logic
21	VDD	Power supply for PLL Logic
22	CLK768FS	FSEL=L: 33.8688 MHz output, FSEL=OPEN: 36.864 MHz output
23	OE	Output enable pin L: POWER DOWN, OPEN: NORMAL, equipped with pull-up resistor
24	CLK54M	54MHz output

●Audio Clock Functions

1) Output phase relation

The Audio clocks (i.e., CLK768FS, CLK384FS, and CLK512FS) of the BU2365FV are designed so that these clocks will intentionally becomes out of the phase of each output, in order to provide low jitter and noise levels. Thus, overlapped through currents generated at the clock edges can be suppressed to provide low jitter and noise levels.

For the generation of CLK384FS (18.432 MHz), generate two-phase CLK768FS (36.864 MHz) first. The CLK768FS1 and CLK768FS2 will get to the phase relation with one clock out of the PLL2 output (VCO=147.456 MHz). By dividing the frequency in sync with the leading edge of this CLK768FS1, the CLK384FS will fall out of the phase of the CLK768FS2.
Since the frequency of CLK512FS is divided into six portions in sync with the trailing edge of the PLL2 output, the CLK512FS will fall out of the phases of CLK768FS and CLK384FS by half cycle.
As described above, the Audio clocks of the BU2365FV fall out of the phases each other, thus providing low jitter and noise levels.

Furthermore, the true values of phase difference (Delay rate) between CLK384FS and CLK768FS are specified as shown below with consideration given to variations in the measurements on the tests before shipment.

	MIN	TYP	MAX
True value [nsec]	17.0	20.0	23.0

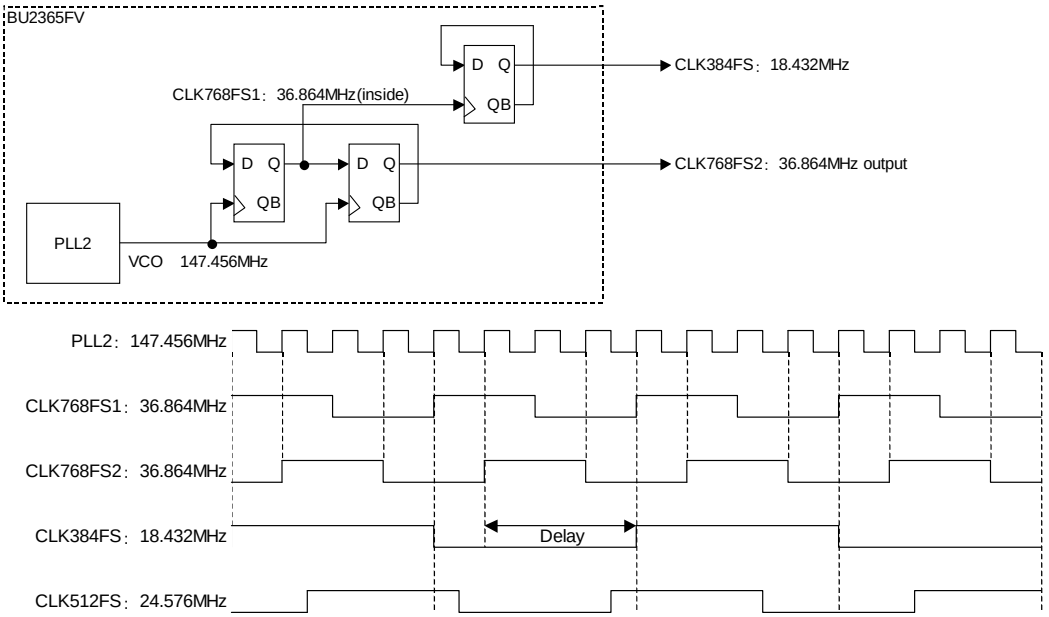


Fig.79 Audio Clock Output Circuit Configuration and Timing Chart

2) Half-pulse clock protection [HPC]

The CLK768FS output is provided with a function used to prevent the occurrence of asynchronous droop of half cycle or less (i.e., half-pulse clock) while in frequency selection under the FSEL pin control.
This function is designed to set the frequency to output L fixed after the elapse of two trailing clocks of output before the selection and to a desired frequency after the elapse of two trailing clocks of output after the selection, when switching the FSEL pin.
Specifically speaking, when the FSEL pin is set to High, the CLK768FS outputs a frequency of 36.864 MHz. With this setting, if the FSEL pin is switched to Low, the CLK768FS will be set to L Fixed after the lapse of two trailing clocks of 36.864 MHz, and then the CLK768FS will output a frequency of 33.8688 MHz after the lapse of two trailing clocks of 33.8688 MHz.

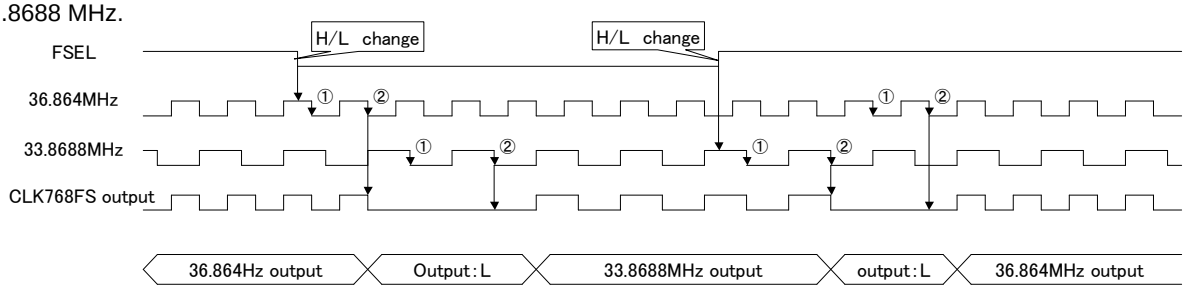


Fig.80 HPC timing chart

●**Package Outline**

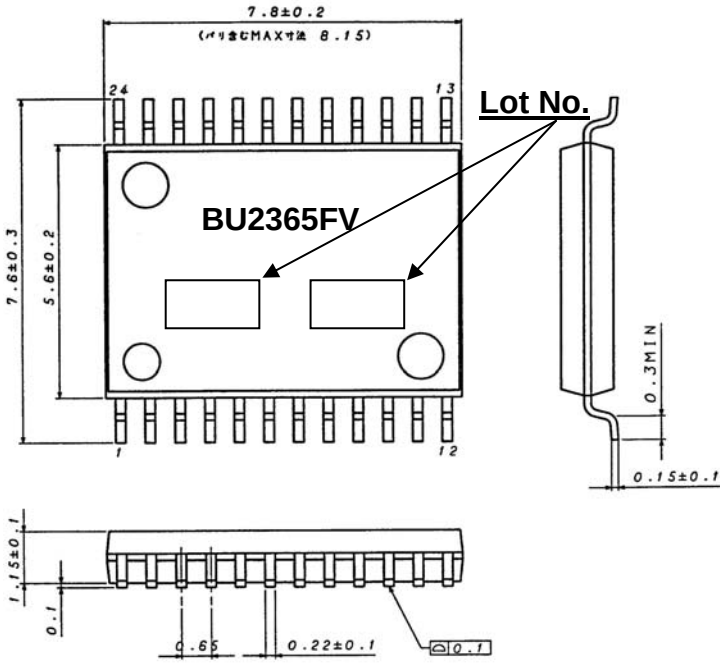
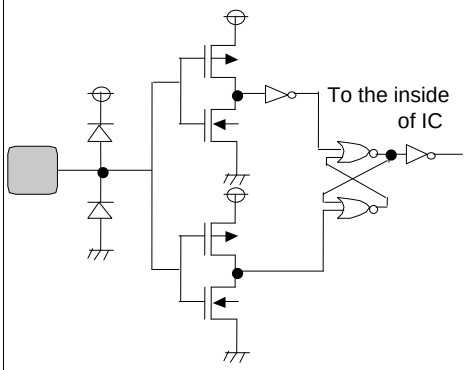
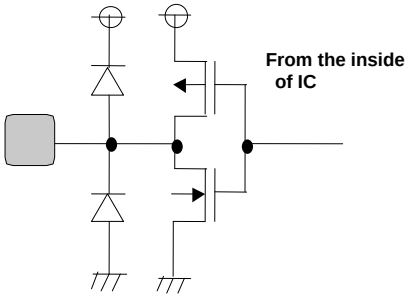
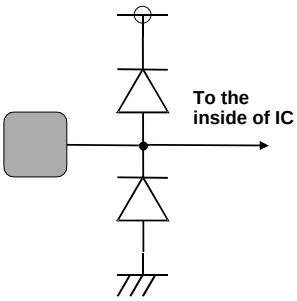
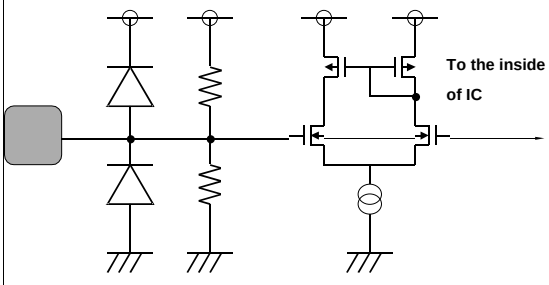
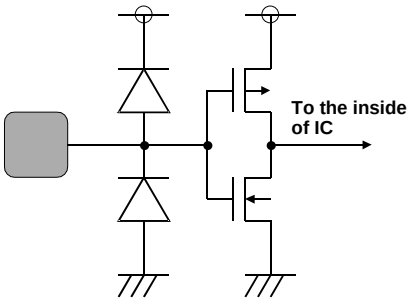
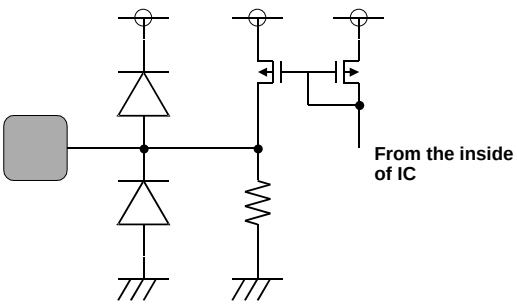


Fig.81 (UNIT:mm)

●**Equivalent circuit**

PIN No.	Equivalent circuit of I/O	PIN No.	Equivalent circuit of I/O
3,23 (With pull-up) 4 (With pull-down)		13,14, 18,19, 22,24	
10		7	
16		8	

●Application Circuit

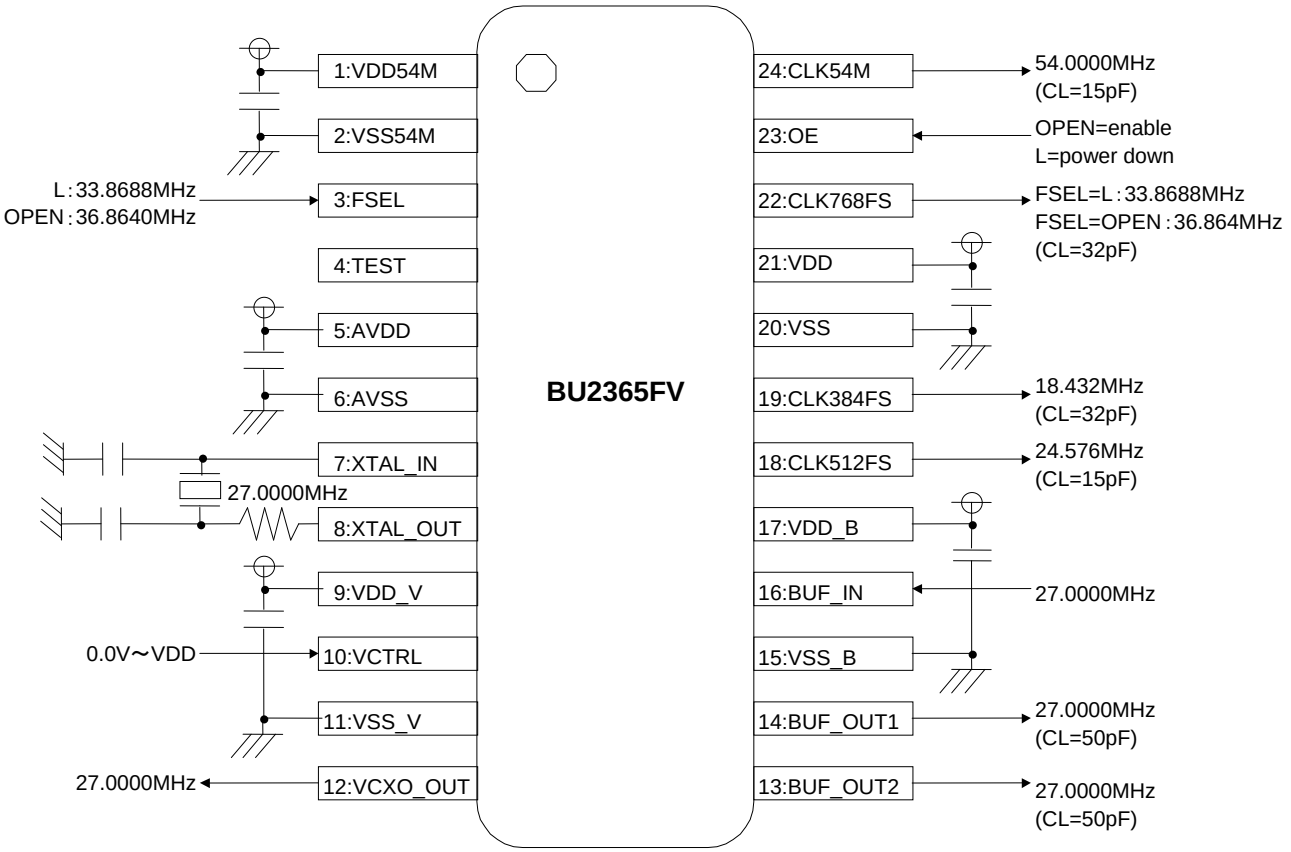


Fig.82

Note)

1) Basically, mount ICs to the substrate for use. If the ICs are not mounted to the substrate, the characteristics of ICs may not be fully demonstrated.
2) Mount 0.1uF capacitors in the vicinity of the IC pins between 1PIN (VDD54M) and 2PIN (VSS54M), 5PIN (AVDD) and 6PIN (AVSS), 9PIN (VDD_V) and 11PIN (VSS_V), 17PIN (VDD_B) and 15PIN (VSS_B), and 21PIN (VDD) and 20PIN (VSS), respectively.
3) For the fine-tuning of frequencies, insert several numbers of pF in the 7PIN and 8PIN to GND.
4) The electrical characteristics have been all evaluated with the use of the crystal oscillator NX5032GA (Spec. No. EXS00A-00278) manufactured by NIHON DEMPA KOGYO CO., LTD., under the conditions of Limiting resistance Rd=30Ω and Load CL=10pF. Consequently, in order to use the BU2365FV, the said crystal oscillator is recommended.
5) As to the jitters, the TYP values vary with the substrate, power supply, output loads, noises, and others. Besides, for the use of the BU2365FV, the operating margin should be thoroughly checked.
6) Depending on the conditions of the substrate, mount an additional electrolytic capacitor between the power supply and GND terminal.
7) For EMI protection, it is effective to put ferrite beads in the origin of power supply to be fed to the BU2365FV from the substrate or to insert a capacitor (of 1Ω or less impedance), which bypasses high frequency desired, between the power supply and the GND terminal.
8) Even though we believe that the example of the application circuit is worth of a recommendation, please be sure to thoroughly recheck the characteristics before use.

●Cautions on use

(1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as applied voltage (VDD or VIN), operating temperature range (Topr), etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Recommended operating conditions
These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector
The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.
In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB
On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern
If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

●Ordering part number

B	U	2	3	6	5	F	V	-	E	2

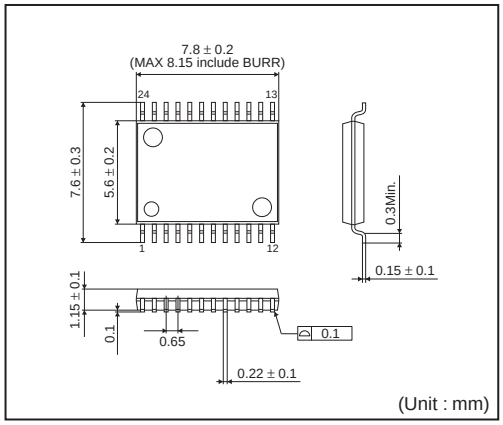
Part No

Part No

Package
FV: SSOP-B24

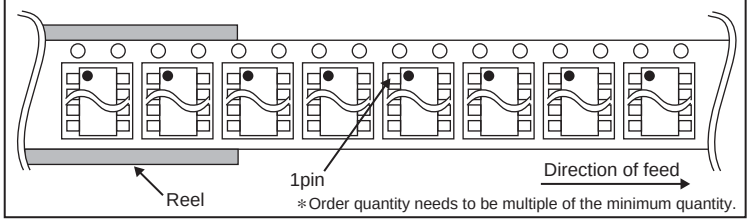
Packaging and forming specification
E2: Embossed tape and ree

SSOP-B24



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



＊Order quantity needs to be multiple of the minimum quantity.

Notes

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