LVDS Interface ICs

35bit LVDS Transmitter 35:5 Serializer

BU8254KVT

No.13057ECT06

●Description

LVDS Interface IC of ROHM "Serializer" "Deserializer" operate from 8MHz to 150MHz wide clock range, and number of bits range is from 35 to 70. Data is transmitted seven times (7X) stream and reduce cable number by 3(1/3) or less. The ROHM's LVDS has low swing mode to be able to expect further low EMI.

●Features

1) 35bits data of parallel LVCMOS level inputs are converted to five channels of LVDS data stream.
2) 30bits of RGB data and 5bits of timing and control data(HSYNC,VSYNC,DE,CNTL1,CNTL2) are transmitted up to 784Mbps effective rate per LVDS channel.
3) Support clock frequency from 8MHz up to 112MHz.
4) Support consumer video format including 480i, 480P, 720P and 1080i as well.
5) Clock edge selectable
6) Power down mode
7) Support spread spectrum clock generator.
8) Support reduced swing LVDS for low EMI.
9) 30bit LVDS receiver is recommended to use BU90R104.

●Applications

Flat Panel Display

●Precaution

■This chip is not designed to protect from radioactivity.
■The chip is made strictly for the specific application or equipment.
Then it is necessary that the unit is measured as need.
■This document may be used as strategic technical data which subjects to COCOM regulations.

●Block Diagram

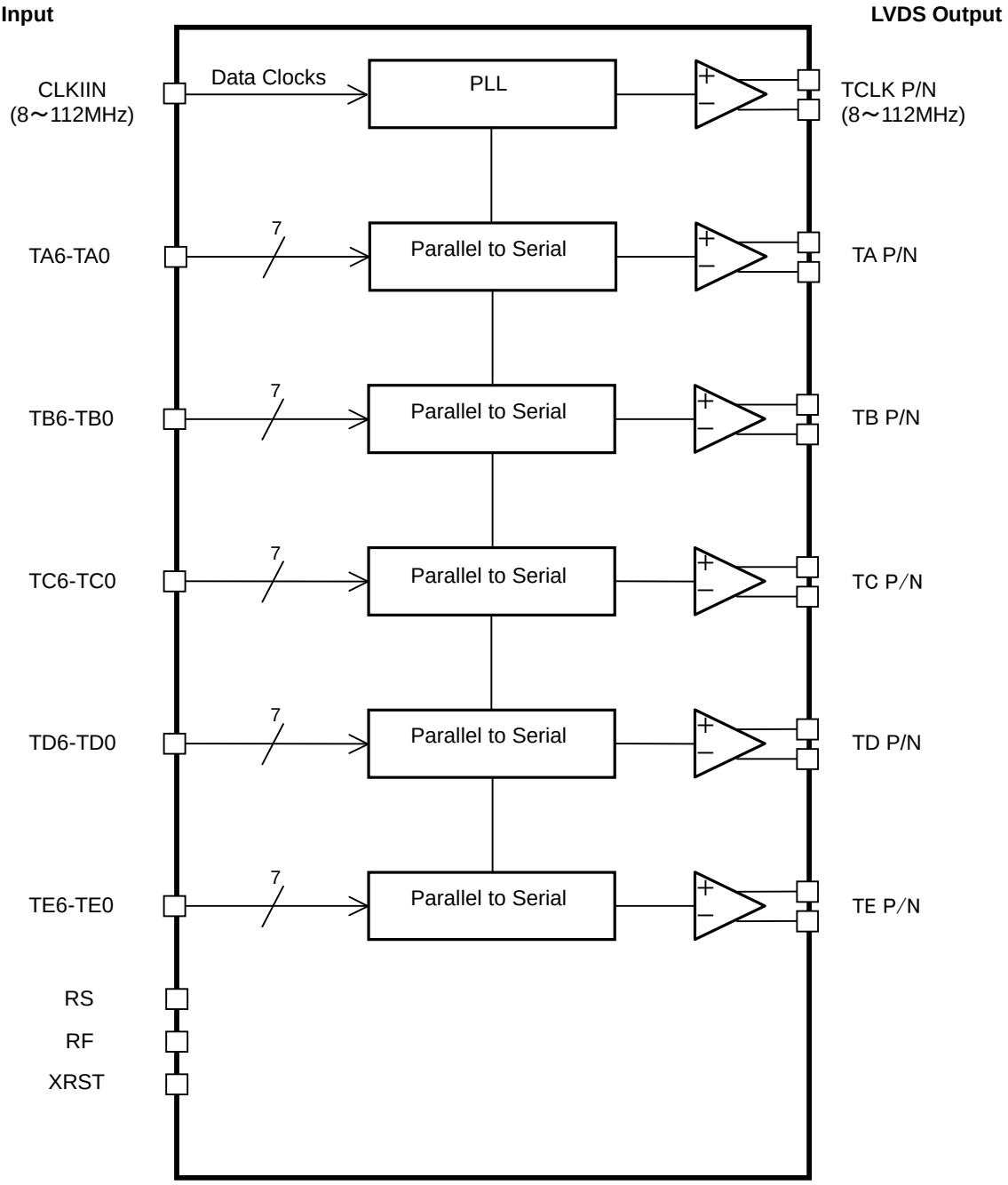


Fig.1 Block Diagram

●**TQFP64V Package Outline and Specification**

TQFP64V

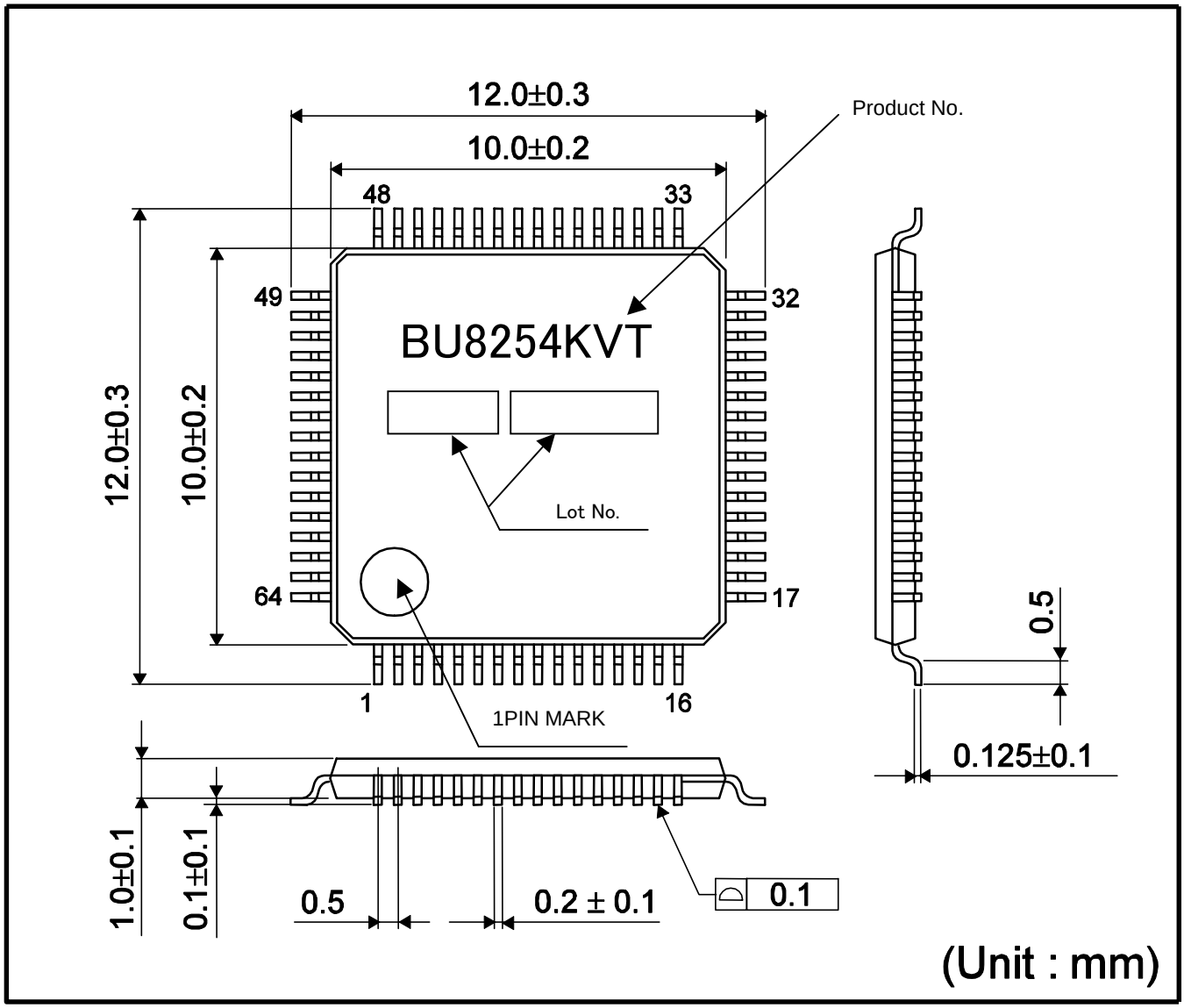


Fig.2 TQFP64V Package Outline and Specification

●Pin configuration

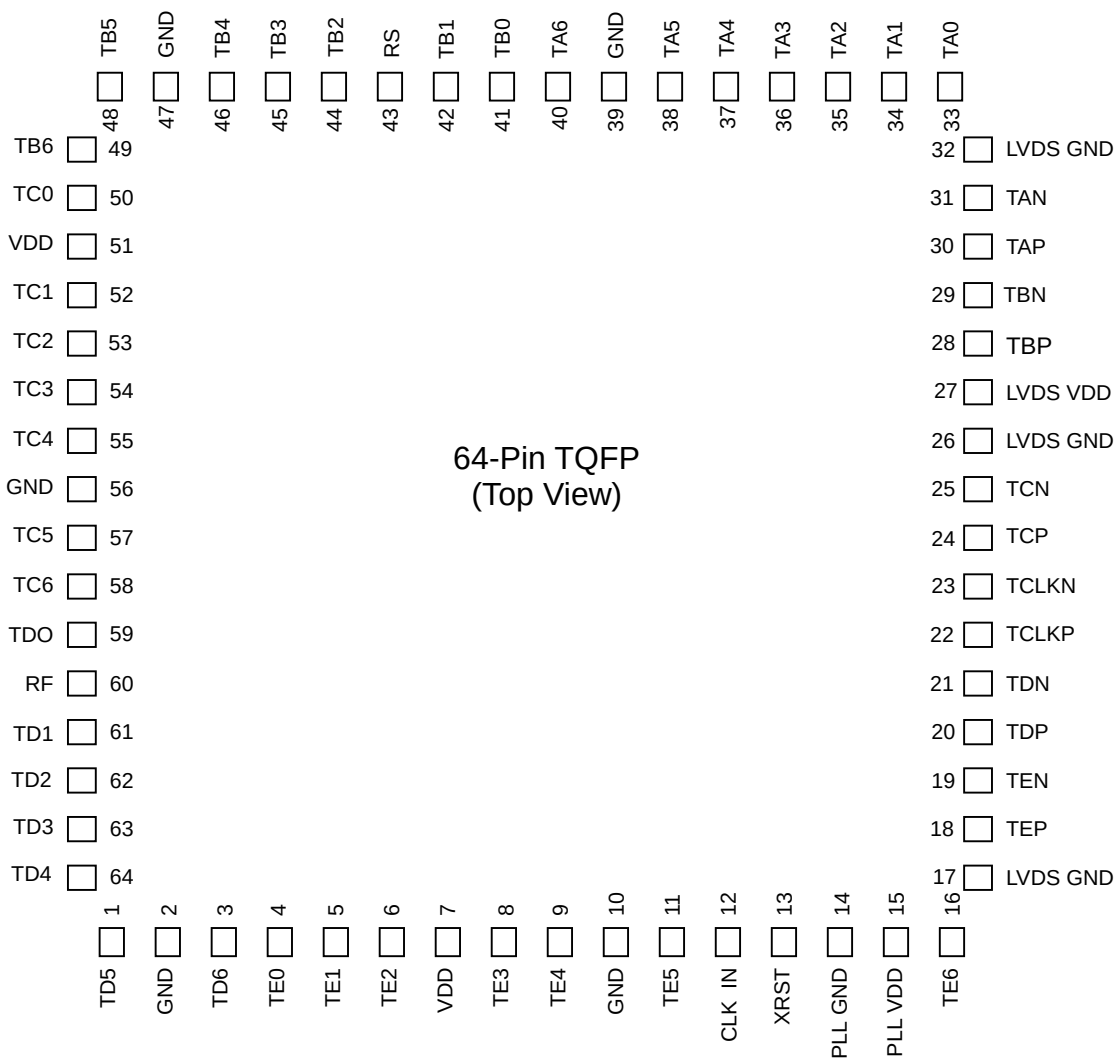


Fig.3 Pin Diagram (Top View)

●Pin Description

Table 1 : Pin Description

<table>
<tr><th>Pin Name</th><th>Pin No.</th><th>Type</th><th>Descriptions</th></tr>
<tr><td>TAP, TAN</td><td>30,31</td><td>LVDS OUT</td><td rowspan="5">LVDS data out.</td></tr>
<tr><td>TBP, TBN</td><td>28,29</td><td>LVDS OUT</td></tr>
<tr><td>TCP, TCN</td><td>24,25</td><td>LVDS OUT</td></tr>
<tr><td>TDP, TDN</td><td>20,21</td><td>LVDS OUT</td></tr>
<tr><td>TEP, TEN</td><td>18,19</td><td>LVDS OUT</td></tr>
<tr><td>TCLKP, TCLKN</td><td>22,23</td><td>LVDS OUT</td><td>LVDS clock out.</td></tr>
<tr><td>TA0～TA6</td><td>33,34,35,36,37,38,40</td><td>IN</td><td rowspan="5">Pixel data inputs.</td></tr>
<tr><td>TB0～TB6</td><td>41,42,44,45,46,48,49</td><td>IN</td></tr>
<tr><td>TC0～TC6</td><td>50,52,53,54,55,57,58</td><td>IN</td></tr>
<tr><td>TD0～TD6</td><td>59,61,62,63,64,1,3</td><td>IN</td></tr>
<tr><td>TE0～TE6</td><td>4,5,6,8,9,11,16</td><td>IN</td></tr>
<tr><td>XRST</td><td>13</td><td>IN</td><td>H : Normal operation,
L : Power down (all outputs are Hi-Z)</td></tr>
<tr><td>RS</td><td>43</td><td>IN</td><td>LVDS swing mode, V_{REF} *1select.
<table>
<tr><th>RS</th><th>LVDS Swing</th><th>Small Swing Input Support</th></tr>
<tr><td>V_{DD}</td><td>350mV</td><td>N/A</td></tr>
<tr><td>0.6～1.4V</td><td>350mV</td><td>RS-V_{REF}</td></tr>
<tr><td>GND</td><td>200mV</td><td>N/A</td></tr>
</table>
*1 V_{REF} is Input Reference Voltage.</td></tr>
<tr><td>RF</td><td>60</td><td>IN</td><td>Input clock triggering edge select.
H : Rising edge, L : Falling edge.</td></tr>
<tr><td>VDD</td><td>51,7</td><td>Power</td><td>Power supply pins for LVCMOS inputs and digital core.</td></tr>
<tr><td>CLKIN</td><td>12</td><td>IN</td><td>Clock input.</td></tr>
<tr><td>GND</td><td>2,10,39,47,56</td><td>Ground</td><td>Ground pins for LVCMOS inputs and digital core.</td></tr>
<tr><td>LVDS VDD</td><td>27</td><td>Power</td><td>Power supply pins for LVDS outputs.</td></tr>
<tr><td>LVDS GND</td><td>17,26,32</td><td>Ground</td><td>Ground pins for LVDS outputs.</td></tr>
<tr><td>PLLVDD</td><td>15</td><td>Power</td><td>Power supply pin for PLL core.</td></tr>
<tr><td>PLLGND</td><td>14</td><td>Ground</td><td>Ground pins for PLL core.</td></tr>
</table>

●Electrical characteristics

■Rating

Table 2 : Absolute Maximum Ratings

Parameter	Symbol	Ratings		Units
		Min	Max	
Supply Voltage	V_{DD}	-0.3	4.0	V
Input Voltage	V_{IN}	-0.3	V_{DD}+0.3	V
Output Voltage	V_{OUT}	-0.3	V_{DD}+0.3	V
Storage Temperature Range	Tstg	-55	125	℃

Table 3 : Package Power

PACKAGE	Power Dissipation (mW)	De-rating (mW/℃) *1
TQFP64V	700	7.0
	1000*2	10.0*2

*1: At temperature Ta >25℃
*2: Package power when mounting on the PCB board.
The size of PCB board :70 × 70 × 1.6(mm^3)
The material of PCB board :The FR4 glass epoxy board.(3% or less copper foil area)
(It is recommended to apply the above package power requirement to PCB board when the small swing input mode is used)

Table 4 : Recommended Operating Conditions

Parameter	Symbol	Ratings			Units	Conditions
		Min	Typ	Max		
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	VDD,LVDSVDD,PLLVDD
Operating Temperature Range	Topr	-40	-	85	℃	Clock frequency from 8MHz up to 90MHz
		0	-	70	℃	Cock frequency from 90MHz up to 112MHz

■DC characteristics

Table 5 : LVCMOS DC Specifications (VDD=3.0V～3.6V, Ta=-40℃～85℃)

Parameter	Symbol	Rating			Units	Conditions
		Min	Typ	Max		
High Level Input Voltage	V_{IH}	$V_{DD}\times0.8$	-	V_{DD}	V	exclude RS pin
Low Level Input Voltage	V_{IL}	GND	-	$V_{DD}\times0.2$	V	
High Level Input Voltage	V_{IHRS}	$V_{DD}\times0.8$	-	V_{DD}		RS pin
Low Level Input Voltage	V_{ILRS}	GND	-	0.2		
Small Swing Voltage	V_{DDQ} *1	1.2	-	2.8	V	
Input Reference Voltage	V_{REF}	-	$V_{DDQ}/2$	-	-	Small Swing(RS=V_{DDQ}/2)
Small Swing High Level Input Voltage	V_{SH} *2	$V_{DDQ}/2$ +200mV	-	-	V	$V_{REF}=V_{DDQ}/2$
Small Swing Low Level Input Voltage	V_{SL} *2	-	-	$V_{DDQ}/2$ -200mV	V	$V_{REF}=V_{DDQ}/2$
Input Current	I_{INC}	-	-	±10	μA	$0V \leq V_{IN} \leq V_{DD}$

*1: V_{DDQ} voltage defines max voltage of small swing input. It is not an actual input voltage.
*2: Small swing signal is applied to TA[6:0], TB[6:0], TC[6:0], TD[6:0] TE[6:0], CLKIN.

Table 6 : LVDS Transmitter DC Specifications(VDD=3.0V～3.6V, Ta=-40℃～85℃)

Parameter	Symbol	Rating			Units	Conditions	
		Min	Typ	Min			
Differential Output Voltage	V_{OD}	250	350	450	mV	RL=100Ω	Normal swing RS=V_{DD}
		100	200	300	mV		Reduced swing RS=GND
Change in VOD between complementary output states	ΔV_{OD}	-	-	35	mV	RL=100Ω	
Common Mode Voltage	V_{OC}	1.125	1.25	1.375	V		
Change in VOC between complementary output states	ΔV_{OC}	-	-	35	mV		
Output Short Circuit Current	I_{OS}	-	-	-24	mA	V_{OUT}=0V, RL=100Ω	
Output TRI-STATE Current	I_{OZ}	-	-	±10	μA	XRST=0V, V_{OUT}=0V to V_{DD}	

■**Supply Current**

Table 7 : Supply Current

Parameter	Symbol	Rating			Units	Conditions	
		Min	Typ	Max			
Transmitter Supply Current	I_{TCCG}	-	57	-	mA	RL=100Ω,CL=5pF V_{DD}=3.3V,RS=V_{DD} Gray Scale Pattern	f=85MHz
		-	42	-	mA	RL=100Ω,CL=5pF V_{DD}=3.3V,RS=GND Gray Scale Pattern	f=85MHz
Transmitter Supply Current	I_{TCCW}	-	62	-	mA	RL=100Ω,CL=5pF V_{DD}=3.3V,RS=V_{DD} Worst Case pattern	f=85MHz
		-	45	-	mA	RL=100Ω,CL=5pF V_{DD}=3.3V,RS=GND Worst Case pattern	f=85MHz
Transmitter Power Down Supply Current	I_{TCCS}	-	-	10	μA	XRST=L	

Gray Scale Pattern

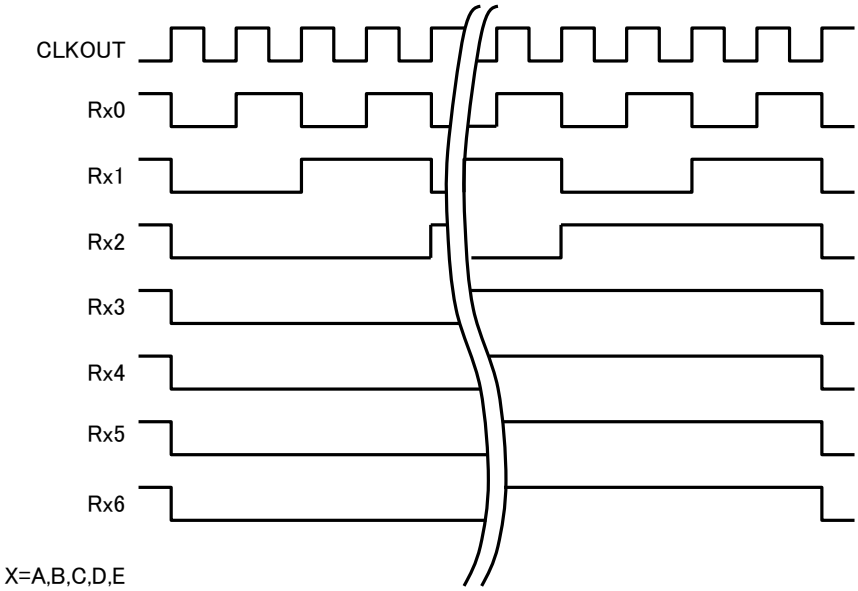


Fig.4 Gray scale pattern

Worst Case Pattern (Maximum Power condition)

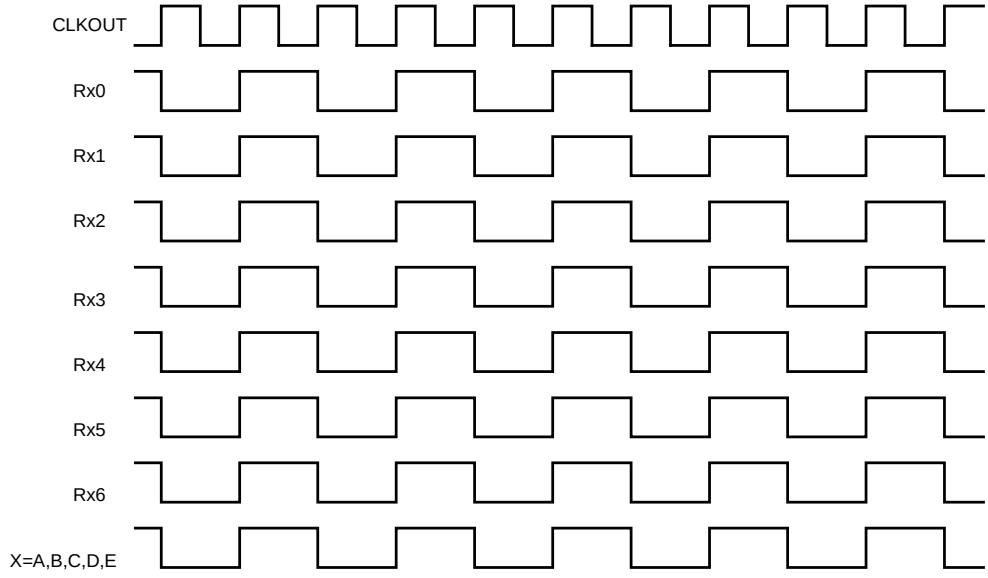


Fig.5 Worst Case Pattern

■AC characteristics

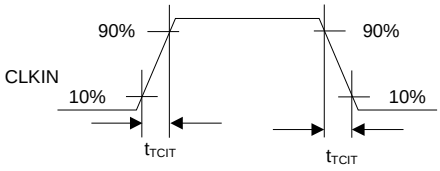
Table 8 : Switching Characteristics

Parameter	Symbol	Min	Typ	Max	Units
CLK IN Transition time	t_{TCIT}	-	-	5.0	ns
CLK IN Period	t_{TCP}	8.93	-	125.0	ns
CLK IN High Time	t_{TCH}	$0.35t_{TCP}$	$0.5t_{TCP}$	$0.65t_{TCP}$	ns
CLK IN Low Time	t_{TCL}	$0.35t_{TCP}$	$0.5t_{TCP}$	$0.65t_{TCP}$	ns
CLK IN to TCLK+/-Delay	t_{TCD}	-	t_{TCP}	-	ns
LVSMOS Data Set up to CLK IN	t_{TS}	2.5	-	-	ns
LVCMOS Data Hold from CLK IN	t_{TH}	0	-	-	ns
LVDS Transition Time	t_{LVT}	-	0.6	1.5	ns
Output Data Position 0	t_{TOP1}	-0.2	0.0	+0.2	ns
Output Data Position 1	t_{TOP0}	$\frac{t_{TCP}}{7}$ -0.2	$\frac{t_{TCP}}{7}$	$\frac{t_{TCP}}{7}$ +0.2	ns
Output Data Position 2	t_{TOP6}	$2\frac{t_{TCP}}{7}$ -0.2	$2\frac{t_{TCP}}{7}$	$2\frac{t_{TCP}}{7}$ +0.2	ns
Output Data Position 3	t_{TOP5}	$3\frac{t_{TCP}}{7}$ -0.2	$3\frac{t_{TCP}}{7}$	$3\frac{t_{TCP}}{7}$ +0.2	ns
Output Data Position 4	t_{TOP4}	$4\frac{t_{TCP}}{7}$ -0.2	$4\frac{t_{TCP}}{7}$	$4\frac{t_{TCP}}{7}$ +0.2	ns
Output Data Position 5	t_{TOP3}	$5\frac{t_{TCP}}{7}$ -0.2	$5\frac{t_{TCP}}{7}$	$5\frac{t_{TCP}}{7}$ +0.2	ns
Output Data Position 6	t_{TOP2}	$6\frac{t_{TCP}}{7}$ -0.2	$6\frac{t_{TCP}}{7}$	$6\frac{t_{TCP}}{7}$ +0.2	ns
Phase Locked Loop Set Time	t_{TPLL}	-	-	10.0	ms

●AC Timing

■AC Timing Diagrams

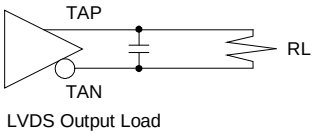
LVCMOS Input



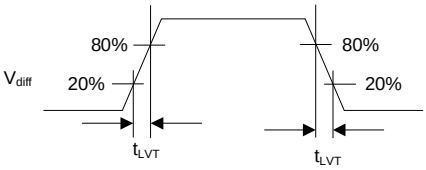
LVCMOS Output

LVDS Output

V_{diff}=(TAP)-(TAN)



LVDS Output Load



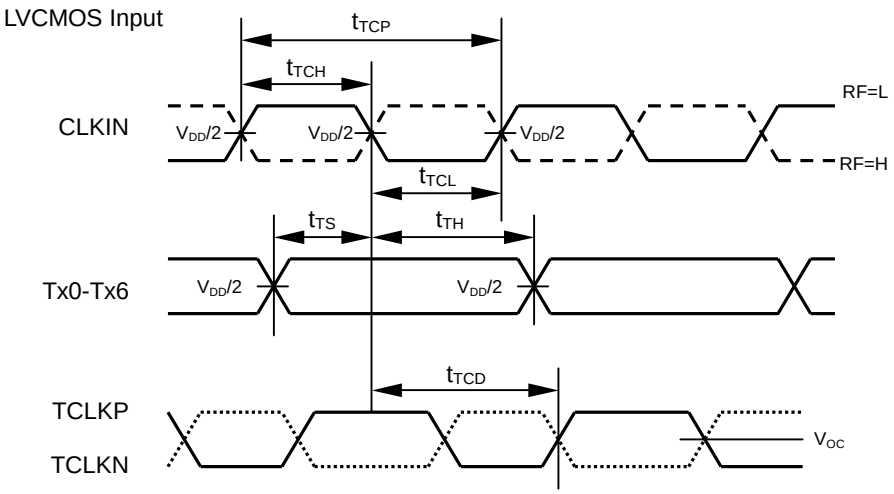


Fig.6 AC Timing Diagrams

■**Small Swing Inputs**

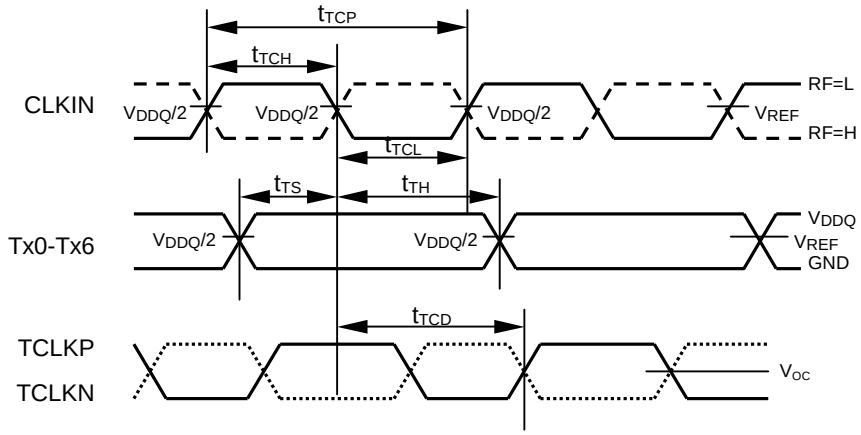


Fig.7 Small Swing Inputs

■**AC Timing Diagrams**

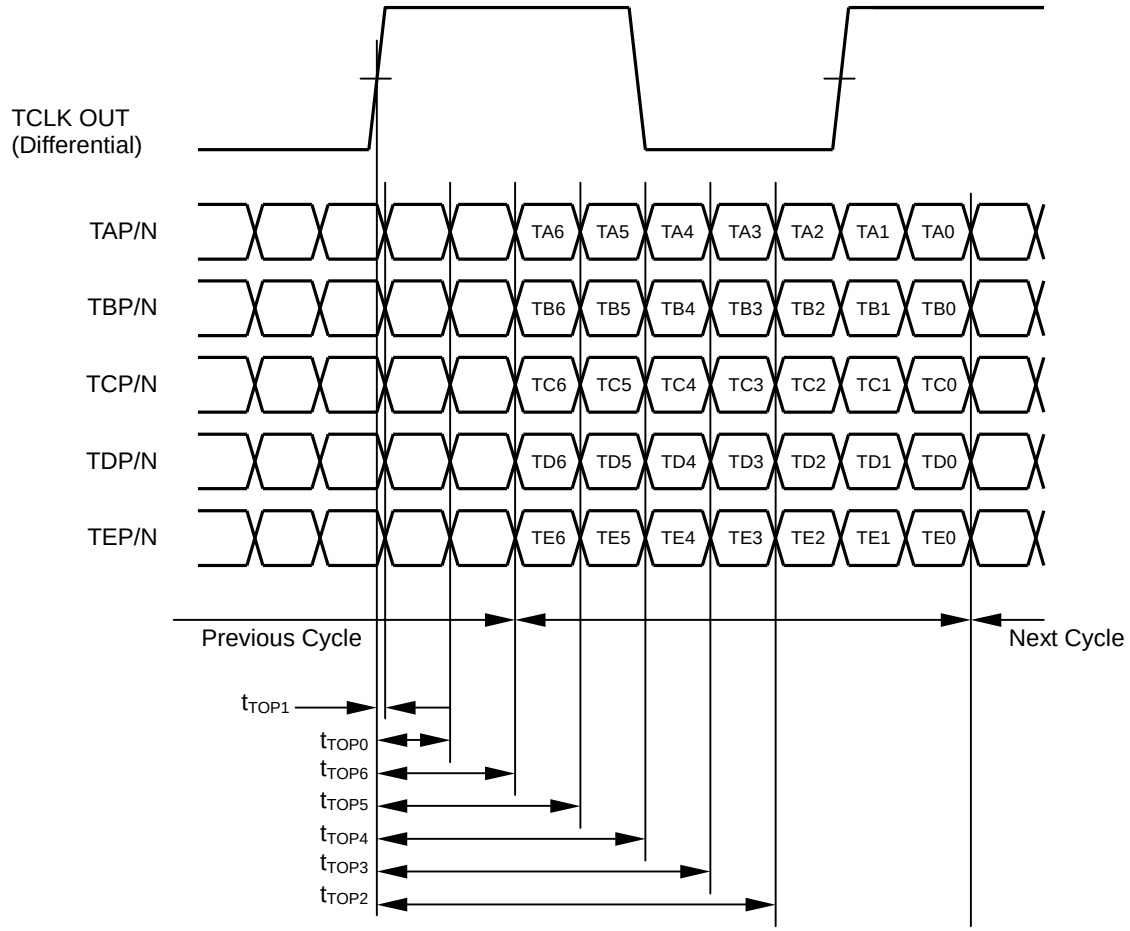


Fig.8 AC Timing Diagrams

■**Phase Locked Loop Set Time**

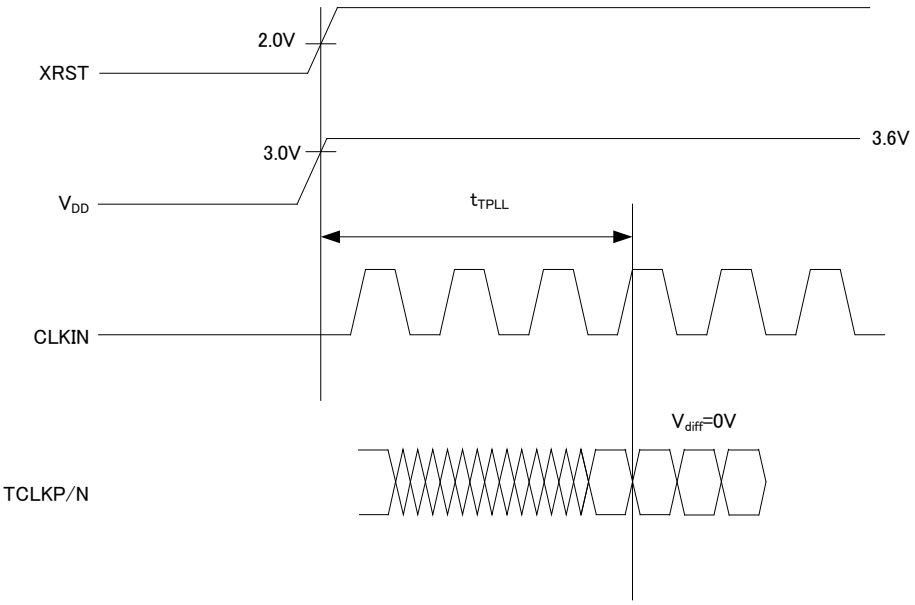


Fig.9 Phase Locked Loop Set Time

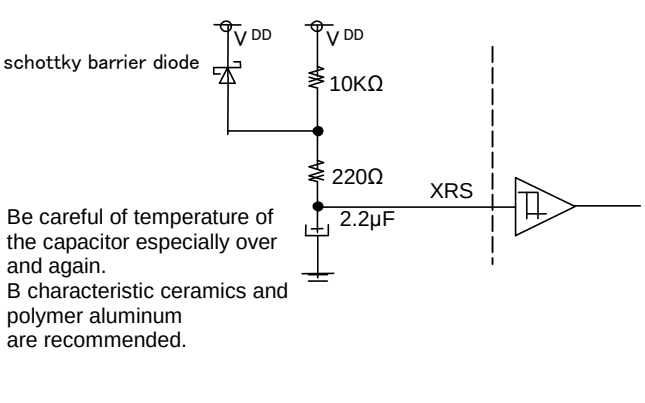
●System Timing Requirement

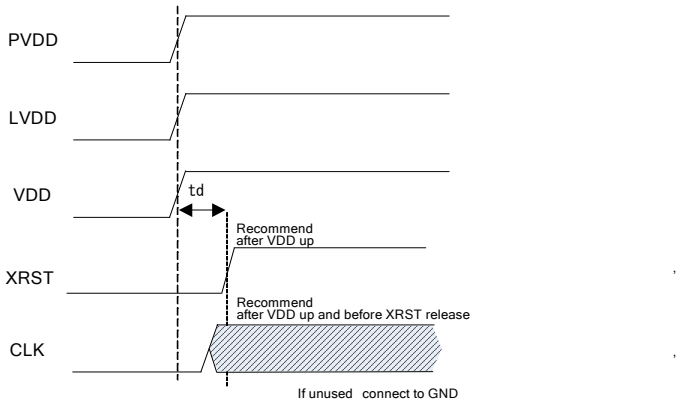
System Timing Requirement is mandatory by following two methods.

①The method of using CR circuit.(In the case that CLK does not stop after power supply)
②The method of using external specific IC. (In the case that CLK turns on/off after power supply)

It is recommend to do enough examination for target application.

①The method of using CR circuit.(In the case that CLK does not stop after power supply)

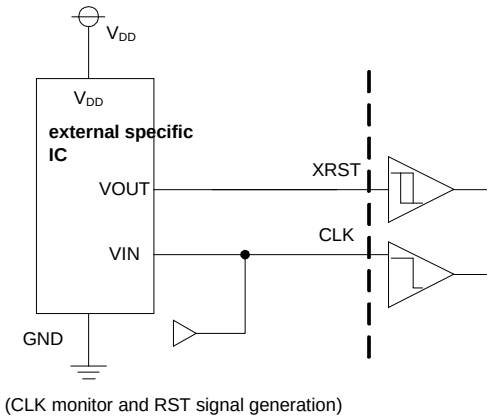




td is approximately equal to 20ms when the left RC coleus are applied.

Fig.10 The method of using CR circuit.

② The method of using external specific IC. (In the case that CLK turns on/off after power supply)



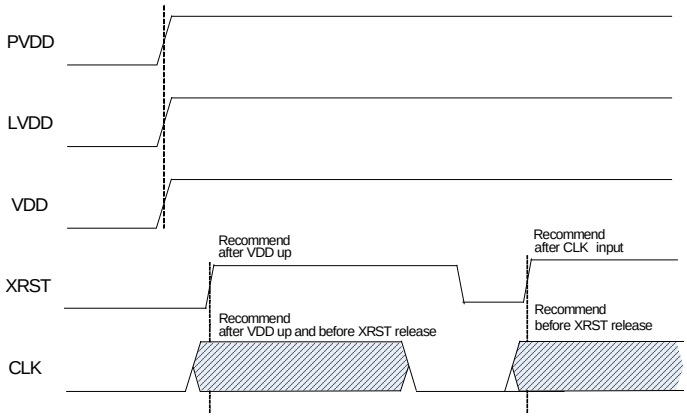
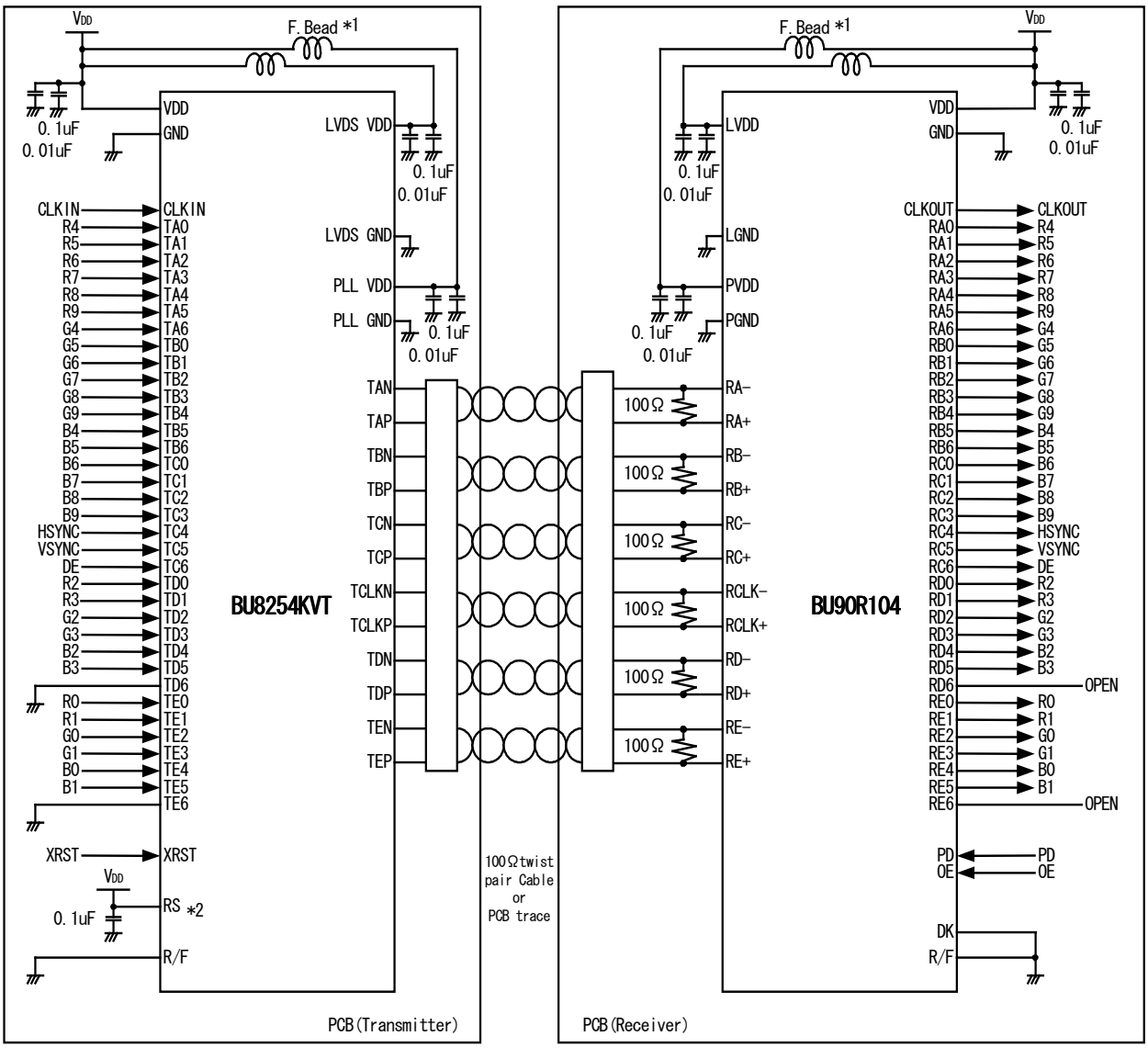


Fig.11 The method of using external specific IC.

●10bit LVCMOS Level Input

Example:
BU8254KVT: LVCMOS level input/Falling edge/Normal swing
BU90R104: Falling edge

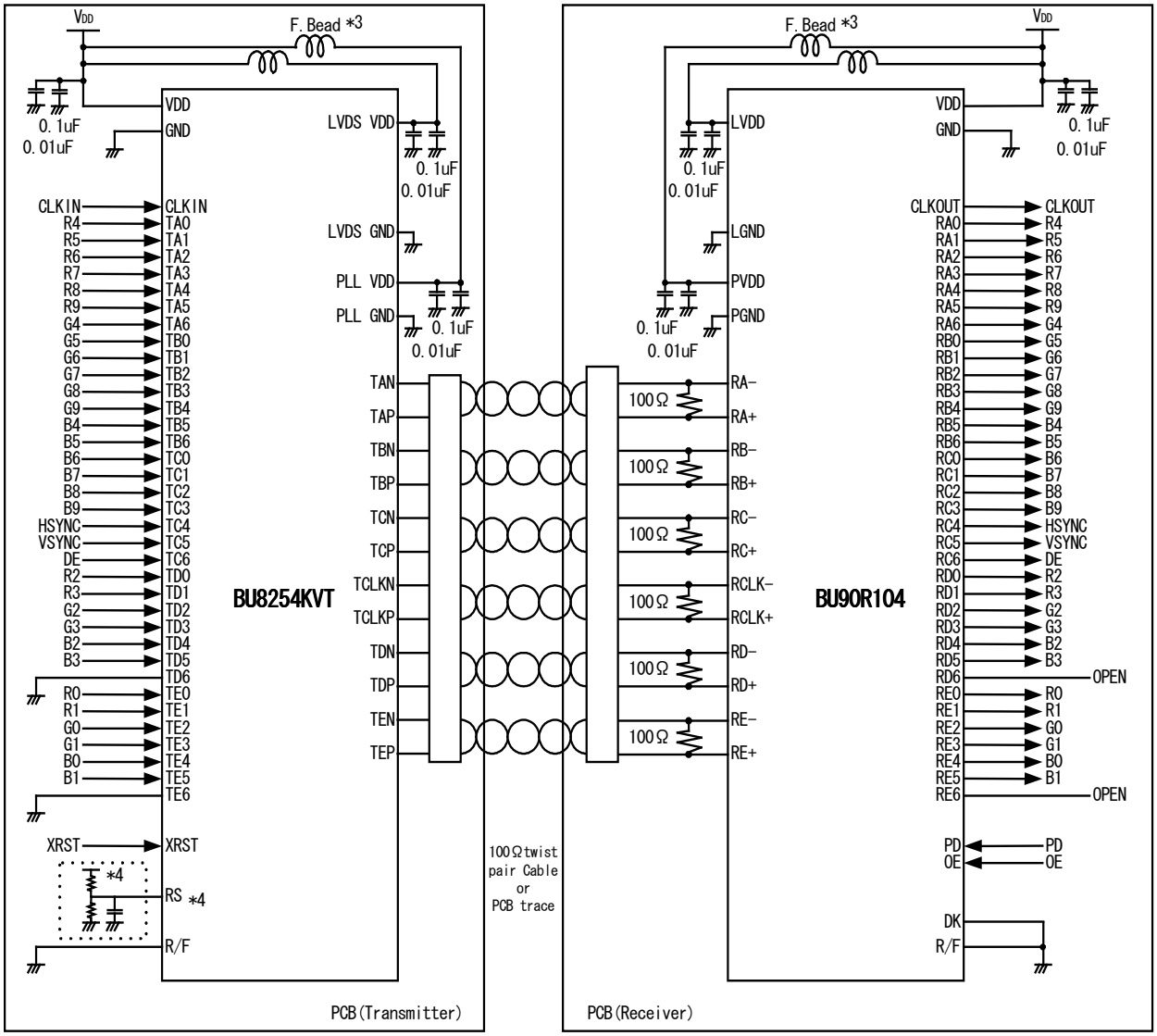


*1 : Recommended Parts:
F.Bead : BLM18A-Series (Murata Manufacturing)

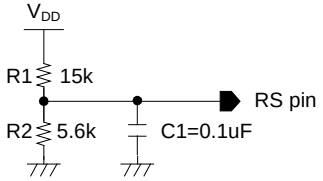
*2 If RS pin is tied to VDD, LVDS swing is 350m V.
If RS pin is tied to GND, LVDS swing is 200m V.

●10bit Small Swing Input

Example:
BU8254KVT : LVCMOS level input/Falling edge/Normal swing
BU90R104: Falling edge



*3 : Recommended Parts:
F.Bead : BLM18A-Series (Murata Manufacturing)
*4 : RS pin acts as VREF input pin when input voltage is set to half of high level signal input.
We recommend to locate by-pass condenser near the RS pin.

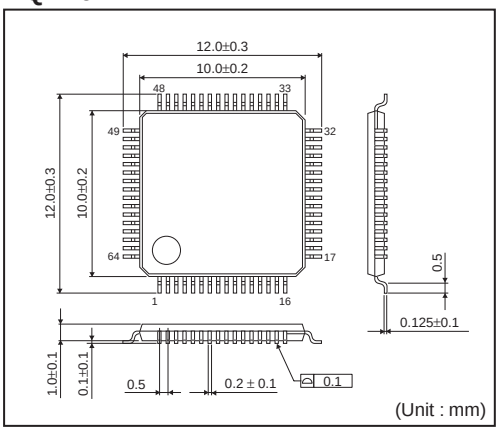


Example for LVCMOS(1.8V input)(R1,R2)=(1.5kΩ,5.6kΩ)

●Ordering Part Number

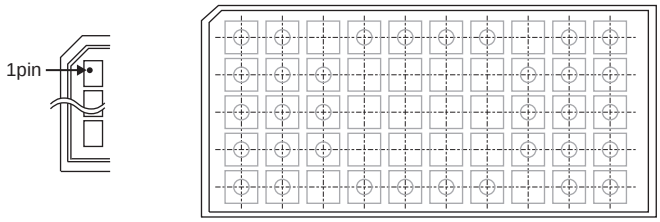
B	U	8	2	5	4	K	V	T		
Part No.		Part No.				Package KVT: TQFP64V			Packaging and forming specification None:Tray	

TQFP64V



<Tape and Reel information>

Container	Tray (with dry pack)
Quantity	1000pcs
Direction of feed	Direction of product is fixed in a tray



∗Order quantity needs to be multiple of the minimum quantity.

Notes

1) The information contained herein is subject to change without notice.

2) Before you use our Products, please contact our sales representative and verify the latest specifications :

3) Although ROHM is continuously working to improve product reliability and quality, semiconductors can break down and malfunction due to various factors.
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4) Examples of application circuits, circuit constants and any other information contained herein are provided only to illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.

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7) The Products specified in this document are not designed to be radiation tolerant.

8) For use of our Products in applications requiring a high degree of reliability (as exemplified below), please contact and consult with a ROHM representative : transportation equipment (i.e. cars, ships, trains), primary communication equipment, traffic lights, fire/crime prevention, safety equipment, medical systems, servers, solar cells, and power transmission systems.

9) Do not use our Products in applications requiring extremely high reliability, such as aerospace equipment, nuclear power control systems, and submarine repeaters.

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ROHM SEMICONDUCTOR

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