ROHM
SEMICONDUCTOR

Technical Note

Digital Sound Processors for FPD TVs

32bit Audio DSP

BU9409FV

No.12083EAT03

●General Description

It is a digital audio sound processor used for thin TV. Digital signal processor is Rohm original DSP only for TV sound signal processing, and it's cost performance is excellent. Digital inputs are two lines. Output is digital output corresponding to 2.1ch or play of sub-voice L/R signal.

●Features

■DSP Part

Data width: 32bit (Data RAM)
Quickest machine cycle:40.7ns (512fs,fs=48kHz)
Multiplier: 32 x 24 → 56bit
Adder: 32 + 32 → 32bit
Data RAM: 256 x 32bit
Coefficient RAM: 128 x 24bit
Sampling frequency: fs=48kHz
Master clock: 512fs
（24.576MHz,fs=48kHz）

■Input output I/F

2 stereo digital signal input port : 16/20/24bit (I2S,left-align,right-align)
2 stereo digital signal output port : 16/20/24bit (I2S,left-align,right-align), S/PDIF output

■Sound signal processing function for TV

Prescaler, DC cut HPF, channel mixer, P^{2}Volume(Perfect Pure Volume),BASS,MIDDLE, TREBLE, pseudo stereo, surround, P^{2}Bass, P^{2}Treble, 7 band parametric equalizer, master volume, L/R balance, postscaler, output clipper, subwoofer output processing （P^{2}Volume, P^{2}Bass, P^{2}Treble are Rohm original sound effect functions.）

●Applications

Flat Panel TVs (LCD, Plasma)

●Absolute maximum rating（Ta=25°C）

Item	Symbol	Rating	Unit
Power-supply voltage	V_{DD}	4.5	V
Allowable dissipation	P_d	700 (*1)	mW
operating temperature range	T_{opr}	-25～+85	°C
Storage temperature range	T_{stg}	-55～+125	°C

*1 7mW is decreased for 1°C when using it with Ta=25°C or more.
Operation can't be guaranteed.

●Operating condition（Ta=-25～+85°C）

Item	Symbol	Rating	Unit
Power-supply voltage	V_{DD}	3.0～3.6	V

* 1 It isn't Radiation-proof designed for the product.

●Electrical Characteristics(Digital serial)

V_{DD}=3.3V unless specified, Ta=25°C

Item		Symbol	Rating value			Unit	Terms	Adaptive terminal
			Min.	Standard	Max.			
Hysteresis Input voltage	H Level voltage	V_{IH}	2.5	-	-	V		*1,2,3
	L Level voltage	V_{IL}	-	-	0.8	V		*1,2,3
Input current		I_I	-1	-	+1	μA	V_{IN}=0～3.3V	*1
Pull-up resistor input L current		I_{IL}	-150	-100	-50	μA	V_{IN}=0V	*2
Pull-down resistor input H current		I_{IH}	35	70	105	μA	V_{IN}=3.3V	*3
Output voltage	H Level voltage	V_{OH}	2.75	-	-	V	I_O=-0.6mA	*4
	L Level voltage	V_{OL}	-	-	0.55	V	I_O=0.6mA	*4
SDA terminal Output voltage	L Level voltage	V_{OL}	-	-	0.4	V	I_O=3mA	*5

Adaptive terminal

*1 CMOS hysteresis input terminal
SCLI(8pin), SDAI(9pin), MODE(20pin)

*2 Pull-up resistor built-in CMOS hysteresis input terminal
LRCKI(2pin), SDATA1(3pin), SDATA2(4pin), MCLK(39pin), BCKI(40pin)

*3 Pull-down resistor built-in CMOS hysteresis input terminal
RESETX(5pin), MUTEX_SP(6pin), MUTEX_DAC(7pin), ADDR(21pin)

*4 CMOS output terminal
SPDIFO(22pin), SDAO(28pin), SCLO(29pin), MUTEX_DACO(30pin), MUTEX_SPO(31pin),
RESETXO(32pin), DATAO2(33pin), DATAO1(34pin), LRCKO(35pin), BCKO(36pin), SYSCKO(37pin)

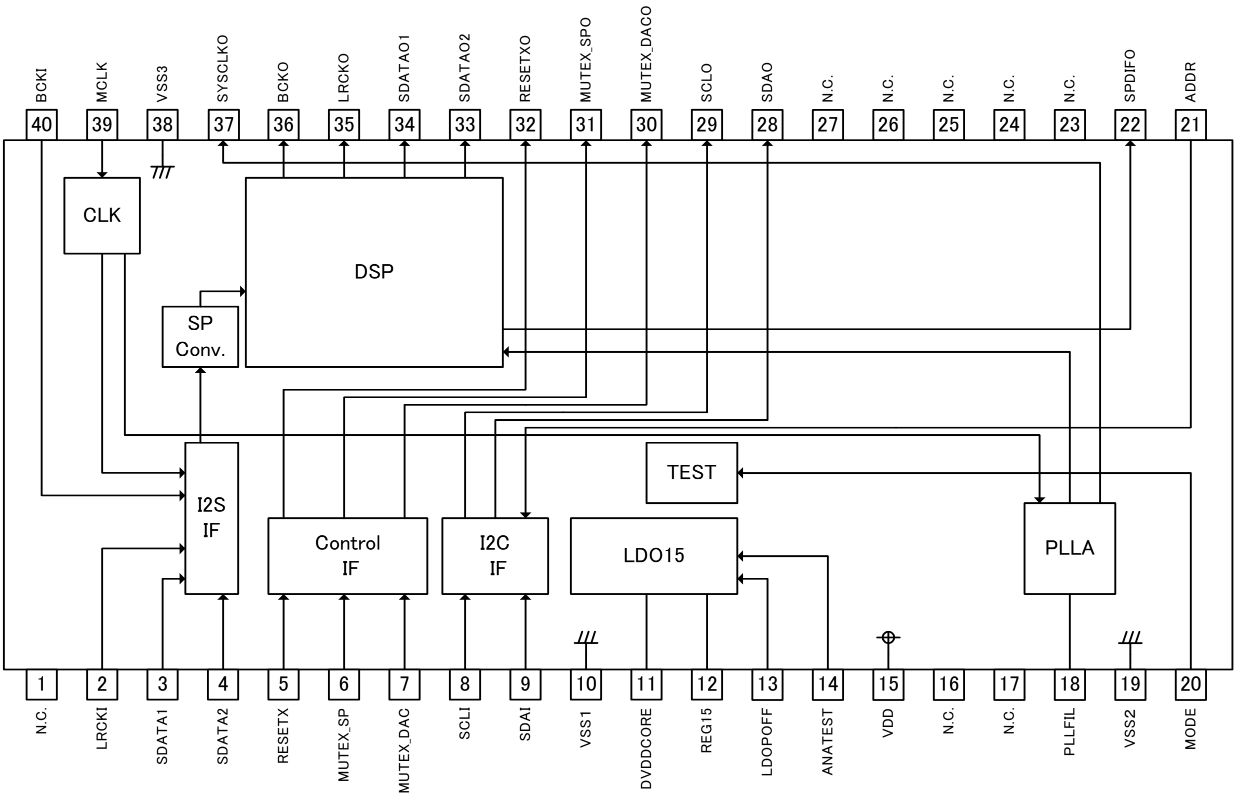
*5 Open drain output terminal
SDAI(9pin)

Electric characteristic(Analogue serial)

V_{DD}=3.3V Unless specified, Ta=25°C,R_L=10kΩ, V_C standard

Item	Symbol	Rating Value			Unit	Object pin/Condition
		Min	Standard	Max		
whole						
Circuit current	I_Q	-	15	30	mA	VDD
Regulator part						
Output voltage	V_{REG}	1.3	1.5	1.7	V	I_O=100mA
PLL part						
Lock frequency	F_{LK8}	-	24.576	-	MHz	256fs(fs=48kHz) input

●Block diagram


BCKI 40
MCLK 39
VSS3 38
SYSCLKO 37
BCKO 36
LRCKO 35
SDATAO1 34
SDATAO2 33
RESETXO 32
MUTEX_SPO 31
MUTEX_DACO 30
SCLO 29
SDAO 28
N.C. 27
N.C. 26
N.C. 25
N.C. 24
N.C. 23
SPDIFO 22
ADDR 21
CLK
DSP
SP Conv.
I2S IF
Control IF
I2C IF
TEST
LDO15
PLLA
1 N.C.
2 LRCKI
3 SDATA1
4 SDATA2
5 RESETX
6 MUTEX_SP
7 MUTEX_DAC
8 SCLI
9 SDAI
10 VSS1
11 DVDDCORE
12 REG15
13 LDOPOFF
14 ANATEST
15 VDD
16 N.C.
17 N.C.
18 PLLFIL
19 VSS2
20 MODE

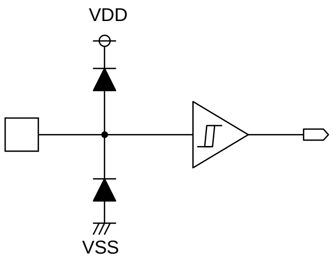
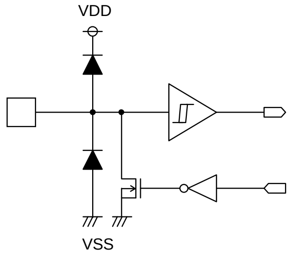
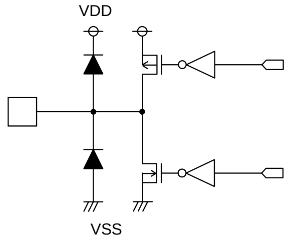
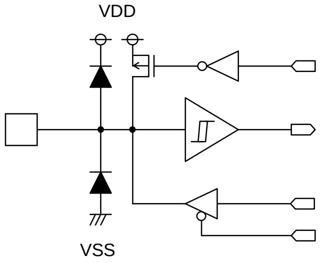
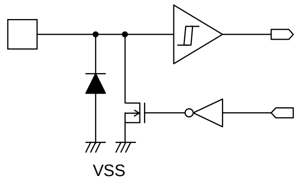
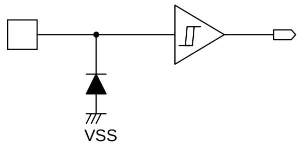
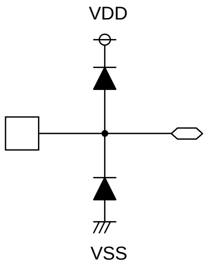
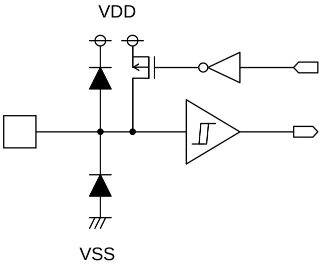
●Pin Description(s)

No.	Name	Description of terminals	Type
1	N.C	(*2)	-
2	LRCKI	I^2S Audio LR signal input	D
3	SDATA1	I^2S Audio data input 1	D
4	SDATA2	I^2S Audio data input 2	D
5	RESETX	Reset status with “L”	B
6	MUTEX_SP	DAC mute signal input(*1)	B
7	MUTEX_DAC	SP mute signal input(*1)	B
8	SCLI	I^2C Forwarding clock input	F
9	SDAI	I^2C Data input output	E
10	VSS1	Digital I/O GND	-
11	DVDDCORE	Connect to REG15 terminal	-
12	REG15	Built-in regulator voltage output	G
13	LDOPOFF	Built-in regulator POFF signal input	G
14	ANATEST	Analog test monitor terminal	G
15	VDD	Digital I/O power supply	-
16	N.C		-
17	N.C		-
18	PLLFIL	Filter connection terminal for PLL	G
19	VSS2	Digital I/O GND	-
20	MODE	Test mode selection input	A

No.	Name	Description of terminals	Type
21	ADDR	I^2C Slave address selection terminal	B
22	SPDIFO	S/PDIF Signal output	C
23	N.C		-
24	N.C		-
25	N.C		-
26	N.C		-
27	N.C		-
28	SDAO	2 line serial data output（*1）	C
29	SCLO	2 line serial clock output（*1）	C
30	MUTEX_DACO	DAC mute signal output(*1)	C
31	MUTEX_SPO	SP mute signal output(*1)	C
32	RESETXO	Reset signal output(*1)	C
33	SDATAO2	I^2S Audio data output 2	C
34	SDATAO1	I^2S Audio data output 1	C
35	LRCKO	I^2S Audio LR signal output 1	C
36	BCKO	I^2S Audio clock output 1	C
37	SYSCLKO	System clock output（*1）	C
38	VSS3	Digital I/O GND	-
39	MCLK	Master clock input	H
40	BCKI	I^2S Audio clock input	D

N.C.：Non Connection
(*1)：signal terminal is used with D class amplifier IC (BD5446EFV etc.) for input I2S made by Rohm.
(*2) ：It connects with the lead frame of a package. Please use by OPEN or GND connection.

●Terminal equal circuit figure

A	B	C
		
D	**E**	**F**
		
G	**H**	
		

1.Command interface

I^{2}C bus method is used in command interface with host CPU on BU9409FV.

In BU9409FV, not only writing but read-out is possible except for some registers.

Besides the slave address in BU9409FV, one byte select address can be Specified, written and readout.

The format of I^{2}C bus slave mode is shown below.

	MSB LSB		MSB LSB		MSB LSB		
S	Slave Address	A	Select Address	A	Data	A	P

S: Start condition

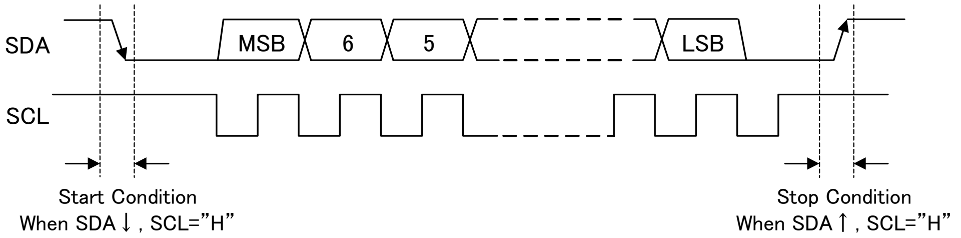
Slave Address: Putting up the bit of read mode (H") or write mode (L") after slave address (7bit) set with ADDR, the data of eight bits in total will be sent. (MSB first)

A: The acknowledge bit in each byte adds into the data when acknowledge is sent and received.
When data is correctly sent and received, "L" will be sent and received.
There was no acknowledge for "H".

Select Address: 1 byte select address is used in BU9409FV. (MSB first)

Data: Data-byte, data(MSB first)sent and received

P: Stop Condition



1-1. Data writing

S	Slave Address	A	Select Address	A	Data	A	P

▨ : From master to slave ☐ rom slave to master

ADDR=0

MSB LSB

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	0	0

ADDR=1

MSB LSB

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	1	0

Setting of BU9409FV slave address

Terminal setting ADDR	Write-mode Slave-address
0	80h
1	82h

S	Slave Address	A	Select Address	A	Data	A	Data	A	Data	A	P
(example)	80h		20h		00h		00h		00h		

▨ : From master to slave ☐ : From slave to master

Writing procedure

Step	Clock	Master	Slave(BU9409FV)	Note
1		Start Condition		
2	7	Slave Address		&h80 (&h82)
3	1	R/W (0)		
4	1		Acknowledge	
5	8	Select Address		Writing object register 8 bit
6	1		Acknowledge	
7	8	Data		Writing data 8 bit
8	1		Acknowledge	
9		Stop Condition		

- The select address add +1 by auto increment function when the data is transferred continuously.
  Repeat of Step 7~8.

1-2. Data readout

First of all, the readout target address(ex.&h20h) is written in &hD0 address register at the time of readout.

In the following stream, data is read out after the slave address. Please do not return the acknowledge when ending the reception.

S	Slave Address	A	Req_Addr	A	Select Address	A	P
（example）	80h		D0h		20h		

S	Slave Address	A	Data 1	A	Data 2	A	- - - -	A	Data N	Ā	P
（example）	81h		**h		**h				**h		

▨ : Master to slave, ☐ : Slave to master, A：With acknowledge, Ā：without acknowledge

Readout Procedure

Step	Clock	Master	Slave(BU9409FV)	Note
1		Start Condition		
2	7	Slave Address		&h80 (&h82)
3	1	R/W (0)		
4	1		Acknowledge	
5	8	Req_Addr		Address for I^2C readout &hD0
6	1		Acknowledge	
7	8	Select Address		Readout object register 8 bit
8	1		Acknowledge	
9	1	Stop Condition		
10	1	Start Condition		
11	7	Slave Address		&h81 (&h82)
12	1	R/W (1)		
13	1		Acknowledge	
14	8		Data	Readout data 8 bit
15	1	Acknowledge		
16		Stop Condition		

○ The select address adds +1 by auto increment function when continuous data is transferred.
Repeat Step14~15.

1-3. Control signal specification

○ Bus line, I/O stage electrical specification and timing.

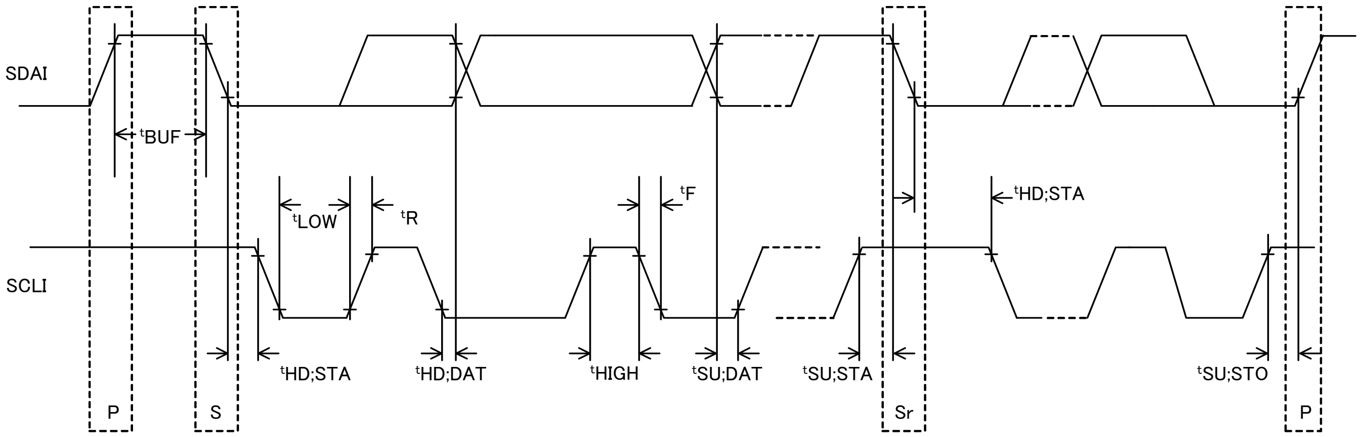


Fig.1-1: Timing chart

Table 1-1: SDAI and SCLI bus-line characteristic (Unless specified, Ta=25 , Vcc=3.3V)

Parameter		Code	High-speed mode		Unit
			Min.	Max.	
1	SCLI clock frequency	fSCL	0	400	kHz
2	Bus-free-time between "Stop" condition and "Start" condition	^{t}BUF	1.3	－	μs
3	"Start" condition of hold-time (resending). After this period, the first clock-pulse is generated.	^{t}HD;STA	0.6	－	μs
4	LOW status hold-time of SCLI clock	^{t}LOW	1.3	－	μs
5	HIGH status hold-time of SCLI clock	^{t}HIGH	0.6	－	μs
6	Setup time of resending “Start” condition	^{t}SU;STA	0.6	－	μs
7	Data-hold-time	^{t}HD;DAT	0[1]	－	μs
8	Data-setup time	^{t}SU;DAT	500/250/150	－	ns
9	Rising time of SDAI and SCL signal	^{t}R	20+Cb	300	ns
10	Fall time of SDAI and SCL signal	^{t}F	20+Cb	300	ns
11	Setup time of "Stop" condition	^{t}SU;STO	0.6	－	μs
12	Capacitive load of each bus-line	Cb	－	400	pF

The above-mentioned numerical values are all the values corresponding to $V_{IH\ min}$ and $V_{IL\ max}$ level.

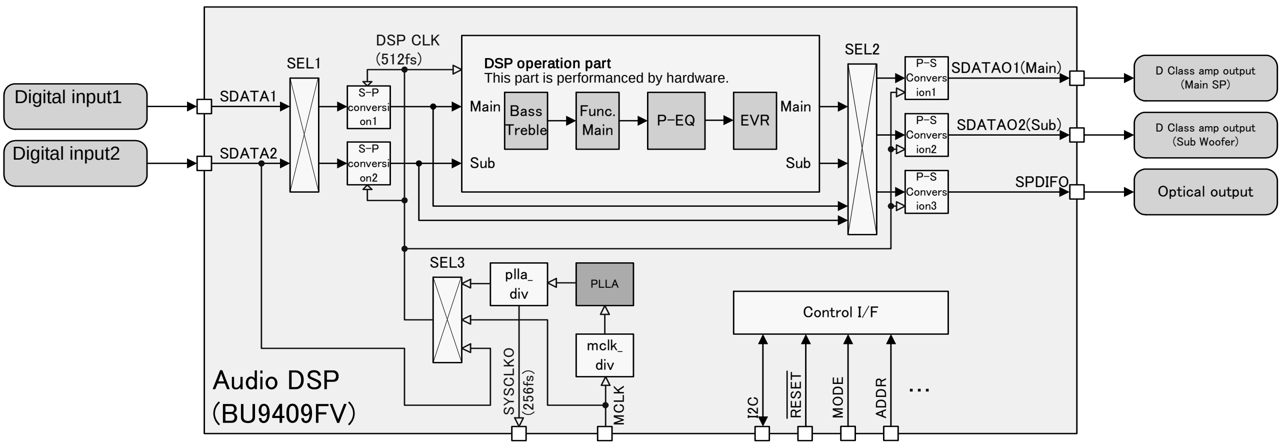
1) To exceed an undefined area on falling edged of SCLI, transmission device should internally offer the hold-time of 300ns or more for SDAI signal($V_{IH\ min}$ of SCLI signal).

2) Data-setup time changes with setup of MCLK. In MCLK=512fs, data setup time is 150ns.
In MCLK=256fs, data setup time is 250ns. In MCLK=128fs, data setup time is 500ns.

The above-mentioned characteristic is a theory value in IC design and it doesn't be guaranteed by shipment inspection.
When problem occurs by any chance, we talk in good faith and correspond.
Neither terminal SCLI nor terminal SDAI correspond to 5V tolerant. Please use it within absolute maximum rating 4.5V.

2.Switching of data and clock

I/O system chart of BU9409FV audio data is shown below.


Digital input1
Digital input2
SDATA1
SDATA2
SEL1
DSP CLK
(512fs)
S-P conversion1
S-P conversion2
DSP operation part
This part is performanced by hardware.
Main
Sub
Bass Treble
Func. Main
P-EQ
EVR
Main
Sub
SEL2
P-S Conversion1
P-S Conversion2
P-S Conversion3
SDATAO1(Main)
SDATAO2(Sub)
SPDIFO
D Class amp output (Main SP)
D Class amp output (Sub Woofer)
Optical output
SEL3
plla_div
PLLA
mclk_div
Control I/F
Audio DSP
(BU9409FV)
SYSCLKO (256fs)
MCLK
I2C
RESET
MODE
ADDR
…

BU9409FV has 2 digital stereo input and 3 digital stereo output with the same sampling rate.
Output from DSP operation part is converted into I^2S mode digital output or S/PDIF mode digital serial output.
System clock uses master clock input from MCLK terminal, makes 512fs multiplying clock in PLL block. Moreover, 256fs synchronous clock can be output from terminal SYSCLKO, and the clock is supplied to external DAC or D class SP amplifier.

SPDIFO and output data selection of SDATAO1 and SDATAO2 should unify the DSP processing after (post) or processing before (pre) with all outputs.

2-1. S-P conversion1 input data selection(SEL1)

Default = 0

Select Address	Value	Operating Description
&h03 [0]	0	Input data from SDATA1
	1	Input data from SDATA2

2-2. S-P conversion2 input data selection(SEL1)

Default = 0

Select Address	Value	Operating Description
&h03 [4]	0	Input data from SDATA1
	1	Input data from SDATA2

2-3. Output data selection(SEL2) to P-S conversion1 (SDATAO1 Terminal)

Default = 0

Select Address	Value	Operating Description
&h04 [1 : 0]	0	Main data output after DSP is processed.
	1	Sub data output after DSP is processed.
	2	Main data output before DSP is processed.
	3	Sub data output before DSP is processed.

2-4. Output data selection(SEL2) to P-S conversion2 (SDATAO2 Terminal)

Default = 0

Select Address	Value	Operating Description
&h04 [5 : 4]	0	Sub data output after DSP is processed.
	1	Main data output after DSP is processed.
	2	Sub data output before DSP is processed.
	3	Main data output before DSP is processed.

2-5. SPDIFO Terminal output data selection（SEL2）

Default = 0

Select Address	Value	Operating Description
&h05 [1 : 0]	0	Main data output after DSP is processed.
	1	Sub data output after DSP is processed.
	2	Main data output before DSP is processed.
	3	Sub data output before DSP is processed.

2-6. System clock selection（SEL3）

Select the DSP clock supplied to S-P conversion1、S-P conversion2、DSP、P-S conversion1、P-S conversion2、S/PDIF output part.

Default = 0

Select Address	Value	Operating Description
&h08 [5 : 4]	0	Chose the input from a MCLK terminal as a clock.
	1	Chose the PLL output as a clock.
	2	Chose the input from a SDATA2terminal as a clock. (used for IC test).
	3	

After power on or reset released, system block selection uses clock(even if not 512fs is ok) input from terminal MCLK to receive I2C command and initialize BU9409. Then set the dividing frequency ratio of PLL block (mclk_div, pll_div) that is suitable for the clock frequency from terminal MCLK , when PLL_512fs clock from PLL is steady, set &h08 = 10h.

2-7. Dividing frequency ratio setting of PLL block which corresponding to input clock from terminal MCLK

Sampling rate of input clock	Setting of mclk_div &hF3	Setting of pll_div &hF5	PLL initialization &hF6
512fs（24.576MHz、fs=48kHz）	10h	01h	23h
256fs（12.288MHz、fs=48kHz）	08h	01h	23h
128fs（6.144MHz、fs=48kHz）	04h	01h	23h

3. S-P Conversion 1, S-P Conversion 2

BU9409FV has two serial-parallel conversion circuits. （S-P conversion 1, S-P conversion 2）

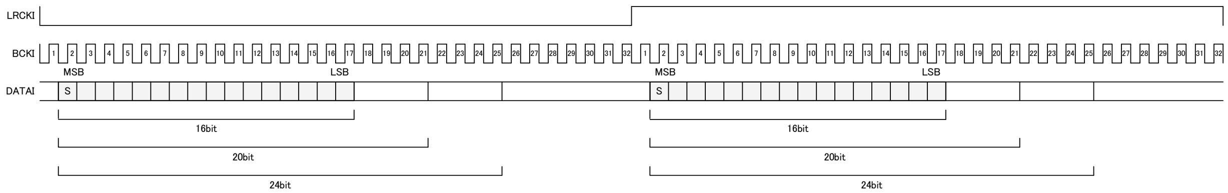
S-P conversion 1 & 2 receives the audio data of three-wire serial input from terminal and converts it into parallel data.

They select the inputs from LRCKI (2pin), BCKI (40pin), SDATA1 (3pin), and SDATA2(4pin).

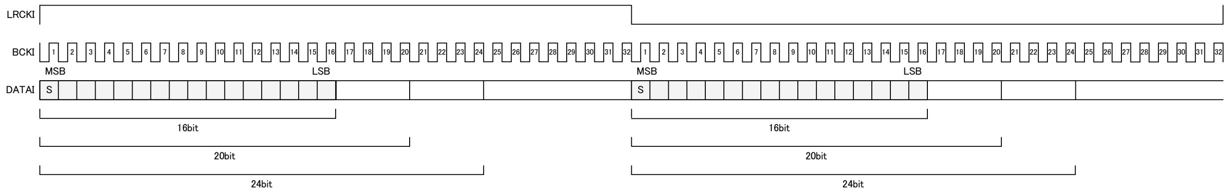
Input format has IIS method, left-justified method and right-justified method. Moreover, for bit clock frequency, 64fs or 48fs can be selected, and when 48fs is selected, the input format becomes the fixed right-justification. In addition, 16bit, 20bit and 24bit inputs can be selected respectively.

Timing chart of each transmission method is shown in the diagram below.

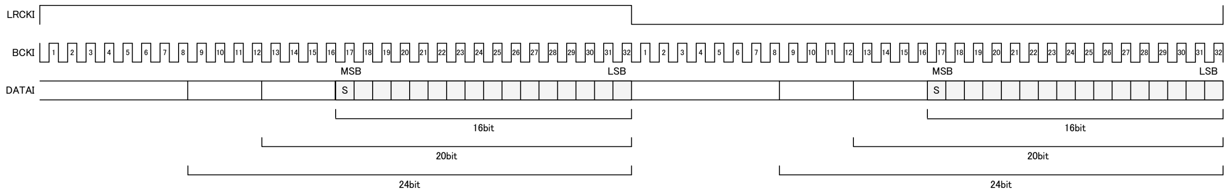
IIS method


LRCKI
BCKI
1 … 32
DATAI
MSB
LSB
S
16bit
20bit
24bit

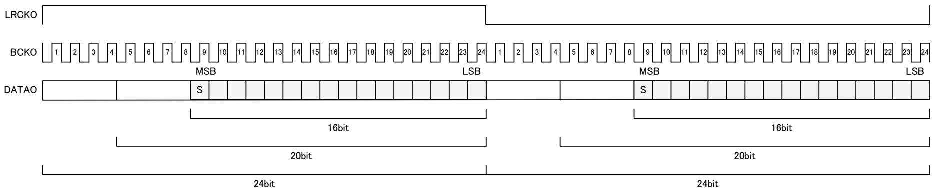
Left-justified method


LRCKI
BCKI
1 … 32
DATAI
MSB
LSB
S
16bit
20bit
24bit

Right-justified method


LRCKI
BCKI
1 … 32
DATAI
MSB
LSB
S
16bit
20bit
24bit

48fs


LRCKO
BCKO
1 … 24
DATAO
MSB
LSB
S
16bit
20bit
24bit

3-1. Three-wire serial input's bit clock frequency setting

Default = 0

Select Address	Value	Operational explanation
S-P conversion1, S-Pconversion2 &h0B [4]	0	64fs method
	1	48fs method

3-2. Three-wire serial input's format setting

Default = 0

Select Address	Value	Operational explanation
S-P conversion1 &h0B [3 : 2] S-P conversion2 &h0C [3 : 2]	0	IIS method
	1	left-justified method
	2	right-justified method

3-3. Three-wire serial input's data bit width setting

Default = 0

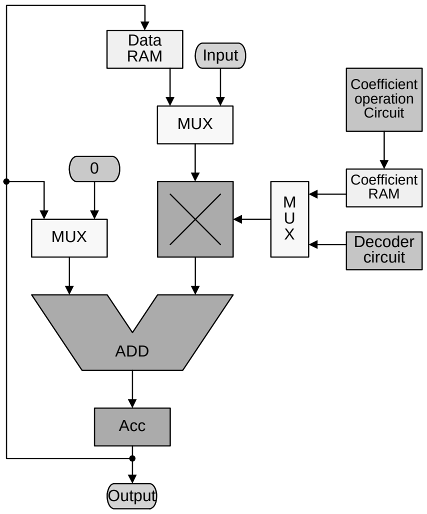
Select Address	Value	Operational explanation
S-P conversion1 &h0B [1 : 0] S-P conversion2 &h0C [1 : 0]	0	16 bit
	1	20 bit
	2	24 bit

4. Digital sound processing（DSP）

BU9409FV's Digital Sound Processing（DSP） consists of special hardware most suitable to Thin TV.
BU9409FV uses this special DSP to perform the following processing.
Prescaler, DC Cut HPF, Channel Mixer, P^{2}Volume（Perfect Pure Volume）, BASS, MIDDLE, TREBLE,
Pseudo Stereo, Surround, P^{2}Bass, P^{2}Treble, 7 Band・Parametric Equalizer, Master Volume, L/R Balance, PostScaler, Output Clipper、 Sub-woofer output Processing.

DSP Outline and Signal Flow

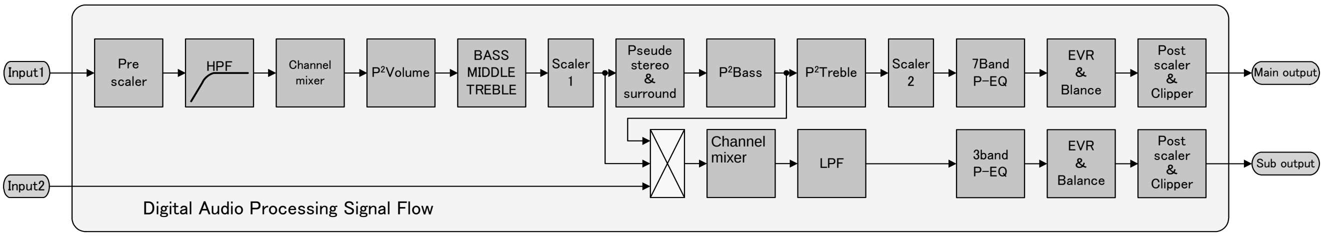
Data width : 32 bit （DATA RAM）
Machine cycle : 40.7ns （512fs, fs=48kHz）
Multiplier : 32×24 → 56 bit
Adder : 32＋32 → 32 bit
Data RAM : 256×32 bit
Coefficient RAM : 128×24 bit
Sampling frequency : fs=48kHz
Master clock : 512fs （24.576MHz, fs=48kHz）


Data RAM
Input
Coefficient operation Circuit
MUX
0
Coefficient RAM
M U X
MUX
Decoder circuit
ADD
Acc
Output

Digital signal from 16bit to 24bit is inputted to DSP,

and it is extended by +8bit（+42dB） as overflow margin on the upper side.

The clip process is performed in DSP when the process exceeding this range is performed.


Input1
Pre scaler
HPF
Channel mixer
P²Volume
BASS MIDDLE TREBLE
Scaler 1
Pseude stereo & surround
P²Bass
P²Treble
Scaler 2
7Band P-EQ
EVR & Blance
Post scaler & Clipper
Main output
Channel mixer
LPF
3band P-EQ
EVR & Balance
Post scaler & Clipper
Sub output
Input2
Digital Audio Processing Signal Flow

4-1. Prescaler

When digital signal is inputted to audio DSP, if the level is full scale input and the process of surround or equalizer is performed, then it overflows, therefore the input gain is adjusted by prescaler.
Adjustable range is +24dB to -103dB and can be set by the step of 0.5dB.
Prescaler does not incorporate the smooth transition function.

Default = 30h

<table>
<tr><th>Select Address</th><th>Operational explanation</th></tr>
<tr><td>&h20 [7 : 0]</td><td>
<table>
<tr><th>command</th><th>gain</th></tr>
<tr><td>00</td><td>+24dB</td></tr>
<tr><td>01</td><td>+23.5dB</td></tr>
<tr><td>⋮</td><td>⋮</td></tr>
<tr><td>30</td><td>0dB</td></tr>
<tr><td>31</td><td>−0.5dB</td></tr>
<tr><td>32</td><td>−1dB</td></tr>
<tr><td>⋮</td><td>⋮</td></tr>
<tr><td>FE</td><td>−103dB</td></tr>
<tr><td>FF</td><td>−∞</td></tr>
</table>
</td></tr>
</table>

4-2. DC Cut HPF

The DC offset component of digital signal inputted to the audio DSP is cut by this HPF.
The cutoff frequency fc of HPF is 1Hz, and first-order filter is used.

Default = 0

Select Address	Value	Operational explanation
&h21 [0]	0	Not using the DC Cut HPF
	1	Using the DC Cut HPF

4-3. Channel mixer

It performs the setting of mixing the sounds of left channel & right channel of digital signal inputted to the audio DSP.
Here the stereo signal is made to be monaural.

The data inputted to Lch of DSP is mixed.

Default = 0

Select Address	Value	Operational explanation
&h22 [7 : 6]	0	Inputting the Lch data
	1	Inputting the data of （Lch + Rch） / 2
	2	Inputting the data of （Lch + Rch） / 2
	3	Inputting the Rch data

The data inputted to Rch of DSP is mixed.

Default = 0

Select Address	Value	Operational explanation
&h22 [5 : 4]	0	Inputting the Rch data
	1	Inputting the data of （Lch + Rch） / 2
	2	Inputting the data of（Lch + Rch） / 2
	3	Inputting the Lch data

4-4. P^2Volume （Perfect Pure Volume）

There are some scenes in which sound suddenly becomes large like plosive sound in TV Commercial or Movie.

P^2Volume function automatically controls the volume and adjusts the output level.

In addition, it also adjusts in such a way that a whispery sound can be heard easily.

P^2Volume function operates in the fields of (1), (2) & (3) divided according to input level.

(1) at the time of $V_{I\,inf}(-\infty) \sim V_{I\,min}$

Noise is prevented from being lifted by P^2Volume function.

(2) When input level is over $V_{I\,min}$ and output is below V_{Omax}

$$V_O = V_I + \alpha$$

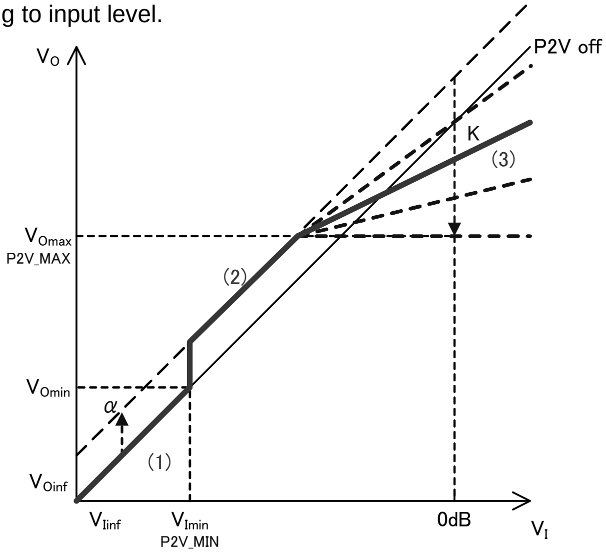
α： Lifting the Whole output level by the offset value α

(3) When output level V_O exceeds V_{Omax}

$$V_O = K \cdot V_I + \alpha$$

K： Slope for suppressing of D range （P2V_K）

It is also possible to set an output level constant.



Selection of using the P^2Volume function.

Default = 0

Select Address	Value	Operational explanation
&h33 [7]	0	Not using the P^2Volume function
	1	Using the P^2Volume function

Setting of $V_{I\,min}$

In order to cancel that noise etc. is lifted by P^2Volume, the P2V_MIN sets the minimum level at which (to the minimum) the P^2Volume functions.

command

Default = 00h

<table>
<tr><th>Select Address</th><th>Operational explanation</th></tr>
<tr><td>&h34 [4:0]</td><td>
<table>
<tr><th>command</th><th>gain</th><th>command</th><th>gain</th><th>command</th><th>gain</th><th>コマンド値</th><th>ゲイン</th></tr>
<tr><td>00</td><td>−∞</td><td>08</td><td>−44dB</td><td>10</td><td>−60dB</td><td>18</td><td>−76dB</td></tr>
<tr><td>01</td><td>−30dB</td><td>09</td><td>−46dB</td><td>11</td><td>−62dB</td><td>19</td><td>−78dB</td></tr>
<tr><td>02</td><td>−32dB</td><td>0A</td><td>−48dB</td><td>12</td><td>−64dB</td><td>1A</td><td>−80dB</td></tr>
<tr><td>03</td><td>−34dB</td><td>0B</td><td>−50dB</td><td>13</td><td>−66dB</td><td>1B</td><td>−82dB</td></tr>
<tr><td>04</td><td>−36dB</td><td>0C</td><td>−52dB</td><td>14</td><td>−68dB</td><td>1C</td><td>−84dB</td></tr>
<tr><td>05</td><td>−38dB</td><td>0D</td><td>−54dB</td><td>15</td><td>−70dB</td><td>1D</td><td>−86dB</td></tr>
<tr><td>06</td><td>−40dB</td><td>0E</td><td>−56dB</td><td>16</td><td>−72dB</td><td>1E</td><td>−88dB</td></tr>
<tr><td>07</td><td>−42dB</td><td>0F</td><td>−58dB</td><td>17</td><td>−74dB</td><td>1F</td><td>−90dB</td></tr>
</table>
</td></tr>
</table>

Setting of V_{Omax}

P2V_MAX sets the output suppression level. It represents the output level V_{Omax} at the time of input level V_I = 0dB in the case of setting of P2V_K = “0h”（slope is 0）.

Default = 00h

<table>
<tr><th>Select Address</th><th>Operational explanation</th></tr>
<tr><td>&h35 [4:0]</td><td>
<table>
<tr><th>command</th><th>gain</th><th>command</th><th>gain</th><th>command</th><th>gain</th><th>command</th><th>gain</th></tr>
<tr><td>00</td><td>0dB</td><td>08</td><td>−8dB</td><td>10</td><td>−16dB</td><td>18</td><td>−24dB</td></tr>
<tr><td>01</td><td>−1dB</td><td>09</td><td>−9dB</td><td>11</td><td>−17dB</td><td>19</td><td>−25dB</td></tr>
<tr><td>02</td><td>−2dB</td><td>0A</td><td>−10dB</td><td>12</td><td>−18dB</td><td>1A</td><td>−26dB</td></tr>
<tr><td>03</td><td>−3dB</td><td>0B</td><td>−11dB</td><td>13</td><td>−19dB</td><td>1B</td><td>−27dB</td></tr>
<tr><td>04</td><td>−4dB</td><td>0C</td><td>−12dB</td><td>14</td><td>−20dB</td><td>1C</td><td>−28dB</td></tr>
<tr><td>05</td><td>−5dB</td><td>0D</td><td>−13dB</td><td>15</td><td>−21dB</td><td>1D</td><td>−29dB</td></tr>
<tr><td>06</td><td>−6dB</td><td>0E</td><td>−14dB</td><td>16</td><td>−22dB</td><td>1E</td><td>−30dB</td></tr>
<tr><td>07</td><td>−7dB</td><td>0F</td><td>−15dB</td><td>17</td><td>−23dB</td><td>1F</td><td>−</td></tr>
</table>
</td></tr>
</table>

Setting of K

P2V_K sets the slop of D range. It sets the P2V_MAX = “1Eh”（-30dB） and represents the output level V_{Omax} at the time of input level V_I = 0dB.

Default = 00h

Select Address	Operational explanation
&h36 [3:0]	

command	gain	comman	gain
0	−30dB	8	−14dB
1	−28dB	9	−12dB
2	−26dB	A	−10dB
3	−24dB	B	−8dB
4	−22dB	C	−6dB
5	−20dB	D	−4dB
6	−18dB	E	−2dB
7	−16dB	F	0dB

Setting of α

P2V_OFS makes small voice easy to be heard because the whole output level is lifted.

Default = 00h

Select Address	Operational explanation
&h37 [4:0]	

command	gain	command	gain	command	gain	command	gain
00	0dB	08	+8dB	10	+16dB	18	+24dB
01	+1dB	09	+9dB	11	+17dB	19	−
02	+2dB	0A	+10dB	12	+18dB	1A	−
03	+3dB	0B	+11dB	13	+19dB	1B	−
04	+4dB	0C	+12dB	14	+20dB	1C	−
05	+5dB	0D	+13dB	15	+21dB	1D	−
06	+6dB	0E	+14dB	16	+22dB	1E	−
07	+7dB	0F	+15dB	17	+23dB	1F	−

Setting 1 of transition time at the time of attack

A_RATE is the setting of transition time when the state of P^2Volume function is transited to (2)→(3).

Default = 0

Select Address	Operational explanation
&h38 [6:4]	

command	A_RATE time	command	A_RATE time
0	1ms	4	5ms
1	2ms	5	10ms
2	3ms	6	20ms
3	4ms	7	40ms

Setting 1 of transition time at the time of recovery

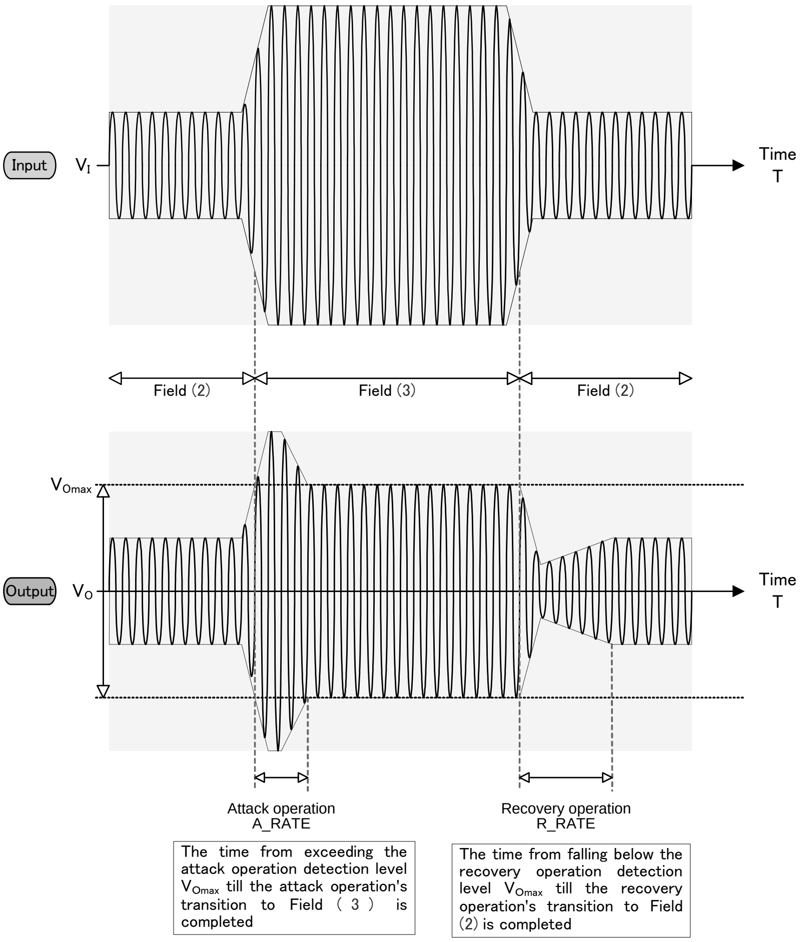
R_RATE is the setting of transition time when the state of P^2Volume function is transited to (3)→(2).

Default = 0h

Select Address	Operational explanation
&h38 [3:0]	

command	R_RATE time	command	R_RATE time
0	0.25s	8	3s
1	0.5s	9	4s
2	0.75s	A	5s
3	1s	B	6s
4	1.25s	C	7s
5	1.5s	D	8s
6	2s	E	9s
7	2.5s	F	10s

Explanation of A_RATE,R_RATE(field transition of (2)<->(3))


Input
V_I
Time
T
Field (2)
Field (3)
Field (2)
V_{Omax}
Output
V_O
Time
T
Attack operation
A_RATE
The time from exceeding the attack operation detection level V_{Omax} till the attack operation's transition to Field (3) is completed
Recovery operation
R_RATE
The time from falling below the recovery operation detection level V_{Omax} till the recovery operation's transition to Field (2) is completed

Setting 1 of attack detection time

A_TIME is the setting of the initiation of P^2Volume function’s transition operation. If output level at the time of transiting to (2)→(3) continues for more then A_TIME time in succession, then the state transition of P^2Volume is started.

Default = 0

<table>
<tr><th>Select Address</th><th>Operational explanation</th></tr>
<tr><td>&h39 [6:4]</td><td>
<table>
<tr><th>command</th><th>A_TIME</th><th>command</th><th>A_TIME</th></tr>
<tr><td>0</td><td>0.5ms</td><td>4</td><td>3ms</td></tr>
<tr><td>1</td><td>1ms</td><td>5</td><td>4ms</td></tr>
<tr><td>2</td><td>1.5ms</td><td>6</td><td>5ms</td></tr>
<tr><td>3</td><td>2ms</td><td>7</td><td>6ms</td></tr>
</table>
</td></tr>
</table>

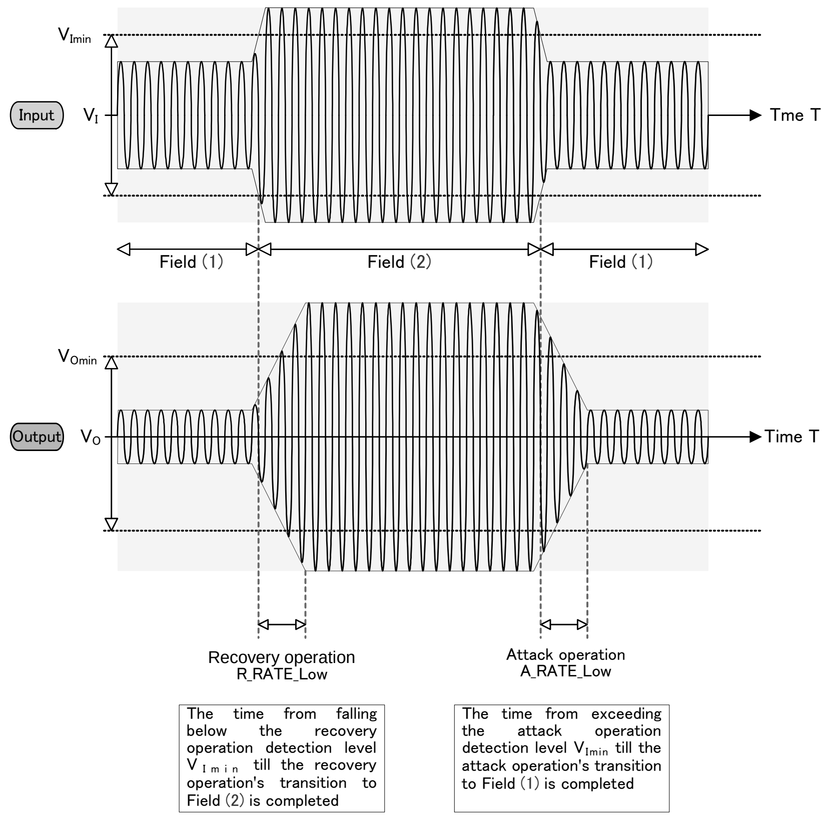
Setting 1 of recovery detection time

R_TIME is the setting of the initiation of P^2Volume function’s transition operation. If output level at the time of transiting to (3)→(2) continues for more then R_TIME time in succession, then the state transition of P^2Volume is started.

Default = 0

<table>
<tr><th>Select Address</th><th>Operational explanation</th></tr>
<tr><td>&h39 [2:0]</td><td>
<table>
<tr><th>command</th><th>R_TIME</th><th>command</th><th>R_TIME</th></tr>
<tr><td>0</td><td>50ms</td><td>4</td><td>300ms</td></tr>
<tr><td>1</td><td>100ms</td><td>5</td><td>400ms</td></tr>
<tr><td>2</td><td>150ms</td><td>6</td><td>500ms</td></tr>
<tr><td>3</td><td>200ms</td><td>7</td><td>600ms</td></tr>
</table>
</td></tr>
</table>

Explanation of A_RATE_Low,R_RATE_Low(field transition of (1)<->(2))



The time from falling below the recovery operation detection level V_{Imin} till the recovery operation's transition to Field (2) is completed

The time from exceeding the attack operation detection level V_{Imin} till the attack operation's transition to Field (1) is completed

Setting 2 of the transition time at the time of attack

A_RATE_LOW is the setting of transition time when the state of P^{2}Volume function is transited to (2)→(1).

Default = 0

<table>
<tr><th>Select Address</th><th>Operational explanation</th></tr>
<tr><td>&h3A [6:4]</td><td>
<table>
<tr><th>Command</th><th>A_RATE_LOW Time</th><th>Command</th><th>A_RATE_LOW Time</th></tr>
<tr><td>0</td><td>1ms</td><td>4</td><td>5ms</td></tr>
<tr><td>1</td><td>2ms</td><td>5</td><td>10ms</td></tr>
<tr><td>2</td><td>3ms</td><td>6</td><td>20ms</td></tr>
<tr><td>3</td><td>4ms</td><td>7</td><td>40ms</td></tr>
</table>
</td></tr>
</table>

Setting 2 of the transition time at the time of recovery

R_RATE_LOW is the setting of transition time when the state of P^{2}Volume function is transited to (1)→(2).

Default = 0 (Caution) This setting value is not reflected in BU9409FV. The value of &h38 [3:0] is set up.

<table>
<tr><th>Select Address</th><th>Operational explanation</th></tr>
<tr><td>&h3A [2:0]</td><td>
<table>
<tr><th>Command</th><th>R_RATE_LOW Time</th><th>Command</th><th>R_RATE_LOW Time</th></tr>
<tr><td>0</td><td>1ms</td><td>4</td><td>5ms</td></tr>
<tr><td>1</td><td>2ms</td><td>5</td><td>10ms</td></tr>
<tr><td>2</td><td>3ms</td><td>6</td><td>20ms</td></tr>
<tr><td>3</td><td>4ms</td><td>7</td><td>40ms</td></tr>
</table>
</td></tr>
</table>

Setting 2 of attack・recovery detection time

AR_TIME_LOW is the setting of the initiation of P^{2}Volume function's transition operation. If output level at the time of transiting to (1)<->(2) continues for more then AR_TIME time in succession, then the state transition of P^{2}Volume is started.

Default = 0

<table>
<tr><th>Select Address</th><th>Operational explanation</th></tr>
<tr><td>&h3B [6:4]</td><td>
<table>
<tr><th>Command</th><th>AR_TIME_LOW</th><th>Command</th><th>AR_TIME_LOW</th></tr>
<tr><td>0</td><td>0.5ms</td><td>4</td><td>3ms</td></tr>
<tr><td>1</td><td>1ms</td><td>5</td><td>4ms</td></tr>
<tr><td>2</td><td>1.5ms</td><td>6</td><td>5ms</td></tr>
<tr><td>3</td><td>2ms</td><td>7</td><td>6ms</td></tr>
</table>
</td></tr>
</table>

○Pulse sound detection and High-speed recovery function（functioning only at the time of transition of (2)<->(3)）

P^2Volume function makes the P^2Volume also compatible with large pulse sounds (clapping of hands, fireworks & shooting etc.) in addition to normal P^2Volume operation. When large pulse sound is inputted, attack operation (A_RATE) or recovery operation (R_RATE) is performed at 4 or 8 times the speed of normal attack operation or recovery operation.

Selection of using the pulse sound detection function.

Default = 0

Select Address	Value	Operational explanation
&h3BC[7]	0	Not using of pulse sound detection function
	1	Using of pulse sound detection function

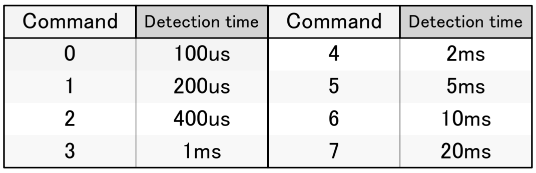
Selection of operating times of Recovery Time (R_RATE) in the case of using the pulse sound detection function

Default = 0

Select Address	Value	Operational explanation
&h3C [3]	0	Operating at 4 times the speed corresponding to the setting time of R_RATE
	1	Operating at 8 times the speed corresponding to the setting time of R_RATE

Selection of pulse sound detection time

Default = 0

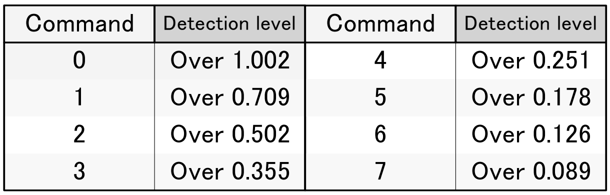
Select Address	Operational explanation
&h3C [6:4]	

Command	Detection time	Command	Detection time
0	100us	4	2ms
1	200us	5	5ms
2	400us	6	10ms
3	1ms	7	20ms

Setting of operating level of pulse sound detection function

Operation is started by the difference between the presently detected value and the last value as a standard.

Default = 0

Select Address	Operational explanation
&h3C [2:0]	

Command	Detection level	Command	Detection level
0	Over 1.002	4	Over 0.251
1	Over 0.709	5	Over 0.178
2	Over 0.502	6	Over 0.126
3	Over 0.355	7	Over 0.089

Example） Present detection level A : -10dB → 10^(-10/20) = 0.32

The last detection level B : -30dB → 10^(-30/20) = 0.032

A – B : 0.32 – 0.032 = 0.288 → Operating by the setting of command ”4” to ”7”.

4-5. BASS

BASS of TONE Control can use Peaking filter or Low-shelf filter.

The setting is converted, in the IC, into digital filter's coefficients （b0, b1, b2, a1, a2）by selecting the F_0, Q and Gain, and transmitted to coefficient RAM. The switching shock noise at the time of alteration of setting can be prevented by the smooth transition function.

○BASS Control

Selection of filter types

Default = 0

Select Address	Value	Operational explanation
&h40 [7]	0	Peaking filter
	1	Low-shelf filter

Selection of smooth transition function

Default = 0

Select Address	Value	Operational explanation
&h40 [6]	0	Using BASS smooth transition function
	1	Not BASS using smooth transition function

Selection of smooth transition time

Default = 0

Select Address	Value	Operational explanation
&h40 [5:4]	0	21.4ms
	1	10.7ms
	2	5.4ms
	3	2.7ms

Setting of smooth transition start

In the case of using the smooth transition function, after being transmitted, by the &h40[0] command, to the coefficient RAM for smooth transition, the alteration of BASS's coefficients is completed by using this command.

Default = 0

Select Address	Value	Operational explanation
&h4C [0]	0	BASS smooth transition stop
	1	BASS smooth transition start

What is necessary is the time of waiting, which is more than the time selected by the setting of Bass smooth transition time, from the time the BASS smooth transition start （&h4C[0] = "1"） is executed until the following command is sent. Please make sure to perform the Bass smooth transition stop（&h4C[0] = "0"） after the smooth transition is completed.

Setting of the Start of transmitting to coefficient RAM

In the case of using the smooth transition, it is transmitted to the coefficient RAM for smooth transition. In the case of not using of the smooth transition, it is transmitted directly to the coefficient RAM.

Default = 0

Select Address	Value	Operational explanation
&h40 [0]	0	BASS coefficient transmission stop
	1	BASS coefficient transmission start

selection of frequency（F_0）

Default = 0Eh

Select Address	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency
&h41 [5:0]	00	20Hz	08	50Hz	10	125Hz	18	315Hz	20	800Hz	28	2kHz	30	5kHz	38	12.5kHz
	01	22Hz	09	56Hz	11	140Hz	19	350Hz	21	900Hz	29	2.2kHz	31	5.6kHz	39	14kHz
	02	25Hz	0A	63Hz	12	160Hz	1A	400Hz	22	1kHz	2A	2.5kHz	32	6.3kHz	3A	16kHz
	03	28Hz	0B	70Hz	13	180Hz	1B	450Hz	23	1.1kHz	2B	2.8kHz	33	7kHz	3B	18kHz
	04	32Hz	0C	80Hz	14	200Hz	1C	500Hz	24	1.25kHz	2C	3.15kHz	34	8kHz	3C	20kHz
	05	35Hz	0D	90Hz	15	220Hz	1D	560Hz	25	1.4kHz	2D	3.5kHz	35	9kHz	3D	−
	06	40Hz	0E	100Hz	16	250Hz	1E	630Hz	26	1.6kHz	2E	4kHz	36	10kHz	3E	−
	07	45Hz	0F	110Hz	17	280Hz	1F	700Hz	27	1.8kHz	2F	4.5kHz	37	11kHz	3F	−

Selection of quality factor （Q）

Default = 4h

Select Address	Command	Quality factor	Command	Quality factor
&h42 [3:0]	0	0.33	8	2.2
	1	0.43	9	2.7
	2	0.56	A	3.3
	3	0.75	B	3.9
	4	1.0	C	4.7
	5	1.2	D	5.6
	6	1.5	E	6.8
	7	1.8	F	8.2

Selection of Gain

Default = 40h

Select Address	Command	Gain
&h43 [6:0]	1C	−18dB
	⋮	⋮
	3E	−1dB
	3F	−0.5dB
	40	0dB
	41	+0.5dB
	42	+1dB
	⋮	⋮
	64	+18dB

If the coefficient of b0, b1, b2, a1, and a2 exceeds ±4, it may not operate normally.

4-6. MIDDLE

MIDDLE of TONE Control uses Peaking filter.

The setting is converted, in the IC, into digital filter's coefficients （b0, b1, b2, a1, a2）by selecting the F，Q and Gain, and transmitted to coefficient RAM. The switching shock noise at the time of alteration of setting can be prevented by the smooth transition function.

○MIDDLE Control

Selection of smooth transition function

Default = 0

Select Address	Value	Operational explanation
&h44 [6]	0	Using MIDDLE smooth transition function
	1	Not MIDDLE using smooth transition function

Selection of smooth transition time

Default = 0

Select Address	Value	Operational explanation
&h44 [5:4]	0	21.4ms
	1	10.7ms
	2	5.4ms
	3	2.7ms

Setting of smooth transition start

In the case of using the smooth transition function, after being transmitted, by the &h44[0] command, to the coefficient RAM for smooth transition, the alteration of MIDDLE's coefficients is completed by using this command.

Default = 0

Select Address	Value	Operational explanation
&h4C [1]	0	MIDDLE smooth transition stop
	1	MIDDLE smooth transition start

What is necessary is the time of waiting, which is more than the time selected by the setting of MIDDLE smooth transition time, from the time the MIDDLE smooth transition start （&h4C[1] = "1"） is executed until the following command is sent. Please make sure to perform the MIDDLE smooth transition stop（&h4C[1] = "0"） after the smooth transition is completed.

Setting of the Start of transmitting to coefficient RAM

In the case of using the smooth transition, it is transmitted to the coefficient RAM for smooth transition. In the case of not using of the smooth transition, it is transmitted to the direct coefficient RAM.

Default = 0

Select Address	Value	Operational explanation
&h44 [0]	0	MIDDLE coefficient transmission stop
	1	MIDDLE coefficient transmission sart

Selection of frequency（F_0）

Default = 0Eh

Select Address	Operational explanation
&h45 [5:0]	

Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency
00	20Hz	08	50Hz	10	125Hz	18	315Hz	20	800Hz	28	2kHz	30	5kHz	38	12.5kHz
01	22Hz	09	56Hz	11	140Hz	19	350Hz	21	900Hz	29	2.2kHz	31	5.6kHz	39	14kHz
02	25Hz	0A	63Hz	12	160Hz	1A	400Hz	22	1kHz	2A	2.5kHz	32	6.3kHz	3A	16kHz
03	28Hz	0B	70Hz	13	180Hz	1B	450Hz	23	1.1kHz	2B	2.8kHz	33	7kHz	3B	18kHz
04	32Hz	0C	80Hz	14	200Hz	1C	500Hz	24	1.25kHz	2C	3.15kHz	34	8kHz	3C	20kHz
05	35Hz	0D	90Hz	15	220Hz	1D	560Hz	25	1.4kHz	2D	3.5kHz	35	9kHz	3D	–
06	40Hz	0E	100Hz	16	250Hz	1E	630Hz	26	1.6kHz	2E	4kHz	36	10kHz	3E	–
07	45Hz	0F	110Hz	17	280Hz	1F	700Hz	27	1.8kHz	2F	4.5kHz	37	11kHz	3F	–

Selection of quality factor（Q）

Default = 4h

Select Address	Operational explanation
&h46 [3:0]	

Command	Quality factor	Command	Quality factor
0	0.33	8	2.2
1	0.43	9	2.7
2	0.56	A	3.3
3	0.75	B	3.9
4	1.0	C	4.7
5	1.2	D	5.6
6	1.5	E	6.8
7	1.8	F	8.2

Selection of Gain

Default = 40h

Select Address	Operational explanation
&h47 [6:0]	

Command	Gain
1C	−18dB
⋮	⋮
3E	−1dB
3F	−0.5dB
40	0dB
41	+0.5dB
42	+1dB
⋮	⋮
64	+18dB

If the coefficient of b0, b1, b2, a1, and a2 exceeds ±4, it may not operate normally.

4-7. TREBLE

TREBLE of TONE Control can use Peaking filter or High-shelf filter.

The setting is converted, in the IC, into digital filter's coefficients （b0, b1, b2, a1, a2）by selecting the F_0, Q and Gain, and transmitted to coefficient RAM. The switching shock noise at the time of alteration of setting can be prevented by the smooth transition function.

○TREBLE Control

Selection of filter types

Default = 0

Select Address	Value	Operational explanation
&h48 [7]	0	Peaking filter
	1	High-shelf filter

Selection of smooth transition function

Default = 0

Select Address	Value	Operational explanation
&h48 [6]	0	Using smooth transition function
	1	Not using smooth transition function

Selection of smooth transition time

Default = 0

Select Address	Value	Operational explanation
&h48 [5:4]	0	21.4ms
	1	10.7ms
	2	5.4ms
	3	2.7ms

Setting of smooth transition start

In the case of using the smooth transition function, after being transmitted, by the &h48[0] command, to the coefficient RAM for smooth transition, the alteration of TREBLE's coefficients is completed by using this command.

Default = 0

Select Address	Value	Operational explanation
&h4C [2]	0	TREBLE smooth transition stop
	1	TREBLE smooth transition start

What is necessary is the time of waiting, which is more than the time selected by the setting of TREBLE smooth transition time, from the time the TREBLE smooth transition start（&h4C[2] = “1”）is executed until the following command is sent. Please make sure to perform the TREBLE smooth transition stop（&h4C[2] = “0”） after the smooth transition is completed.

Setting of the Start of transmitting to coefficient RAM

In the case of using the smooth transition, it is transmitted to the coefficient RAM for smooth transition. In the case of not using of the smooth transition, it is transmitted to the direct coefficient RAM.

Default = 0

Select Address	Value	Operational explanation
&h48 [0]	0	TREBLE coefficient transmission stop
	1	TREBLE coefficient transmission start

Selection of frequency（F_0）

Default = 0Eh

Select Address	Operational explanation
&h49 [5:0]	

Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency
00	20Hz	08	50Hz	10	125Hz	18	315Hz	20	800Hz	28	2kHz	30	5kHz	38	12.5kHz
01	22Hz	09	56Hz	11	140Hz	19	350Hz	21	900Hz	29	2.2kHz	31	5.6kHz	39	14kHz
02	25Hz	0A	63Hz	12	160Hz	1A	400Hz	22	1kHz	2A	2.5kHz	32	6.3kHz	3A	16kHz
03	28Hz	0B	70Hz	13	180Hz	1B	450Hz	23	1.1kHz	2B	2.8kHz	33	7kHz	3B	18kHz
04	32Hz	0C	80Hz	14	200Hz	1C	500Hz	24	1.25kHz	2C	3.15kHz	34	8kHz	3C	20kHz
05	35Hz	0D	90Hz	15	220Hz	1D	560Hz	25	1.4kHz	2D	3.5kHz	35	9kHz	3D	−
06	40Hz	0E	100Hz	16	250Hz	1E	630Hz	26	1.6kHz	2E	4kHz	36	10kHz	3E	−
07	45Hz	0F	110Hz	17	280Hz	1F	700Hz	27	1.8kHz	2F	4.5kHz	37	11kHz	3F	−

Selection of quality factor（Q）

Default = 4h

Select Address	Operational explanation
&h4A [3:0]	

Command	Quality factor	Command	Quality factor
0	0.33	8	2.2
1	0.43	9	2.7
2	0.56	A	3.3
3	0.75	B	3.9
4	1.0	C	4.7
5	1.2	D	5.6
6	1.5	E	6.8
7	1.8	F	8.2

Selection of Gain

Default = 40h

Select Address	Operational explanation
&h4B [6:0]	

Command	Gain
1C	−18dB
⋮	⋮
3E	−1dB
3F	−0.5dB
40	0dB
41	+0.5dB
42	+1dB
⋮	⋮
64	+18dB

If the coefficient of b0, b1, b2, a1, and a2 exceeds ±4, it may not operate normally.

4-8. Scaler 1

Scaler adjusts the gain in order to prevent the overflow in DSP.

Adjustable range is +24dB to -103dB and can be set by the step of 0.5dB.

Scaler 1 does not incorporate the smooth transition function.

Default = 30h

<table>
<tr><th>Select Address</th><th>Operational explanation</th></tr>
<tr><td>&h24 [7 : 0]</td><td>
<table>
<tr><th>Command</th><th>Gain</th></tr>
<tr><td>00</td><td>+24dB</td></tr>
<tr><td>01</td><td>+23.5dB</td></tr>
<tr><td>⋮</td><td>⋮</td></tr>
<tr><td>30</td><td>0dB</td></tr>
<tr><td>31</td><td>−0.5dB</td></tr>
<tr><td>32</td><td>−1dB</td></tr>
<tr><td>⋮</td><td>⋮</td></tr>
<tr><td>FE</td><td>−103dB</td></tr>
<tr><td>FF</td><td>−∞</td></tr>
</table>
</td></tr>
</table>

4-9. Pseudo stereo

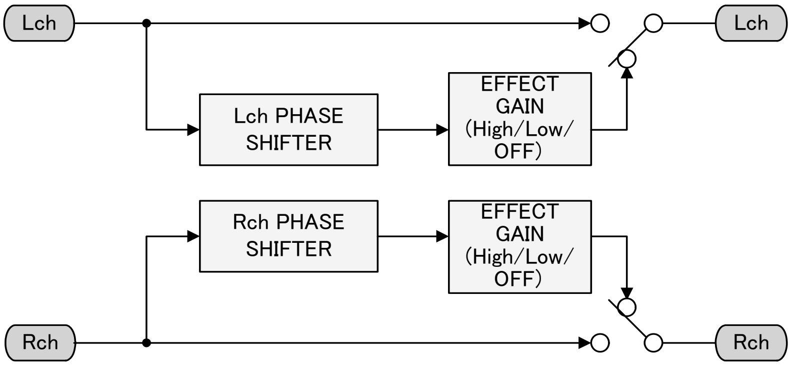
The sense of stereo is reproduced by signal processing of monaural voice.

Selection of filter effects of pseudo stereo

Default = 0

Select Address	Value	Operational explanation
&h71 [1 : 0]	0	Not using of pseudo stereo
	1	Gain is set as "high"
	2	Gain is set as "low"

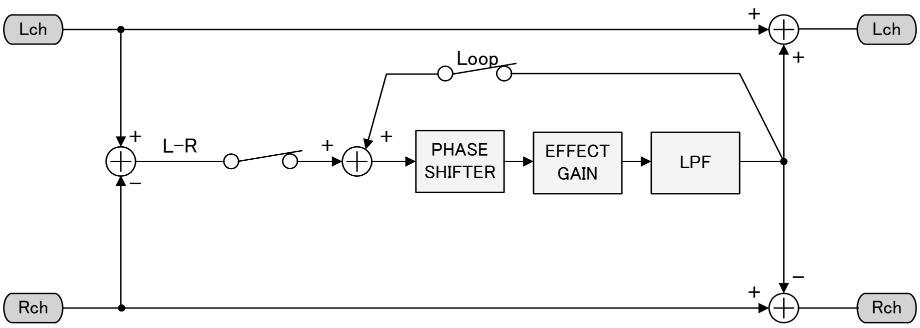
If combined with the Surround’s setting of ON（&h70[7] = 1）, it will become even wider.


Lch
Lch
Lch PHASE SHIFTER
EFFECT GAIN (High/Low/OFF)
Rch PHASE SHIFTER
EFFECT GAIN (High/Low/OFF)
Rch
Rch

4-10. Surround （Matrix Surround 3 D）

It realizes the Surround with little feeling of fatigue even after wide seat spot and long-time watching & listening to. It reproduces the feeling of broadening of the natural sounds in medium & high bands and realizes the sound field that do no damage to the feeling of locating of the vocal.

If loop is used, then the number of stages of phase shifter can be increased in a pseudo way.


Lch
+
+
Lch
Loop
+
L−R
−
+
+
PHASE SHIFTER
EFFECT GAIN
LPF
−
+
Rch
Rch

ON/OFF of Surround function

Default = 0

Select Address	Value	Operational explanation
&h70 [7]	0	Turning the Surround effect OFF
	1	Turning the Surround effect ON

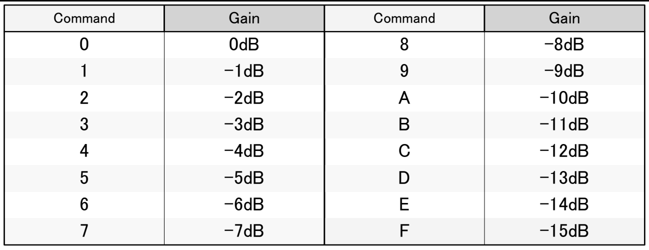
Setting of using the LOOP

Default = 0

Select Address	Value	Operational explanation
&h70 [5]	0	Not using of LOOP
	1	Using of LOOP

Setting of Surround gain

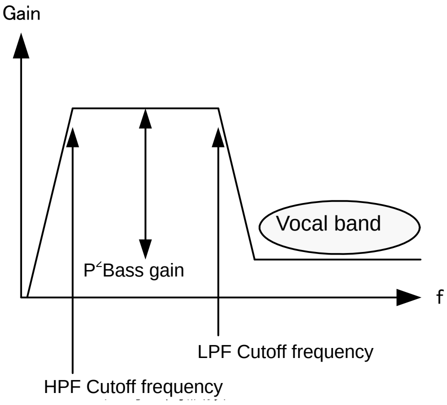
Default = Fh

<table>
<tr><th>Select Address</th><th>Operational explanation</th></tr>
<tr><td>&h70 [3 : 0]</td><td>
<table>
<tr><th>Command</th><th>Gain</th><th>Command</th><th>Gain</th></tr>
<tr><td>0</td><td>0dB</td><td>8</td><td>−8dB</td></tr>
<tr><td>1</td><td>−1dB</td><td>9</td><td>−9dB</td></tr>
<tr><td>2</td><td>−2dB</td><td>A</td><td>−10dB</td></tr>
<tr><td>3</td><td>−3dB</td><td>B</td><td>−11dB</td></tr>
<tr><td>4</td><td>−4dB</td><td>C</td><td>−12dB</td></tr>
<tr><td>5</td><td>−5dB</td><td>D</td><td>−13dB</td></tr>
<tr><td>6</td><td>−6dB</td><td>E</td><td>−14dB</td></tr>
<tr><td>7</td><td>−7dB</td><td>F</td><td>−15dB</td></tr>
</table></td></tr>
</table>

4-11. P^{2}Bass （Perfect Pure Bass： Deep Bass Equalizer）

It is the deep bass equalizer making it possible that even thin-screen TV, by which the enclosure of speaker is restricted, can reproduce the real sound close to powerful deep bass & original sound.

Solid & clear deep bass with little feeling of distortion is realized. Even boosting of bass does not interfere with vocal band, therefore rich and natural deep band is realized.



ON/OFF of P^{2}Bass function

Default = 0

Select Address	Value	Operational explanation
&h73 [7]	0	Not using of P^{2}Bass function
	1	Using of P^{2}Bass function

Setting of P^{2}Bass smooth transition time

Default = 0

Select Address	Value	Operational explanation
&h73 [3：2]	0	21.4ms
	1	10.7ms
	2	5.4ms
	3	2.7ms

P^{2}Bass smooth transition control

Default = 0

Select Address	Value	Operational explanation
&h77 [1：0]	0	P^{2}Bass smooth transition stop
	1	Setting of the values into Coefficient RAM for P^{2}Bass smooth transition
	2	P^{2}Bass smooth transition start

What is necessary is the time of waiting, which is more than the time selected by the setting of P^{2}Bass smooth transition time, from the time the P^{2}Bass smooth transition start（&h77[1:0] = “2”） is executed until the following command is sent. Please make sure to perform the P^{2}Bass smooth transition stop（&h77[1:0] = “0”） after the smooth transition is completed.

Setting of P^2Bass deep bass gain

Default = 00h

Select Address	Operational explanation			
	Command	Gain	Command	Gain
&h74 [7 : 4]	0	0dB	8	+8dB
	1	+1dB	9	+9dB
	2	+2dB	A	+10dB
	3	+3dB	B	+11dB
	4	+4dB	C	+12dB
	5	+5dB	D	+13dB
	6	+6dB	E	+14dB
	7	+7dB	F	+15dB

Setting of P^2Bass HPF cutoff frequency

Default = 0

Select Address	Value	Operational explanation
&h74 [3 : 2]	0	60Hz
	1	80Hz
	2	100Hz
	3	120Hz

Setting of P^2Bass LPF cutoff frequency

Default = 0

Select Address	Value	Operational explanation
&h74 [1 : 0]	0	120Hz
	1	160Hz
	2	200Hz
	3	240Hz

ON/OFF of pseudo bass function

It can contribute to bass emphasis effect caused by pseudo bass. And it can also be used independently.

Default = 0

Select Address	Value	Operational explanation
&h72 [7]	0	Not using of pseudo bass function
	1	Using of pseudo bass function

Setting of pseudo bass gain

Default = 00h

Select Address	Operational explanation			
	Command	Gain	Command	Gain
&h72 [6 : 4]	0	−4dB	4	+4dB
	1	−2dB	5	+6dB
	2	0dB	6	+8dB
	3	+2dB	7	+10dB

4-12. P^{2}Treble （Perfect Pure Treble：Medium・High-band equalizer）

It realizes good Clearness, sound stretch, and clear-cut manner.

It realizes such an effect that the sound is raised and can be heard when speaker is located on the underside of a device.

ON/OFF of P^{2}Treble function

Default = 0

Select Address	Value	Operational explanation
&h75 [7]	0	Not using of P^{2}Treble function
	1	Using of P^{2}Treble function

Setting of P^{2}Treble smooth transition time

Default = 0

Select Address	Value	Operational explanation
&h75 [3 : 2]	0	21.4ms
	1	10.7ms
	2	5.4ms
	3	2.7ms

P^{2}Treble smooth transition control

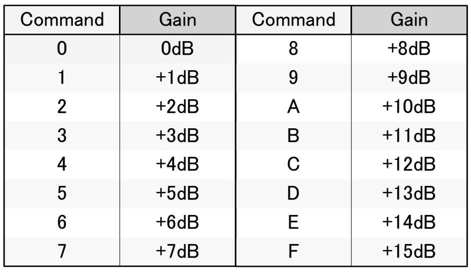
Default = 0

Select Address	Value	Operational explanation
&h78 [1 : 0]	0	P^{2}Treble smooth transition stop
	1	Setting of the values into Coefficient RAM for P^{2}Treble smooth transition
	2	P^{2}Treble smooth transition Start

What is necessary is the time of waiting, which is more than the time selected by the setting of P^{2}Treble smooth transition time, from the time the P^{2}Treble smooth transition start（&h78[1:0] = “2”） is executed until the following command is sent. Please make sure to perform the P^{2}Treble smooth transition stop（&h78[1:0] = “0”） after the smooth transition is completed.

Setting of P^{2}Treble medium・high-band gain

Default = 0h

<table>
<tr><th>Select Address</th><th>Operational explanation</th></tr>
<tr><td>&h76 [7 : 4]</td><td>
<table>
<tr><th>Command</th><th>Gain</th><th>Command</th><th>Gain</th></tr>
<tr><td>0</td><td>0dB</td><td>8</td><td>+8dB</td></tr>
<tr><td>1</td><td>+1dB</td><td>9</td><td>+9dB</td></tr>
<tr><td>2</td><td>+2dB</td><td>A</td><td>+10dB</td></tr>
<tr><td>3</td><td>+3dB</td><td>B</td><td>+11dB</td></tr>
<tr><td>4</td><td>+4dB</td><td>C</td><td>+12dB</td></tr>
<tr><td>5</td><td>+5dB</td><td>D</td><td>+13dB</td></tr>
<tr><td>6</td><td>+6dB</td><td>E</td><td>+14dB</td></tr>
<tr><td>7</td><td>+7dB</td><td>F</td><td>+15dB</td></tr>
</table>
</td></tr>
</table>

4-13. Scaler 2

Scaler adjusts the gain in order to prevent the overflow in DSP.

Adjustable range is +24dB to -103dB and can be set by the step of 0.5dB.

Scaler 2 does not incorporate the smooth transition function.

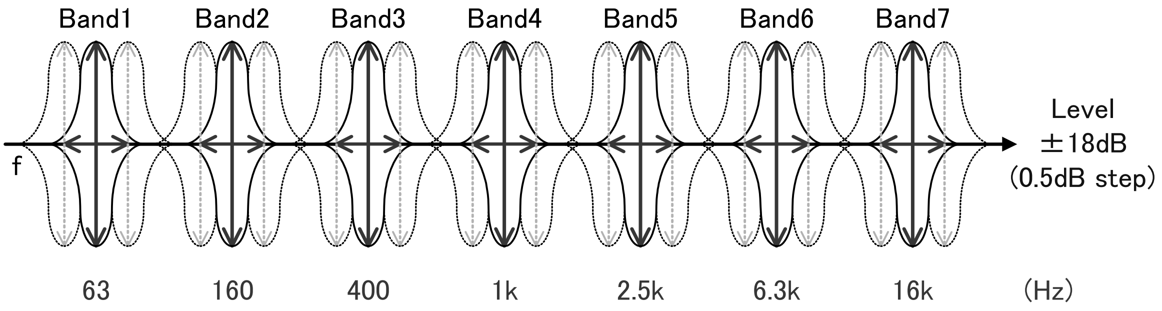
Default = 30h

<table>
<tr><th>Select Address</th><th>Operational explanation</th></tr>
<tr><td>&h25 [7 : 0]</td><td>
<table>
<tr><th>Command</th><th>Gain</th></tr>
<tr><td>00</td><td>+24dB</td></tr>
<tr><td>01</td><td>+23.5dB</td></tr>
<tr><td>⋮</td><td>⋮</td></tr>
<tr><td>30</td><td>0dB</td></tr>
<tr><td>31</td><td>−0.5dB</td></tr>
<tr><td>32</td><td>−1dB</td></tr>
<tr><td>⋮</td><td>⋮</td></tr>
<tr><td>FE</td><td>−103dB</td></tr>
<tr><td>FF</td><td>−∞</td></tr>
</table>
</td></tr>
</table>

4-14. 7 band・parametric equalizer

7-band parametric equalizer can use Peaking filter, Low-shelf filter or high-shelf filter.

The setting is converted, in the IC, into digital filter's coefficients （b0, b1, b2, a1, a2）by selecting the F, Q and Gain, and transmitted to coefficient RAM. There is no smooth transition function.



Selection of filter types

Default = 0

Select Address	Value	Operational explanation
bit[7:6] It sets to all band	0	Peaking filter
	1	Low-shelf filter
	2	High-shelf filter

Setting of the Start of transmitting to coefficient RAM

It is transmitted to direct coefficient RAM.

Default = 0

Select Address	Value	Operational explanation
bit [0] It sets to all band	0	Coefficient transmission stop
	1	Coefficient transmission start

Selection of frequency（F_0）

Default = 0Eh

<table>
<tr><th>Select Address</th><th>Operational explanation</th></tr>
<tr><td>bit [5:0]
It sets to all band</td><td>
<table>
<tr><th>Command</th><th>Frequency</th><th>Command</th><th>Frequency</th><th>Command</th><th>Frequency</th><th>Command</th><th>Frequency</th><th>Command</th><th>Frequency</th><th>Command</th><th>Frequency</th><th>Command</th><th>Frequency</th><th>Command</th><th>Frequency</th></tr>
<tr><td>00</td><td>20Hz</td><td>08</td><td>50Hz</td><td>10</td><td>125Hz</td><td>18</td><td>315Hz</td><td>20</td><td>800Hz</td><td>28</td><td>2kHz</td><td>30</td><td>5kHz</td><td>38</td><td>12.5kHz</td></tr>
<tr><td>01</td><td>22Hz</td><td>09</td><td>56Hz</td><td>11</td><td>140Hz</td><td>19</td><td>350Hz</td><td>21</td><td>900Hz</td><td>29</td><td>2.2kHz</td><td>31</td><td>5.6kHz</td><td>39</td><td>14kHz</td></tr>
<tr><td>02</td><td>25Hz</td><td>0A</td><td>63Hz</td><td>12</td><td>160Hz</td><td>1A</td><td>400Hz</td><td>22</td><td>1kHz</td><td>2A</td><td>2.5kHz</td><td>32</td><td>6.3kHz</td><td>3A</td><td>16kHz</td></tr>
<tr><td>03</td><td>28Hz</td><td>0B</td><td>70Hz</td><td>13</td><td>180Hz</td><td>1B</td><td>450Hz</td><td>23</td><td>1.1kHz</td><td>2B</td><td>2.8kHz</td><td>33</td><td>7kHz</td><td>3B</td><td>18kHz</td></tr>
<tr><td>04</td><td>32Hz</td><td>0C</td><td>80Hz</td><td>14</td><td>200Hz</td><td>1C</td><td>500Hz</td><td>24</td><td>1.25kHz</td><td>2C</td><td>3.15kHz</td><td>34</td><td>8kHz</td><td>3C</td><td>20kHz</td></tr>
<tr><td>05</td><td>35Hz</td><td>0D</td><td>90Hz</td><td>15</td><td>220Hz</td><td>1D</td><td>560Hz</td><td>25</td><td>1.4kHz</td><td>2D</td><td>3.5kHz</td><td>35</td><td>9kHz</td><td>3D</td><td>－</td></tr>
<tr><td>06</td><td>40Hz</td><td>0E</td><td>100Hz</td><td>16</td><td>250Hz</td><td>1E</td><td>630Hz</td><td>26</td><td>1.6kHz</td><td>2E</td><td>4kHz</td><td>36</td><td>10kHz</td><td>3E</td><td>－</td></tr>
<tr><td>07</td><td>45Hz</td><td>0F</td><td>110Hz</td><td>17</td><td>280Hz</td><td>1F</td><td>700Hz</td><td>27</td><td>1.8kHz</td><td>2F</td><td>4.5kHz</td><td>37</td><td>11kHz</td><td>3F</td><td>－</td></tr>
</table>
</td></tr>
</table>

Selection of quality factor（Q）

Default = 4h

<table>
<tr><th>Select Address</th><th>Operational explanation</th></tr>
<tr><td>bit [3:0]
It sets to every band</td><td>
<table>
<tr><th>Command</th><th>Quality factor</th><th>Command</th><th>Quality factor</th></tr>
<tr><td>0</td><td>0.33</td><td>8</td><td>2.2</td></tr>
<tr><td>1</td><td>0.43</td><td>9</td><td>2.7</td></tr>
<tr><td>2</td><td>0.56</td><td>A</td><td>3.3</td></tr>
<tr><td>3</td><td>0.75</td><td>B</td><td>3.9</td></tr>
<tr><td>4</td><td>1.0</td><td>C</td><td>4.7</td></tr>
<tr><td>5</td><td>1.2</td><td>D</td><td>5.6</td></tr>
<tr><td>6</td><td>1.5</td><td>E</td><td>6.8</td></tr>
<tr><td>7</td><td>1.8</td><td>F</td><td>8.2</td></tr>
</table>
</td></tr>
</table>

Selection of Gain

Default = 40h

<table>
<tr><th>Select Address</th><th>Operational explanation</th></tr>
<tr><td>bit [6:0]
It sets to every band</td><td>
<table>
<tr><th>Command</th><th>Gain</th></tr>
<tr><td>1C</td><td>−18dB</td></tr>
<tr><td>⋮</td><td>⋮</td></tr>
<tr><td>3E</td><td>−1dB</td></tr>
<tr><td>3F</td><td>−0.5dB</td></tr>
<tr><td>40</td><td>0dB</td></tr>
<tr><td>41</td><td>+0.5dB</td></tr>
<tr><td>42</td><td>+1dB</td></tr>
<tr><td>⋮</td><td>⋮</td></tr>
<tr><td>64</td><td>+18dB</td></tr>
</table>
</td></tr>
</table>

If the coefficient of b0, b1, b2, a1, and a2 exceeds ±4, it may not operate normally.

The Select Address of each band is shown in the table below:

<table>
<tr><th></th><th>Band1</th><th>Band2</th><th>Band3</th><th>Band4</th><th>Band5</th><th>Band6</th><th>Band7</th></tr>
<tr><td>Selection of filter type bit [7:6]</td><td rowspan="2">&h50h</td><td rowspan="2">&h54h</td><td rowspan="2">&h58h</td><td rowspan="2">&h5Ch</td><td rowspan="2">&h60h</td><td rowspan="2">&h64h</td><td rowspan="2">&h68h</td></tr>
<tr><td>Setting of the Start of transmitting to coefficient RAM bit [0]</td></tr>
<tr><td>F（frequency）selection bit [5:0]</td><td>&h51h</td><td>&h55h</td><td>&h59h</td><td>&h5Dh</td><td>&h61h</td><td>&h65h</td><td>&h69h</td></tr>
<tr><td>Q（Quality Factor） selection bit [3:0]</td><td>&h52h</td><td>&h56h</td><td>&h5Ah</td><td>&h5Eh</td><td>&h62h</td><td>&h66h</td><td>&h6Ah</td></tr>
<tr><td>Gain selection bit [6:0]</td><td>&h53h</td><td>&h57h</td><td>&h5Bh</td><td>&h5Fh</td><td>&h63h</td><td>&h67h</td><td>&h6Bh</td></tr>
</table>

4-15. Main output EVR （Electronic volume）

Volume is from+24dB to -103dB, and can be selected by the step of 0.5dB.
At the time of switching of Volume, smooth transition is performed. The smooth transition time takes about 22ms in the case of transiting from 0dB. (Fixed)

Setting of Volume

Default = FFh

<table>
<tr><th>Select Address</th><th>Operational explanation</th></tr>
<tr><td>&h26 [7 : 0]</td><td>
<table>
<tr><th>Command</th><th>Gain</th></tr>
<tr><td>00</td><td>+24dB</td></tr>
<tr><td>01</td><td>+23.5dB</td></tr>
<tr><td>⋮</td><td>⋮</td></tr>
<tr><td>30</td><td>0dB</td></tr>
<tr><td>31</td><td>−0.5dB</td></tr>
<tr><td>32</td><td>−1dB</td></tr>
<tr><td>⋮</td><td>⋮</td></tr>
<tr><td>FE</td><td>−103dB</td></tr>
<tr><td>FF</td><td>−∞</td></tr>
</table>
</td></tr>
</table>

4-16. Main output balance

Balance can be attenuated, by the step width of 1dB, from the Volume setting value. At the time of switching, smooth transition is performed. At the time of switching of Balance, smooth transition is performed. The smooth transition time takes about 22ms. (Fixed)

Setting of L/R Balance

Default = 80h

<table>
<tr><th>Select Address</th><th>Operational explanation</th></tr>
<tr><td>&h27 [7 : 0]</td><td>
<table>
<tr><th>Command</th><th>Lch</th><th>Rch</th></tr>
<tr><td>00</td><td>0dB</td><td>−∞</td></tr>
<tr><td>01</td><td>0dB</td><td>−126dB</td></tr>
<tr><td>⋮</td><td>⋮</td><td>⋮</td></tr>
<tr><td>7E</td><td>0dB</td><td>−1dB</td></tr>
<tr><td>7F</td><td>0dB</td><td>0dB</td></tr>
<tr><td>80</td><td>0dB</td><td>0dB</td></tr>
<tr><td>81</td><td>−1dB</td><td>0dB</td></tr>
<tr><td>⋮</td><td>⋮</td><td>⋮</td></tr>
<tr><td>FE</td><td>−126dB</td><td>0dB</td></tr>
<tr><td>FF</td><td>−∞</td><td>0dB</td></tr>
</table>
</td></tr>
</table>

4-17. Main output postscaler

It performs the level adjustment when the data calculated in the 32-bit-width DSP is outputted in the form of 24bitwidth.

Adjustable range is from +24dB to -103dB and can be set by the step of 0.5dB.

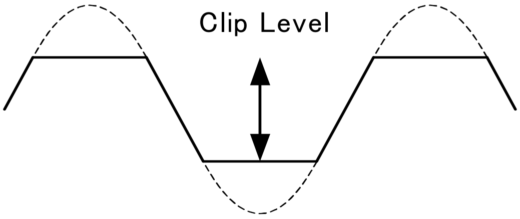
There is no smooth transition function in Postscaler.

Default = 30h

<table>
<tr><th>Select Address</th><th>Operational explanation</th></tr>
<tr><td>&h28 [7 : 0]</td><td>
<table>
<tr><th>Command</th><th>Gain</th></tr>
<tr><td>00</td><td>+24dB</td></tr>
<tr><td>01</td><td>+23.5dB</td></tr>
<tr><td>⋮</td><td>⋮</td></tr>
<tr><td>30</td><td>0dB</td></tr>
<tr><td>31</td><td>−0.5dB</td></tr>
<tr><td>32</td><td>−1dB</td></tr>
<tr><td>⋮</td><td>⋮</td></tr>
<tr><td>FE</td><td>−103dB</td></tr>
<tr><td>FF</td><td>−∞</td></tr>
</table>
</td></tr>
</table>

4-18. Main output clipper

When measuring the rated output (practical maximum output), it is measured where the total distortion rate （THD+N） is 10%. Clipping with any output amplitude is possible by using of clipper function, for example, the rated output of 10W or 5W can be obtained by using an amplifier with 15W output.



Please set the &h27[7] at “H” when using of clipper function.

Default = 0

Select Address	Value	Operational explanation
&h29 [7]	0	Not using clipper function
	1	Using clipper function

Clip level is set in the form of higher-order 8 bit&h2A[7:0] and lower-order 8 bit&h2B[7:0].

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	← Maximum value
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	← Minimum value
0	clip_level[15:0]																0	0	0	0	0	0	0	← A positive clip level
1	~clip_level[15:0]																1	1	1	1	1	1	1	← A negative clip level

The clip level becomes narrow if the setting value is reduced.

Negative clip level is set in such a way that it is the inversion data of positive clip level.

4-19. Selection of sub input data

Selection of Sub input (Sub woofer processing etc.).

The Sub woofer output interlocked with P^2Bass’s gain setting is possible by inputting the data that after P^2Bass processing.

In addition, in BU9409FV, the data can be inputted from SP conversion2.

Default = 0

Select Address	Value	Operational explanation
&h2F [1:0]	0	Inputting of data that are after scaler 1
	1	Inputting of data that are after P^2Bass processing
	2	Inputting of data from SP conversion2

4-20. Sub output channel mixer

Mixing setting of sound of the left channel and the right channel of the digital signal for sub output which is input into sound DSP is done. The monaural conversion of the stereo signal is done here.

The data which is input into Lch of Sub output signal processing is mixed.

Default = 0

Select Address	Value	Operating explanation
&h22 [3 ： 2]	0	Inputting the Lch data
	1	Inputting the data of （Lch + Rch） / 2
	2	Inputting the data of （Lch + Rch） / 2
	3	Inputting the Rch data

The data which is input into Rch of Sub output signal processing is mixed.

Default = 0

Select Address	Value	Operating explanation
&h22 [1 ： 0]	0	Inputting the Rch data
	1	Inputting the data of （Lch + Rch） / 2
	2	Inputting the data of （Lch + Rch） / 2
	3	Inputting the Lch data

4-21. LPF for sub woofer output

It is the crossover filter (LPF) for sub woofer output.
LPF function ON/OFF.

Default = 0

Select Address	Value	Operating explanation
&h7A [7]	0	LPF function is not used
	1	LPF function is used

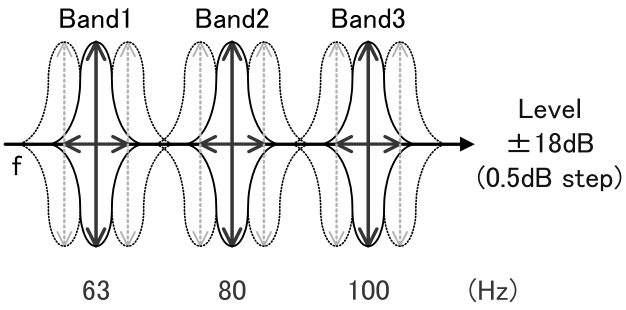
Setting of the cut off frequency (Fc) of LPF

Default = 0h

<table>
<tr><th>Select Address</th><th>Operating explanation</th></tr>
<tr><td>&h7A [6 ： 4]</td><td>
<table>
<tr><th>Command</th><th>Fc</th><th>Command</th><th>Fc</th></tr>
<tr><td>0</td><td>60Hz</td><td>4</td><td>160Hz</td></tr>
<tr><td>1</td><td>80Hz</td><td>5</td><td>200Hz</td></tr>
<tr><td>2</td><td>100Hz</td><td>6</td><td>240Hz</td></tr>
<tr><td>3</td><td>120Hz</td><td>7</td><td>280Hz</td></tr>
</table>
</td></tr>
</table>

4-22. Sub output 3 band Parametric Equalizer

The peaking filter or the low shelf filter or the high shelf filter can be used by the parametric equalizer of 3 bands. By the fact that F, Q and Gain are selected, it converts the setting to the coefficient (b0, b1, b2, a1 and a2) of the digital filter inside IC, and transfers it to the coefficient RAM. There is no smooth transition function.



Selection of filter type

Default = 0

Select Address	Value	Operating explanation
bit[7:6] It sets to all band	0	Peaking filter
	1	Low shelf filter
	2	High shelf filter

Transfer start setting to coefficient RAM.

It transfers directly to coefficient RAM.

Default = 0

Select Address	Value	Operating explanation
bit [0] It sets to all band	0	Coefficient transmission stop
	1	Coefficient transmission start

Selection of frequency (F_0)

Default = 0Eh

<table>
<tr><th>Select Address</th><th>Operating explanation</th></tr>
<tr><td>bit [5:0]
It sets to all band</td><td>
<table>
<tr><th>Command</th><th>Frequency</th><th>Command</th><th>Frequency</th><th>Command</th><th>Frequency</th><th>Command</th><th>Frequency</th><th>Command</th><th>Frequency</th><th>Command</th><th>Frequency</th><th>Command</th><th>Frequency</th><th>Command</th><th>Frequency</th></tr>
<tr><td>00</td><td>20Hz</td><td>08</td><td>50Hz</td><td>10</td><td>125Hz</td><td>18</td><td>315Hz</td><td>20</td><td>800Hz</td><td>28</td><td>2kHz</td><td>30</td><td>5kHz</td><td>38</td><td>12.5kHz</td></tr>
<tr><td>01</td><td>22Hz</td><td>09</td><td>56Hz</td><td>11</td><td>140Hz</td><td>19</td><td>350Hz</td><td>21</td><td>900Hz</td><td>29</td><td>2.2kHz</td><td>31</td><td>5.6kHz</td><td>39</td><td>14kHz</td></tr>
<tr><td>02</td><td>25Hz</td><td>0A</td><td>63Hz</td><td>12</td><td>160Hz</td><td>1A</td><td>400Hz</td><td>22</td><td>1kHz</td><td>2A</td><td>2.5kHz</td><td>32</td><td>6.3kHz</td><td>3A</td><td>16kHz</td></tr>
<tr><td>03</td><td>28Hz</td><td>0B</td><td>70Hz</td><td>13</td><td>180Hz</td><td>1B</td><td>450Hz</td><td>23</td><td>1.1kHz</td><td>2B</td><td>2.8kHz</td><td>33</td><td>7kHz</td><td>3B</td><td>18kHz</td></tr>
<tr><td>04</td><td>32Hz</td><td>0C</td><td>80Hz</td><td>14</td><td>200Hz</td><td>1C</td><td>500Hz</td><td>24</td><td>1.25kHz</td><td>2C</td><td>3.15kHz</td><td>34</td><td>8kHz</td><td>3C</td><td>20kHz</td></tr>
<tr><td>05</td><td>35Hz</td><td>0D</td><td>90Hz</td><td>15</td><td>220Hz</td><td>1D</td><td>560Hz</td><td>25</td><td>1.4kHz</td><td>2D</td><td>3.5kHz</td><td>35</td><td>9kHz</td><td>3D</td><td>－</td></tr>
<tr><td>06</td><td>40Hz</td><td>0E</td><td>100Hz</td><td>16</td><td>250Hz</td><td>1E</td><td>630Hz</td><td>26</td><td>1.6kHz</td><td>2E</td><td>4kHz</td><td>36</td><td>10kHz</td><td>3E</td><td>－</td></tr>
<tr><td>07</td><td>45Hz</td><td>0F</td><td>110Hz</td><td>17</td><td>280Hz</td><td>1F</td><td>700Hz</td><td>27</td><td>1.8kHz</td><td>2F</td><td>4.5kHz</td><td>37</td><td>11kHz</td><td>3F</td><td>－</td></tr>
</table>
</td></tr>
</table>

Selection of quality factor (Q)

Default = 4h

<table>
<tr><th>Select Address</th><th>Operating explanation</th></tr>
<tr><td>bit [3:0]
It sets to all band</td><td>
<table>
<tr><th>Command</th><th>Quality factor</th><th>Command</th><th>Quality factor</th></tr>
<tr><td>0</td><td>0.33</td><td>8</td><td>2.2</td></tr>
<tr><td>1</td><td>0.43</td><td>9</td><td>2.7</td></tr>
<tr><td>2</td><td>0.56</td><td>A</td><td>3.3</td></tr>
<tr><td>3</td><td>0.75</td><td>B</td><td>3.9</td></tr>
<tr><td>4</td><td>1.0</td><td>C</td><td>4.7</td></tr>
<tr><td>5</td><td>1.2</td><td>D</td><td>5.6</td></tr>
<tr><td>6</td><td>1.5</td><td>E</td><td>6.8</td></tr>
<tr><td>7</td><td>1.8</td><td>F</td><td>8.2</td></tr>
</table>
</td></tr>
</table>

Selection of Gain

Default = 40h

<table>
<tr><th>Select Address</th><th>Operating explanation</th></tr>
<tr><td>bit [6:0]
It sets to all band</td><td>
<table>
<tr><th>Command</th><th>Gain</th></tr>
<tr><td>1C</td><td>−18dB</td></tr>
<tr><td>⋮</td><td>⋮</td></tr>
<tr><td>3E</td><td>−1dB</td></tr>
<tr><td>3F</td><td>−0.5dB</td></tr>
<tr><td>40</td><td>0dB</td></tr>
<tr><td>41</td><td>+0.5dB</td></tr>
<tr><td>42</td><td>+1dB</td></tr>
<tr><td>⋮</td><td>⋮</td></tr>
<tr><td>64</td><td>+18dB</td></tr>
</table>
</td></tr>
</table>

If the coefficient of b0, b1, b2, a1, and a2 exceeds ±4, it may not operate normally.

Select Address of every band is as in chart below

	Band1	Band2	Band3
Selection of filter type bit [7:6]	&h80h	&h84h	&h88h
Transfer start setting to coefficient RAM bit [0]			
F (frequency) selection bit [5:0]	&h81h	&h85h	&h89h
Q (quality factor) selection bit [3:0]	&h82h	&h86h	&h8Ah
Gain selection bit [6:0]	&h83h	&h87h	&h8Bh

4-23. Sub output EVR (electronic volume)

The volume for sub output can select with 0.5dB step from +24dB to -103dB.
When changing volume, smooth transition is done. Smooth transition duration is required approximately 22ms when it is from 0dB. (Fixed)

Volume setting

Default = FFh

<table>
<tr><th>Select Address</th><th>Operating explanation</th></tr>
<tr><td>&h2C [7 : 0]</td><td>
<table>
<tr><th>Command</th><th>Gain</th></tr>
<tr><td>00</td><td>+24dB</td></tr>
<tr><td>01</td><td>+23.5dB</td></tr>
<tr><td>⋮</td><td>⋮</td></tr>
<tr><td>30</td><td>0dB</td></tr>
<tr><td>31</td><td>−0.5dB</td></tr>
<tr><td>32</td><td>−1dB</td></tr>
<tr><td>⋮</td><td>⋮</td></tr>
<tr><td>FE</td><td>−103dB</td></tr>
<tr><td>FF</td><td>−∞</td></tr>
</table>
</td></tr>
</table>

4-24. Sub output balance

As for sub output balance, it is possible to be attenuated at 1dB step width from volume setting value. When changing, smooth transition is done.
When changing balance, smooth transition is done. Smooth transition duration is required approximately 22ms. (Fixed)
L/R Balance setting

Default = 80h

<table>
<tr><th>Select Address</th><th>Operating explanation</th></tr>
<tr><td>&h2D [7 : 0]</td><td>
<table>
<tr><th>Command</th><th>Lch</th><th>Rch</th></tr>
<tr><td>00</td><td>0dB</td><td>−∞</td></tr>
<tr><td>01</td><td>0dB</td><td>−126dB</td></tr>
<tr><td>⋮</td><td>⋮</td><td>⋮</td></tr>
<tr><td>7E</td><td>0dB</td><td>−1dB</td></tr>
<tr><td>7F</td><td>0dB</td><td>0dB</td></tr>
<tr><td>80</td><td>0dB</td><td>0dB</td></tr>
<tr><td>81</td><td>−1dB</td><td>0dB</td></tr>
<tr><td>⋮</td><td>⋮</td><td>⋮</td></tr>
<tr><td>FE</td><td>−126dB</td><td>0dB</td></tr>
<tr><td>FF</td><td>−∞</td><td>0dB</td></tr>
</table>
</td></tr>
</table>

4-25. Sub output post scaler

The occasion when the data which is calculated with DSP of 32bit width is output at 24bit width, level adjustment is done.

The adjustment range can be set with 0.5dB step from +24dB to -103dB.

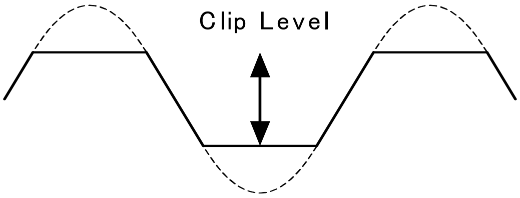
There is no smooth transition function in the sub output post scaler.

Default = 30h

<table>
<tr><th>Select Address</th><th>Operating explanation</th></tr>
<tr><td>&h2E [7 : 0]</td><td>
<table>
<tr><th>Command</th><th>Gain</th></tr>
<tr><td>00</td><td>+24dB</td></tr>
<tr><td>01</td><td>+23.5dB</td></tr>
<tr><td>⋮</td><td>⋮</td></tr>
<tr><td>30</td><td>0dB</td></tr>
<tr><td>31</td><td>−0.5dB</td></tr>
<tr><td>32</td><td>−1dB</td></tr>
<tr><td>⋮</td><td>⋮</td></tr>
<tr><td>FE</td><td>−103dB</td></tr>
<tr><td>FF</td><td>−∞</td></tr>
</table>
</td></tr>
</table>

4-26. Sub output clipper

The case when rated output (practical maximum output) of the television is measured, total harmonic distortion + noise (THD+N) measures at the place of 10%. It can obtain the rated output of 10W and 5W for example making use of the amplifier of 15W output, because it is possible to clip with optional output amplitude by using the clipper function.



Please designate &h30 [7] as" H when using sub output clipper function.

Default = 0

Select Address	Value	Operating explanation
&h30 [7]	0	Clipper function is not used
	1	Clipper function is used

As for clip level, it sets with superior 8 bits &h31 [7: 0] and subordinate 8 bits &h32 [7: 0].

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	◄– Maximum value
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	◄– Minimum value
0	clip_level[15:0]																0	0	0	0	0	0	0	◄– A positive clip level
1	~clip_level[15:0]																1	1	1	1	1	1	1	◄– A negative clip level

When setting value is made small, clip level becomes narrow.

As for negative clip level, the reversal data of positive clip level is set.

4-27. Direct setting five coefficient of b0, b1, b2, a1 and a2 of Bi-quad Filter

7 bands Parametric Equalizer of main output and of 3 bands Parametric Equalizer of sub output have used the secondary IIR type digital filter (Bi-quad Filter).

It is possible to set five coefficient 24 bit of b0, b1, b2, a1 and a2 of Bi-quad Filter (-4〜+4) directly from an external.

When this function is used, it can do the filter type and frequency setting, Q value (quality factor) setting and gain setting other than Peaking, Low-Shelf and High-Shelf unrestrictedly.

(Note) five coefficient have the necessity to make below the ±4, there is no read-out function of setting value and an automatic renewal function of coefficient RAM.

Register for the coefficient transfer of 24bit

Before transferring into coefficient RAM in a lumping, the data is housed in the register for coefficient transfer from the micro-computer.

Default = 00h

Select Address	Operating explanation
&h8D [7:0]	bit[23:16] which transfers 24 bit coefficient
&h8E [7:0]	bit[15:8] which transfers 24 bit coefficient
&h8F [7:0]	bit[7:0] which transfers 24 bit coefficient

It starts to transmit the coefficient of 24bit into coefficient RAM

Default = 0

Select Address	Value	Operating explanation
&h8C [7]	0	Coefficient transmission stop
	1	Coefficient transmission start

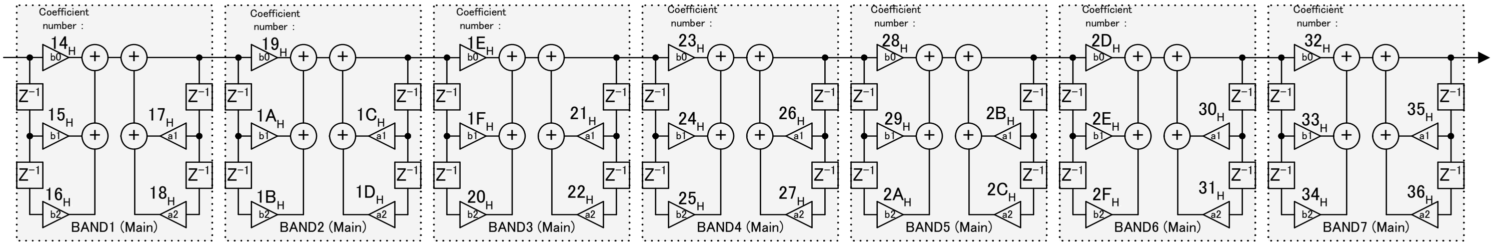
Coefficient number appointment of coefficient RAM

Default = 00h

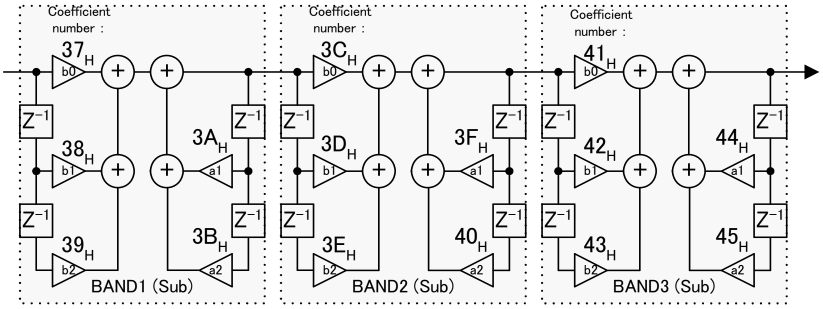
Select Address	Operating explanation
&h8C [6:0]	Coefficient number appointment of coefficient RAM

Appointment of coefficient number other than 14H↔45H is prohibition

Main output 7Band Parametric EQ


Coefficient number :
14H b0
15H b1
16H b2
17H a1
18H a2
BAND1 (Main)
19H b0
1AH b1
1BH b2
1CH a1
1DH a2
BAND2 (Main)
1EH b0
1FH b1
20H b2
21H a1
22H a2
BAND3 (Main)
23H b0
24H b1
25H b2
26H a1
27H a2
BAND4 (Main)
28H b0
29H b1
2AH b2
2BH a1
2CH a2
BAND5 (Main)
2DH b0
2EH b1
2FH b2
30H a1
31H a2
BAND6 (Main)
32H b0
33H b1
34H b2
35H a1
36H a2
BAND7 (Main)
Z-1
+

Sub output 3Band Parametric EQ


Coefficient number :
37H b0
38H b1
39H b2
3AH a1
3BH a2
BAND1 (Sub)
3CH b0
3DH b1
3EH b2
3FH a1
40H a2
BAND2 (Sub)
41H b0
42H b1
43H b2
44H a1
45H a2
BAND3 (Sub)
Z-1
+

4-28. About the automatic renewal of five coefficients of b0, b1, b2, a1 and a2 of Bi-quad Filter

BASS, MIDDLE, TREBLE, main output 7 bands Parametric Equalizer and sub output 3 band Parametric Equalizer have used coefficient RAM. As for this coefficient RAM, because direct access is not possible from the micro-computer, it cannot refresh the register efficiently.

There is an automatic renewal function of coefficient RAM in this DSP, the automatic write-in renewal of coefficient RAM is possible by using this function. However when 4-26 「the function of direct setting a coefficient RAM」 is utilized, it is not possible to utilize automatic write-in renewal.

Selection of using the automatic write-in renewal function

Default = 0

Select Address	Value	Operating explanation
&h6D [0]	0	Automatic write-in renewal function is used
	1	Automatic write-in renewal function is not used

The separate setting of Filter of automatic write-in renewal function

Default = 00h

Select Address	Filter	Operating explanation
&h6E [0]	BASS	0：Automatic renewal function OFF 1：Automatic renewal function ON
&h6E [1]	MIDDLE	0：Automatic renewal function OFF 1：Automatic renewal function ON
&h6E [2]	TREBLE	0：Automatic renewal function OFF 1：Automatic renewal function ON
&h6E [4]	Sub BAND1	0：Automatic renewal function OFF 1：Automatic renewal function ON
&h6E [5]	Sub BAND2	0：Automatic renewal function OFF 1：Automatic renewal function ON
&h6E [6]	Sub BAND3	0：Automatic renewal function OFF 1：Automatic renewal function ON
&h6F [0]	Main MAND1	0：Automatic renewal function OFF 1：Automatic renewal function ON
&h6F [1]	Main MAND2	0：Automatic renewal function OFF 1：Automatic renewal function ON
&h6F [2]	Main MAND3	0：Automatic renewal function OFF 1：Automatic renewal function ON
&h6F [3]	Main MAND4	0：Automatic renewal function OFF 1：Automatic renewal function ON
&h6F [4]	Main MAND5	0：Automatic renewal function OFF 1：Automatic renewal function ON
&h6F [5]	Main MAND6	0：Automatic renewal function OFF 1：Automatic renewal function ON
&h6F [6]	Main MAND7	0：Automatic renewal function OFF 1：Automatic renewal function ON

5. P-S conversion 1 ,P-S conversion 2

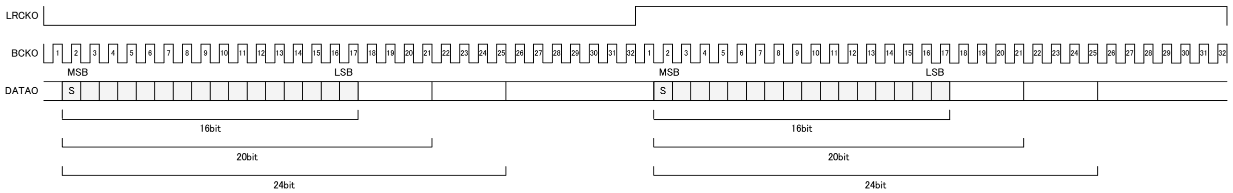
Two parallel serial conversion circuits are built in BU9409FV. (P-S conversion 1, P-S conversion 2)

P-S conversion 1 convert the Main output of DSP from SDATAO1, LRCKO, and BCKO (34,35,36pin) into three line serial data and output the data.

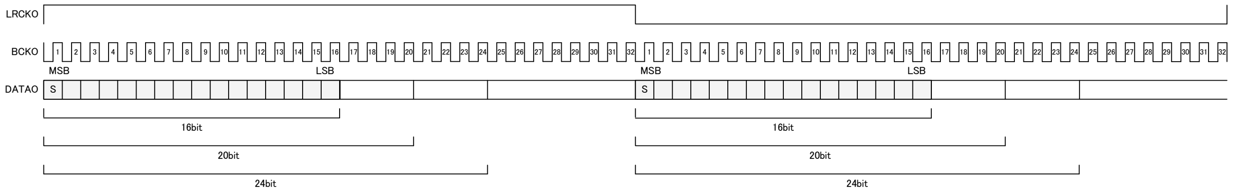
P-S conversion 2 convert the sub output of DSP from SDATAO1, LRCKO, and BCKO (33,35,36pin) into three line serial data and output the data.

Output format has the IIS mode, left-align mode, and right-align mode. 16 each bit, 20bit, and 24bit output can also be selected. The figure below shows the timing chart of each transmission mode.

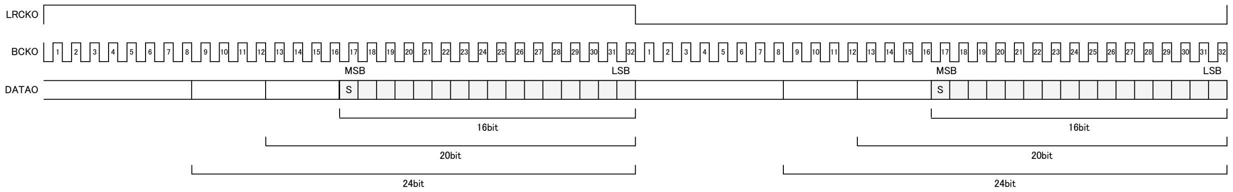
IIS mode


LRCKO
BCKO
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32
DATAO
MSB
LSB
S
16bit
20bit
24bit

left-align mode


LRCKO
BCKO
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32
DATAO
MSB
LSB
S
16bit
20bit
24bit

right-align mode


LRCKO
BCKO
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32
DATAO
MSB
LSB
S
16bit
20bit
24bit

5-1. Format setting of three line serial output

Default = 0

Select Address	Value	Operating Description
P-S conversion 1 &h0D [3 : 2] P-S conversion 2 & h0E [3 : 2]	0	IIS mode
	1	left-align mode
	2	right-align mode

5-2. Setting data bit width of three line serial output

Default = 0

Select Address	Value	Operating Description
P-S conversion 1 &h0D [1 : 0] P-S conversion 2 & h0E [1 : 0]	0	16 bit
	1	20 bit
	2	24 bit

6. Mute function by command

Mute function by command is provided in BU9409FV.
It's possible to mute DSP's main and sub digital output by setting to &hFD [4] = 1h and MUTEX_DAC terminal and a MUTEX_SP terminal both to L.

Setting the transition time of smooth mute
Mute the Main and Sub output of DSP.
Select the transition time of entering from 0dB to mute state.
Smooth transition time when releasing mute is about 22ms(fixed) .
Default = 0

Select Address	Value	Operating Description
&h10 [1 : 0]	0	Don't use mute function.
	1	10.8ms
	2	5.4ms
	3	2.7ms

7. Clock halt function of DSP part

Clock halt function of DSP part with terminal MUTEX_DAC and MUTEX_SP is provided in BU9409FV.

Clock halt function's setting
Default = 0

Select Address	Value	Operating Description
&hA9 [7]	0	Don't use the clock halt function
	1	Use the clock halt function

When setting on using the clock halt function, then set the MUTEX_DAC and MUTEX_SP terminal on L ,the clock of DSP part will be halted. If clock is halted, command can't be sent and received in a part of the block. If &hA9 [7] is input from MCLK into clock, command can be sent and received even on the clock halt condition.
When MUTEX_DAC or MUTEX_SP terminal is on H, the clock halt will be released.

Power consumption decreases in the clock halt condition.

8. Command sent after releasing reset

Please send the following command after releasing reset including power supply on.

0. Power supply turning on

↓

○ Please input the clock from the outside. When the clock is not input, reset can't normally be done.

↓

1. Reset release (RESETB="H")

↓

2. &hA0[7:0] = C2h ：Set PLLA.

↓

3. &hF3[5:0] = 10h ：Set the dividing frequency ratio of MCLK. Please do as follows to set a value by fs of MCLK.
（MCLK:512fs=10h、256fs=08h、128fs=04h）

↓

4. &hF5[3:0] = 1h：Set the dividing frequency ratio of PLL.

↓

5. &hF6[5:0] = 23h：Set the phase match of PLL.

↓

6. &hF1[4] = 0 ：Turn on the analog input.

↓

7. &h08[5:4] = 1h ：Select the system clock.

↓

8. &hA7[7:0] = F4h：Synchronous detection condition setting 1 for PLLA is initialized.

↓

9. &hA8[7:0] = 33h：Synchronous detection condition setting 2 for PLLA is initialized.

↓

10. &hA9[3:0] = 3h：Synchronous detection condition setting 3 for PLLA is initialized.

↓

11. &hA9[5:4] = 2h or 1h or 0h ：Set MCLK.
(Set in “2h”While MCLK is 512fs, set in “1h”While MCLK is 256fs, set in “0h”While MCLK is 128fs.)

↓

○ It is about 20ms weight until PLL is steady.

↓

10. &h01[5:4] = 0h ：Turn off the RAM Clear.

↓

11. Other register setting
&h26[7:0] = **h ：Release the mute of the Main output volume（30h=0dB）.
&h2C[7:0] = **h ：Release the mute of the Sub output volume（30h=0dB）.

9. About frequency setting such as tone control and parametric equalizer

Because the sampling rate converter is not built into BU9409FV, the calculation clock of DSP is changed according to the input sampling rate of I2S.

Because sampling rate describes the frequency on the assumption of 48kHz in this function specification, conversion is needed in case of sampling frequency of 44.1kHz and 32kHz.

Please refer to the table below for F0 setting of tone control (Bass, Middle, Treble) and parametric equalizer.

F_0 (fs=48kHz)

Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency
00	20Hz	08	50Hz	10	125Hz	18	315Hz	20	800Hz	28	2kHz	30	5kHz	38	12.5kHz
01	22Hz	09	56Hz	11	140Hz	19	350Hz	21	900Hz	29	2.2kHz	31	5.6kHz	39	14kHz
02	25Hz	0A	63Hz	12	160Hz	1A	400Hz	22	1kHz	2A	2.5kHz	32	6.3kHz	3A	16kHz
03	28Hz	0B	70Hz	13	180Hz	1B	450Hz	23	1.1kHz	2B	2.8kHz	33	7kHz	3B	18kHz
04	32Hz	0C	80Hz	14	200Hz	1C	500Hz	24	1.25kHz	2C	3.15kHz	34	8kHz	3C	20kHz
05	35Hz	0D	90Hz	15	220Hz	1D	560Hz	25	1.4kHz	2D	3.5kHz	35	9kHz	3D	－
06	40Hz	0E	100Hz	16	250Hz	1E	630Hz	26	1.6kHz	2E	4kHz	36	10kHz	3E	－
07	45Hz	0F	110Hz	17	280Hz	1F	700Hz	27	1.8kHz	2F	4.5kHz	37	11kHz	3F	－

F_0 (fs=44.1kHz)

Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency
00	18Hz	08	46Hz	10	115Hz	18	289Hz	20	735Hz	28	1.84kHz	30	4.59kHz	38	11.5kHz
01	20Hz	09	51Hz	11	129Hz	19	322Hz	21	827Hz	29	2.02kHz	31	5.15kHz	39	12.9kHz
02	23Hz	0A	58Hz	12	147Hz	1A	368Hz	22	919Hz	2A	2.3kHz	32	5.79kHz	3A	14.7kHz
03	26Hz	0B	64Hz	13	165Hz	1B	413Hz	23	1.01kHz	2B	2.57kHz	33	6.43kHz	3B	16.5kHz
04	29Hz	0C	74Hz	14	184Hz	1C	459Hz	24	1.15kHz	2C	2.89kHz	34	7.35kHz	3C	18.4kHz
05	32Hz	0D	83Hz	15	202Hz	1D	515Hz	25	1.29kHz	2D	3.22kHz	35	8.27kHz	3D	－
06	37Hz	0E	92Hz	16	230Hz	1E	579Hz	26	1.47kHz	2E	3.68kHz	36	9.19kHz	3E	－
07	41Hz	0F	101Hz	17	257Hz	1F	643Hz	27	1.65kHz	2F	4.13kHz	37	10.1kHz	3F	－

F_0 (fs=32kHz)

Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency
00	13Hz	08	33Hz	10	83Hz	18	210Hz	20	533Hz	28	1.33kHz	30	3.33kHz	38	8.33kHz
01	15Hz	09	37Hz	11	93Hz	19	233Hz	21	600Hz	29	1.47kHz	31	3.73kHz	39	9.33kHz
02	17Hz	0A	42Hz	12	107Hz	1A	267Hz	22	667Hz	2A	1.67kHz	32	4.2kHz	3A	10.7kHz
03	19Hz	0B	47Hz	13	120Hz	1B	300Hz	23	733Hz	2B	1.87kHz	33	4.67kHz	3B	12kHz
04	21Hz	0C	53Hz	14	133Hz	1C	333Hz	24	833Hz	2C	2.1kHz	34	5.33kHz	3C	13.3kHz
05	23Hz	0D	60Hz	15	147Hz	1D	373Hz	25	933Hz	2D	2.33kHz	35	6kHz	3D	－
06	27Hz	0E	67Hz	16	167Hz	1E	420Hz	26	1.07kHz	2E	2.67kHz	36	6.67kHz	3E	－
07	30Hz	0F	73Hz	17	187Hz	1F	467Hz	27	1.2kHz	2F	3kHz	37	7.33kHz	3F	－

10. About a setup of a clock, and the input of a command

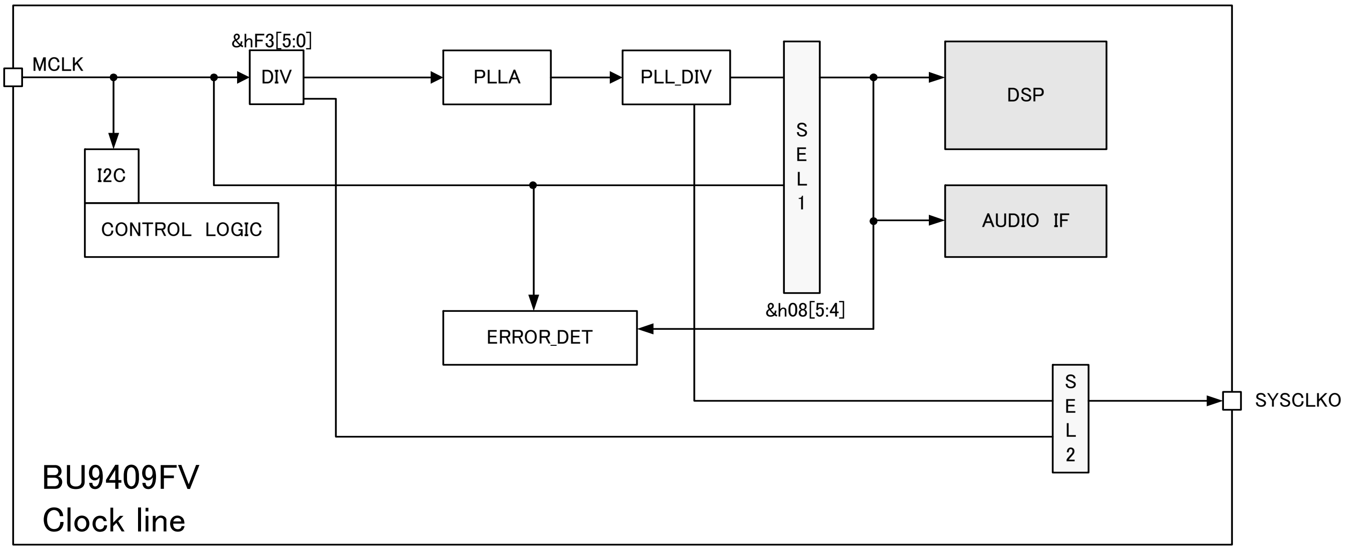
The input of MCLK is decided by combination of three kinds of sampling rates (fs=32kHz, 44.1kHz, 48kHz), and three kinds of magnifications (128 times, 256 times, 512 times).

	Sampling rate(fs)		
MCLK clock	32kHz	44.1kHz	48kHz
128fs	4.096MHz	5.6448MHz	6.144MHz
256fs	8.192MHz	11.2896MHz	12.288MHz
512fs	16.384MHz	22.5792MHz	24.576MHz

In order that PLL may multiple the dividing output of MCLK, the dividing ratio of MCLK is not concerned with a sampling rate like explanation in Chapter 8, but is decided by the magnification of MCLK.

MCLK clock	&hF3[5:0]
128fs	04h
256fs	08h
512fs	10h

Therefore, as for the case of the input of 4.096MHz-6.144NHz, and a 256fs setup, in the input frequency of MCLK, in a 128fs setup, a 16.384MHz - 24.576MHz input serves as a range which can be operated in a 8.192MHz - 12.288MHz input and a 512fs setup.



The clock system figure of BU9409FV is as mentioned above.
(1) In the case of &h08 [5:4] =1, the block of an above figure light blue operates with a PLL clock.
(2) In the case of &h08 [5:4] =0, the block of an above figure light blue operates by MCLK.

Be careful of the following points at the time of a command input.
In (1), a part of blocks containing DSP are operating with the clock of PLL.
Therefore, even if MCLK is the range which is 4.096MHz - 24.576MHz, when a setup of PLL and the setup of &hF3 are not performed correctly, a command may not be received other than command &h08 of a system control system, &hA0-&hA9, &hB0-&hBA, &hD0, &hF0 - &hFA.
In (2), the whole operates with the clock of MCLK.
If MCLK is the range which is 4.096MHz - 24.576MHz, all blocks will receive an I2C command.

11. About the change of a sampling rate

11-1. When a sampling rate change can predict beforehand

When the change of a sampling rate can predict beforehand, please switch a sampling rate in the following procedures.

1. The mute of the DAC is carried out (MUTEX_SP and MUTEX_DAC are set to L and it is a mute about BD5446.).
↓
2. EVR is set as -infinity.
↓
3. Set prescaler as -infinity.
↓
4. A RAM clearance is carried out by setting it as &h01= C0h.
↓
5. &h08[5:4] = by setting it as 0, the whole clock is switched to MCLK.
↓
6. Switch a sampling rate.
↓
7. Switch to a PLL clock after stabilizing the input of MCLK by setting it as more 20 msec WAIT and &h08 [5:4] =1h, since it is PLL stability.
↓
8. A RAM clearance is canceled by setting it as &h01 = 0.
↓
9. Since the coefficient is cleared, please set up DSP.
↓
10. Please cancel a DAC mute.

11-2. When a sampling rate change cannot predict beforehand

Please do the following work, when the change of a sampling rate cannot predict beforehand, and having switched is detected.

1. The mute of the DAC is carried out (MUTEX_SP and MUTEX_DAC are set to L and it is a mute about BD5446.).
↓
○When the input of MCLK has stopped, please do not input a command until MCLK is inputted again.
Please perform the following setup, after MCLK is inputted on the frequency of specification within the limits.
↓
２. It is set as &h08[5:4] = 0 and the whole clock is switched to MCLK.
↓
３. Switch to a PLL clock after stabilizing the input of MCLK by setting it as more 20 msec WAIT and &h08 [5:4] =1h, since it is PLL stability.
↓
４. A RAM clearance is carried out by setting it as &h01= C0h.
↓
５. EVR is set as -infinity.
↓
６. Prescaler is set as -infinity.
↓
７. A RAM clearance is canceled by setting it as &h01 = 0.
↓
８. Since the coefficient is cleared, please set up DSP.
↓
９. Please cancel a DAC mute.

11-3. When the frequency more than a stop or the specification range does not enter [MCLK] at the time of a sampling rate change

When switching a sampling rate, the clock of the frequency more than the specification range does not go into MCLK, but when input data is 0, it can return with the following procedures.

1. Carry out the mute of the DAC (MUTEX_SP and MUTEX_DAC are set to L and it is a mute about BD5446.)

↓

○When the input of MCLK has stopped, please do not input a command until MCLK is inputted again.
Please perform the following setup, after MCLK is inputted on the frequency of specification within the limits.

↓

2. It is 20ms or more WAIT because of PLL stability.

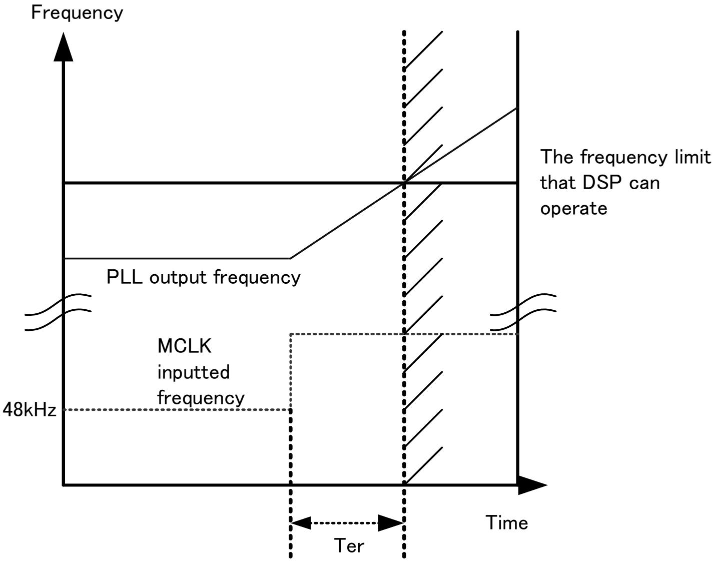
↓

○When the section where MCLK stopped or the relation with I2S input had collapsed in the midst of the midst of soft transition and transmission of a coefficient exists, the coefficient may not be able to be transmitted well. When soft transition and a coefficient are transmitting, please perform a setup from 11-2 4.
Please perform the following setup, when you are not the midst of soft transition or transmission of a coefficient.

↓

3. Please cancel a DAC mute.

12. When the clock which exceeded the specification range from MCLK is inputted


Frequency
The frequency limit that DSP can operate
PLL output frequency
MCLK inputted frequency
48kHz
Time
Ter

When the frequency beyond fs=48kHz is inputted from MCLK in the state where it was set as &h08 [5:4] =1, since PLL follows inputted MCLK, as shown in the right figure, when it exceeds Time Ter, it will exceed the frequency in which DSP can operate.

In this case, an allophone may carry out irrespective of the existence of data.

When you change into such a state, please carry out the mute of the DAC immediately, apply reset (RESETB=L), and do the work after reset release of Chapter 8.

The time of Ter serves as about 70 usec.

13. Audio Interface Signal Specification

○Electric specification and timing of MCK, BCK, LRCK, and SDATA1 and SDATA2

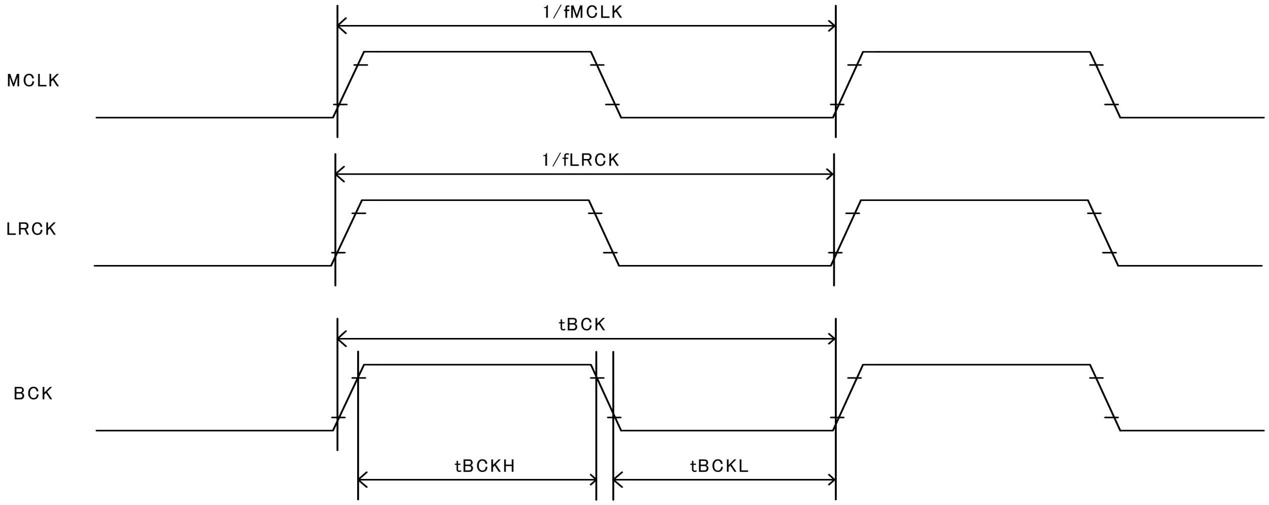

1/fMCLK
MCLK
1/fLRCK
LRCK
tBCK
BCK
tBCKH
tBCKL

Fig 1-2 Clock timing

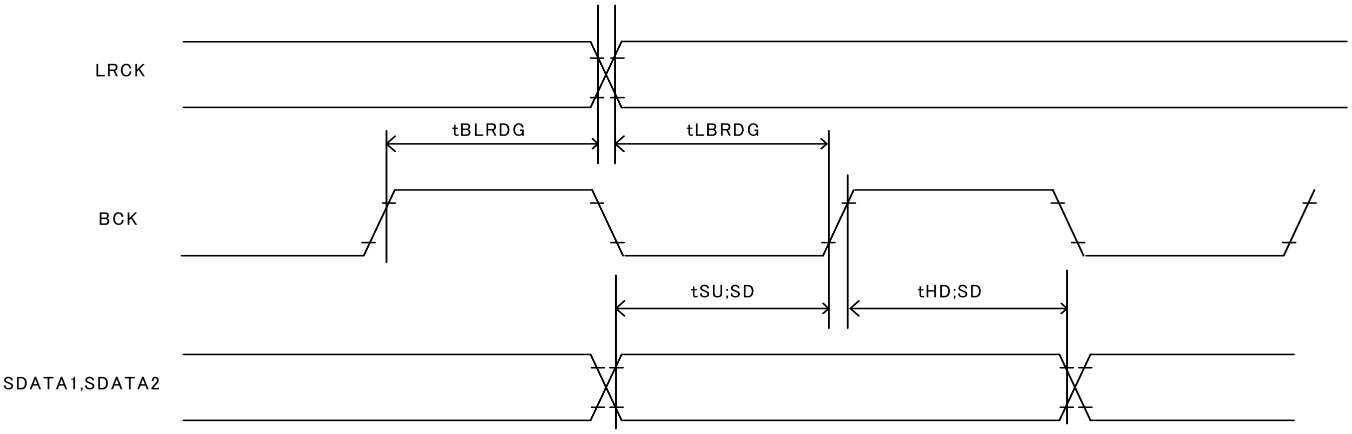

LRCK
tBLRDG
tLBRDG
BCK
tSU;SD
tHD;SD
SDATA1,SDATA2

Fig 1-3 Audio interface timing

Parameter			Sign			Unit
				Min.	Max.	
1	MCK	Frequency	fSCLK	4.096	24.576	MHz
2		DUTY	dSCLK	40	60	%
3	LRCK	Frequency	fLRCK	32	48	kHz
4		DUTY	dLRCK	40	60	%
5	BCK	Cycle	tBCK	325	—	ns
6		H width	tBCKH	130	—	ns
7		L width	tBCKL	130	—	ns
8	It is time to the edge of LRCK from a BCK rising edge.*1		tBLRDG	20	—	ns
9	It is time to a BCK rising edge from the edge of LRCK.*1		tLBRDG	20	-	ns
10	Setup time of SDATA		tSU;SD	20	-	ns
11	Hold time of SDATA		tHD;SD	20	—	ns

*1 This standard value has specified that the edge of LRCK and the rising edge of BCK do not overlap.

14. Notes at the Time of Reset

Since the state of IC is not decided, please make it into RESETX=L at the time of a power supply injection, and surely apply reset.

Reset of BU9409FV is performing noise removal by MCLK.

Therefore, in order to apply reset, a MCLK clock pulse is required of the state of RESETX=L more than 10 times.

The power-on reset after a power supply injection, and when you usually apply reset at the time of operation, please be sure to carry out in the state where the clock is inputted, from MCLK.

15. Read-out of Soft Transition Flag

It is set to &hF4[0] =H when BASS, MIDDLE, TREBLE or P2Bass, and P2Treble are soft transiting.

It is possible to check whether soft transition is completed by reading &hF4 [0]

Soft transition will be completed if the read-out result of &hF4 [0] is L.

●Cautions

(1) ABSOLUTE MAXIMUM RATINGS

Permanent device damage may occur and break mode (open or short) can not be specified if power supply, operating temperature, and those of ABSOLUTE MAXIMUM RATINGS are exceeded. If such a special condition is expected, components for safety such as fuse must be used.

(2)Regarding of SCLI and SDAI terminals

SCLI and the SDAI terminal do not support 5 V-tolerant. Please use it within absolute maximum rating (4.5V).

(3) Power Supply

Power and Ground line must be designed as low impedance in the PCB. Print patterns if digital power supply and analog power supply must be separated even if these have same voltage level. Print patterns for ground must be designed as same as power supply. These considerations avoid analog circuits from the digital circuit noise. All pair of power supply and ground must have their own de-coupling capacitor. Those capacitor should be checked about their specification, etc. (nominal electrolytic capacitor degrades its capacity at low temperature) and choose the constant of an electrolytic capacitor.

(4) Functionality in the strong electro-magnetic field

Malfunction may occur if in the strong electro-magnetic field.

(5) Input terminals

All LSI contain parasitic components. Some are junctions which normally reverse bias. When these junctions forward bias, currents flows on unwanted path, malfunction or device damage may occur. To prevent this, all input terminal voltage must be between ground and power supply, or in the range of guaranteed value in the Electrical characteristics. And no voltage should be supplied to all input terminal when power is not supplied.

●Ordering Information

B U 9 4 0 9 F V E2

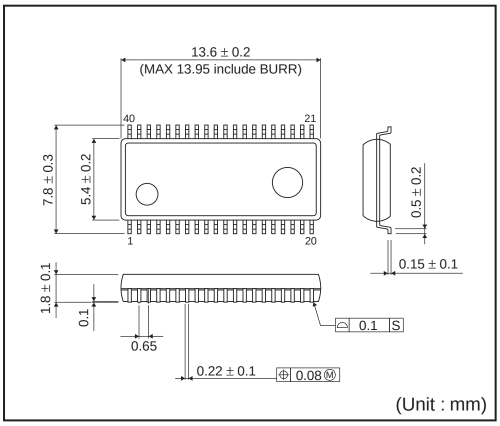
Part Number

Package
FV: SSO-B40

Packaging and forming specification
E2: Embossed tape and reel

●Physical Dimension Tape and Reel Information

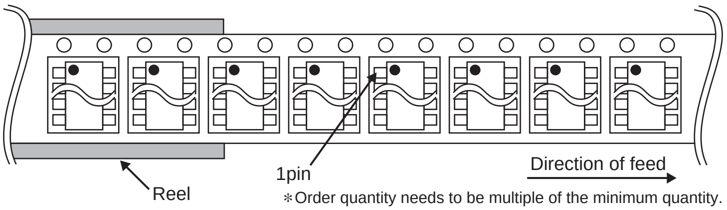
SSOP-B40


13.6 ± 0.2
(MAX 13.95 include BURR)
40
21
1
20
7.8 ± 0.3
5.4 ± 0.2
0.5 ± 0.2
0.15 ± 0.1
1.8 ± 0.1
0.1
0.1 S
0.65
0.22 ± 0.1
0.08 M

(Unit : mm)

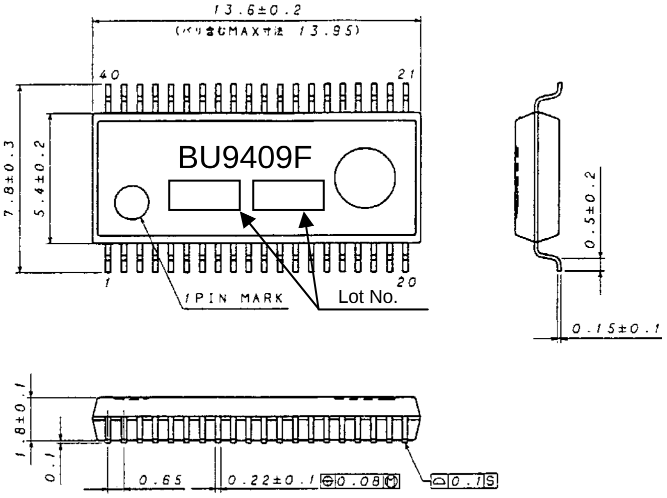
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)


Reel
1pin
Direction of feed

∗Order quantity needs to be multiple of the minimum quantity.

●Marking Diagram(s)(TOP VIEW)


13.6±0.2
(バリ含むMAX寸法 13.95)
40
21
1
20
7.8±0.3
5.4±0.2
BU9409F
1PIN MARK
Lot No.
0.5±0.2
0.15±0.1
1.8±0.1
0.1
0.65
0.22±0.1
0.08 M
0.1 S

Notes

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