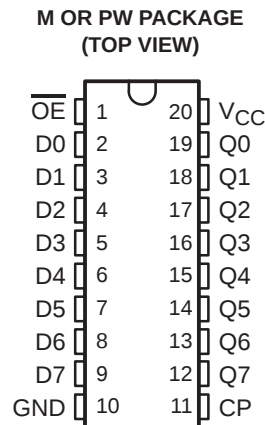


CD74HCT574-EP HIGH-SPEED CMOS LOGIC OCTAL D-TYPE FLIP-FLOP 3-STATE, POSITIVE-EDGE TRIGGERED

SCLS571 – FEBRUARY 2004

- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of –40°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product Change Notification**
- **Qualification Pedigree[†]**
- **Buffered Inputs**
- **Common 3-State Output-Enable Control**
- **3-State Outputs**
- **Bus-Line Driving Capability**
- **Typical Propagation Delay (Clock to Q): 15 ns at $V_{CC} = 5\text{ V}$, $C_L = 15\text{ pF}$, $T_A = 25^\circ\text{C}$**
- **Fanout (Over Temperature Range)**
 - Standard Outputs . . . 10 LSTTL Loads
 - Bus Driver Outputs . . . 15 LSTTL Loads
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **V_{CC} Voltage = 4.5 V to 5.5 V**
- **Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8\text{ V}$ (Max), $V_{IH} = 2\text{ V}$ (Min)**
- **CMOS Input Compatibility, $I_I \leq 1\text{ }\mu\text{A}$ at V_{OL} , V_{OH}**

[†] Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.



description/ordering information

The CD74HCT574 is an octal D-type flip-flop with 3-state outputs and the capability to drive 15 LSTTL loads. The eight edge-triggered flip-flops enter data into their registers on the low-to-high transition of the clock (CP). The output enable ($\overline{OE}$) controls the 3-state outputs and is independent of the register operation. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

ORDERING INFORMATION

T_A	PACKAGE [‡]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – M	Tape and reel	CD74HCT574QM96EP	HCT574EP
	TSSOP – PW	Tape and reel	CD74HCT574QPWREP	HCT574EP

[‡] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2004, Texas Instruments Incorporated

CD74HCT574-EP
HIGH-SPEED CMOS LOGIC OCTAL D-TYPE FLIP-FLOP
3-STATE, POSITIVE-EDGE TRIGGERED

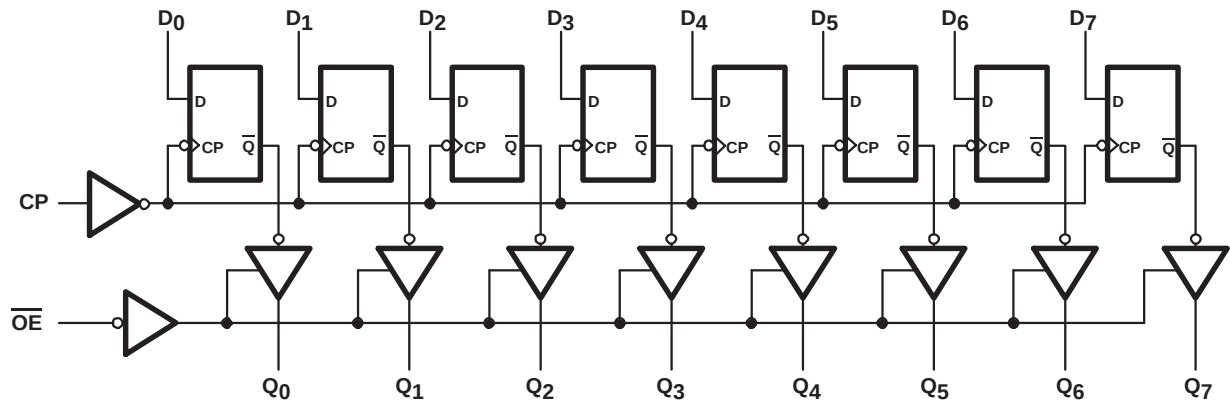
SCLS571 – FEBRUARY 2004

FUNCTION TABLE

INPUTS			OUTPUT Q
$\overline{OE}$	CP	D	
L	$\uparrow$	H	H
L	$\uparrow$	L	L
L	L	X	Q_0
H	X	X	Z

NOTE: H = High voltage level (steady state)
L = Low voltage level (steady state)
X = Don't care
 $\uparrow$ = Transition from low to high level
 Q_0 = Level before the indicated steady-state conditions were established
Z = High-impedance state

logic diagram (positive logic)



CD74HCT574-EP

HIGH-SPEED CMOS LOGIC OCTAL D-TYPE FLIP-FLOP

3-STATE, POSITIVE-EDGE TRIGGERED

SCLS571 – FEBRUARY 2004

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} (see Note 1)	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	±20 mA
Output clamp current, I_{OK} ($V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)	±20 mA
Drain current per output, I_O ($V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	±35 mA
Output source or sink current per output, I_O ($V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	±25 mA
Continuous current through V_{CC} or GND, I_{CC}	±50 mA
Package thermal impedance, θ_{JA} (see Note 2): M package	58°C/W
PW package	69°C/W
Maximum junction temperature, T_J	150°C
Lead temperature (during soldering):	
At distance 1/16 ± 1/32 inch (1,59 ± 0,79 mm) from case for 10 s max	300°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages referenced to GND unless otherwise specified.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V _{CC}	Supply voltage		4.5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 4.5 V to 5.5 V	2		V
V _{IL}	Low-level input voltage	V _{CC} = 4.5 V to 5.5 V		0.8	V
V _I	Input voltage		0	V _{CC}	V
V _O	Output voltage		0	V _{CC}	V
t _t	Input transition (rise and fall) time	V _{CC} = 2 V	0	1000	ns
		V _{CC} = 4.5 V	0	500	
		V _{CC} = 6 V	0	400	
T _A	Operating free-air temperature		−40	125	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



CD74HCT574-EP

HIGH-SPEED CMOS LOGIC OCTAL D-TYPE FLIP-FLOP

3-STATE, POSITIVE-EDGE TRIGGERED

SCLS571 – FEBRUARY 2004

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		I_O (mA)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ TO 125°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	CMOS loads	-0.02	4.5 V	4.4			4.4		V
		TTL loads	-6	4.5 V	3.98			3.7		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	CMOS loads	0.02	4.5 V			0.1		0.1	V
		TTL loads	6	4.5 V			0.26		0.4	
I_I	$V_I = V_{CC}$ or GND		0	5.5 V			± 0.1		± 1	μA
I_{OZ}	$V_I = V_{IL}$ or V_{IH} , $V_O = V_{CC}$ or GND			6 V			± 0.5		± 10	μA
I_{CC}	$V_I = V_{CC}$ or GND		0	5.5 V			8		160	μA
ΔI_{CC}	$V_I = V_{CC} - 2.1\text{ V}$, See Note 4			4.5 V to 5.5 V		100	360		490	μA
C_{IN}	$C_L = 50\text{ pF}$						10		10	pF
C_{OUT}	3-state						20		20	pF

NOTE 4: For dual-supply systems, theoretical worst-case ($V_I = 2.4\text{ V}$, $V_{CC} = 5.5\text{ V}$) specification is 1.8 mA.

HCT input loading

TYPE	INPUT	UNIT LOADS [†]
'574	D0-D7	0.4
	CP	0.75
	$\overline{OE}$	0.6

[†] Unit load is ΔI_{CC} limit specified in electrical characteristics table, e.g., 360 μA max at 25°C .

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER		V_{CC}	$T_A = 25^\circ\text{C}$		$T_A = -40^\circ\text{C}$ TO 125°C		UNIT
			MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	4.5 V	30		20		MHz
t_W	Clock pulse duration	4.5 V	16		24		ns
t_{su}	Setup time, data before clock $\uparrow$	4.5 V	12		18		ns
t_h	Hold time, data after clock $\uparrow$	4.5 V	5		5		ns



CD74HCT574-EP

HIGH-SPEED CMOS LOGIC OCTAL D-TYPE FLIP-FLOP

3-STATE, POSITIVE-EDGE TRIGGERED

SCLS571 – FEBRUARY 2004

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V _{CC}	T _A = 25°C			T _A = -40°C TO 125°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
t _{pd}	CP	Q	C _L = 50 pF	4.5 V			33		50	ns
			C _L = 15 pF	5 V		15				
t _{dis}	$\overline{\text{OE}}$	Q	C _L = 50 pF	4.5 V			28		42	ns
			C _L = 15 pF	5 V		11				
t _{en}	$\overline{\text{OE}}$	Q	C _L = 50 pF	4.5 V			30		45	ns
			C _L = 15 pF	5 V		12				
t _t		Q	C _L = 50 pF	4.5 V			12		18	ns
f _{max}	CP		C _L = 15 pF	5 V		60				MHz

operating characteristics, V_{CC} = 5 V, T_A = 25°C, input t_r, t_f = 6 ns

PARAMETER		TYP	UNIT
C _{pd}	Power dissipation capacitance (see Note 5)	47	pF

NOTE 5: C_{pd} is used to determine the dynamic power consumption (P_D), per package.

$$P_D = (C_{PD} \times V_{CC}^2 \times f_I) + \Sigma (C_L \times V_{CC}^2 \times f_O)$$

f_I = input frequency

f_O = output frequency

C_L = output load capacitance

V_{CC} = supply voltage

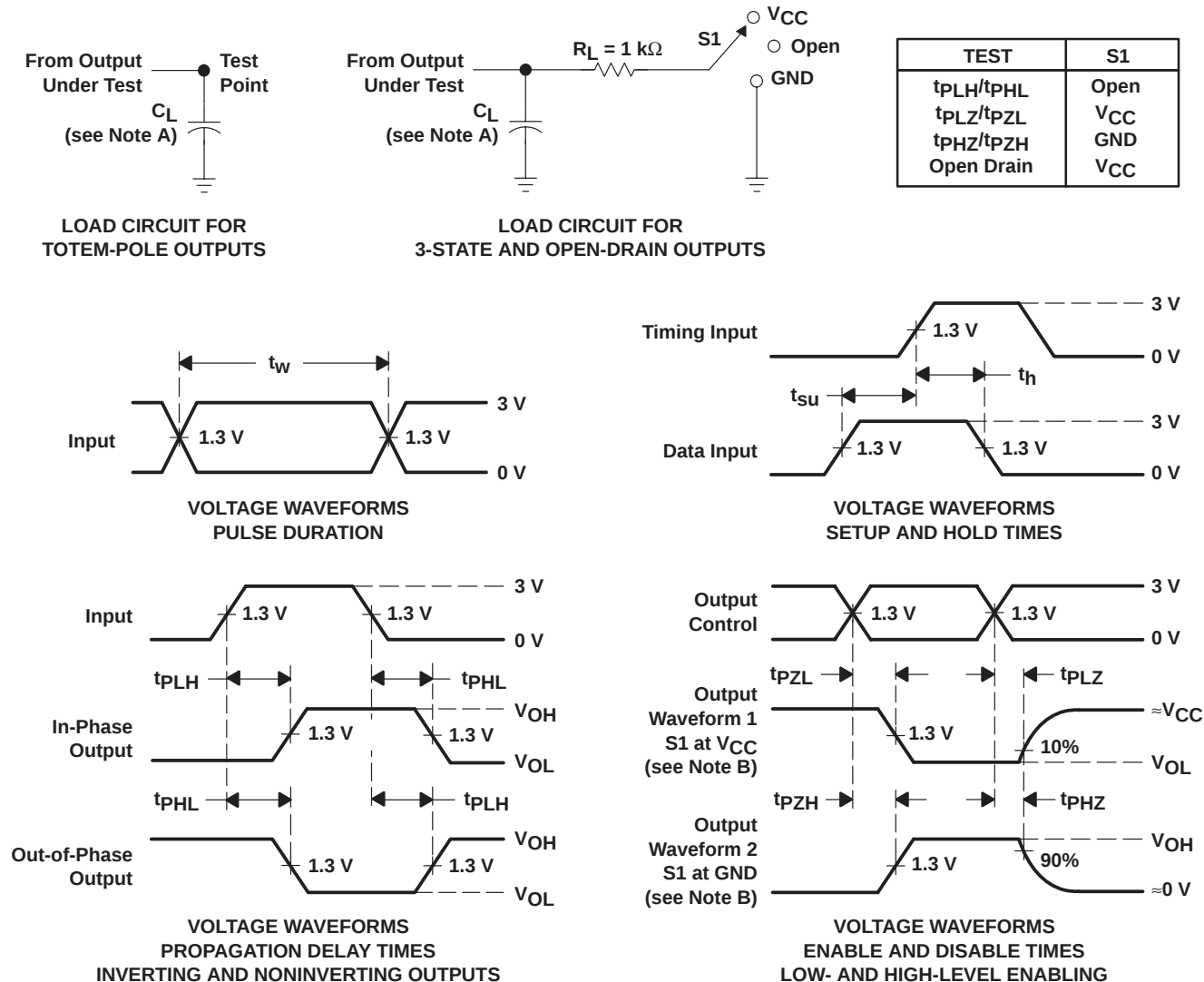
CD74HCT574-EP

HIGH-SPEED CMOS LOGIC OCTAL D-TYPE FLIP-FLOP

3-STATE, POSITIVE-EDGE TRIGGERED

SCLS571 – FEBRUARY 2004

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 6\text{ ns}$, $t_f \leq 6\text{ ns}$.
 - D. The outputs are measured one at a time, with one input transition per measurement.
 - E. All parameters and waveforms are not applicable to all devices.
 - F. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - G. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - H. t_{PZH} and t_{PZL} are the same as t_{en} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CD74HCT574QM96EP	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCT574EP	Samples
CD74HCT574QPWREP	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCT574EP	Samples
V62/04739-01XE	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCT574EP	Samples
V62/04739-01YE	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCT574EP	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD74HCT574-EP :

- Catalog: [CD74HCT574](#)
- Automotive: [CD74HCT574-Q1](#)
- Military: [CD54HCT574](#)

NOTE: Qualified Version Definitions:

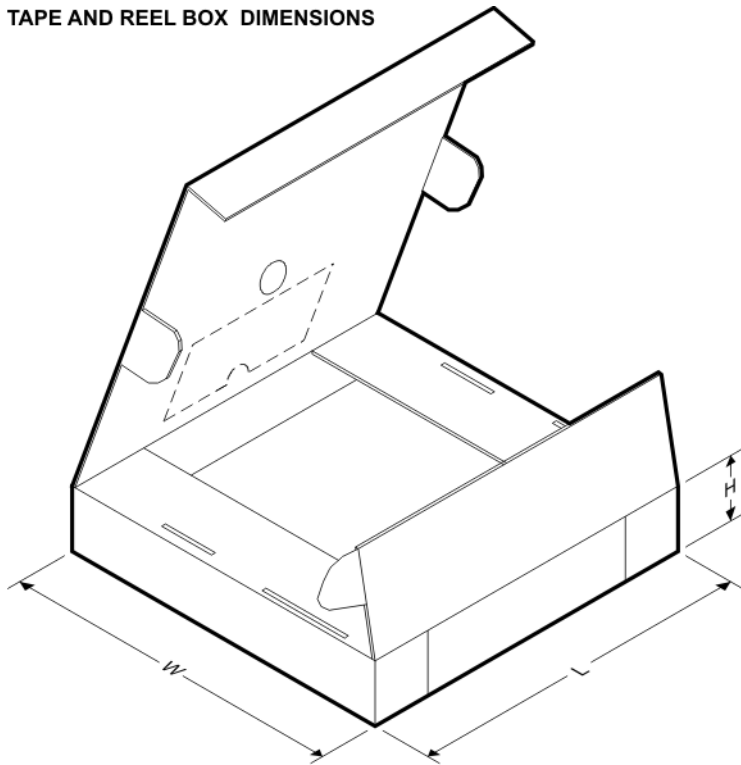
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HCT574QM96EP	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HCT574QPWREP	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

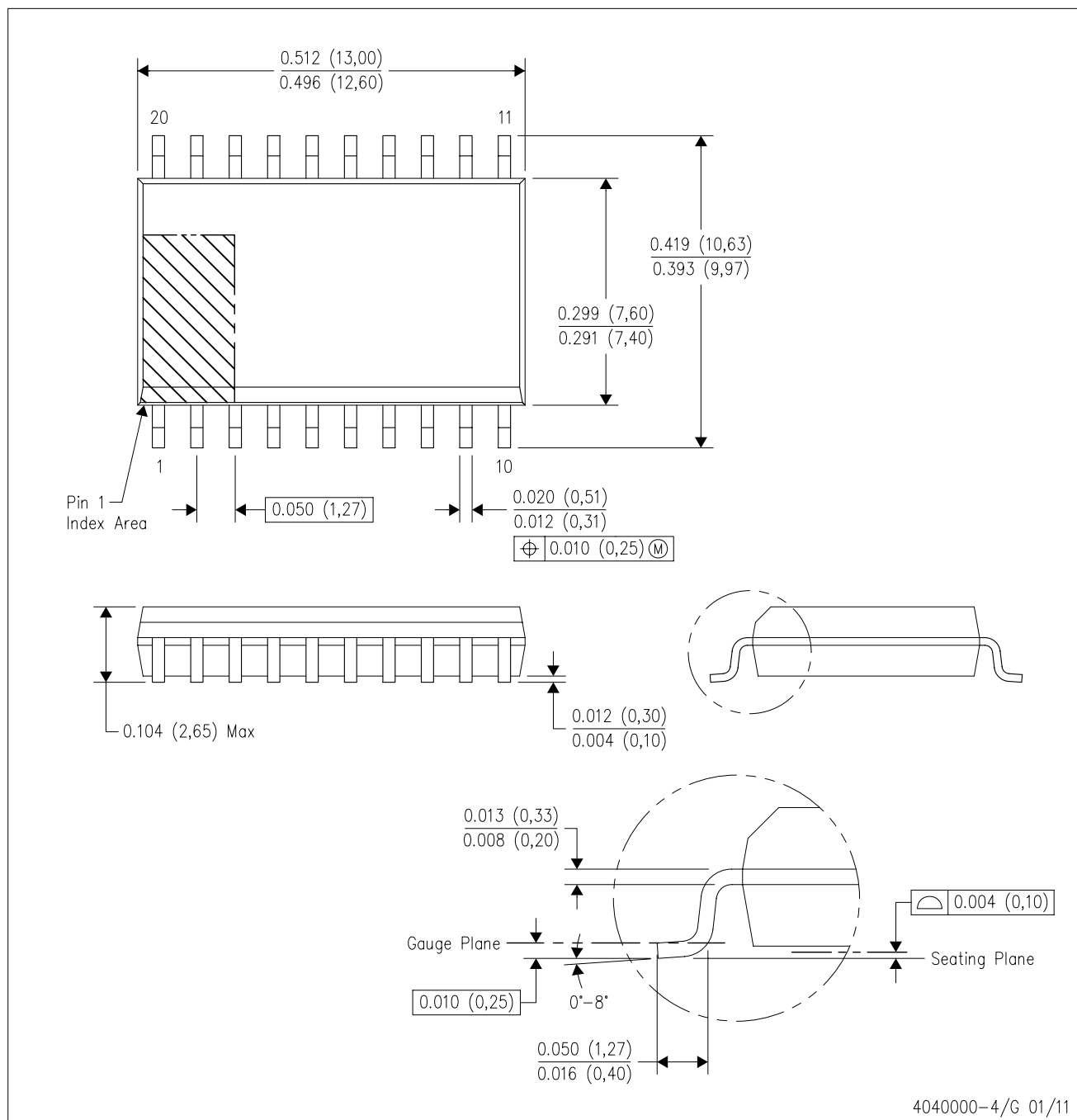


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HCT574QM96EP	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HCT574QPWREP	TSSOP	PW	20	2000	367.0	367.0	38.0

DW (R-PDSO-G20)

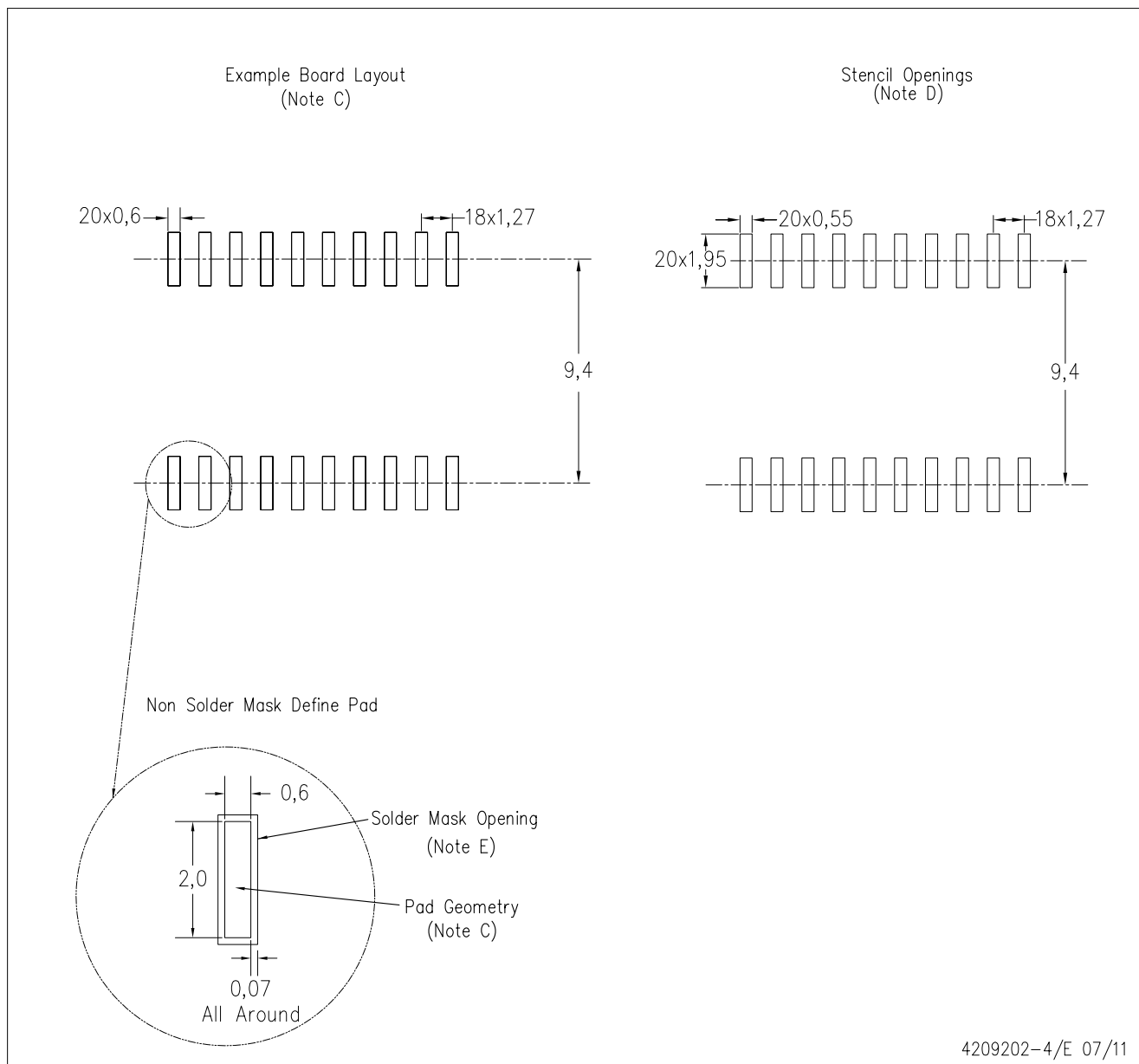
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



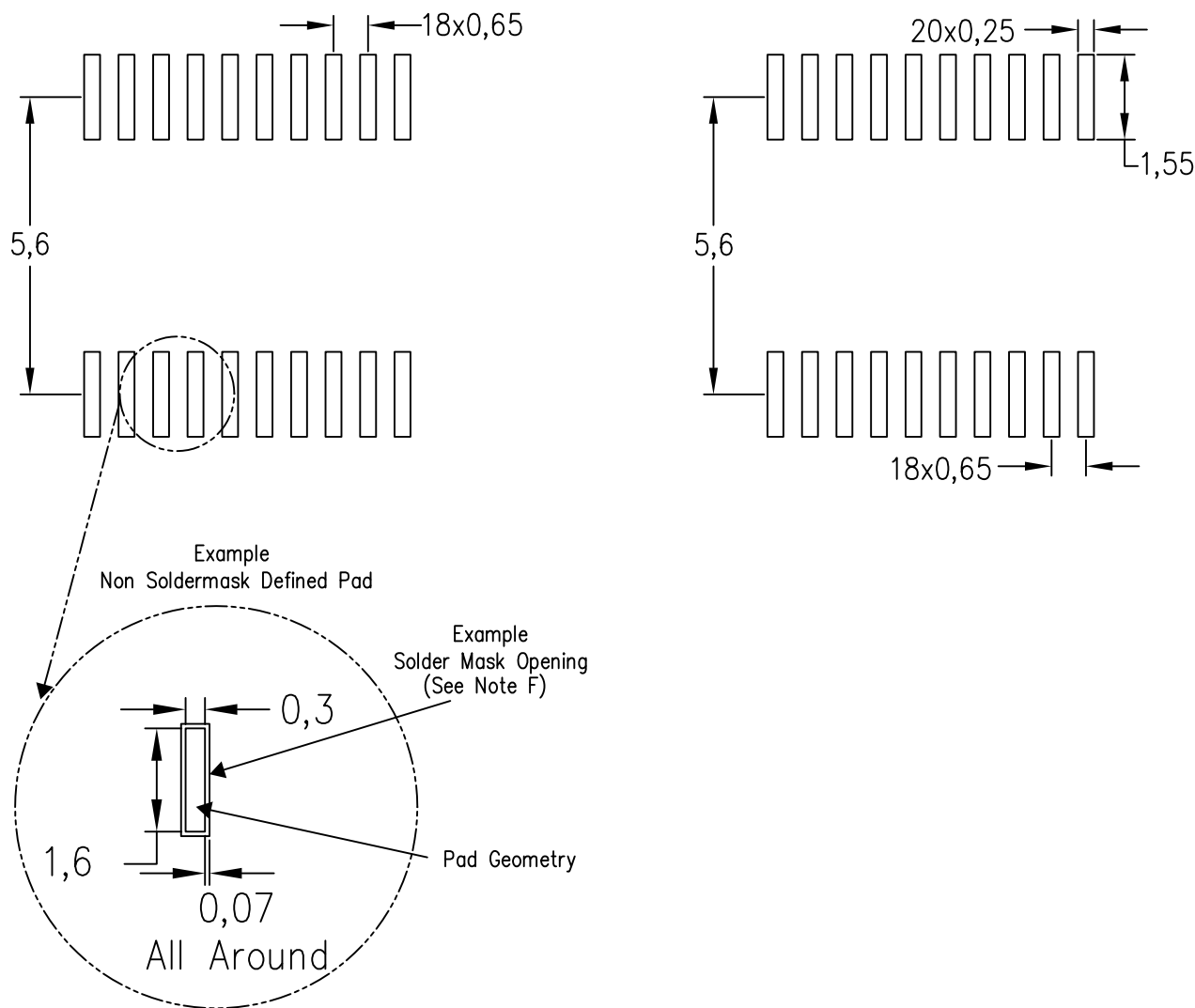
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness
of .127mm (.005inch).



4211284-5/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com