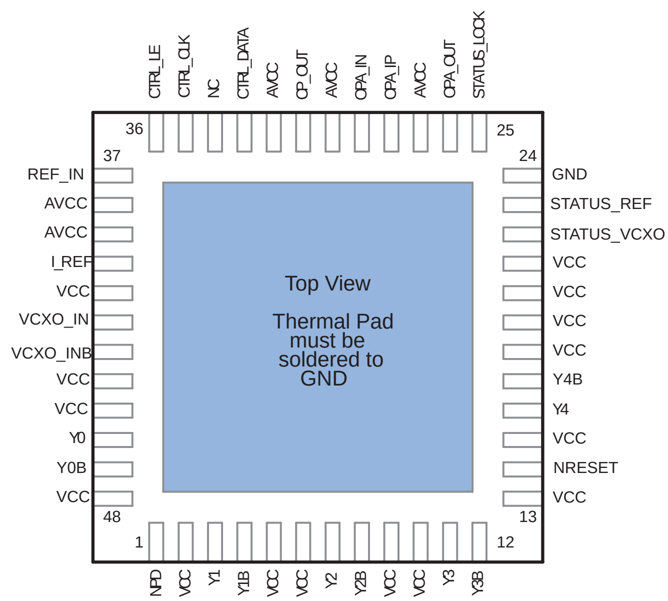
- **High Performance 1:5 PLL Clock Synchronizer**
- **Two Clock Inputs: VCXO_IN Clock Is Synchronized To REF_IN Clock**
- **Synchronizes Frequencies Up To 800 MHz (VCXO_IN)**
- **Supports Five Differential LVPECL Outputs**
- **Each Output Frequency Is Selectable By x1, /2, /4, /8, /16**
- **All Outputs Are Synchronized**
- **Integrated Low-Noise OPA For External Low-Pass Filter**
- **Efficient Jitter Screening From Low PLL Loop Bandwidth**
- **Low-Phase Noise Characteristic**
- **Programmable Delay For Phase Adjustments**
- **Predivider Loop BW Adjustment**
- **SPI Controllable Division Setting**
- **Power-Up Control Forces LVPECL Outputs to 3-State at VCC < 1.5 V**
- **3.3-V Power Supply**
- **Packaged In 64-Pin BGA (0,8 mm Pitch – ZVA) or 48-Pin QFN (RGZ)**
- **Industrial Temperature Range –40°C To 85°C**

TERMINAL ASSIGNMENTS (TOP VIEW)

	1	2	3	4	5	6	7	8
A	CTRL_LE	CTRL_CLK	CTRL_DATA	CP_OUT	OPA_IN	OPA_IP	OPA_OUT	STATUS_LOCK
B	REF_IN	GND	GND	GND	GND	GND	GND	GND
C	I_REF	GND	AV_{CC}	AV_{CC}	AV_{CC}	AV_{CC}	AV_{CC}	STATUS_REF
D	VCXO_IN	GND	GND	GND	GND	GND	V_{CC}	STATUS_VCXO
E	VCXO_INB	GND	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
F	Y0	GND	GND	GND	GND	GND	V_{CC}	Y4B
G	Y0B	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	Y4
H	NPD	Y1	Y1B	Y2	Y2B	Y3	Y3B	NRESET

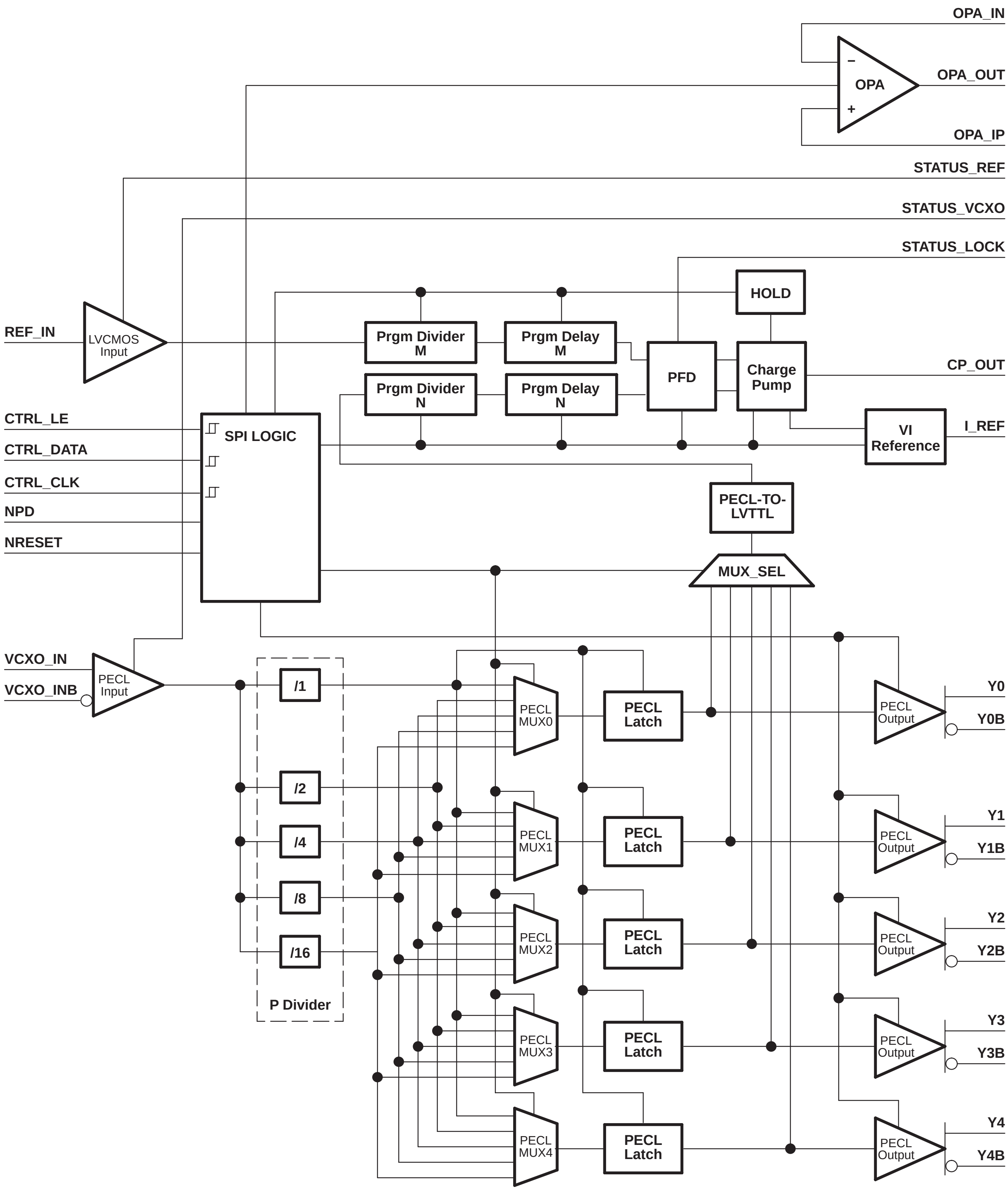


description

The CDC7005 is a high-performance, low-phase noise, and low-skew clock synthesizer and jitter cleaner that synchronizes the voltage controlled crystal oscillator (VCXO) frequency to the reference clock. The programmable predividers M and N give a high flexibility to the frequency ratio of the reference clock to VCXO: VCXO_IN/REF_IN = (NxP)/M. The VCXO_IN clock operates up to 800 MHz. Through the selection of external VCXO and loop filter components, the PLL loop bandwidth and damping factor can be adjusted to meet different system requirements. Each of the five differential LVPECL outputs are programmable by the serial peripheral interface (SPI). The SPI allows individual control of frequency and enable/disable state of each output. The device operates in 3.3-V environment. The built-in latches ensure that all outputs are synchronized.

The CDC7005 is characterized for operation from –40°C to 85°C.

functional block diagram



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	BGA	QFN		
AV_{CC}	C3, C4, C5, C6, C7	27, 30, 32, 38, 39	Power	3.3-V analog power supply
CP_OUT	A4	31	O	Charge pump output
CTRL_LE	A1	36	I	LVCMOS input, control load enable for serial programmable interface (SPI) with hysteresis. Unused or floating inputs must be tied to proper logic level. It is recommend to use a 20kΩ or larger pull−up resistor to VCC.
CTRL_CLK	A2	35	I	LVCMOS input, serial control clock input for SPI, with hysteresis. Unused or floating inputs must be tied to proper logic level. It is recommend to use a 20kΩ or larger pull−up resistor to VCC.
CTRL_DATA	A3	33	I	LVCMOS input, serial control data input for SPI, with hysteresis. Unused or floating inputs must be tied to proper logic level. It is recommend to use a 20kΩ or larger pull−up resistor to VCC.
GND	B2, B3, B4, B5, B6, B7, B8, C2, D2, D3, D4, D5, D6, E2, F2, F3, F4, F5, F6	Thermal pad and pin 24	Ground	Ground
I_REF	C1	40	O	Current path for external reference resistor (12 kΩ ±1%) to support an accurate charge pump current, optional. Do not use any capacitor across this resistor to prevent noise coupling via this node. If internal 12 kΩ is selected (default setting), this pin can be left open.
NC	−	34	−	Not connected
NPD	H1	1	I	LVCMOS input, asynchronous power down (PD) signal active on low. Switches all current sources off, resets all dividers to default values, and 3-states all outputs. Has an internal 150-kΩ pullup resistor. Note 2: It is recommended to ramp up NPD at the same time with VCC and AVCC or later. The ramp up rate should not be faster than the ramp up rate of VCC and AVCC
NRESET	H8	14	I	LVCMOS input, asynchronous reset signal active on low. Resets the counter of all dividers to zero keeping its divider values the same. It has an internal 150-kΩ pullup resistor. Yx outputs are switched low during reset.
OPA_IN	A5	29	I	Inverting input of the op amp, see Note 1
OPA_OUT	A7	26	O	Output of the op amp, see Note 1
OPA_IP	A6	28	I	Noninverting input of the op amp, see Note 1
REF_IN	B1	37	I	LVCMOS reference clock input
STATUS_LOCK	A8	25	O	This pin is high if the PLL lock definition is valid. PLL lock definition means the rising edge of REF_IN clock and VCXO_IN clock for PFD are inside the lock detect window for at least five successive input clock cycles. If the rising edge of REF_IN clock and VCXO_IN clock are out of the selected lock detect window, this pin will be low, but it does not refer to the real lock condition of the PLL. This means, that i.e. due to a strong jitter at REF_IN or VCXO_IN STATUS_LOCK can be low, even if the PLL is in Lock. The PLL is in lock for sure, if STATUS_LOCK is high.See Table 8 and Figure 4.
STATUS_REF	C8	23	O	LVCMOS output provides the status of the reference input (frequencies above 3.5 MHz are interpreted as valid clock, active high)
STATUS_VCXO	D8	22	O	LVCMOS outputs provides the status of the VCXO input (frequencies above 10 MHz are interpreted as valid clock, active high)

V_{CC}	D7, E3, E4, E5, E6, E7, E8, F7, G2, G3, G4, G5, G6, G7	2, 5, 6, 9, 10, 13, 15, 18, 19, 20, 21, 41, 44, 45, 48	Power	3.3-V supply VCC and AVCC should have always same supply voltage
VCXO_IN	D1	42	I	VCXO LVPECL input
VCXO_INB	E1	43	I	Complementary VCXO LVPECL input
Y[0:4]	F1, H2, H4, H6, G8	46, 3, 7, 11, 16	O	LVPECL output
Y[0:4]B	G1, H3, H5, H7, F8	47, 4, 8, 12, 17	O	Complementary LVPECL output

NOTE 1: If the internal operational amplifier is not used, these pins can be left open.

SPI control interface

The serial interface of the CDC7005 is a simple SPI-compatible interface for writing to the registers of the device. It consists of three control lines: CTRL_CLK, CTRL_DATA, and CTRL_LE. There are four 32-bit wide registers, which can be addressed by the two LSBs of a transferred word (bit 0 and bit 1). Every transmitted word must have 32 bits, starting with MSB first. Each word can be written separately. It is recommended to program Word 0, Word 1, Word 2 and Word 3 right after power up and NPD becomes HIGH. The transfer is initiated with the falling edge of CTRL_LE; as long as CTRL_LE is high, no data can be transferred. During CTRL_LE, low data can be written. The data has to be applied at CTRL_DATA and has to be stable before the rising edge of CTRL_CLK. The transmission is finished by a rising edge of CTRL_LE. With the rising edge of CTRL_LE, the new word is asynchronously transferred to the internal register (e.g., N, M, P, ...). Each word has to be separately transmitted by this procedure. Unused or floating inputs must be tied to proper logic level. It is recommend to use a 20kΩ or larger pull−up resistor to VCC.

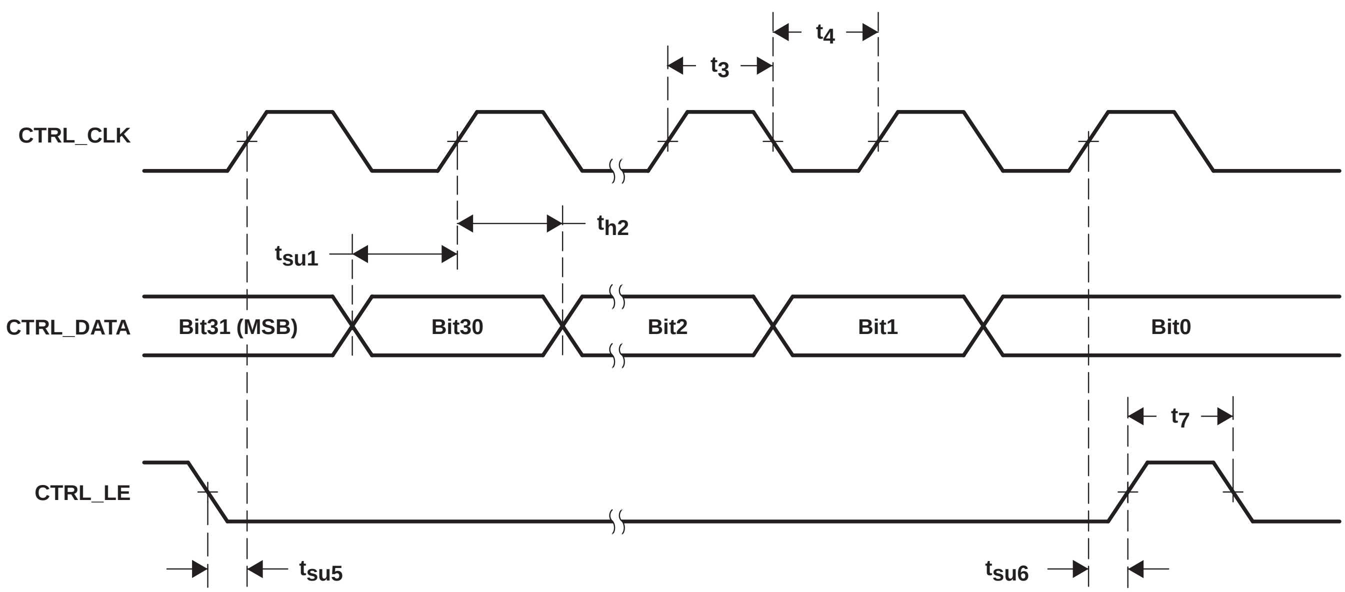


Figure 1. Timing Diagram SPI Control Interface

Table 1. Word 0

BIT	BIT NAME		DESCRIPTION / FUNCTION	TYPE	POWER-UP CONDITION	PIN AFFECTED
0	C0		Register selection	W	0	
1	C1		Register selection	W	0	
2	M0	Reference Divider M	Reference divider M bit 0	W	1	
3	M1		Reference divider M bit 1	W	1	
4	M2		Reference divider M bit 2	W	1	
5	M3		Reference divider M bit 3	W	1	
6	M4		Reference divider M bit 4	W	1	
7	M5		Reference divider M bit 5	W	1	
8	M6		Reference divider M bit 6	W	1	
9	M7		Reference divider M bit 7	W	0	
10	M8		Reference divider M bit 8	W	0	
11	M9		Reference divider M bit 9	W	0	
12	MD0	Reference Delay M	Reference delay M bit 0	W	0	
13	MD1		Reference delay M bit 1	W	0	
14	MD2		Reference delay M bit 2	W	0	
15	PFD0	PFD Pulse Width	PFD pulse width PFD bit 0	W	0	A4
16	PFD1		PFD pulse width PFD bit 1	W	0	A4
17	PFD2		PFD pulse width PFD bit 2	W	0	A4
18	CP0	CP Current	CP current setting bit 0	W	1	A4
19	CP1		CP current setting bit 1	W	0	A4
20	CP2		CP current setting bit 2	W	0	A4
21	CP3		CP current setting bit 3	W	1	A4
22	Y03St	Output 3-State	Y0 3-state (1 = output enabled)	W	1	F1, G1
23	Y13St		Y1 3-state (1 = output enabled)	W	1	H2, H3
24	Y23St		Y2 3-state (1 = output enabled)	W	1	H4, H5
25	Y33St		Y3 3-state (1 = output enabled)	W	1	H6, H7
26	Y43St		Y4 3-state (1 = output enabled)	W	1	G8, F8
27	CP3St		CP 3-state (1 = output enabled)	W	1	A4
28	OP3St		OPA 3-state and disable (1 = OPA enabled)	W	0	A7
29	MUXS0	MUXSEL	MUXSEL select bit 0	W	1	
30	MUXS1		MUXSEL select bit 1	W	1	
31	MUXS2		MUXSEL select bit 2	W	0	

Table 2. Word 1

BIT	BIT NAME		DESCRIPTION / FUNCTION	TYPE	POWER-UP CONDITION	PIN AFFECTED
0	C0		Register selection	W	1	
1	C1		Register selection	W	0	
2	N0	VCXO Divider N†	VCXO divider N bit 0	W	1	
3	N1		VCXO divider N bit 1	W	1	
4	N2		VCXO divider N bit 2	W	1	
5	N3		VCXO divider N bit 3	W	1	
6	N4		VCXO divider N bit 4	W	1	
7	N5		VCXO divider N bit 5	W	1	
8	N6		VCXO divider N bit 6	W	1	
9	N7		VCXO divider N bit 7	W	0	
10	N8		VCXO divider N bit 8	W	0	
11	N9		VCXO divider N bit 9	W	0	
12	ND0	VCXO Delay N	VCXO delay N bit 0	W	0	
13	ND1		VCXO delay N bit 1	W	0	
14	ND2		VCXO delay N bit 2	W	0	
15	MUX00	MUX0	MUX0 select bit 0	W	0	F1, G1
16	MUX01		MUX0 select bit 1	W	0	F1, G1
17	MUX02		MUX0 select bit 2	W	0	F1, G1
18	MUX10	MUX1	MUX1 select bit 0	W	1	H2, H3
19	MUX11		MUX1 select bit 1	W	0	H2, H3
20	MUX12		MUX1 select bit 2	W	0	H2, H3
21	MUX20	MUX2	MUX2 select bit 0	W	0	H4, H5
22	MUX21		MUX2 select bit 1	W	1	H4, H5
23	MUX22		MUX2 select bit 2	W	0	H4, H5
24	MUX30	MUX3	MUX3 select bit 0	W	1	H6, H7
25	MUX31		MUX3 select bit 1	W	1	H6, H7
26	MUX32		MUX3 select bit 2	W	0	H6, H7
27	MUX40	MUX4	MUX4 select bit 0	W	1	G8, F8
28	MUX41		MUX4 select bit 1	W	1	G8, F8
29	MUX42		MUX4 select bit 2	W	0	G8, F8
30	CP_DIR		Determines in which direction CP should regulate, if REF_CLK is faster than VCXO_CLK, and vice versa (see Figure 2)	W	1	A4
31	REXT		Enable external reference resistor (1 = enabled)	W	0	C1

† The frequency applied to the Divider N must be smaller than 250 MHz. A sufficient P Divider must be selected with the MUX_SEL to maintain this criteria.

Table 3. Word 2

BIT	BIT NAME		DESCRIPTION / FUNCTION	TYPE	POWER-UP CONDITION	PIN AFFECTED
0	C0		Register selection	W	0	
1	C1		Register selection	W	1	
2	HOLD		Enables the hold functionality (1 = enabled)	W	0	A4
3	NPD		PD current sources, resets the dividers and 3-states all outputs (0 = active)	W	1	
4	NRESET		RESET all dividers (0 = active)	W	1	
5	ENBG		Enable bandgap (1 = enabled), see Note 2	W	1	C1
6	LOCKW 0		Lock detect window bit 0	W	0	A8
7	LOCKW 1		Lock detect window bit 1	W	0	A8
8	RES		Reserved	W	X	
9	RES		Reserved	W	X	
10	RES		Reserved	W	X	
11	RES		Reserved	W	X	
12	RES		Reserved	W	X	
13	RES		Reserved	W	X	
14	RES		Reserved	W	X	
15	RES		Reserved	W	X	
16	RES		Reserved	W	X	
17	RES		Reserved	W	X	
18	RES		Reserved	W	X	
19	RES		Reserved	W	X	
20	RES		Reserved	W	X	
21	RES		Reserved	W	X	
22	RES		Reserved	W	X	
23	RES		Reserved	W	X	
24	RES		Reserved	W	X	
25	RES		Reserved	W	X	
26	RES		Reserved	W	X	
27	RES		Reserved	W	X	
28	RES		Reserved	W	X	
29	RES		Reserved	W	X	
30	RES		Reserved	W	X	
31	RES		Reserved	W	X	

NOTE 2: The reference voltage for the charge pump and LVPECL output circuitry can be generated in two ways. One way is to enable ENBG and the other way is to use the voltage divider circuitry (internal or external). It is recommended to enable ENBG because it gives an accurate value and it is independent on temperature variation.

Table 4. Word 3 (See Note 3)

BIT	BIT NAME		DESCRIPTION / FUNCTION	TYPE	POWER-UP CONDITION	PIN AFFECTED
0	C0		Register selection	W	1	
1	C1		Register selection	W	1	
2	RES		Reserved	W	0	
3	RES		Reserved	W	0	
4	RES		Reserved	W	0	
5	RES		Reserved	W	0	
6	RES		Reserved	W	0	
7	RES		Reserved	W	0	
8	RES		Reserved	W	0	
9	RES		Reserved	W	0	
10	RES		Reserved	W	0	
11	RES		Reserved	W	0	
12	RES		Reserved	W	0	
13	RES		Reserved	W	0	
14	RES		Reserved	W	0	
15	RES		Reserved	W	0	
16	RES		Reserved	W	0	
17	RES		Reserved	W	0	
18	RES		Reserved	W	0	
19	RES		Reserved	W	0	
20	RES		Reserved	W	0	
21	RES		Reserved	W	0	
22	RES		Reserved	W	0	
23	RES		Reserved	W	0	
24	RES		Reserved	W	0	
25	RES		Reserved	W	0	
26	RES		Reserved	W	0	
27	RES		Reserved	W	0	
28	RES		Reserved	W	0	
29	RES		Reserved	W	0	
30	RES		Reserved	W	0	
31	RES		Reserved	W	0	

NOTE 3: It is recommended to program all register bits of Word 3 to 0 along with other Registers.

functional description of the logic

Table 5. Reference Divider M and VCXO Divider N (See Note 4)

M9	M8	M7	M6	M5	M4	M3	M2	M1	M0	DIV BY†	DEFAULT
0	0	0	0	0	0	0	0	0	0	1	
0	0	0	0	0	0	0	0	0	1	2	
0	0	0	0	0	0	0	0	1	0	3	
0	0	0	0	0	0	0	0	1	1	4	
					• • •						
0	0	0	1	1	1	1	1	1	1	128	Yes
					• • •						
1	1	1	1	1	1	1	1	0	1	1022	
1	1	1	1	1	1	1	1	1	0	1023	
1	1	1	1	1	1	1	1	1	1	1024	

NOTE 4: If the divider value is Q, then the code will be the binary value of (Q−1).
† The frequency applied to the Divider N must be smaller than 250 MHz. A sufficient P Divider must be selected with the MUX_SEL to maintain this criteria.

Table 6. Reference Delay M and VCXO Delay N

MD2/ND2	MD1/ND1	MD0/ND0	DELAY†	DEFAULT
0	0	0	0 ps	Yes
0	0	1	150 ps	
0	1	0	300 ps	
0	1	1	450 ps	
1	0	0	600 ps	
1	0	1	750 ps	
1	1	0	1.5 ns	
1	1	1	2.75 ns	

† Typical values at V_{CC} = 3.3 V, temperature = 25°C

Table 7. PFD Pulse Width Delay

PFD2	PFD1	PFD0	ADDITIONAL PULSE WIDTH†	DEFAULT
0	0	0	0 ps	Yes
0	0	1	300 ps	
0	1	0	600 ps	
0	1	1	900 ps	
1	0	0	1.5 ns	
1	0	1	2.1 ns	
1	1	0	2.7 ns	
1	1	1	3.7 ns	

† Typical values at V_{CC} = 3.3 V, temperature = 25°C

functional description of the logic (continued)

Table 8. Lock Detect Window

LockW 1	LockW 0	REF_IN TO Yn TOLERABLE PHASE OFFSET (See Figure 4 and Note 1)	DEFAULT
0	0	±1.2 ns	Yes
0	1	±1.8 ns	
1	0	±2.4 ns	
1	1	±3 ns	

NOTE 1: Determined at PFD − REF_IN and Yn feed through M/N Divider and M/N Delay.

Table 9. Charge Pump Current

CP3	CP2	CP1	CP0	NOMINAL CHARGE PUMP CURRENT†	DEFAULT
0	0	0	0	0.625 mA	
0	0	0	1	1.25 mA	
0	0	1	0	1.875 mA	
0	0	1	1	2.5 mA	
0	1	0	0	3.125 mA	
0	1	0	1	3.75 mA	
0	1	1	0	4.375 mA	
0	1	1	1	5 mA	
1	0	0	0	1 mA	
1	0	0	1	2 mA	Yes
1	0	1	0	3 mA	
1	0	1	1	4 mA	
1	1	0	0	5 mA	
1	1	0	1	6 mA	
1	1	1	0	7 mA	
1	1	1	1	8 mA	

† With an internal or external reference resistor (12 kΩ) in use.

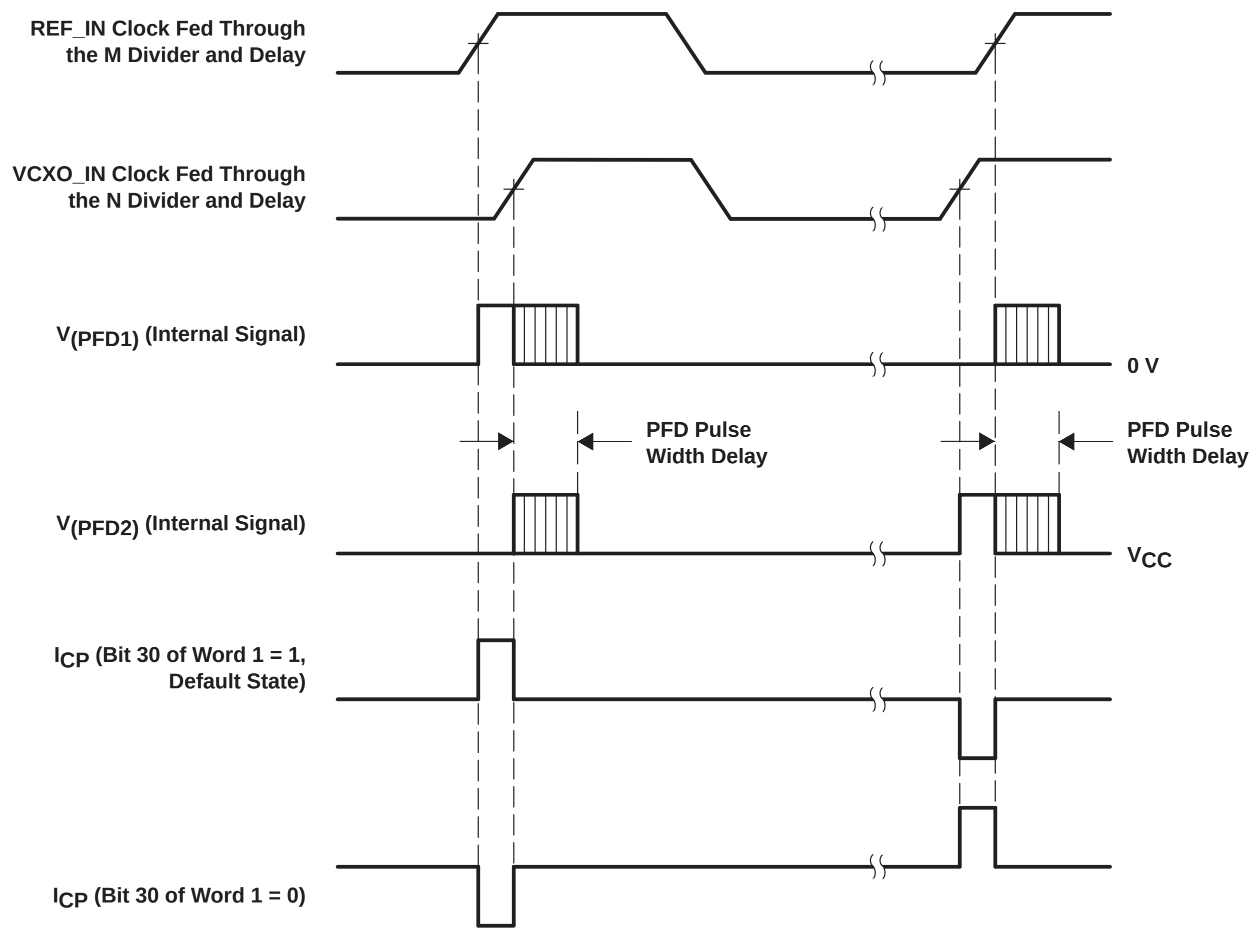
Table 10. MUXSEL Selection

MUXS2	MUXS1	MUXS0	SELECTED VCXO SIGNAL FOR THE PHASE DISCRIMINATOR	DEFAULT
0	0	0	Y0	
0	0	1	Y1	
0	1	0	Y2	
0	1	1	Y3	Yes
1	0	0	Y4	
1	0	1	Y3	
1	1	0	Y3	
1	1	1	Y3	

functional description of the logic (continued)

Table 11. MUX0, MUX1, MUX2, MUX3, and MUX4 Selection

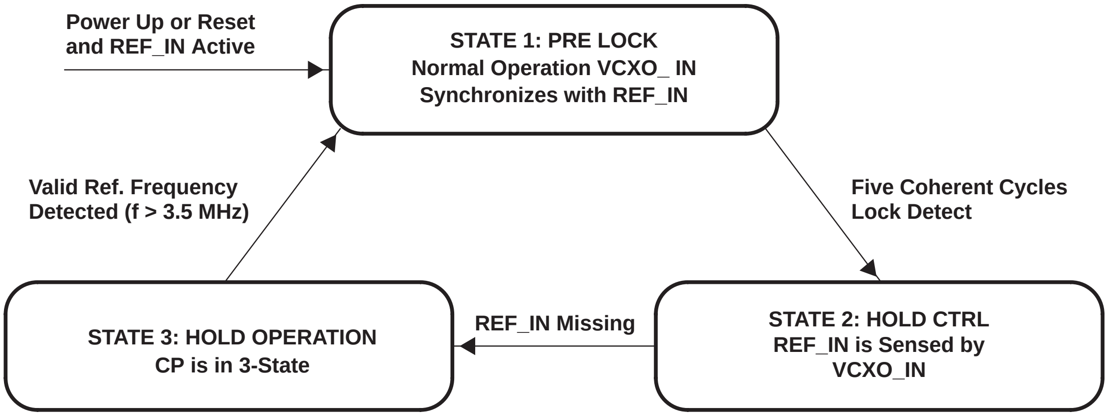
MUX2	MUX1	MUX0	SELECTED DIVIDED VCXO SIGNAL	DEFAULT
0	0	0	Div by 1	For Y0
0	0	1	Div by 2	For Y1
0	1	0	Div by 4	For Y2
0	1	1	Div by 8	For Y3 and Y4
1	0	0	Div by 16	
1	0	1	Div by 8	
1	1	0	Div by 8	
1	1	1	Div by 8	



NOTE: The purpose of the PFD pulse width delay is to improve spurious suppression. (See Table 7)

Figure 2. Charge Pump Current Direction

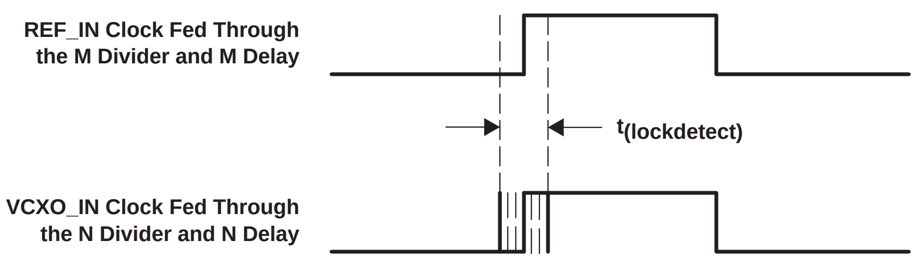
functional description of the logic (continued)



NOTES: A. For a proper hold functionality the following conditions must be maintained:
- Counter M and counter N need to have the same divider ratio
- fref_in max = 75 MHz
- Duty cycle of 45% to 55% for 25 MHz <= fref_in < 50 MHz
- Duty cycle of 40% to 60% for 50 MHz <= fref_in < 75 MHz
- Duty cycle of f_{VCXO} should be in 50% range

The hold functionality is triggered by the first missing REF_IN cycle. It is disabled in default mode (bit 2 of word 2 = 0). While the device is in frequency hold mode, a possible leakage current caused by the external filter and VCXO may change the VCXO control voltage, and therefore changing the VCXO frequency. To keep the frequency drift as low as possible, a low leakage current filter design is recommended or the number of the disrupted / missing REF_IN clock cycles should be kept low (< 100).

Figure 3. State Machine Operation



NOTE: If the rising edge of REF_IN clock and VCXO_IN clock for PFD are inside the lock detect window ($t_{(lockdetect)}$) for at least five successive input clock periods, then the PLL is considered to be locked. In this case, the STATUS_LOCK output is set to high level. The size of the lock detect window is programmable via the SPI control logic (bit 6 and 7 of word 2). (See Table 8)

Figure 4. Lock Detect Window

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC}, AV_{CC} (see Note 2) . . . . −0.5 V to 4.6 V
Input voltage range, V_I (see Note 3) . . . . −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 3) . . . . −0.5 V to V_{CC} + 0.5 V
Input current (V_I < 0, V_I > V_{CC}) . . . . ±20 mA
Output current for LVPECL outputs (0 < V_O < V_{CC}) . . . . −50 mA
Continuous output current, I_O . . . . ±50 mA
Storage temperature range T_{stg} . . . . −65°C to 150°C
Maximum junction temperature, T_J . . . . 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 2. All supply voltages must be the same value and must be supplied at the same time.
NOTES: 3. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

package thermal resistance for RGZ (QFN) package (see Note 4 and Note 5)

AIRFLOW (LFM)	θ_{JA} (°C/W)	θ_{JC} (°C/W)	θ_{JP} (°C/W)	Ψ_{JT} (°C/W)
0	29.9	22.4	1.5	0.2
15	24.7			0.2
250	23.2			0.2
500	21.5			0.3

NOTE 4: The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).
NOTE 5: Connected to GND with nine thermal vias (0,3 mm diameter).

package thermal resistance for ZVA (BGA) package (see Note 6)

AIRFLOW (m/s)	θ_{JA} (°C/W)	θ_{JC} (°C/W)	θ_{JB} (°C/W)	Ψ_{JT} (°C/W)
0	54	29.9	44.5	0.9
1	49			0.9
2.5	47.2			0.9

NOTE 6: The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
Operating free-air temperature, T_A	−40		85	°C
Low-level input voltage LVCMOS, V_{IL}			0.3 V_{CC}	V
High-level input voltage LVCMOS, V_{IH}	0.7 V_{CC}			V
Input threshold voltage LVCMOS, V_{IT}		0.5 V_{CC}		V
High-level output current LVCMOS, I_{OH}			−6	mA
Low-level output current LVCMOS, I_{OL}			6	mA
Input voltage range LVCMOS, V_I	0		3.6	V
Input amplitude LVPECL, V_{INPP} [(V_{VCXO_IN} − V_{VCXO_INB}), See Note 7]	0.5		1.3	V
Common-mode input voltage LVPECL, V_{IC}	V_{CC}−2		V_{CC}−0.4	V

NOTE 7: V_{INPP} minimum and maximum is required to maintain ac specifications; the actual device function tolerates at a minimum V_{INPP} of 100 mV.

timing requirements over recommended ranges of supply voltage, load, and operating free-air temperature

PARAMETER		MIN	TYP	MAX	UNIT
REF_IN Requirements					
f_{REF_IN}	LVCMOS reference clock frequency	3.5		180	MHz
t_r / t_f	Rise and fall time of REF_IN signal from 20% to 80% of V_{CC}			4	ns
$duty_{REF}$	Duty cycle of REF_IN at V_{CC} / 2	40%		60%	
VCXO_IN, VCXO_INB Requirements					
f_{VCXO_IN}	LVPECL VCXO clock frequency	10		800	MHz
t_r / t_f	Rise and fall time 20% to 80% of V_{INPP} at 80 MHz to 800 MHz (see Note 8)			3	ns
$duty_{VCXO}$	Duty cycle of VCXO clock	40%		60%	
SPI/Control Requirements (See Figure 1)					
f_{CTRL_CLK}	CTRL_CLK frequency			20	MHz
t_{su1}	CTRL_DATA to CTRL_CLK setup time	10			ns
t_{h2}	CTRL_DATA to CTRL_CLK hold time	10			ns
t_3	CTRL_CLK high duration	25			ns
t_4	CTRL_CLK low duration	25			ns
t_{su5}	CTRL_LE to CTRL_CLK setup time	10			ns
t_{su6}	CTRL_CLK to CTRL_LE setup time	10			ns
t_7	CTRL_LE pulse width	20			ns
t_r / t_f	Rise and fall time of CTRL_DATA CTRL_CLK, CTRL_LE from 20% to 80% of V_{CC}			5	ns
NPD / NRESET Requirements					
t_r / t_f	Rise and fall time of the NRESET, NPD signal from 20% to 80% of V_{CC}			4	ns

NOTES: 8. Use a square wave for lower frequencies (< 80 MHz).

device characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Overall						
I_{CC}	Supply current (see Note 9)	f_{VCXO} = 245 MHz, f_{REF_IN} = 30 MHz, V_{CC} = 3.6 V, AV_{CC} = 3.6 V, f_{PFD} = 240 kHz, I_{CP} = 2 mA, (see Note 11 and Note 13)		230	265	mA
I_{CCPD}	Power-down current	f_{IN} = 0 MHz, V_{CC} = 3.6 V, AV_{CC} = 3.6 V, V_I = 0 V or V_{CC}		100	300	µA
t_{pho}	Phase offset (REF_IN to Y output) (see Note 10)	V_{REF_IN} = V_{CC}/2, Crossing point of Y, See Figure 12	−150		150	ps
LVCMOS						
V_{IK}	LVCMOS input voltage	V_{CC} = 3 V, I_I = –18 mA			−1.2	V
I_I	LVCMOS input current	V_I = 0 V or V_{CC}, V_{CC} = 3.6 V			±5	µA
I_{IH}	LVCMOS input current for NPD, NRESET	V_I = V_{CC}, V_{CC} = 3.6 V			5	µA
I_{IL}	LVCMOS input current for NPD, NRESET	V_I = 0 V, V_{CC} = 3.6 V	−15		−35	µA
V_{OH}	LVCMOS high-level output voltage	I_{OH} = −12 mA, V_{CC} = 3 V	2.1			V
V_{OL}	LVCMOS low-level output voltage	I_{OL} = 12 mA, V_{CC} = 3 V			0.55	V
C_I	Input capacitance at REF_IN	V_I = 0 V or V_{CC}		2		pF
C_I	Input capacitance at CTRL_LE, CTRL_CLOCK, CTRL_DATA	V_I = 0 V or V_{CC}		2		pF
$t_{detectREF}$	Frequency detect time until STATUS_REF is valid	f_{REF_IN} = 3.5 MHz		5		µs
$t_{detectVCXO}$	Frequency detect time until STATUS_VCXO is valid	f_{VCXO_IN} = 10 MHz		5		µs
LVPECL						
I_I	LVPECL input current	V_I = 0 V or V_{CC}			±100	µA
I_{OZ}	LVPECL output current 3-state	V_O = 0 V or V_{CC}−0.8 V			20	µA
V_{OH}	LVPECL high-level output voltage	See Note 11	V_{CC}−1.18		V_{CC}−0.81	V
V_{OL}	LVPECL low-level output voltage	See Note 11	V_{CC}−1.98		V_{CC}−1.55	V
$\lvert V_{OD}\rvert$	Differential output voltage	10 ≤ f_{OUT} ≤ 800 MHz, See Figure 6	500			mV

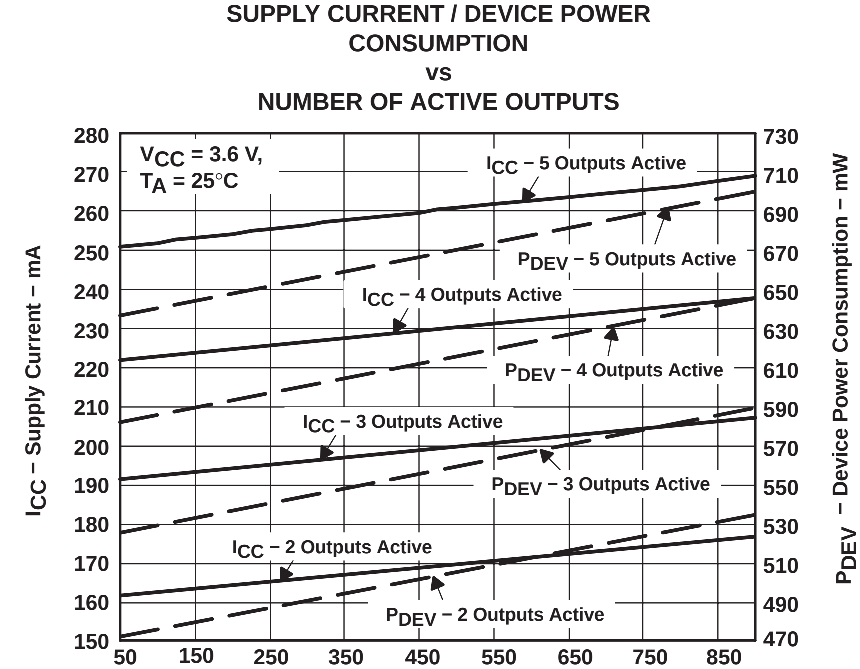
† All typical values are at V_{CC} = 3.3 V, temperature = 25°C.

NOTES:
9. For I_{CC} over frequency see Figure 5.
10. This is valid only for same REF_IN clock and Y output clock frequency. It can be adjusted by the SPI controller (reference delay M and VCXO delay N).
11. Outputs are terminated through a 50-Ω resistor to V_{CC} − 2 V.
12. The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.
13. All output switching at default divider ratios.

device characteristics over recommended operating free-air temperature range (unless otherwise noted)(continued)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}/t_{PHL}	Propagation delay rising/falling edge	VCXO_IN to Yn	500		950	ps
$t_{sk(p)}$	LVPECL pulse skew				15	ps
$t_{sk(o)}$	LVPECL output skew (see Note 14)	See Figure 11, Mode 1−2−4−8−8			60	ps
		See Figure 11, Mode 1−1−1−1−1			30	ps
t_r / t_f	Rise and fall time	20% to 80% of V_{OD}, See Figure 10	180		350	ps
C_I	Input capacitance at VCXO_IN, VCXO_IB			1.5		pF
Phase Detector						
f_{CPmax}	Maximum charge pump frequency	PFD pulse width delay is 0 ps		100		MHz
Charge Pump						
I_{CP}	Charge pump sink/source current range	V_{CP} = 0.5 V_{CC}, See Table 9	±0.625		±8	mA
I_{CP3St}	Charge pump 3-state current	0.5 V < V_{CP} < V_{CC} − 0.5 V		1	30	nA
I_{CPA}	I_{CP} absolute accuracy	V_{CP} = 0.5 V_{CC}			20%	
I_{CPM}	Sink/source current matching	V_{CP} = 0.5 V_{CC}		5%		
I_{VCPM}	I_{CP} vs V_{CP} matching	0.5 V < V_{CP} < V_{CC} − 0.5 V		10%		
Operational Amplifier						
I_S	Supply current	AV_{CC} = 3.6 V		2	5	mA
V_{IO}	Input offset voltage			2		mV
I_{IB}	Input bias current	(| I_{OPA_IP} | + | I_{OPA_IN} |) / 2		1	30	nA
I_{IO}	Input offset current	| I_{OPA_IP} − I_{OPA_IN} |		1	10	nA
R_I	Input resistance	0.5 V_{CC} ±500 mV	10			MΩ
V_{ICR}	Common-mode input voltage range		0.2		V_{CC}−0.2	V
A_{OL}	Open-loop voltage gain	See Figure 17, f = 1 kHz		70		dB
GBW	Gain bandwidth	See Figure 14		3		MHz
SR	Slew rate	See Figure 14, 20% − 80% of V_O		1		V/µs
V_O	Output voltage swing	R_L = 10 kΩ	0.2		V_{CC}−0.2	V
		R_L = 2 kΩ	0.3		V_{CC}−0.3	
R_O	Output resistance			60		Ω
I_{OS}	Short-circuit output current	Sourcing		−20		mA
		Sinking		50		
CMRR	Common-mode rejection ratio	V_{INPP} = 500 mV and f = 1 kHz, (see Figure 15)		80		dB
PSRR	Power supply rejection ratio	AVCC modulated with sine wave from 3 V to 3.6 V and f = 100 Hz (see Figure 16)		60		dB
V_n	Input noise voltage	f = 1 kHz, see Figure 14, V_{IN} = 0 V		500		$nV/\sqrt{Hz}$

† All typical values are at V_{CC} = 3.3 V, temperature = 25°C.
NOTE 14: The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.



NOTE A: $P_{DEV} = P_{Tot} - P_{Term}$
P_{DEV} = Device power consumption, P_{Tot} = Total power consumption, P_{Term} = Termination power consumption

Figure 5. I_{CC} / P_{DEV} vs Frequency

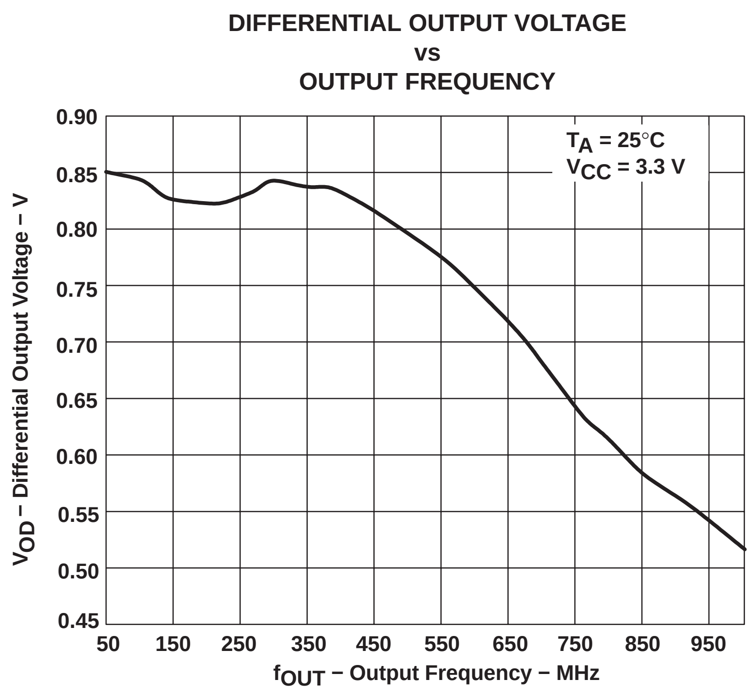


Figure 6. Differential Output Swing (V_{OD}) vs Frequency

APPLICATION INFORMATION

Phase Noise Reference Circuit (See the EVM)

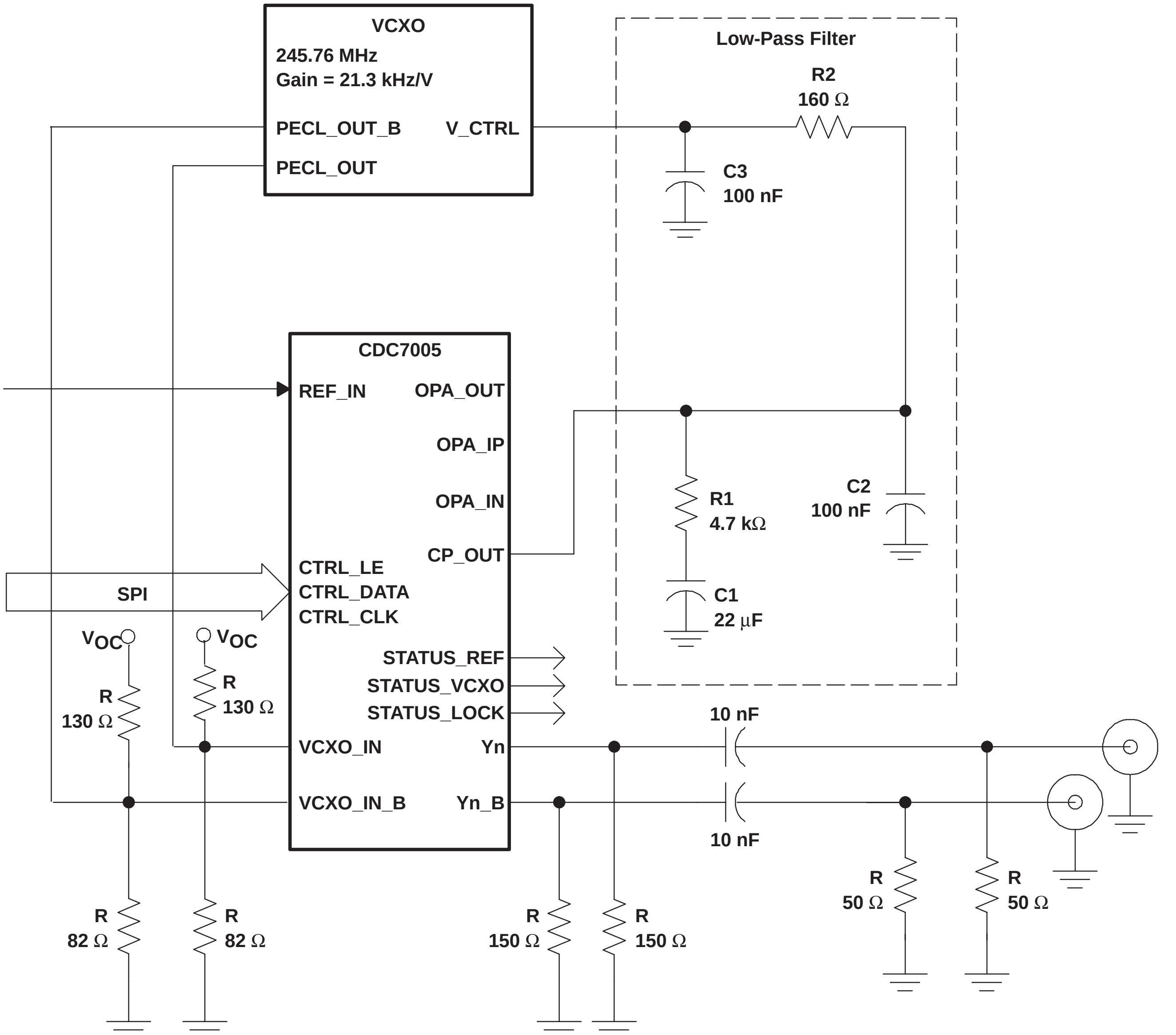


Figure 7. Typical Applications Diagram With Passive Loop Filter

application specific device characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		REF_IN PHASE NOISE AT 30.72 MHz	VCXO PHASE NOISE AT 245.76 MHz	Yn PHASE NOISE AT 30.72 MHz			UNIT
				MIN	TYP†	MAX	
phn_{10}	Phase noise at 10 Hz	−115	−77		−105		dBc/Hz
phn_{100}	Phase noise at 100 Hz	−125	−95		−116		dBc/Hz
phn_{1k}	Phase noise at 1 kHz	−131	−118		−135		dBc/Hz
phn_{10k}	Phase noise at 10 kHz	−136	−136		−147		dBc/Hz
phn_{100k}	Phase noise at 100 kHz	−138	−138		−152		dBc/Hz
phn_{240k}	Phase noise at 240 kHz	−140	−143		−152		dBc/Hz
t_{stabi}	PLL stabilization time, (see Note 15)				200		ms

† Output phase noise is dependent on the noise of the REF_IN clock and VCXO clock noise floor.

NOTES: 15. The typical stabilization time is based on the above application example at a loop bandwidth of 20 Hz.
16. For further explanations as well as phase noise/jitter test results using various VCXOs, see application note SCAA067.

APPLICATION INFORMATION

information on the clock generation for interpolating DACs with the CDC7005

The CDC7005, with its specified phase noise performance, is an ideal sampling clock generator for high speed ADCs and DACs. The CDC7005 is especially of interest for the new high speed DACs, which have integrated interpolation filter. Such DACs achieve sampling rates up to 500 MSPS. This high data rate can typically not be supported from the digital side driving the DAC (e.g., DUC, digital up-converter). Therefore, one approach to interface the DUC to the DAC is the integration of an interpolation filter within the DAC to reduce the data rate at the digital input of the DAC. In 3G systems, for example, a common sampling rate of a high speed DAC is 245.76 MSPS. With a four times interpolation of the digital data, the required input data rate results into 61.44 MSPS, which can be supported easily from the digital side. The DUC GC4116, which supports up to two WCDMA carriers, provides a maximum output data rate of 100 MSPS. An example is shown in Figure 8, where the CDC7005 supplies the clock signal for the DUC/DDC and ADC/DAC.

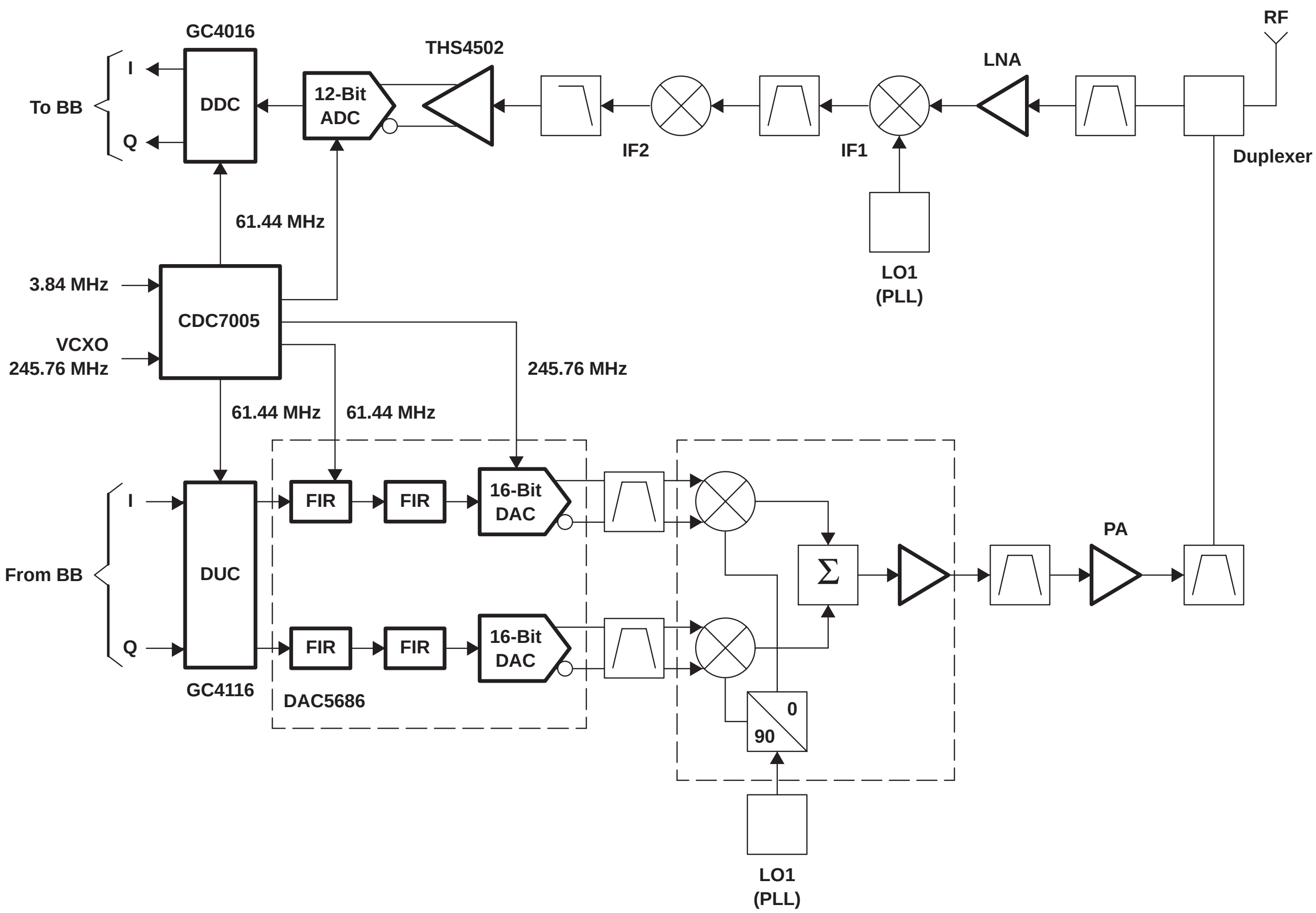


Figure 8. CDC7005 as a Clock Generator for High Speed ADCs and DACs

The generation of the two required clock signals (data input clock, clock for DAC) for such an interpolating DAC can be done in different ways. The easiest way would be to provide an internal PLL multiplier, which is capable of generating the fast sampling clock for the DAC from the data input clock signal. However, the process of the DAC is usually not optimized for best phase noise performance, while the CDC7005 is optimized exactly for this. The CDC7005 therefore provides the preferred clocking scheme for the DAC5686. The DAC5686 demands that the edges of the two input clocks must be phase aligned within ±500 ps for latching the data properly. This phase alignment is well achieved with the CDC7005, which assures a maximum skew of 200 ps of the different different outputs to each other.

APPLICATION INFORMATION

Another advantage of this clock solution is that the ADC or DAC can be driven directly in an ac-coupling interface as shown in Figure 9, with an external termination in a differential configuration. There is no need for a transformer to generate a differential signal from a single-ended clock source.

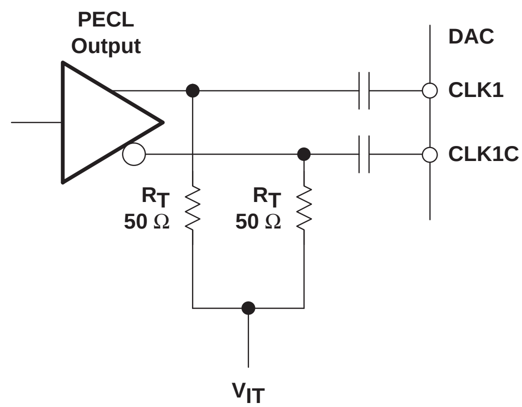


Figure 9. Driving DAC or ADC with PECL Output of the CDC7005

PARAMETER MEASUREMENT INFORMATION

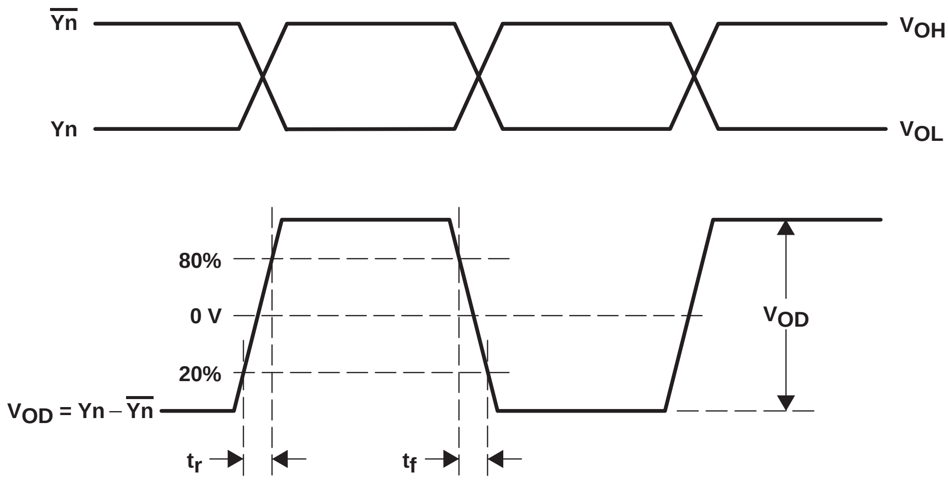


Figure 10. LVPECL Differential Output Voltage and Rise/Fall Time

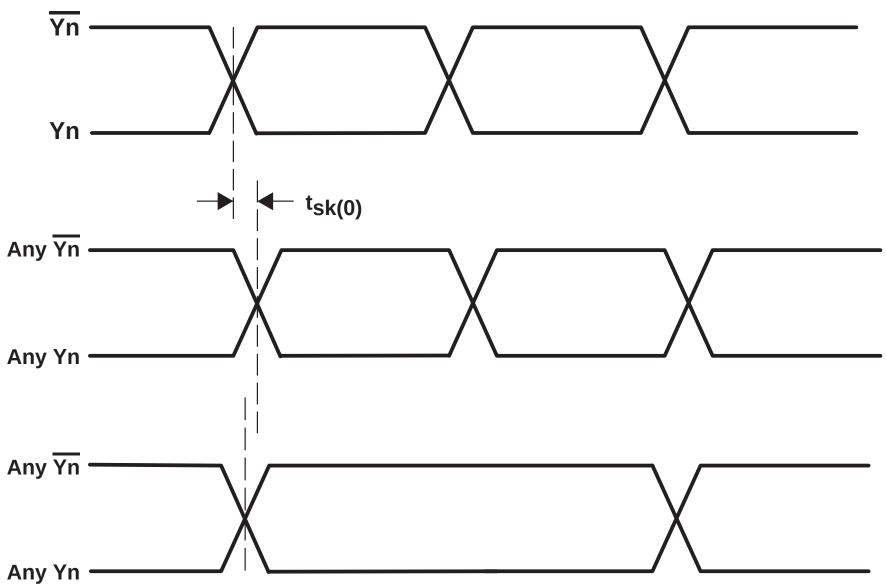


Figure 11. Output Skew

PARAMETER MEASUREMENT INFORMATION

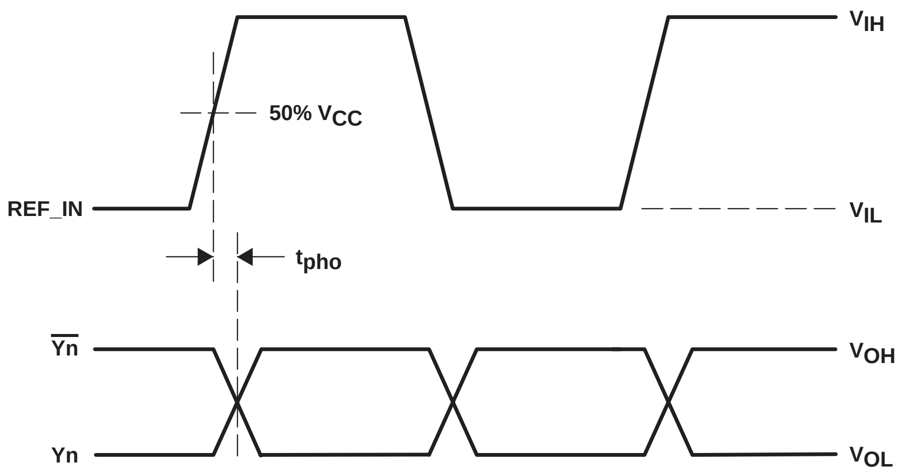


Figure 12. Phase Offset

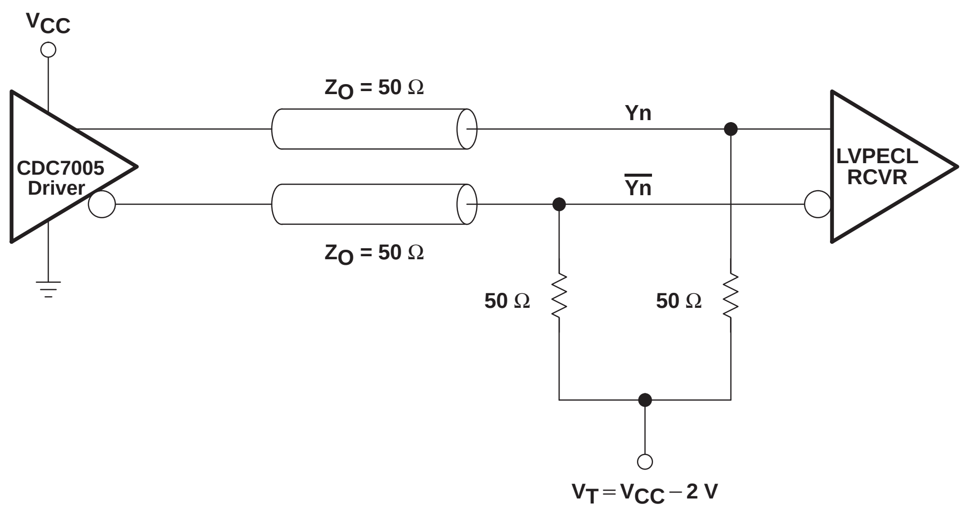


Figure 13. Typical Termination for Output Driver

PARAMETER MEASUREMENT INFORMATION

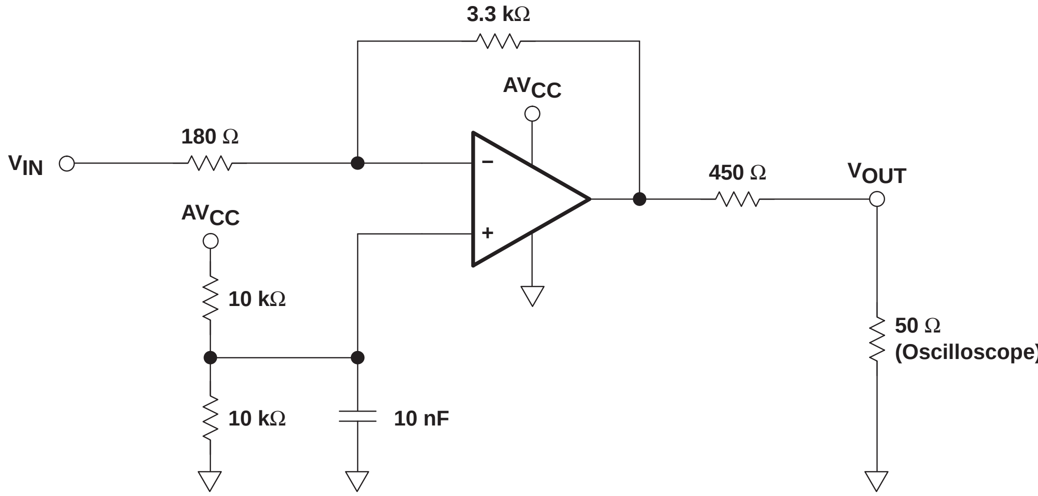
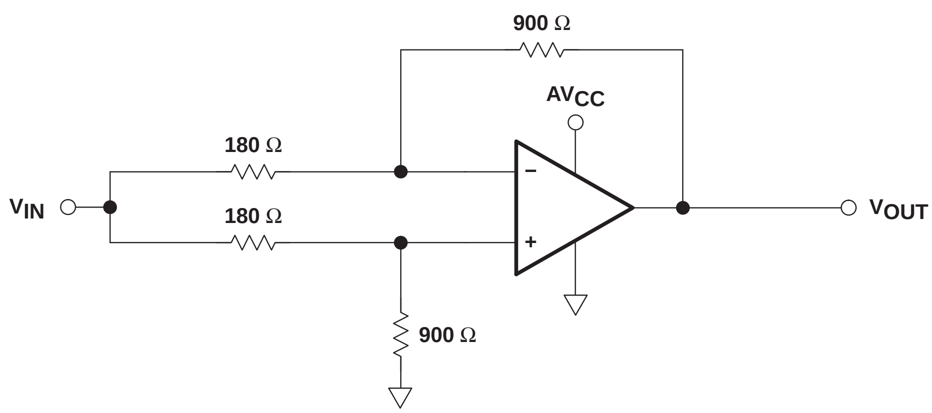
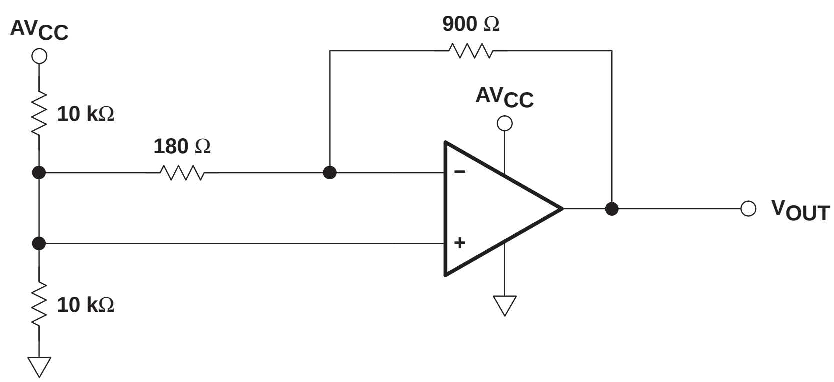


Figure 14. OPA Slew Rate/Gain Bandwidth Test Circuit



NOTE: CMRR (dB) = 20 x Log (V_{IN}/(V_{IN} − V_{OUT})) x (1 + 900/180)

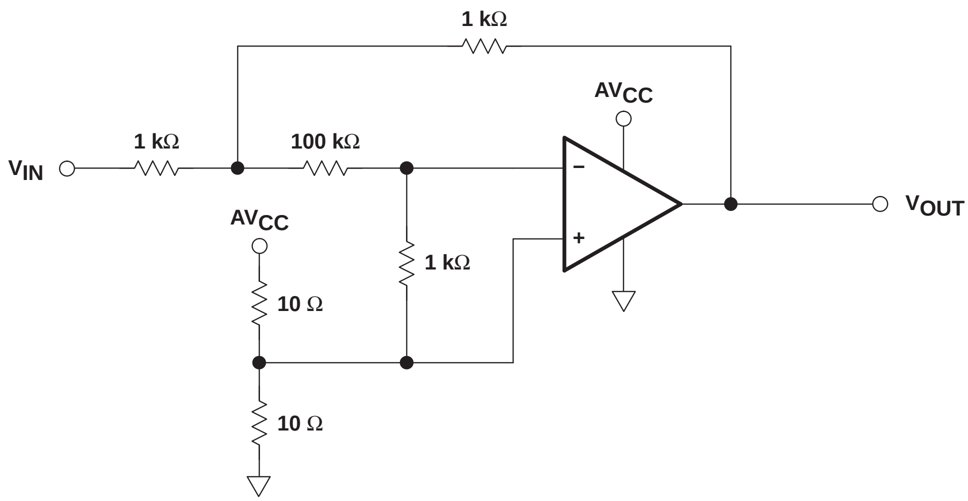
Figure 15. CMRR Test Circuits



NOTE: PSRR (dB) = (ΔAV_{CC}/V_{OUT}) x (900/180)

Figure 16. PSRR Test Circuit

PARAMETER MEASUREMENT INFORMATION



NOTE: $A_{(OL)} = (V_{IN} / V_{OUT}) \times (1 + 100\ k\Omega/1\ k\Omega)$

Figure 17. Open Loop Voltage Gain Test Circuit

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDC7005RGZ	PREVIEW	VQFN	RGZ	48		TBD	Call TI	Call TI	-40 to 85		
CDC7005RGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 85	CDC7005	Samples
CDC7005RGZRG4	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	-40 to 85	CDC7005	Samples
CDC7005RGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 85	CDC7005	Samples
CDC7005RGZTG4	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	-40 to 85	CDC7005	Samples
CDC7005ZVA	ACTIVE	BGA	ZVA	64	348	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR	-40 to 85	CK7005Z	Samples
CDC7005ZVAR	ACTIVE	BGA	ZVA	64	1000	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR	-40 to 85	CK7005Z	Samples
CDC7005ZVAT	ACTIVE	BGA	ZVA	64	250	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR	-40 to 85	CK7005Z	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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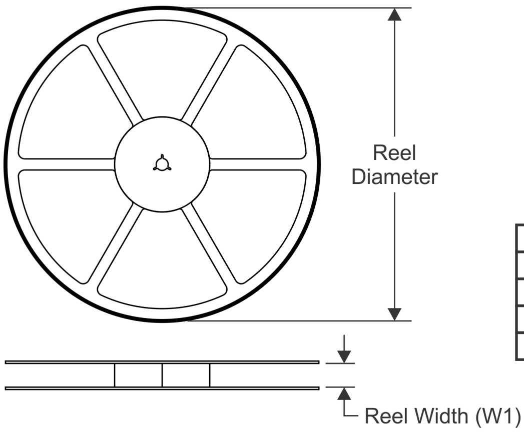
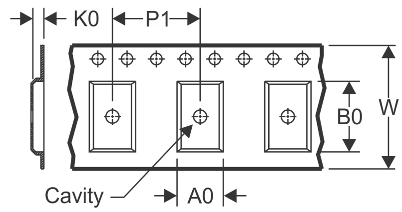
TAPE AND REEL INFORMATION

REEL DIMENSIONS

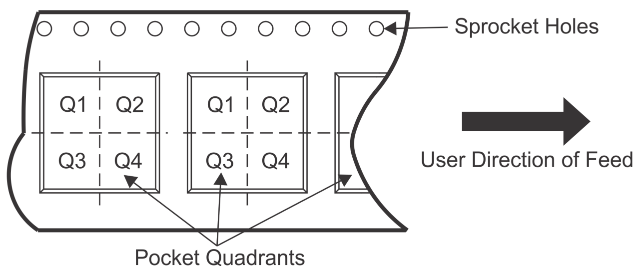


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

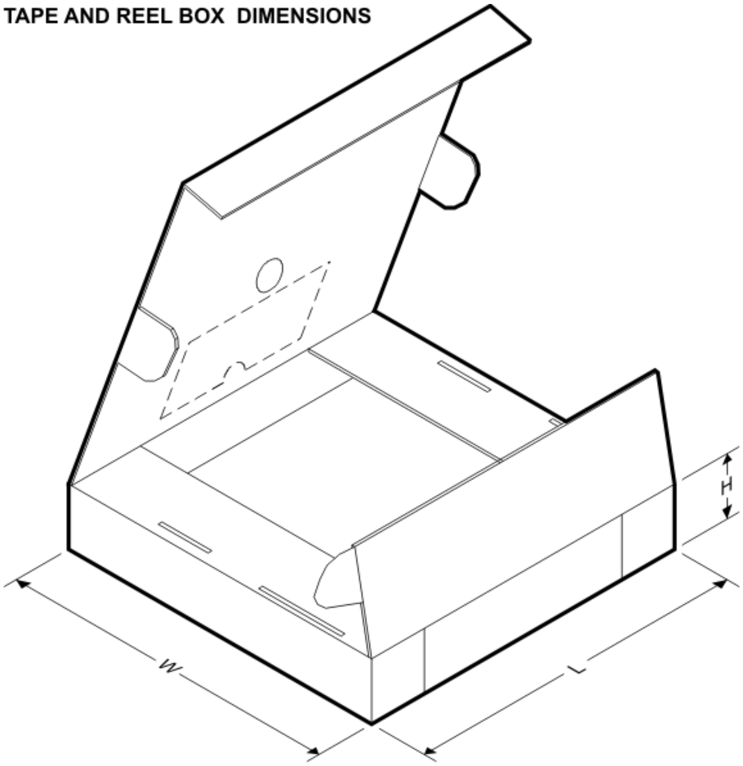
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDC7005RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
CDC7005RGZT	VQFN	RGZ	48	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
CDC7005ZVAR	BGA	ZVA	64	1000	330.0	16.4	8.3	8.3	2.25	12.0	16.0	Q1
CDC7005ZVAT	BGA	ZVA	64	250	330.0	16.4	8.3	8.3	2.25	12.0	16.0	Q1

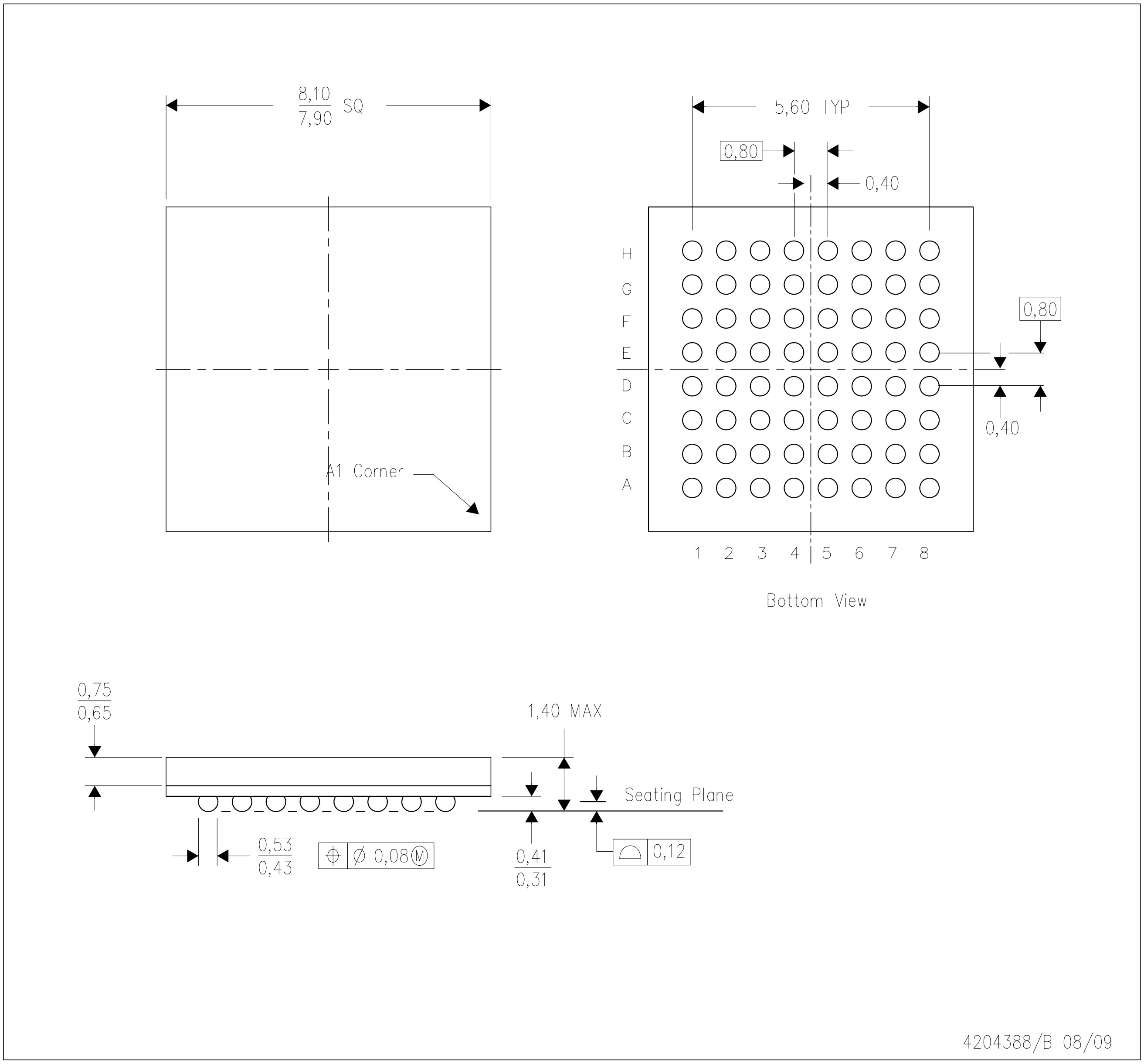
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

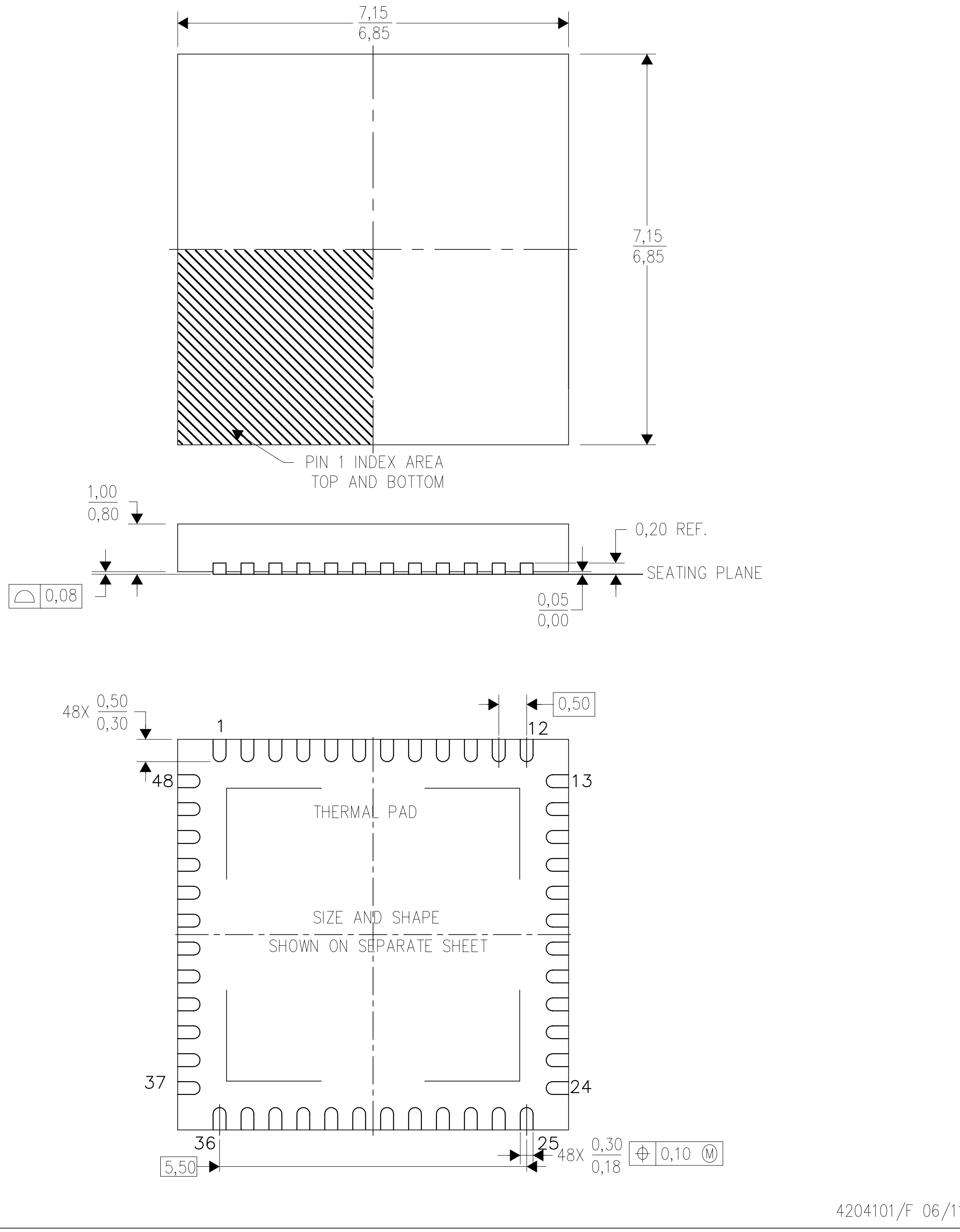
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDC7005RGZR	VQFN	RGZ	48	2500	336.6	336.6	28.6
CDC7005RGZT	VQFN	RGZ	48	250	336.6	336.6	28.6
CDC7005ZVAR	BGA	ZVA	64	1000	336.6	336.6	28.6
CDC7005ZVAT	BGA	ZVA	64	250	336.6	336.6	28.6

ZVA (S–PBGA–N64) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This is a Pb–free package.

RGZ (S-PVQFN-N48) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No—leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO—220.

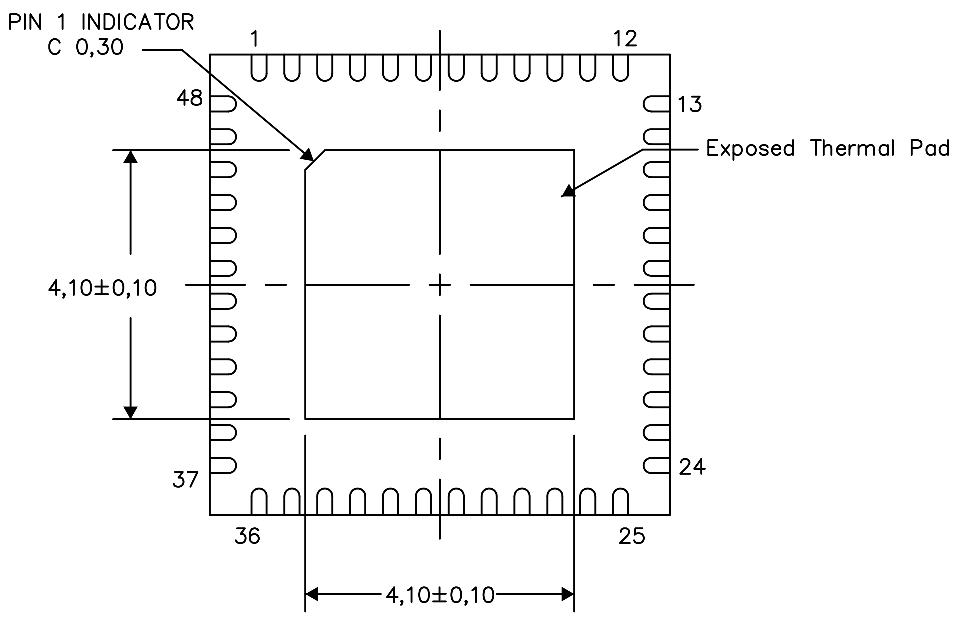
RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206354-3/W 09/13

NOTE: All linear dimensions are in millimeters

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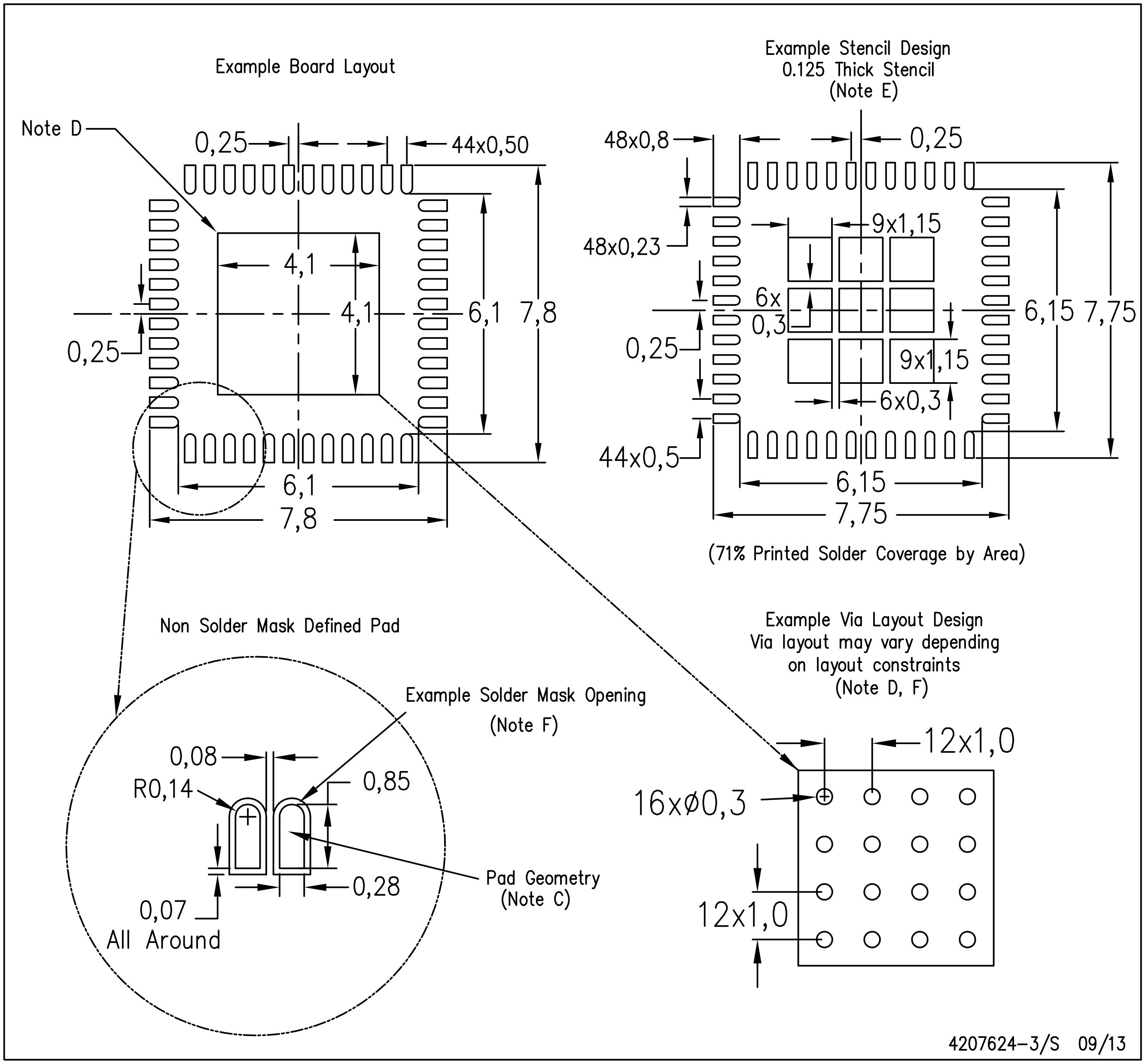

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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