CLC007 Serial Digital Cable Driver with Dual Complementary Outputs

Check for Samples: CLC007

FEATURES

- **No External Pull-Down Resistors**
- **Differential Input and Output**
- **Low Power Dissipation**
- **Single +5V or −5.2V Supply**
- **Replaces GS9007 in Most Applications**

APPLICATIONS

- **Digital Routers and Distribution Amplifiers**
- **Coaxial Cable Driver for Digital Transmission Line**
- **Twisted Pair Driver**
- **Digital Distribution Amplifiers**
- **SMPTE, Sonet/SDH, and ATM Compatible Driver**
- **Buffer Applications**

KEY SPECIFICATION

- **650 ps Rise and Fall Times**
- **Data Rates to 400 Mbps**
- **2 Sets of Complimentary Outputs**
- **200 mV Differential Input**
- **Low Residual Jitter (25 ps_{pp})**

DESCRIPTION

The Texas Instruments Comlinear CLC007 is a monolithic, high-speed cable driver designed for the SMPTE 259M serial digital video data transmission standard. The CLC007 drives 75Ω transmission lines (Belden 8281 or equivalent) at data rates up to 400 Mbps. Controlled output rise and fall times (750 ps typical) minimize transition-induced jitter. The output voltage swing, typically 1.65V, set by an accurate, low-drift internal bandgap reference, delivers an 800 mV swing to back-matched and terminated 75Ω cable.

The CLC007's class AB output stage consumes less power than other designs, 195 mW with all outputs terminated, and requires no external bias resistors. The differential inputs accept a wide range of digital signals from 200 mV_{P-P} to ECL levels within the specified common-mode limits. All this make the CLC007 an excellent general purpose high speed driver for digital applications.

The CLC007 is powered from a single +5V or −5.2V supply and comes in an 8-pin SOIC package.

270 Mbps Eye Pattern

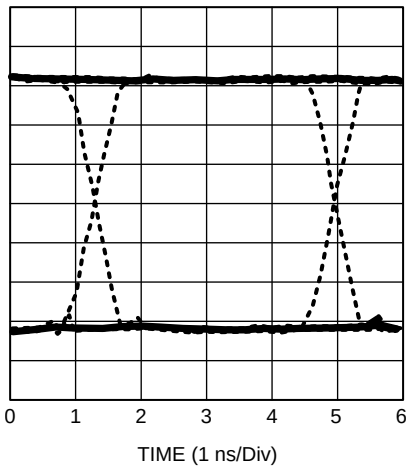


Figure 1.

Connection Diagram

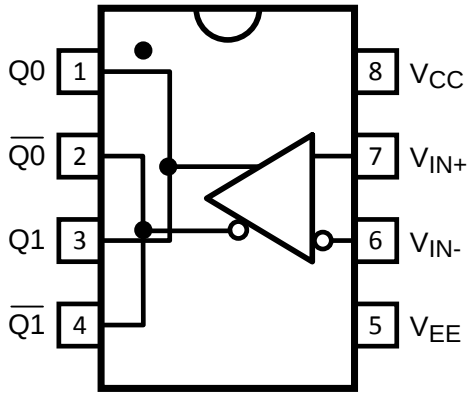
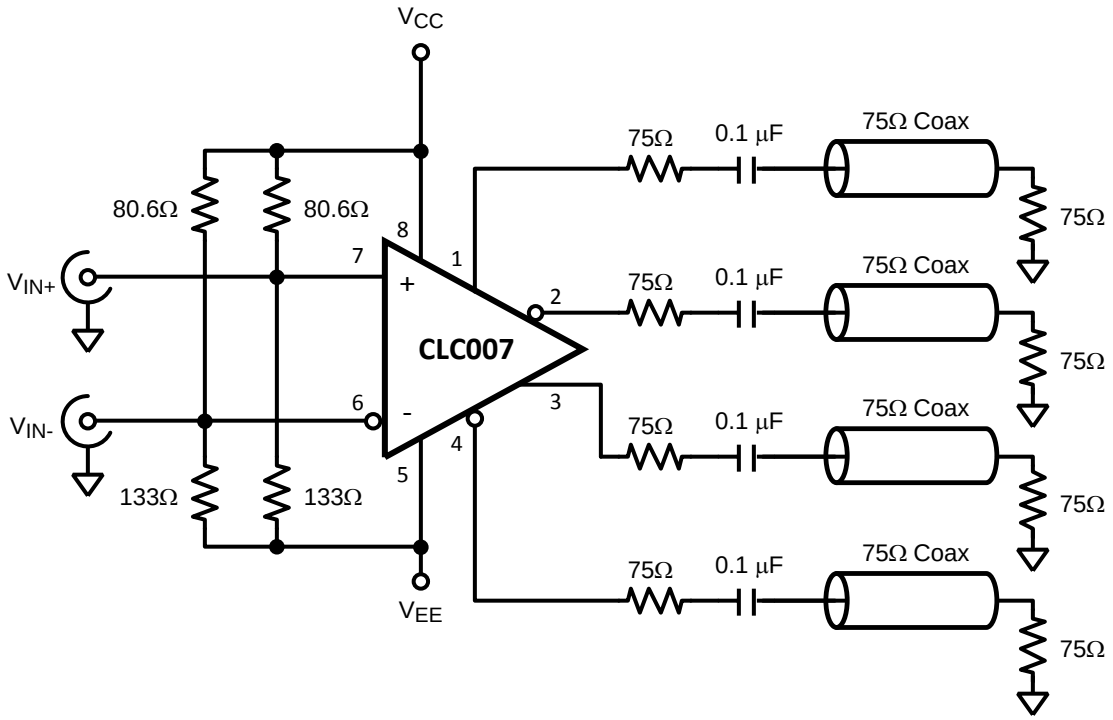


Figure 2. 8-Pin SOIC
See D Package

Typical Application



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)(2)

Supply Voltage		6V
Output Current		30 mA
Maximum Junction Temperature		+125°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering 10 Second)		+300°C
ESD Rating (Human body Model)		1000V
Package Thermal Resistance	θ_{JA} 8–pin SOIC	+160°C
	θ_{JC} 8–pin SOIC	+105°C/W
Reliability Information	MTTF	254 Mhr

(1) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. The table of ELECTRICAL CHARACTERISTICS specifies conditions of device operation.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage (V_{CC} – V_{EE})	+4.5V to +5.5V

ELECTRICAL CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = −5V; unless otherwise specified).

Parameter	Conditions	Typ +25°C	Min/Max +25°C	Min/Max 0°C to+70°C	Min/Max −40°C to +85°C	Units
STATIC PERFORMANCE						
Supply Current, Loaded	See (1)	39	—	—	—	mA
Supply Current, Unloaded	See (2)	34	28/45	26/47	26/47	mA
Output HIGH Voltage (V_{OH})	See (2)	−1.7	−2.0/1.4	−2.0/1.4	−2.0/1.4	V
Output Low Voltage (V_{OL})	See (2)	−3.3	−3.6/3.0	−3.6/3.0	−3.6/3.0	V
Input Bias Current		10	30	50	50	µA
Output Swing	See (2)	1.65	1.55/1.75	1.53/1.77	1.51/1.79	V
Common Mode Input Range Upper Limit		−0.7	−0.8	−0.8	−0.8	V
Common Mode Input Range Lower Limit		−2.6	−2.5	−2.5	−2.5	V
Minimum Differential Input Swing		200	200	200	200	mV
Power Supply Rejection Ratio (2)		26	20	20	20	dB
AC PERFORMANCE						
Output Rise and Fall Time	See (1)(2)(3)	650	425/955	400/1100	400/1100	ps
Overshoot		5				%
Propagation Delay		1.0				ns
Duty Cycle Distortion		50				ps
Residual Jitter		25	—	—	—	ps_{pp}
MISCELLANEOUS PERFORMANCE						
Input Capacitance		1.0				pF
Output Resistance		10				Ω
Output Inductance		6				nH

(1) Measured with both outputs driving 150Ω, AC coupled at 270 Mbps.
(2) Spec is 100% tested at +25°C
(3) Measured between the 20% and 80% levels of the waveform.

OPERATION

Input Interfacing

The CLC007 has high impedance, emitter-follower buffered, differential inputs. Single-ended signals may also be input. Transmission lines supplying input signals must be properly terminated close to the CLC007. Either A.C. or D.C. coupling as in Figure 4 or Figure 5 may be used. Figure 4, Figure 6, and Figure 7 show how Thevenin-equivalent resistor networks are used to provide input termination and biasing. The input D.C. common-mode voltage range is 0.8V to 2.5V below the positive power supply (V_{CC}). Input signals plus bias should be kept within the specified common-mode range. For an 800 mV_{P-P} input signal, typical input bias levels range from 1.2V to 2.1V below the positive supply.

Load Type	Resistor to V_{CC} (R1)	Resistor to V_{EE} (R2)
ECL, 50Ω, 5V, V_T=2V	82.5Ω	124Ω
ECL, 50Ω, 5.2V, V_T=2V	80.6Ω	133Ω
ECL, 75Ω, 5V, V_T=2V	124Ω	187Ω
ECL, 75Ω, 5.2V, V_T=2V	121Ω	196Ω
800 mV_{P-P}, 50Ω, 5V, V_T=1.6V	75.0Ω	154Ω
800 mV_{P-P}, 75Ω, 5V, V_T=1.6V	110Ω	232Ω
800 mV_{P-P}, 2.2 KΩ, 5V, V_T=1.6V	3240Ω	6810Ω

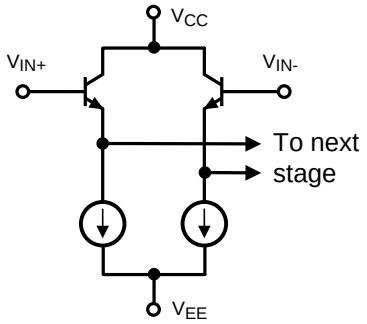


Figure 3. Input Stage

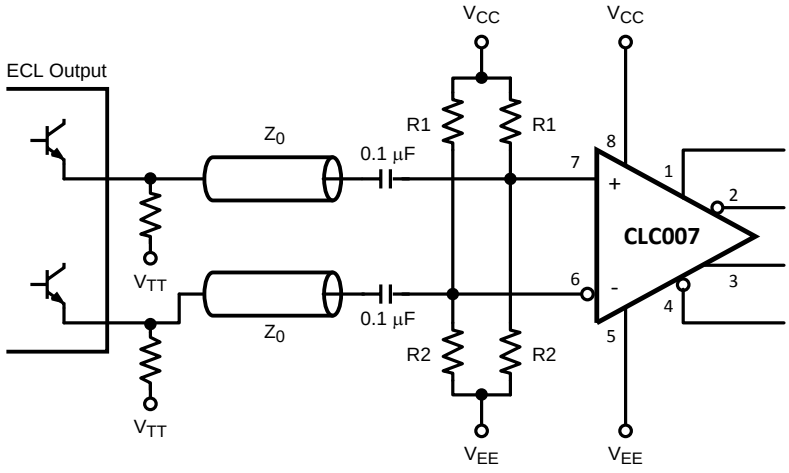


Figure 4. AC Coupled Input

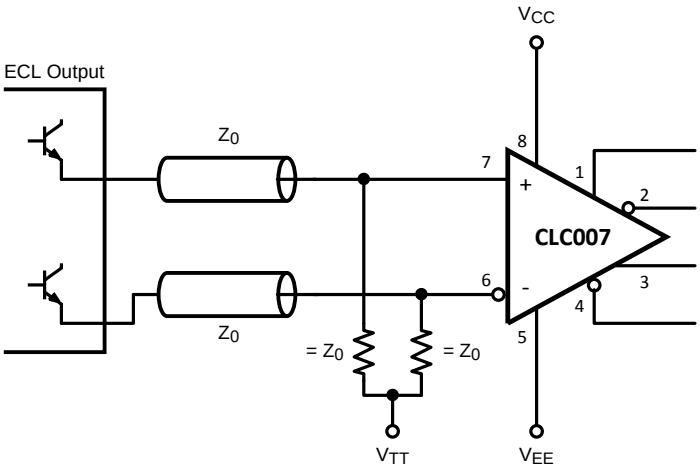


Figure 5. DC Coupled Input

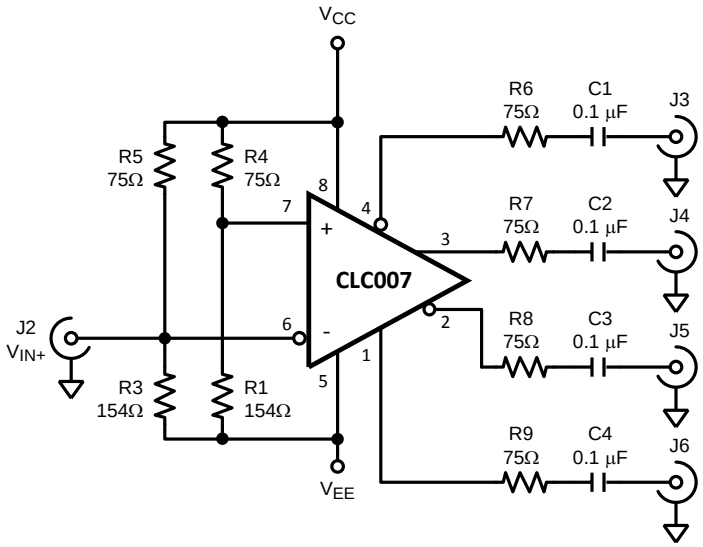


Figure 6. Single Ended 50Ω ECL Input

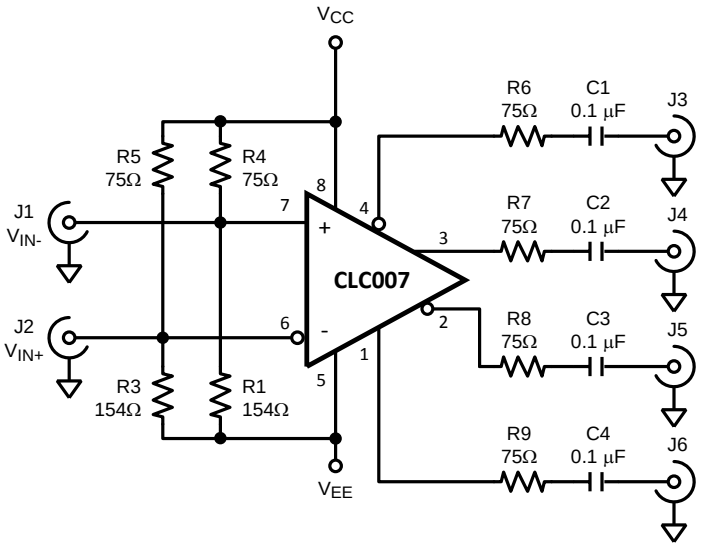


Figure 7. Differential 50Ω ECL Input

Output Interfacing

The CLC007's class AB output stage, Figure 8, requires no standing current in the output transistors and therefore requires no biasing or pull-down resistors. Advantages of this arrangement are lower power dissipation and fewer external components. The output may be either D.C. or A.C. coupled to the load. A bandgap voltage reference sets output voltage levels which are compatible with F100K and 10K ECL when correctly terminated. The outputs do not have the same output voltage temperature coefficient as 10K. Therefore, noise margins will be reduced over the full temperature range when driving 10K ECL. Noise margins will not be affected when interfacing to F100K since F100K is fully voltage and temperature compensated.

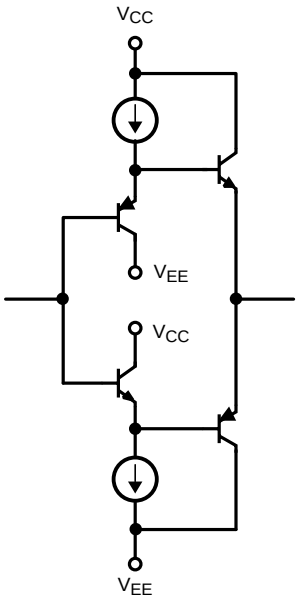


Figure 8. Output Stage

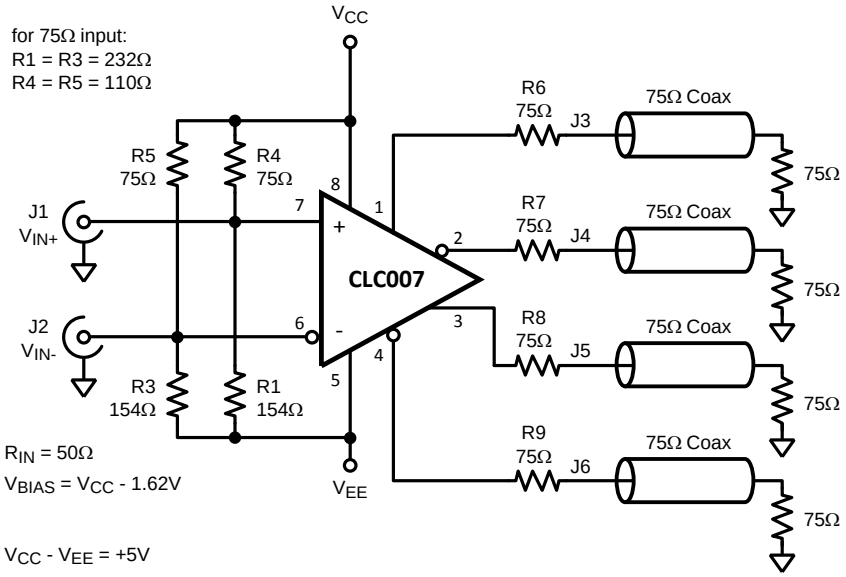


Figure 9. Differential Input DC Coupled Output

Output Rise And Fall Times

Output load capacitance can significantly affect output rise and fall times. The effect of load capacitance, stray or otherwise, may be reduced by placing the output back-match resistor close to the output pin and by minimizing all interconnecting trace lengths. Figure 10 shows the effect on risetime of parallel load capacitance across a 150Ω load.

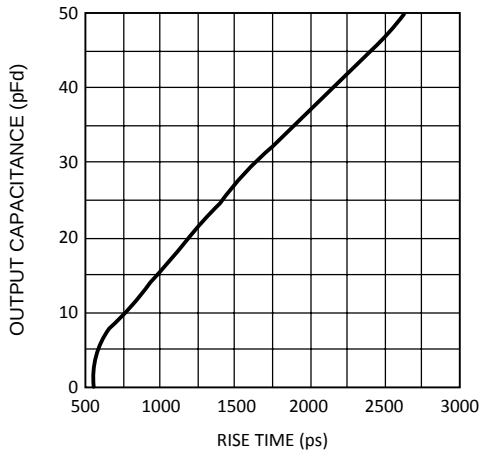


Figure 10. Rise Time vs C_L

PCB Layout Recommendations

Printed circuit board layout affects the performance of the CLC007. The following guidelines will aid in achieving satisfactory device performance.

- Use a ground plane or power/ground plane sandwich design for optimum performance.
- Bypass device power with a 0.01 µF monolithic ceramic capacitor in parallel with a 6.8 µF tantalum electrolytic capacitor located no more than 0.1” (2.5 mm) from the device power pins.
- Provide short, symmetrical ground return paths for:
  - Inputs,
  - Supply bypass capacitors and
  - The output load.
- Provide short, grounded guard traces located
  - Under the centerline of the package,
  - 0.1” (2.5 mm) from the package pins
  - On both top and bottom of the board with connecting vias.

REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	8

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CLC007BM	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	CLC00 7BM>D	
CLC007BM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	CLC00 7BM>D	Samples
CLC007BMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	CLC00 7BM>D	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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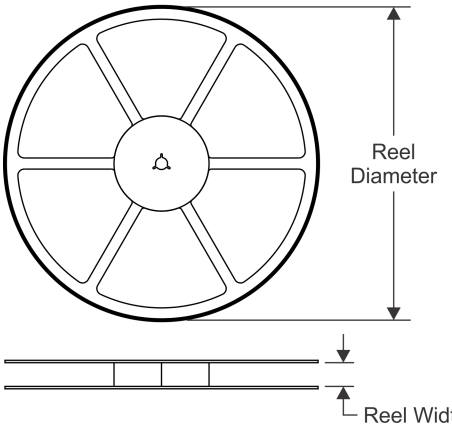
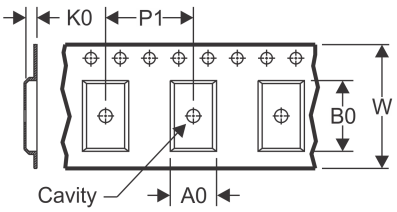
TAPE AND REEL INFORMATION

REEL DIMENSIONS

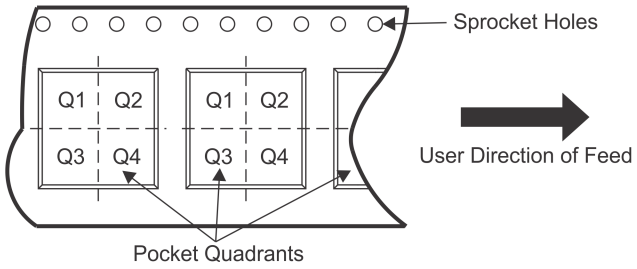


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

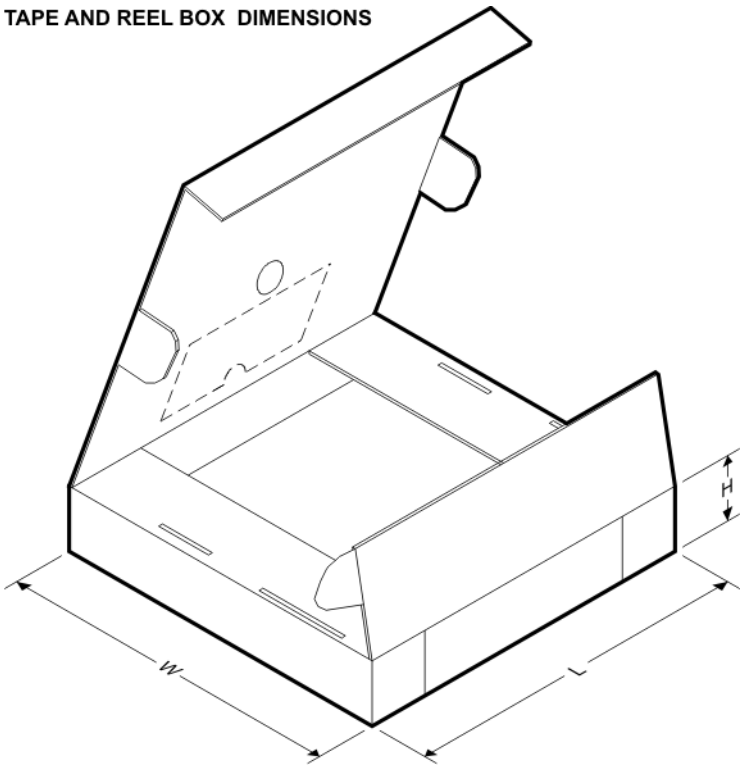
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CLC007BMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

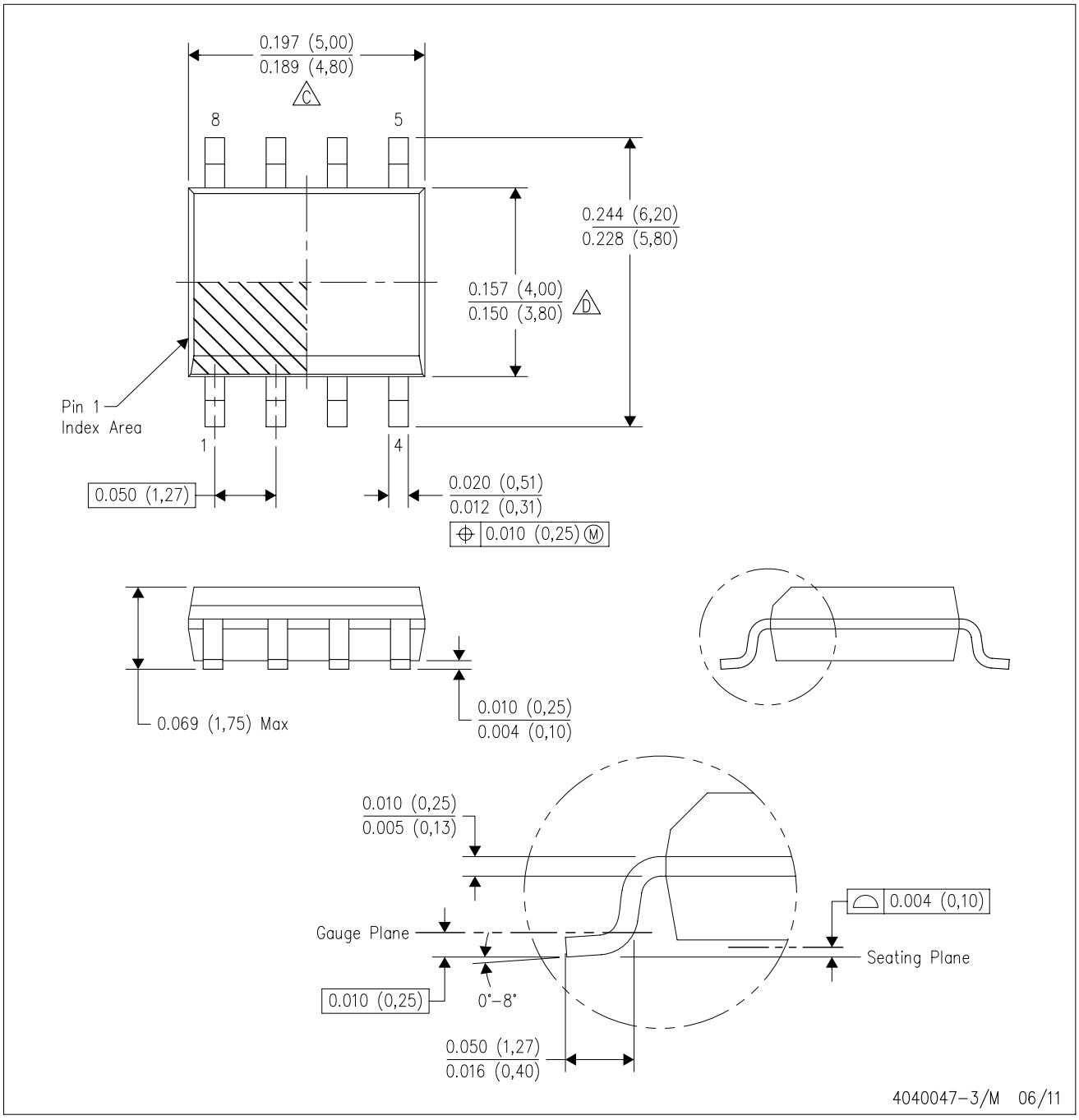
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CLC007BMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265