IGBT SIP Module (Ultrafast IGBT)

IMS-2

PRODUCT SUMMARY	
OUTPUT CURRENT IN A TYPICAL 20 kHz MOTOR DRIVE	
I_{RMS} per phase (2.1 kW total) with T_C = 90 °C	7.1 A_{RMS}
T_J	125 °C
Supply voltage	360 V_{DC}
Power factor	0.8
Modulation depth (see fig. 1)	115 %
$V_{CE(on)}$ (typical) at I_C = 6.8 A, 25 °C	1.7 V
Package	SIP
Circuit	Three Phase Inverter

FEATURES

- Fully isolated printed circuit board mount package
- Switching-loss rating includes all "tail" losses
- HEXFRED® soft ultrafast diodes
- Optimized for medium speed 1 to 10 kHz See fig. 1 for current vs. frequency curve
- UL approved file E78996
- Designed and qualified for industrial level
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS COMPLIANT

DESCRIPTION

The IGBT technology is the key to Vishay's Semiconductors advanced line of IMS (Insulated Metal Substrate) power modules. These modules are more efficient than comparable bipolar transistor modules, while at the same time having the simpler gate-drive requirements of the familiar power MOSFET. This superior technology has now been coupled to a state of the art materials system that maximizes power throughput with low thermal resistance. This package is highly suited to motor drive applications and where space is at a premium.

ABSOLUTE MAXIMUM RATINGS				
PARAMETER	SYMBOL	TEST CONDITIONS	MAX.	UNITS
Collector to emitter voltage	V_{CES}		600	V
Continuous collector current, each IGBT	I_C	T_C = 25 °C	13	A
		T_C = 100 °C	6.8	
Pulsed collector current	I_{CM} (1)		40	
Clamped inductive load current	I_{LM} (2)		40	
Diode continuous forward current	I_F	T_C = 100 °C	6.1	
Diode maximum forward current	I_{FM}		40	
Gate to emitter voltage	V_{GE}		± 20	V
Isolation voltage	V_{ISOL}	Any terminal to case, t = 1 min	2500	V_{RMS}
Maximum power dissipation, each IGBT	P_D	T_C = 25 °C	36	W
		T_C = 100 °C	14	
Operating junction and storage temperature range	T_J, T_{Stg}		- 40 to + 150	°C
Soldering temperature		For 10 s, (0.063" (1.6 mm) from case)	300	
Mounting torque		6-32 or M3 screw	5 to 7 (0.55 to 0.8)	lbf · in (N · m)

Notes

(1) Repetitive rating; V_{GE} = 20 V, pulse width limited by maximum junction temperature (see fig. 20)

(2) V_{CC} = 80 % (V_{CES}), V_{GE} = 20 V, L = 10 μH, R_G = 23 Ω (see fig. 19)

<table>
<tr><th colspan="5">THERMAL AND MECHANICAL SPECIFICATIONS</th></tr>
<tr><th>PARAMETER</th><th>SYMBOL</th><th>TYP.</th><th>MAX.</th><th>UNITS</th></tr>
<tr><td>Junction to case, each IGBT, one IGBT in conduction</td><td>R_{thJC} (IGBT)</td><td>-</td><td>3.5</td><td rowspan="3">°C/W</td></tr>
<tr><td>Junction to case, each DIODE, one DIODE in conduction</td><td>R_{thJC} (DIODE)</td><td>-</td><td>5.5</td></tr>
<tr><td>Case to sink, flat, greased surface</td><td>R_{thCS} (MODULE)</td><td>0.10</td><td>-</td></tr>
<tr><td rowspan="2">Weight of module</td><td rowspan="2"></td><td>20</td><td>-</td><td>g</td></tr>
<tr><td>0.7</td><td>-</td><td>oz.</td></tr>
</table>

<table>
<tr><th colspan="8">ELECTRICAL SPECIFICATIONS (T_J = 25 °C unless otherwise specified)</th></tr>
<tr><th>PARAMETER</th><th>SYMBOL</th><th colspan="2">TEST CONDITIONS</th><th>MIN.</th><th>TYP.</th><th>MAX.</th><th>UNITS</th></tr>
<tr><td>Collector to emitter breakdown voltage</td><td>$V_{(BR)CES}$ (1)</td><td colspan="2">V_{GE} = 0 V, I_C = 250 μA</td><td>600</td><td>-</td><td>-</td><td>V</td></tr>
<tr><td>Temperature coeff. of breakdown voltage</td><td>$\Delta V_{(BR)CES}/\Delta T_J$</td><td colspan="2">$V_{GE}$ = 0 V, I_C = 1.0 mA</td><td>-</td><td>0.63</td><td>-</td><td>V/°C</td></tr>
<tr><td rowspan="3">Collector to emitter saturation voltage</td><td rowspan="3">$V_{CE(on)}$</td><td>I_C = 6.8 A</td><td rowspan="3">V_{GE} = 15 V
See fig. 2, 5</td><td>-</td><td>1.70</td><td>2.2</td><td rowspan="4">V</td></tr>
<tr><td>I_C = 13 A</td><td>-</td><td>2.00</td><td>-</td></tr>
<tr><td>I_C = 6.8 A, T_J = 150 °C</td><td>-</td><td>1.70</td><td>-</td></tr>
<tr><td>Gate threshold voltage</td><td>$V_{GE(th)}$</td><td colspan="2" rowspan="2">V_{CE} = V_{GE}, I_C = 250 μA</td><td>3.0</td><td>-</td><td>6.0</td></tr>
<tr><td>Temperature coeff. of threshold voltage</td><td>$\Delta V_{GE(th)}/\Delta T_J$</td><td>-</td><td>- 11</td><td>-</td><td>mV/°C</td></tr>
<tr><td>Forward transconductance</td><td>g_{fe} (2)</td><td colspan="2">V_{CE} = 100 V, I_C = 6.8 A</td><td>4.0</td><td>6.0</td><td>-</td><td>S</td></tr>
<tr><td rowspan="2">Zero gate voltage collector current</td><td rowspan="2">I_{CES}</td><td colspan="2">V_{GE} = 0 V, V_{CE} = 600 V</td><td>-</td><td>-</td><td>250</td><td rowspan="2">μA</td></tr>
<tr><td colspan="2">V_{GE} = 0 V, V_{CE} = 600 V, T_J = 150 °C</td><td>-</td><td>-</td><td>2500</td></tr>
<tr><td rowspan="2">Diode forward voltage drop</td><td rowspan="2">V_{FM}</td><td>I_C = 12 A</td><td rowspan="2">See fig. 13</td><td>-</td><td>1.4</td><td>1.7</td><td rowspan="2">V</td></tr>
<tr><td>I_C = 12 A, T_J = 150 °C</td><td>-</td><td>1.3</td><td>1.6</td></tr>
<tr><td>Gate to emitter leakage current</td><td>I_{GES}</td><td colspan="2">V_{GE} = ± 20 V</td><td>-</td><td>-</td><td>± 100</td><td>nA</td></tr>
</table>

Notes

(1) Pulse width ≤ 80 μs, duty factor ≤ 0.1 %

(2) Pulse width 5.0 μs; single shot

SWITCHING CHARACTERISTICS (T_J = 25 °C unless otherwise specified)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Total gate charge (turn-on)	Q_g	I_C = 6.8 A V_{CC} = 400 V See fig. 8	-	53	79	nC
Gate to emitter charge (turn-on)	Q_{ge}		-	7.7	12	
Gate to collector charge (turn-on)	Q_{gc}		-	21	31	
Turn-on delay time	$t_{d(on)}$	T_J = 25 °C I_C = 6.8 A, V_{CC} = 480 V V_{GE} = 15 V, R_G = 23 Ω Energy losses include "tail" and diode reverse recovery. See fig. 9, 10, 11, 18	-	43	-	ns
Rise time	t_r		-	14	-	
Turn-off delay time	$t_{d(off)}$		-	95	140	
Fall time	t_f		-	83	190	
Turn-on switching loss	E_{on}		-	0.17	-	mJ
Turn-off switching loss	E_{off}		-	0.15	-	
Total switching loss	E_{ts}		-	0.32	0.45	
Turn-on delay time	$t_{d(on)}$	T_J = 150 °C I_C = 6.8 A, V_{CC} = 480 V V_{GE} = 15 V, R_G = 23 Ω Energy losses include "tail" and diode reverse recovery See fig. 9, 10, 11, 18	-	41	-	ns
Rise time	t_r		-	16	-	
Turn-off delay time	$t_{d(off)}$		-	110	-	
Fall time	t_f		-	230	-	
Total switching loss	E_{ts}		-	0.52	-	mJ
Input capacitance	C_{ies}	V_{GE} = 0 V V_{CC} = 30 V f = 1.0 MHz See fig. 7	-	1100	-	pF
Output capacitance	C_{oes}		-	73	-	
Reverse transfer capacitance	C_{res}		-	14	-	
Diode reverse recovery time	t_{rr}	T_J = 25 °C, See fig. 14, I_F = 12 A, V_R = 200 V, dI/dt = 200 A/μs	-	42	60	ns
		T_J = 125 °C, See fig. 14	-	83	120	
Diode peak reverse recovery charge	I_{rr}	T_J = 25 °C, See fig. 15	-	3.5	6.0	A
		T_J = 125 °C, See fig. 15	-	5.6	10	
Diode reverse recovery charge	Q_{rr}	T_J = 25 °C, See fig. 16	-	80	180	nC
		T_J = 125 °C, See fig. 16	-	220	600	
Diode peak rate of fall of recovery during t_b	$dI_{(rec)M}/dt$	T_J = 25 °C, See fig. 17	-	180	-	A/μs
		T_J = 125 °C, See fig. 17	-	116	-	

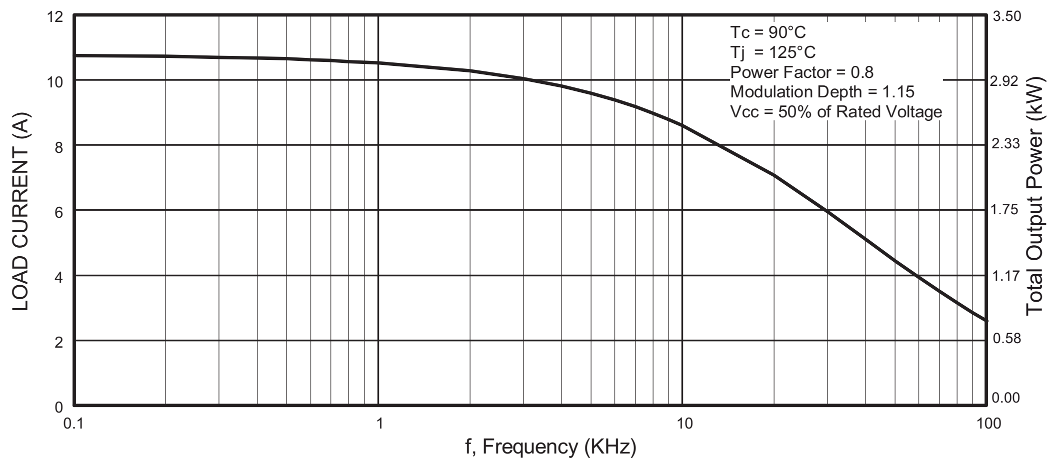


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of Fundamental)

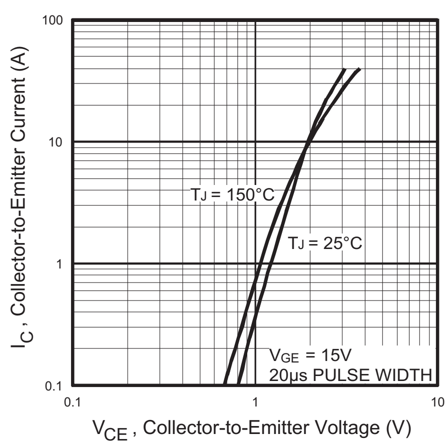


Fig. 2 - Typical Output Characteristics

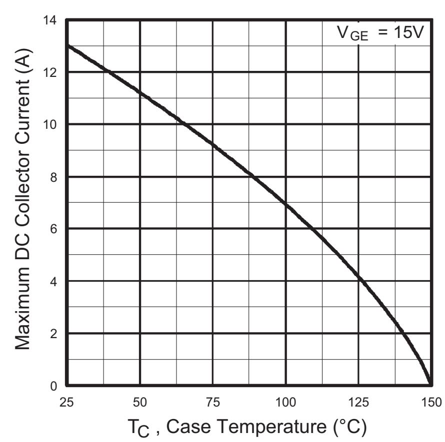


Fig. 4 - Maximum Collector Current vs. Case Temperature

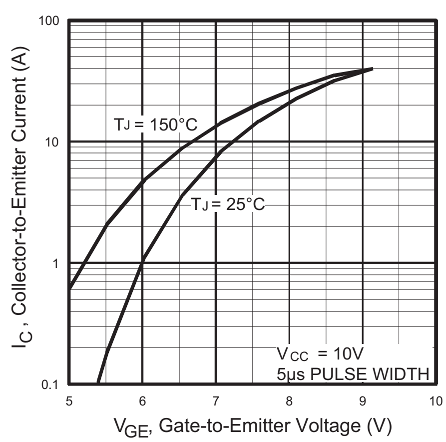


Fig. 3 - Typical Transfer Characteristics

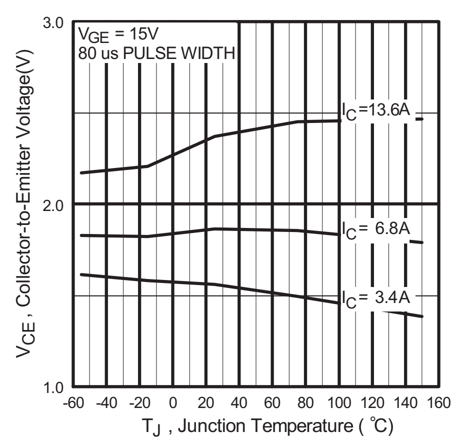


Fig. 5 - Typical Collector to Emitter Voltage vs. Junction Temperature

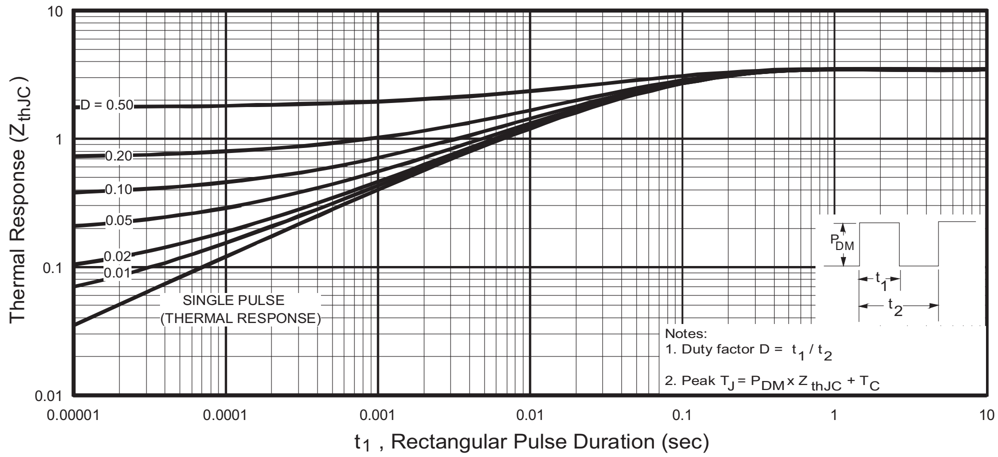


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction to Case

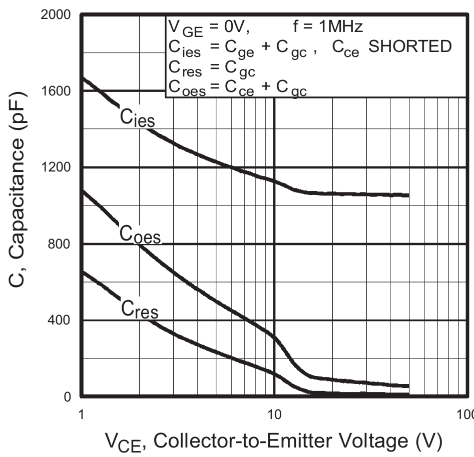


Fig. 7 - Typical Capacitance vs. Collector to Emitter Voltage

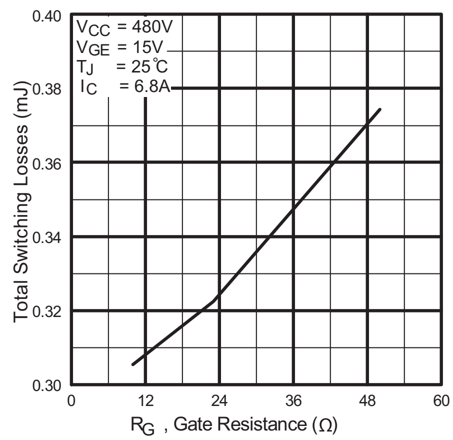


Fig. 9 - Typical Switching Losses vs. Gate Resistance

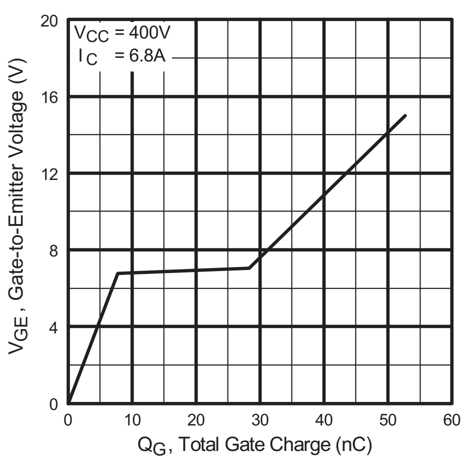


Fig. 8 - Typical Gate Charge vs. Gate to Emitter Voltage

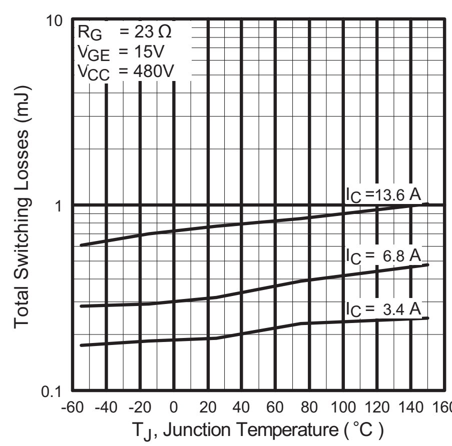


Fig. 10 - Typical Switching Losses vs. Junction Temperature

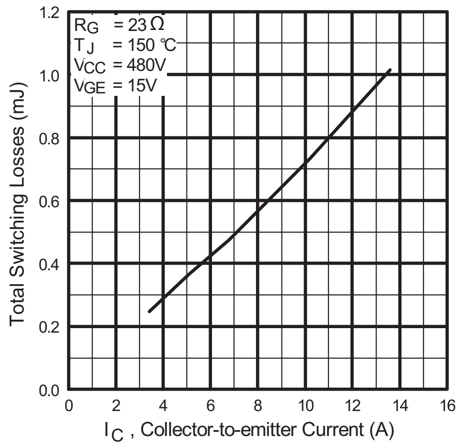


Fig. 11 - Typical Switching Losses vs. Collector to Emitter Current

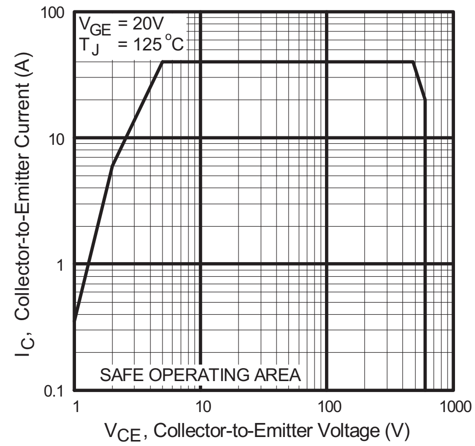


Fig. 12 - Turn-Off SOA

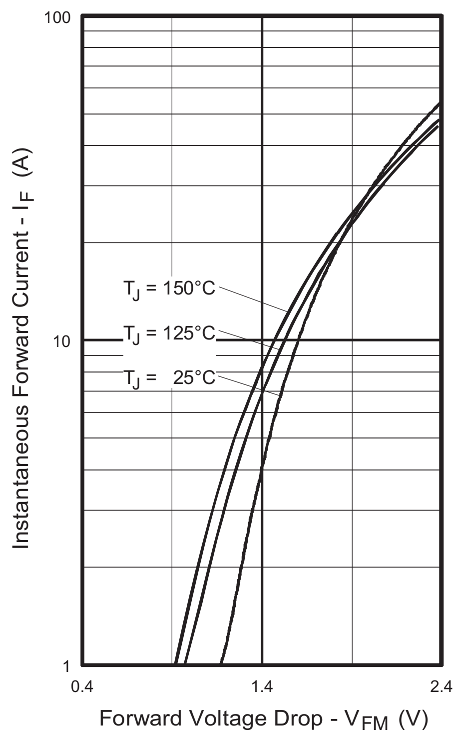


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

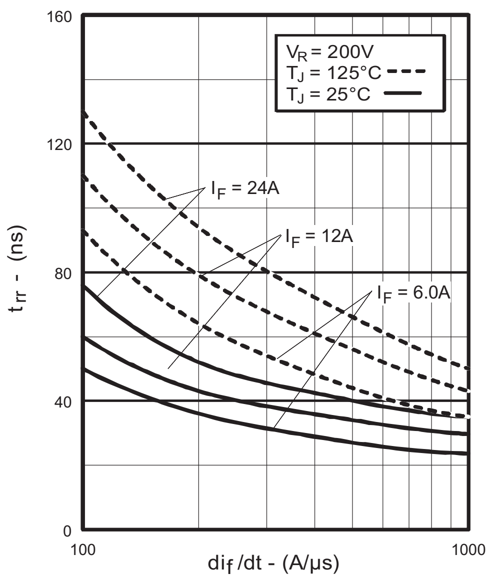


Fig. 14 - Typical Reverse Recovery Time vs. dI_F/dt

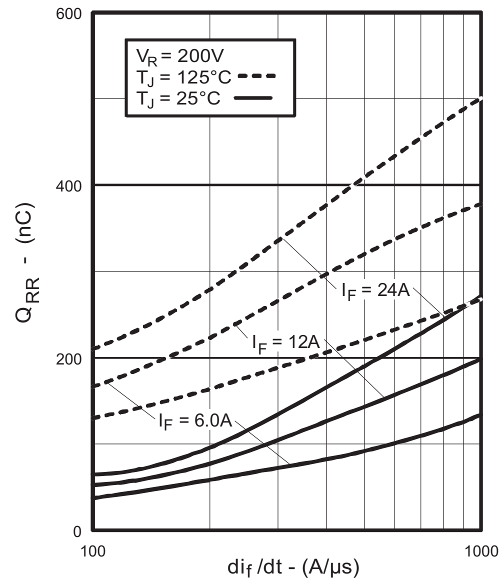


Fig. 16 - Typical Stored Charge vs. dI_F/dt

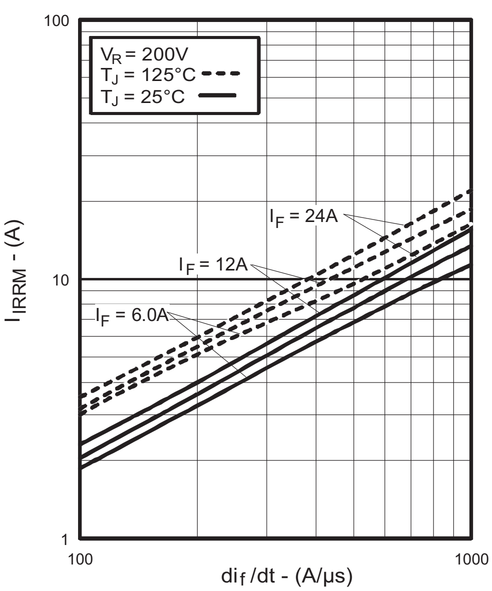


Fig. 15 - Typical Recovery Current vs. dI_F/dt

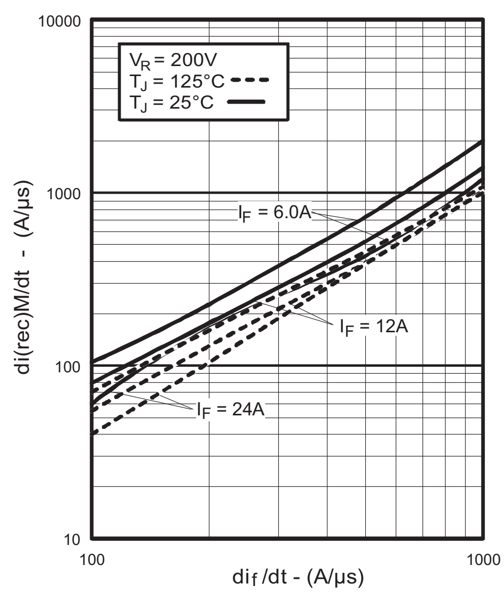


Fig. 17 - Typical $dI_{(rec)M}/dt$ vs dI_F/dt

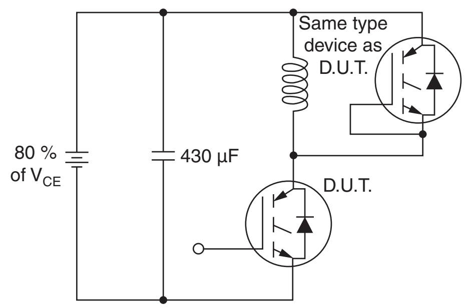


Fig. 18a - Test Circuit for Measurements of I_{LM}, E_{on}, $E_{off(diode)}$, t_{rr}, Q_{rr}, I_{rr}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

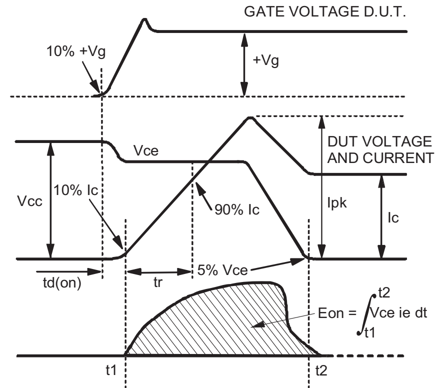


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on}, $t_{d(on)}$, t_r

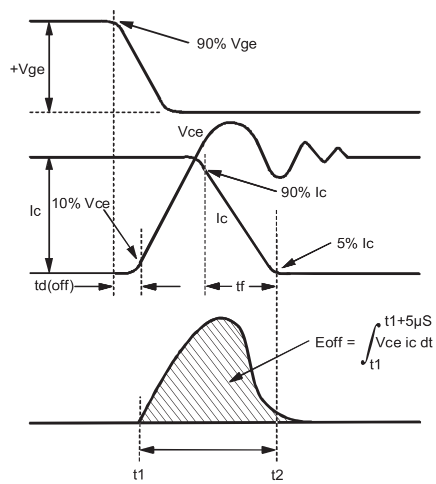


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off}, $t_{d(off)}$, t_f

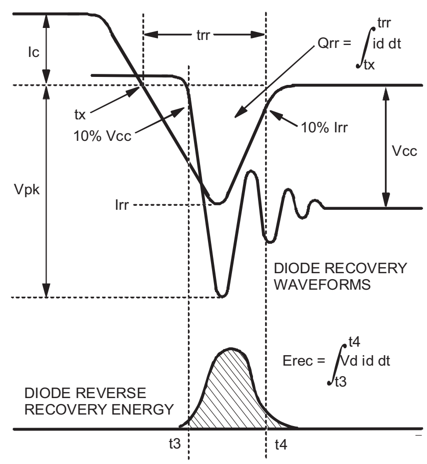


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec}, t_{rr}, Q_{rr}, I_{rr}

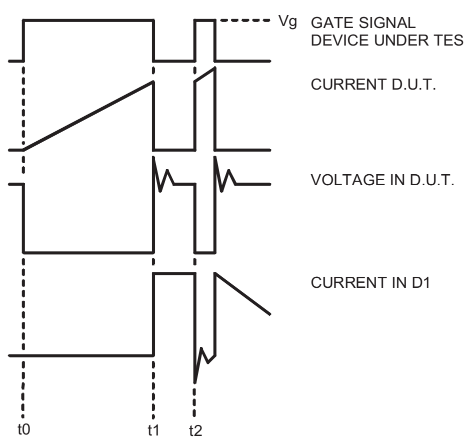


Fig. 18e - Macro Waveforms for Figure 18a's Test Circuit

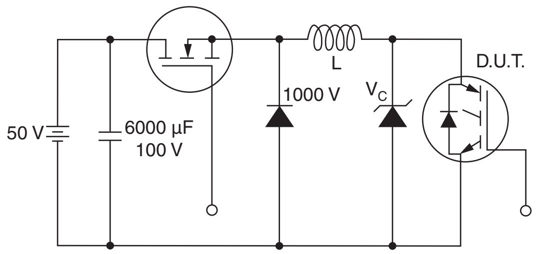


Fig. 19 - Clamped Inductive Load Test Circuit

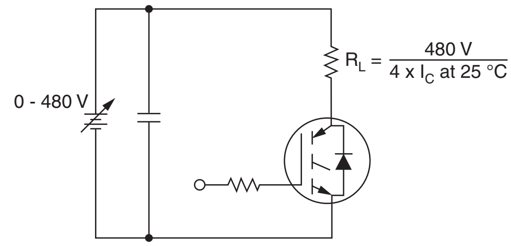
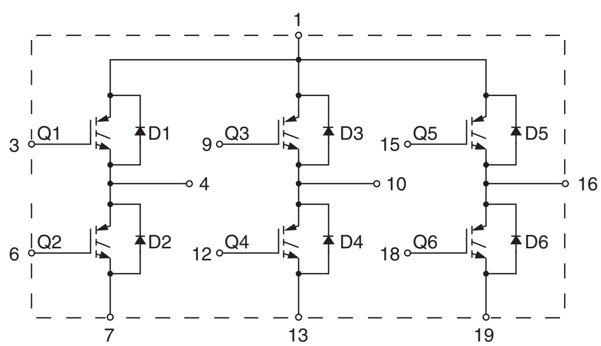


Fig. 20 - Pulsed Collector Current Test Circuit

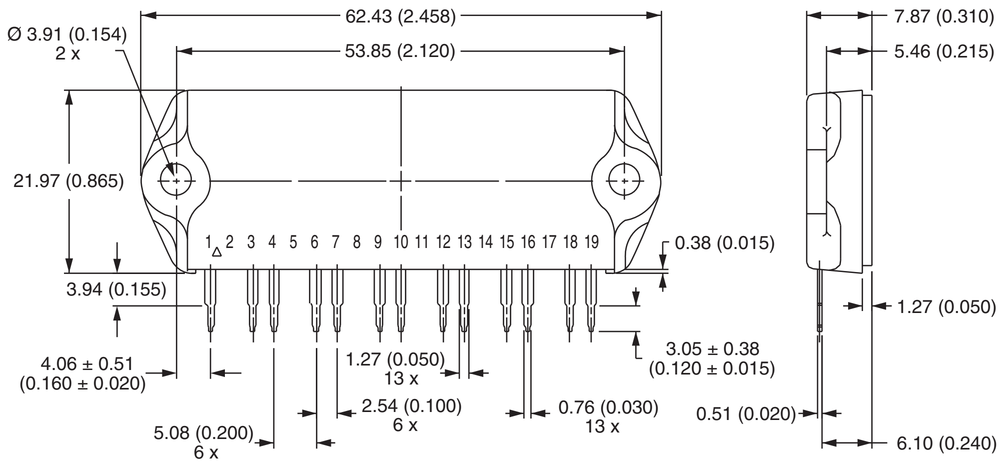
CIRCUIT CONFIGURATION



LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95066

IMS-2 (SIP)

DIMENSIONS in millimeters (inches)



IMS-2 Package Outline (13 Pins)

Notes

(1) Tolerance uless otherwise specified ± 0.254 mm (0.010")
(2) Controlling dimension: inch
(3) Terminal numbers are shown for reference only

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