60-V, N-Channel NexFET™ Power MOSFETs

Check for Samples: CSD18532NQ5B

FEATURES

- **Ultra Low Qg and Qgd**
- **Low Thermal Resistance**
- **Avalanche Rated**
- **Pb Free Terminal Plating**
- **RoHS Compliant**
- **Halogen Free**
- **SON 5-mm × 6-mm Plastic Package**

APPLICATIONS

- **DC-DC Conversion**
- **Secondary Side Synchronous Rectifier**
- **Isolated Converter Primary Side Switch**
- **Motor Control**

DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.

PRODUCT SUMMARY

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain to Source Voltage	60		V
Q_g	Gate Charge Total (10V)	49		nC
Q_{gd}	Gate Charge Gate to Drain	7.9		nC
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 6V	3.5	mΩ
		V_{GS} = 10V	2.7	mΩ
$V_{GS(th)}$	Threshold Voltage	2.8		V

ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD18532NQ5B	SON 5-mm × 6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

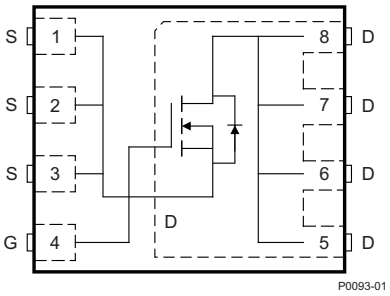
ABSOLUTE MAXIMUM RATINGS

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain to Source Voltage	60	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Continuous Drain Current (Package limited), T_C = 25°C	100	A
	Continuous Drain Current (Silicon limited), T_C = 25°C	163	
	Continuous Drain Current, T_A = 25°C(1)	22	
I_{DM}	Pulsed Drain Current, T_A = 25°C(2)	135	A
P_D	Power Dissipation(1)	3.2	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse I_D = 85A, L = 0.1mH, R_G = 25Ω	360	mJ

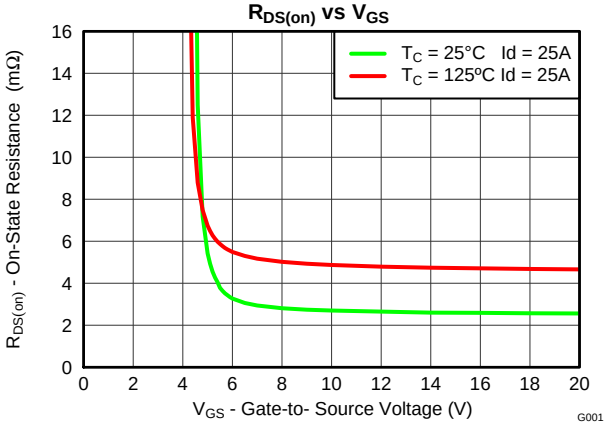
(1) Typical $R_{\theta JA}$ = 40°C/W on a 1-inch^2 , 2-oz. Cu pad on a 0.06-inch thick FR4 PCB.

(2) Pulse duration ≤300µs, duty cycle ≤2%

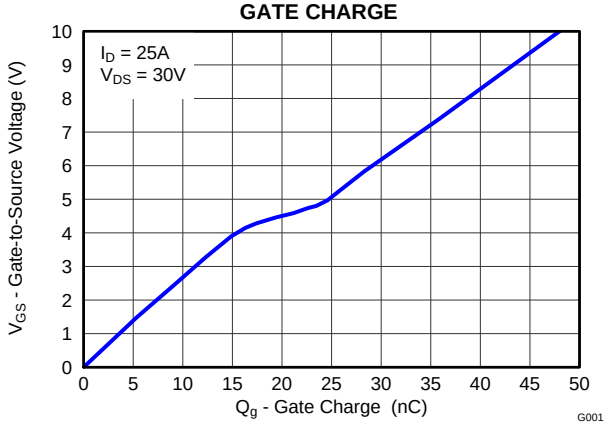
Top View



$R_{DS(on)}$ vs V_{GS}



GATE CHARGE



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

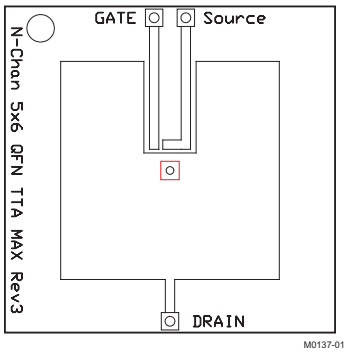
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	V_{GS} = 0V, I_D = 250µA	60			V
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0V, V_{DS} = 48V			1	µA
I_{GSS}	Gate to Source Leakage Current	V_{DS} = 0V, V_{GS} = 20V			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	2.4	2.8	3.4	V
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 6V, I_D = 25A		3.5	4.4	mΩ
		V_{GS} = 10V, I_D = 25A		2.7	3.4	mΩ
g_{fs}	Transconductance	V_{DS} = 30V, I_D = 25A		140		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS} = 30V, f = 1MHz		4100	5340	pF
C_{oss}	Output Capacitance			495	644	pF
C_{rss}	Reverse Transfer Capacitance			16	21	pF
R_G	Series Gate Resistance			1.2	2.4	Ω
Q_g	Gate Charge Total (10V)	V_{DS} = 30V, I_D = 25A		49	64	nC
Q_{gd}	Gate Charge Gate to Drain			7.9		nC
Q_{gs}	Gate Charge Gate to Source			16		nC
$Q_{g(th)}$	Gate Charge at Vth			11		nC
Q_{oss}	Output Charge	V_{DS} = 30V, V_{GS} = 0V		69		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 30V, V_{GS} = 10V, I_{DS} = 25A, R_G = 0Ω		8.2		ns
t_r	Rise Time			8.7		ns
$t_{d(off)}$	Turn Off Delay Time			20		ns
t_f	Fall Time			2.7		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_{SD} = 25A, V_{GS} = 0V		0.8	1	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= 30V, I_F = 25A, di/dt = 300A/µs		139		nC
t_{rr}	Reverse Recovery Time			64		ns

THERMAL CHARACTERISTICS

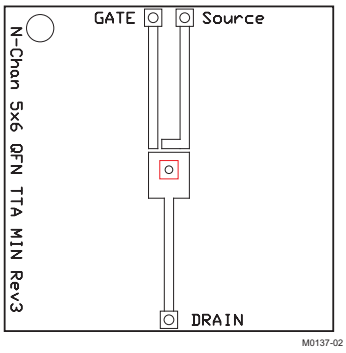
(T_A = 25°C unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case(1)			0.8	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient(1)(2)			50	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 50°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 125°C/W when mounted on a minimum pad area of 2-oz. (0.071-mm thick) Cu.

TYPICAL MOSFET CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

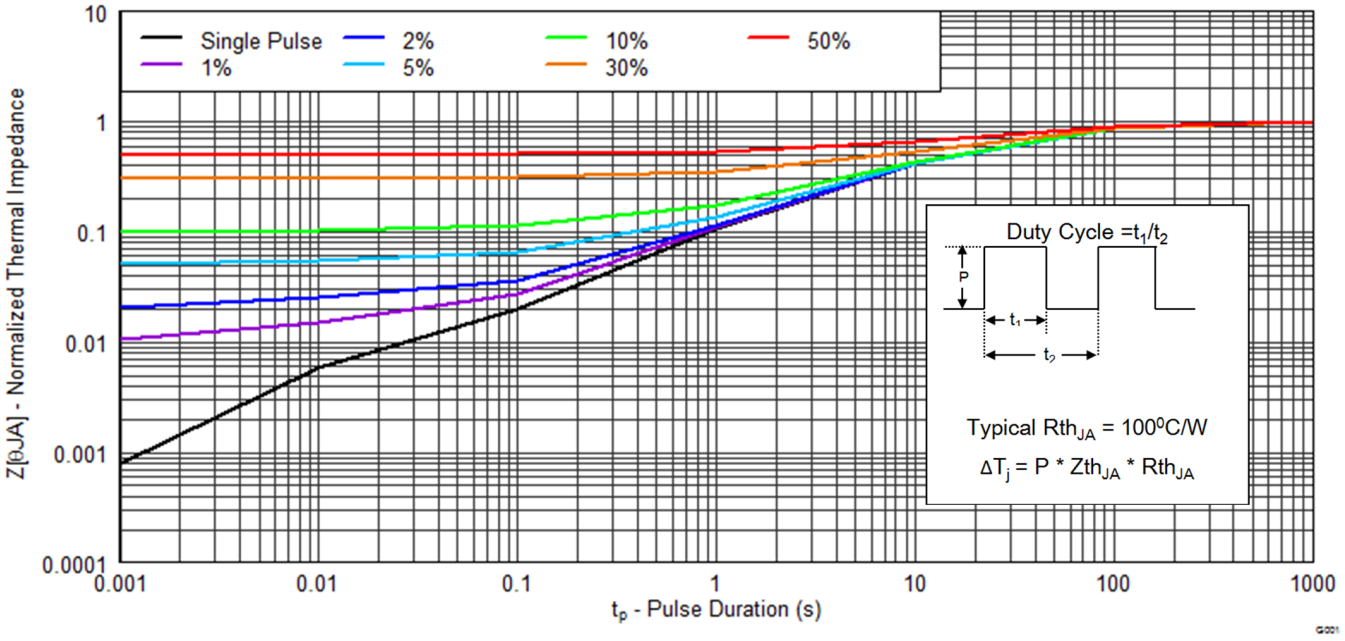


Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

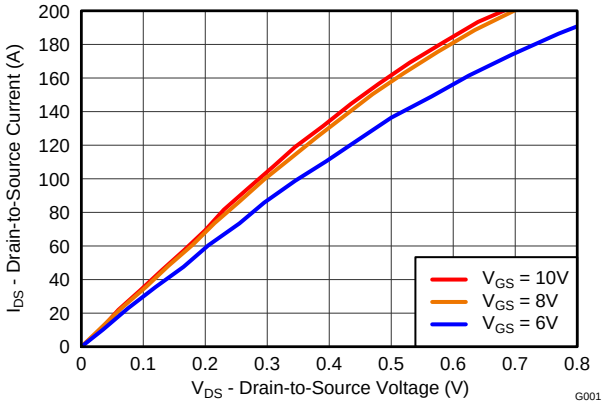


Figure 2. Saturation Characteristics

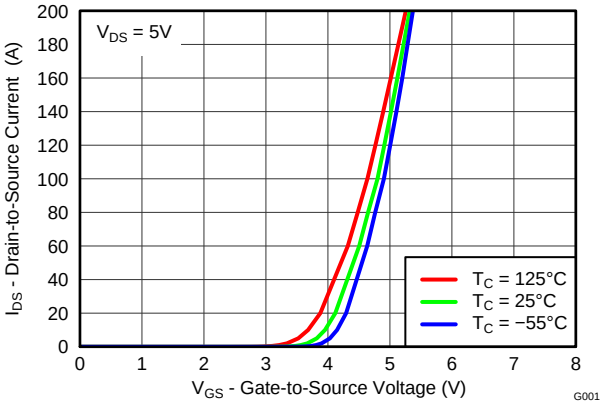


Figure 3. Transfer Characteristics

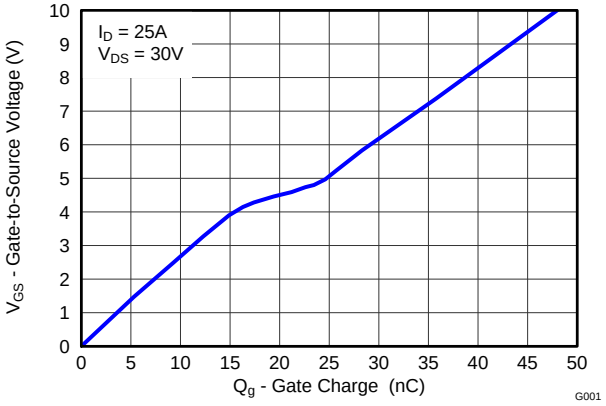


Figure 4. Gate Charge

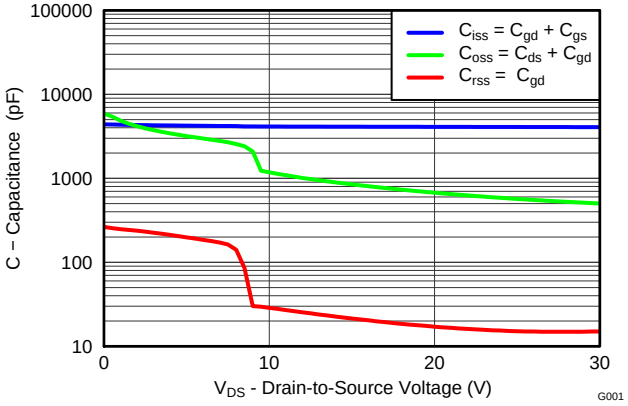


Figure 5. Capacitance

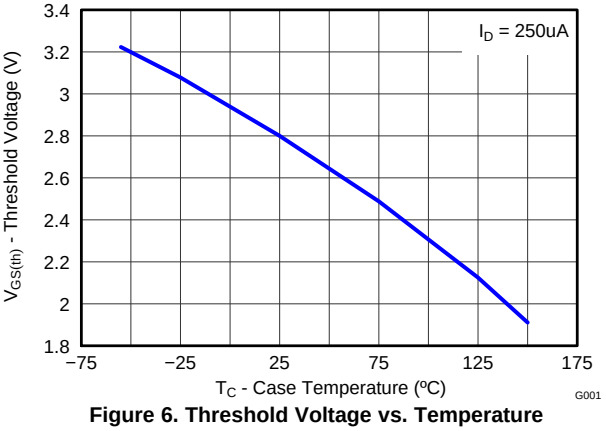


Figure 6. Threshold Voltage vs. Temperature

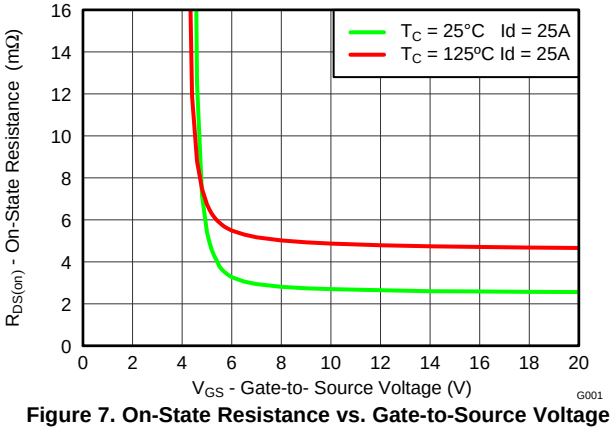


Figure 7. On-State Resistance vs. Gate-to-Source Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

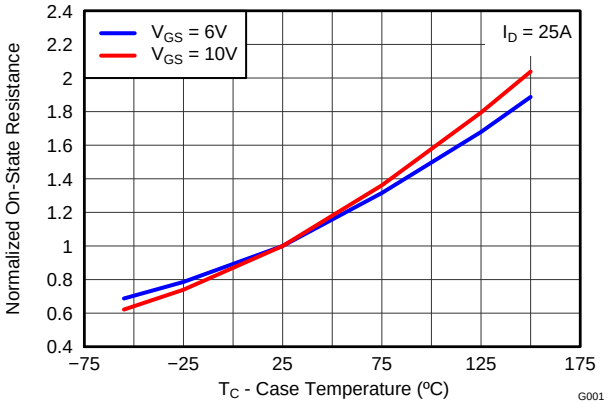


Figure 8. Normalized On-State Resistance vs. Temperature

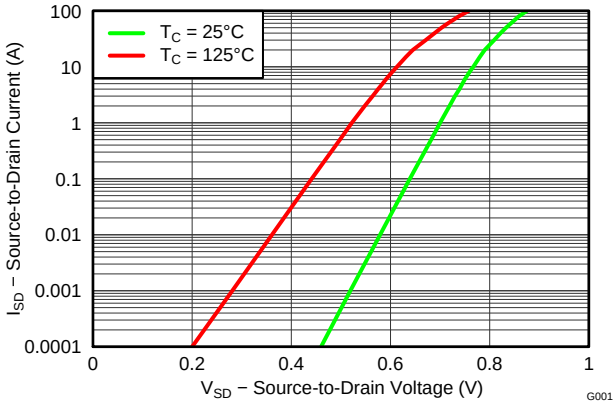


Figure 9. Typical Diode Forward Voltage

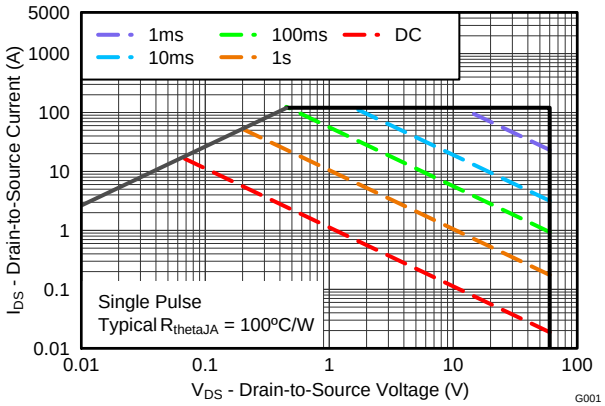


Figure 10. Maximum Safe Operating Area

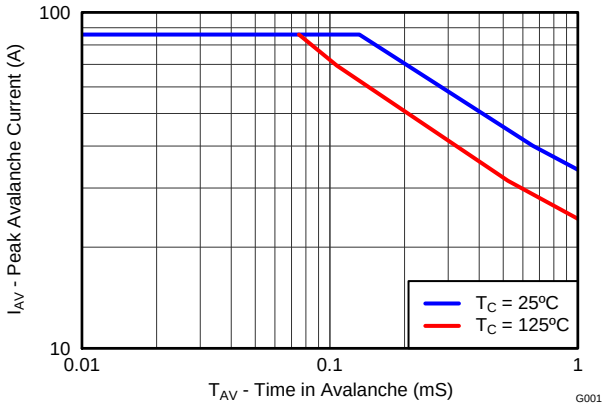


Figure 11. Single Pulse Unclamped Inductive Switching

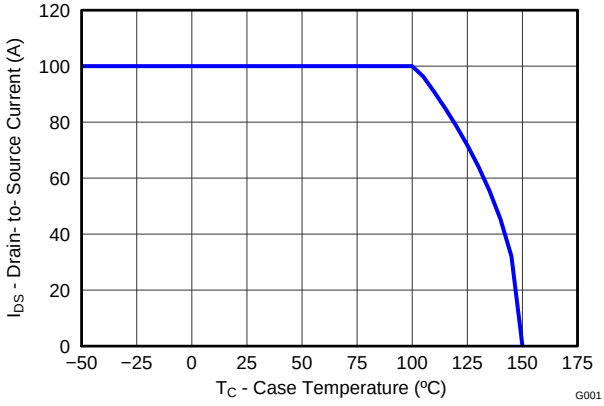
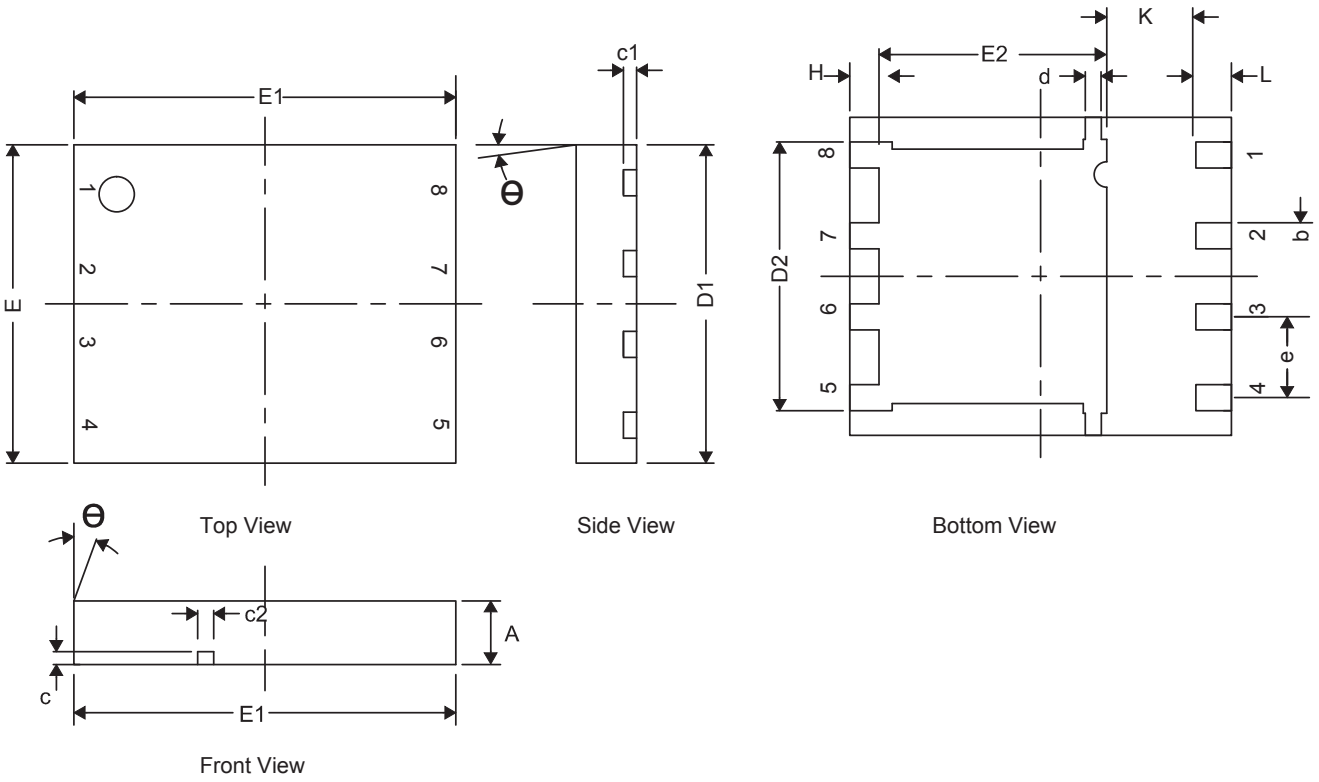


Figure 12. Maximum Drain Current vs. Temperature

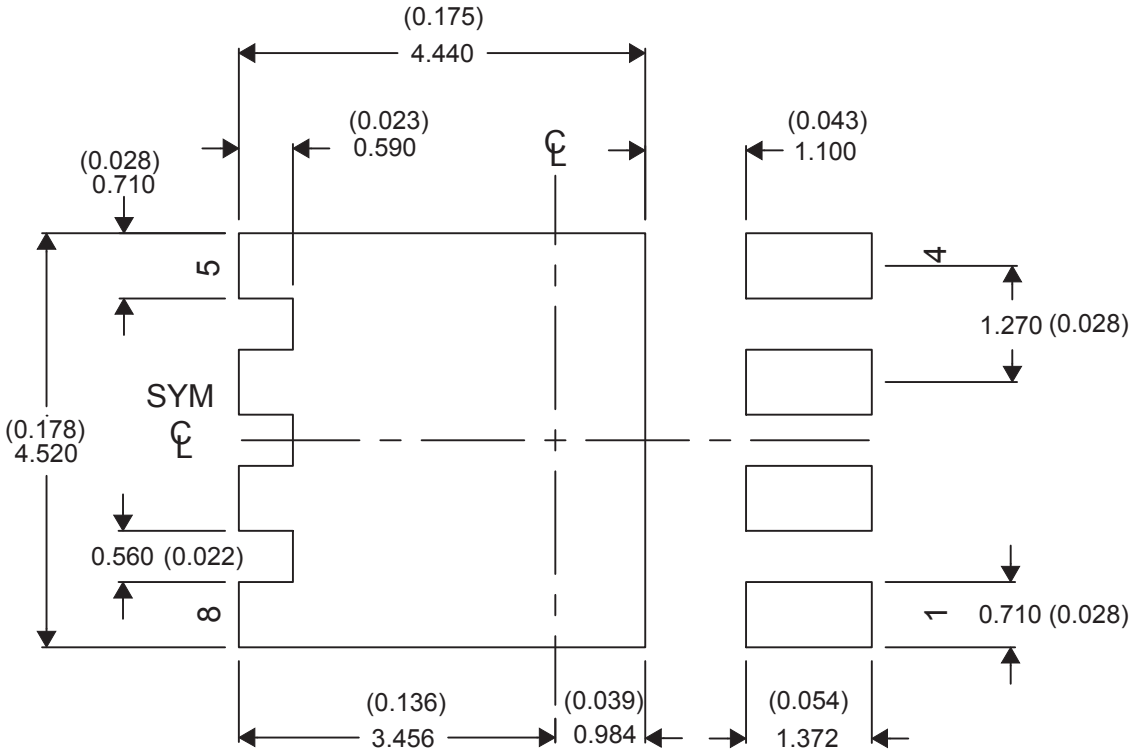
MECHANICAL DATA

Q5B Package Dimensions



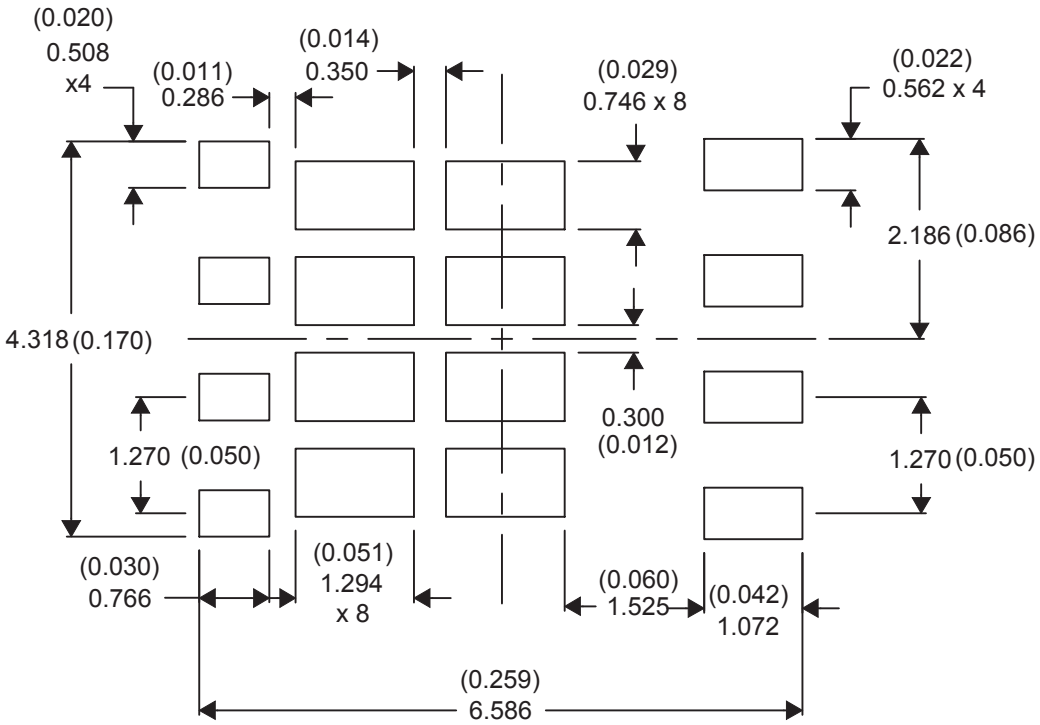
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.80	1.00	1.05
b	0.36	0.41	0.46
c	0.15	0.20	0.25
c1	0.15	0.20	0.25
c2	0.20	0.25	0.30
D1	4.90	5.00	5.10
D2	4.12	4.22	4.32
d	0.20	0.25	0.30
E	4.90	5.00	5.10
E1	5.90	6.00	6.10
E2	3.48	3.58	3.68
e	1.27 TYP		
L	0.46	0.56	0.66
θ	0°	-	-
K	1.40 TYP		

Recommended PCB Pattern

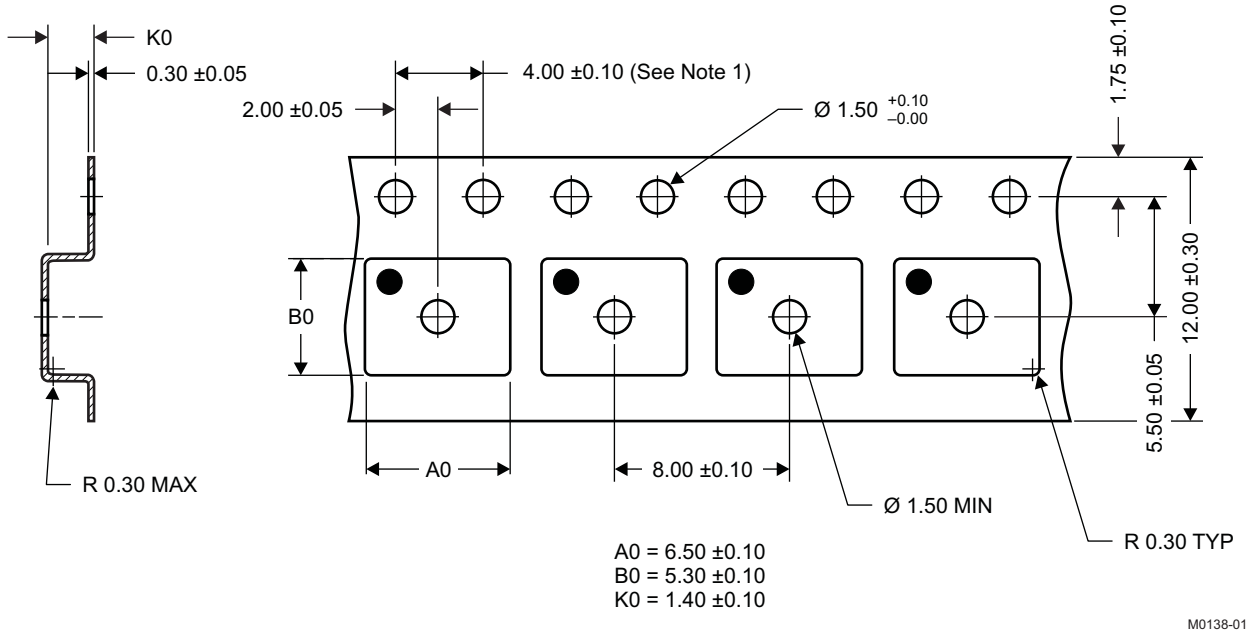


For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

Recommended Stencil Pattern



Q5B Tape and Reel Information



Notes:

1. 10-sprocket hole-pitch cumulative tolerance ±0.2
2. Camber not to exceed 1mm in 100mm, noncumulative over 250mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified)
5. A0 and B0 measured on a plane 0.3mm above the bottom of the pocket

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD18532NQ5B	ACTIVE	VSON	DNK	8	2500	Pb-Free (RoHS Exempt)	CU SN	Level-1-260C-UNLIM	-55 to 150	18532N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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