Synchronous Buck NexFET™ Power Block II

FEATURES

- **Half-Bridge Power Block**
- **90% system Efficiency at 20A**
- **Up To 25A Operation**
- **High Density – 5-mm x 2.5-mm LGA Footprint**
- **Double Side Cooling Capability**
- **Ultra Low Profile – 0.48-mm MAX**
- **Optimized for 5V Gate Drive**
- **Low Switching Losses**
- **Low Inductance Package**
- **RoHS Compliant**
- **Halogen Free**
- **Pb-Free Terminal Plating**

APPLICATIONS

- **Synchronous Buck Converters**
  - **High Current, Low Duty Cycle Applications**
- **Multiphase Synchronous Buck Converters**
- **POL DC-DC Converters**

DESCRIPTION

The CSD87588N NexFET™ power block II is a highly optimized design for synchronous buck applications offering high current and high efficiency capability in a small 5-mm x 2.5-mm outline. Optimized for 5V gate drive applications, this product offers an efficient and flexible solution capable of providing a high density power supply when paired with any 5V gate driver from an external controller/driver.

ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD87588N	5 x 2.5 LGA	13-Inch Reel	2500	Tape and Reel

TYPICAL CIRCUIT
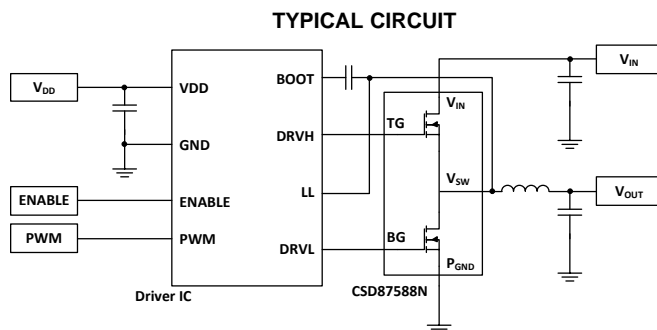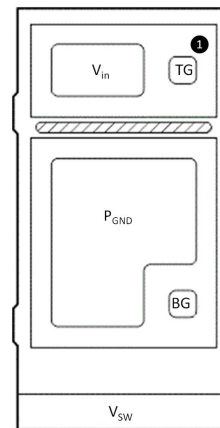
TYPICAL POWER BLOCK EFFICIENCY and POWER LOSS

$V_{GS} = 5V$
$V_{IN} = 12V$
$V_{OUT} = 1.3V$
$L_{OUT} = 0.29\mu H$
$f_{SW} = 500kHz$
$T_A = 25ºC$
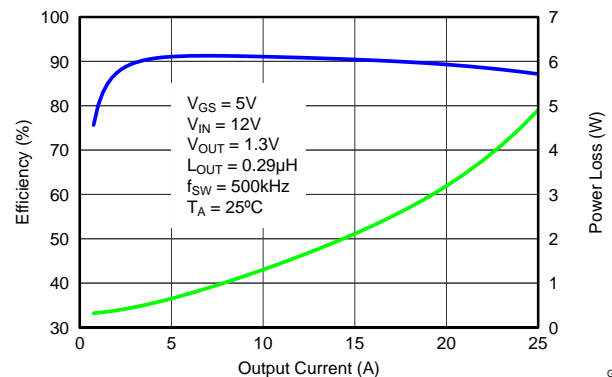
⚠ Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
NexFET is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25°C$ (unless otherwise noted) [1]

Parameter	Conditions	VALUE		UNIT
		MIN	MAX	
Voltage range	V_{IN} to P_{GND}		30	V
	V_{SW} to P_{GND}		30	
	V_{SW} to P_{GND} (10 ns)		32	
	T_G to V_{SW}	-20	20	
	B_G to P_{GND}	-20	20	
Pulsed Current Rating, I_{DM}[2]			50	A
Power Dissipation, P_D[3]			6	W
Avalanche Energy E_{AS}	Sync FET, $I_D = 45A$, $L = 0.1mH$		101	mJ
	Control FET, $I_D = 26A$, $L = 0.1mH$		34	
Operating Junction and Storage Temperature Range, T_J, T_{STG}		-55	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Pulse Duration ≤50 µS. Duty cycle ≤0.01.
(3) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2) Cu.

RECOMMENDED OPERATING CONDITIONS

$T_A = 25°$ (unless otherwise noted)

Parameter	Conditions	MIN	MAX	UNIT
Gate Drive Voltage, V_{GS}		4.5	16	V
Input Supply Voltage, V_{IN}			24	V
Switching Frequency, f_{SW}	$C_{BST} = 0.1µF$ (min)	200	1500	kHz
Operating Current	No Airflow		25	A
	With Airflow		30	A
	With Airflow + Heat Sink		35	A
Operating Temperature, T_J			125	°C

POWER BLOCK PERFORMANCE

$T_A = 25°$ (unless otherwise noted)

Parameter	Conditions	MIN	TYP	MAX	UNIT
Power Loss, P_{LOSS} [1]	$V_{IN} = 12V$, $V_{GS} = 5V$, $V_{OUT} = 1.3V$, $I_{OUT} = 15A$, $f_{SW} = 500kHz$, $L_{OUT} = 0.29µH$, $T_J = 25ºC$		2.1		W
V_{IN} Quiescent Current, I_{QVIN}	T_G to $T_{GR} = 0V$ B_G to $P_{GND} = 0V$		10		µA

(1) Measurement made with six 10µF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins and using a high current 5V driver IC.

THERMAL INFORMATION

T_A = 25°C (unless otherwise stated)

|	THERMAL METRIC	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance (Min Cu) [1]			170	°C/W
	Junction to ambient thermal resistance (Max Cu) [2][1]			70	
$R_{\theta JC}$	Junction to case thermal resistance (Top of package) [1]			3.7	
	Junction to case thermal resistance (P_{GND} Pin) [1]			1.25	

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), 2 oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 board. $R_{\theta JC}$ is specified by design while $R_{\theta JA}$ is determined by the user's board design.
(2)   Device mounted on FR4 material with 1-inch^2 (6.45-cm^2) Cu.

ELECTRICAL CHARACTERISTICS

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	Q1 Control FET			Q2 Sync FET			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Static Characteristics									
BV_{DSS}	Drain to Source Voltage	V_{GS} = 0V, I_{DS} = 250µA	30			30			V
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0V, V_{DS} = 24V			1			1	µA
I_{GSS}	Gate to Source Leakage Current	V_{DS} = 0V, V_{GS} = 20			100			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 250µA	1.1		1.9	1.1		1.9	V
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 4.5V, I_{DS} = 15A		10.4	12.5		3.5	4.2	mΩ
		V_{GS} = 10V, I_{DS} = 15A		8.0	9.6		2.9	3.5	
g_{fs}	Transconductance	V_{DS} = 10V, I_{DS} = 15A		43			93		S
Dynamic Characteristics									
C_{ISS}	Input Capacitance [1]	V_{GS} = 0V, V_{DS} = 15V, f = 1MHz		566	736		2310	3000	pF
C_{OSS}	Output Capacitance [1]			341	444		682	887	pF
C_{RSS}	Reverse Transfer Capacitance [1]			10.3	13.4		62	80.4	pF
R_G	Series Gate Resistance [1]			1.2	2.4		1.1	2.2	Ω
Q_g	Gate Charge Total (4.5V) [1]	V_{DS} = 15V, I_{DS} = 15A		3.2	4.1		13.7	17.9	nC
Q_{gd}	Gate Charge - Gate to Drain			0.7			4.3		nC
Q_{gs}	Gate Charge - Gate to Source			1.4			4.3		nC
$Q_{g(th)}$	Gate Charge at Vth			0.8			2.8		nC
Q_{OSS}	Output Charge	V_{DD} = 12V, V_{GS} = 0V		7.0			18.6		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 15V, V_{GS} = 4.5V, I_{DS} = 15A, R_G = 2Ω		7.3			12.1		ns
t_r	Rise Time			31.6			36.7		ns
$t_{d(off)}$	Turn Off Delay Time			10.2			20.1		ns
t_f	Fall Time			5.0			6.3		ns
Diode Characteristics									
V_{SD}	Diode Forward Voltage	I_{DS} = 15A, V_{GS} = 0V		0.85			0.78		V
Q_{rr}	Reverse Recovery Charge	V_{dd} = 15V, I_F = 15A, di/dt = 300A/µs		12.5			26.7		nC
t_{rr}	Reverse Recovery Time			16			23		ns

(1) Specified by design
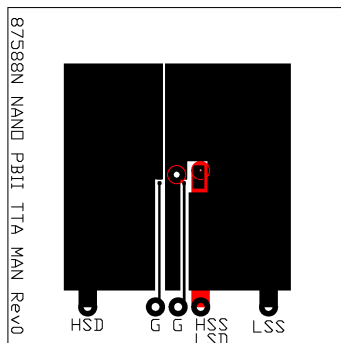
Max $R_{\theta JA}$ = 70°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.
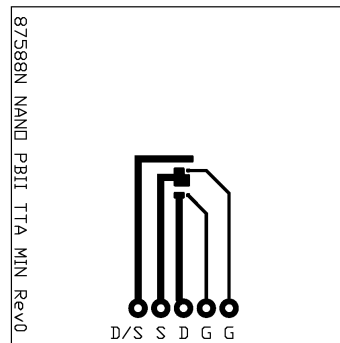
Max $R_{\theta JA}$ = 170°C/W when mounted on minimum pad area of 2-oz. (0.071-mm thick) Cu.

TYPICAL POWER BLOCK DEVICE CHARACTERISTICS

T_J = 125°C, unless stated otherwise.

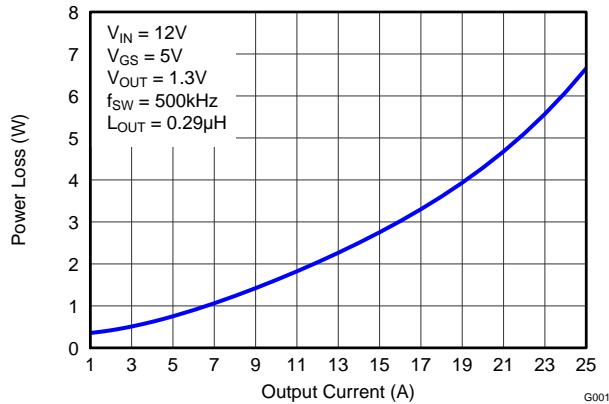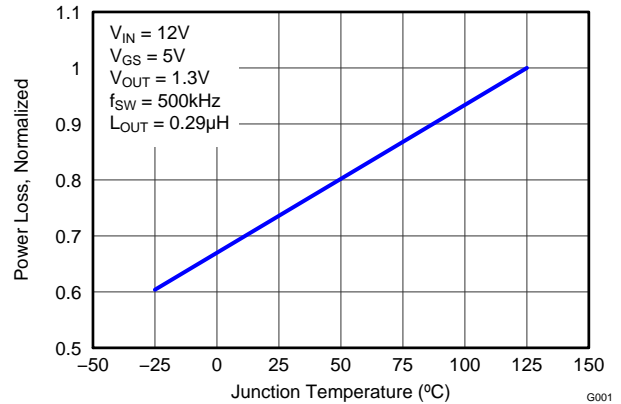**Figure 1. Power Loss vs Output Current**

V_{IN} = 12V
V_{GS} = 5V
V_{OUT} = 1.3V
f_{SW} = 500kHz
L_{OUT} = 0.29μH

Figure 2. Normalized Power Loss vs Temperature

V_{IN} = 12V
V_{GS} = 5V
V_{OUT} = 1.3V
f_{SW} = 500kHz
L_{OUT} = 0.29μH
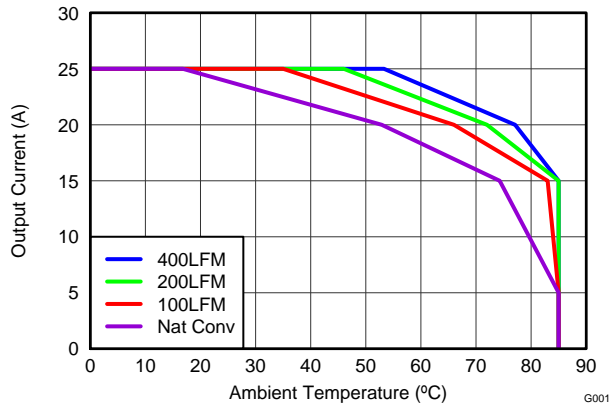
Figure 3. Safe Operating Area – PCB Horizontal Mount [1]

400LFM
200LFM
100LFM
Nat Conv
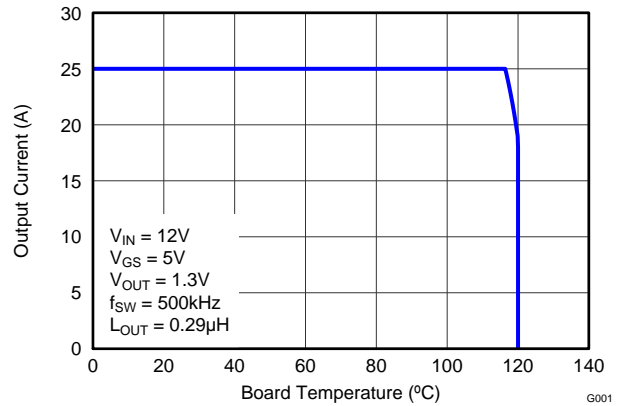
Figure 4. Typical Safe Operating Area [1]

V_{IN} = 12V
V_{GS} = 5V
V_{OUT} = 1.3V
f_{SW} = 500kHz
L_{OUT} = 0.29μH

(1) The Typical Power Block System Characteristic curves are based on measurements made on a PCB design with dimensions of 4.0" (W) × 3.5" (L) x 0.062" (H) and 6 copper layers of 1 oz. copper thickness. See Application Section for detailed explanation.
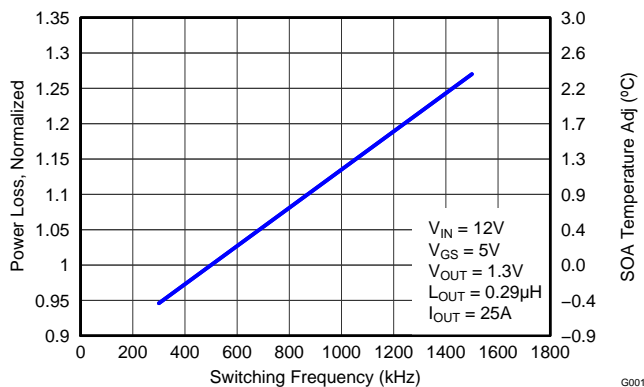
Figure 5. Normalized Power Loss vs Switching Frequency

V_{IN} = 12V
V_{GS} = 5V
V_{OUT} = 1.3V
L_{OUT} = 0.29μH
I_{OUT} = 25A
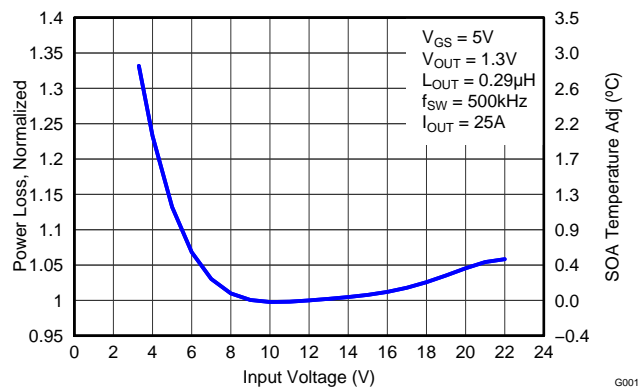
Figure 6. Normalized Power Loss vs Input Voltage

V_{GS} = 5V
V_{OUT} = 1.3V
L_{OUT} = 0.29μH
f_{SW} = 500kHz
I_{OUT} = 25A

TYPICAL POWER BLOCK DEVICE CHARACTERISTICS (continued)

T_J = 125°C, unless stated otherwise.
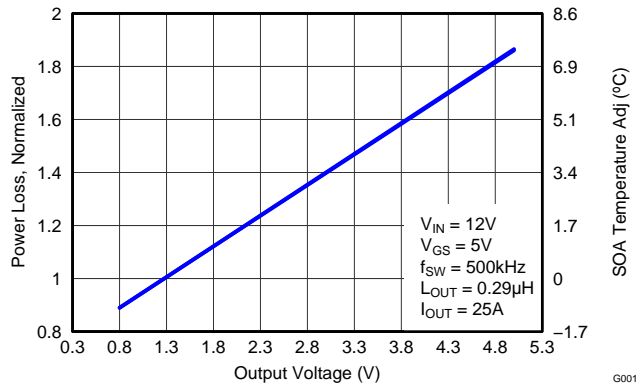
Figure 7. Normalized Power Loss vs. Output Voltage
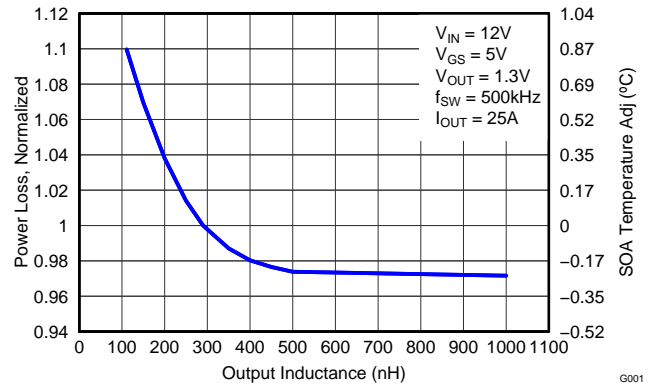
Figure 8. Normalized Power Loss vs. Output Inductance

TYPICAL POWER BLOCK MOSFET CHARACTERISTICS
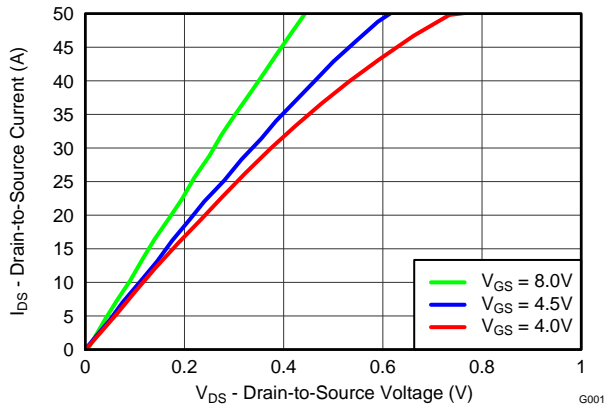
$T_A = 25°C$, unless stated otherwise.
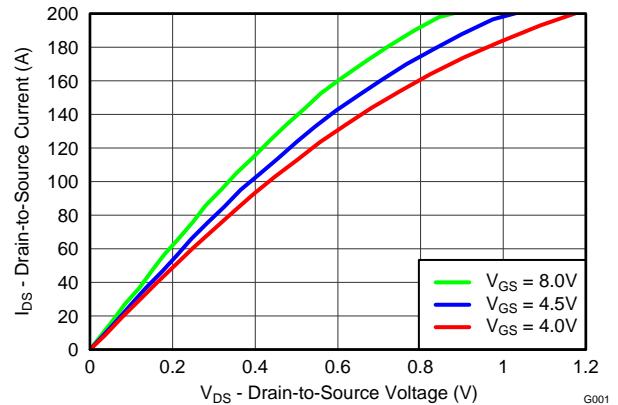

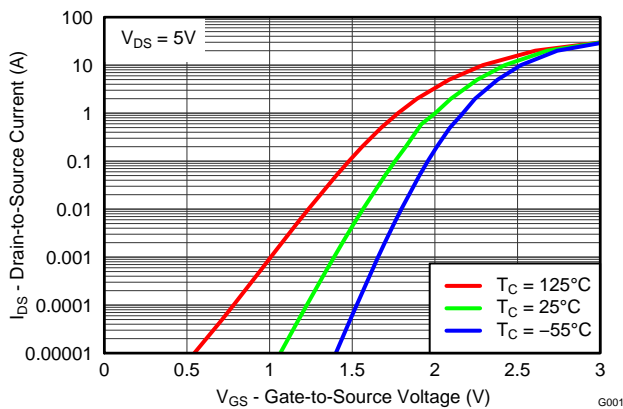**Figure 9. Control MOSFET Saturation**

Figure 10. Sync MOSFET Saturation

Figure 11. Control MOSFET Transfer
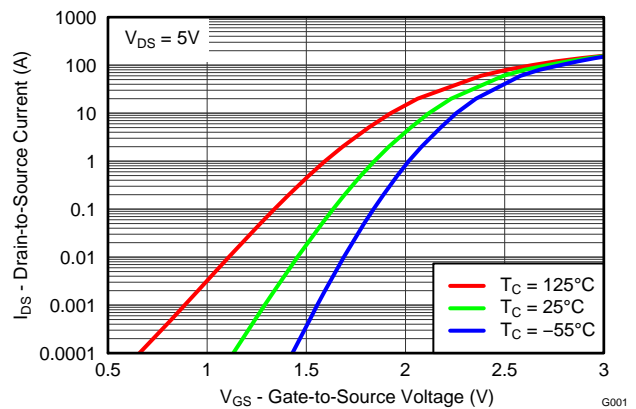
Figure 12. Sync MOSFET Transfer
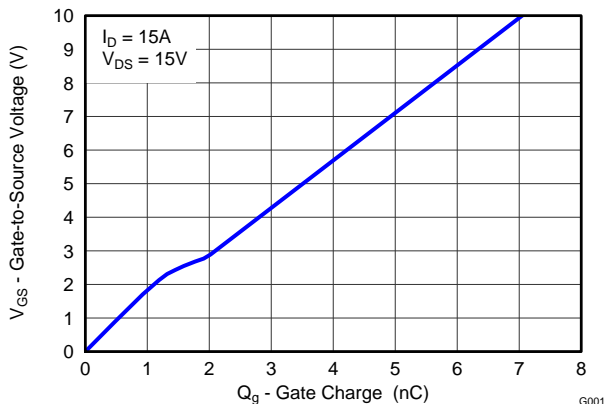
Figure 13. Control MOSFET Gate Charge
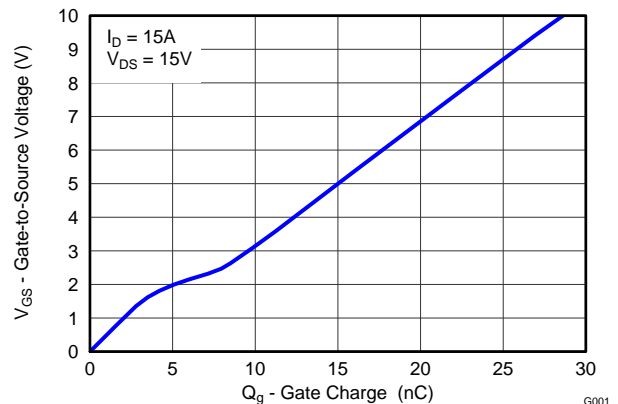
Figure 14. Sync MOSFET Gate Charge

TYPICAL POWER BLOCK MOSFET CHARACTERISTICS (continued)

T_A = 25°C, unless stated otherwise.
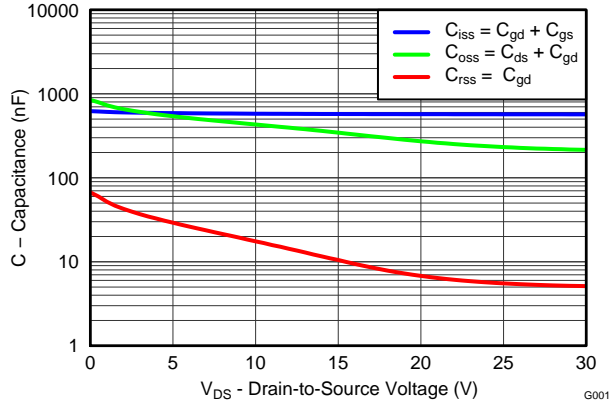
Figure 15. Control MOSFET Capacitance
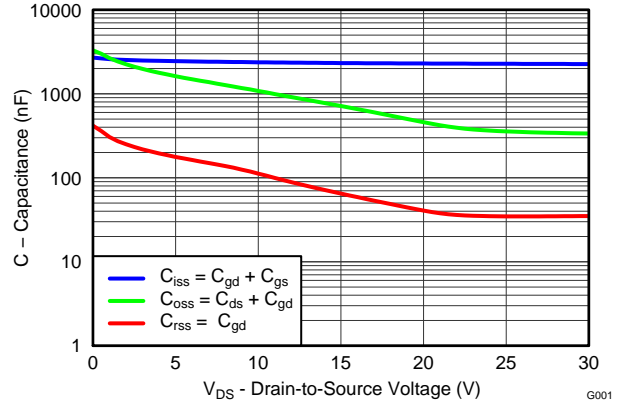
Figure 16. Sync MOSFET Capacitance
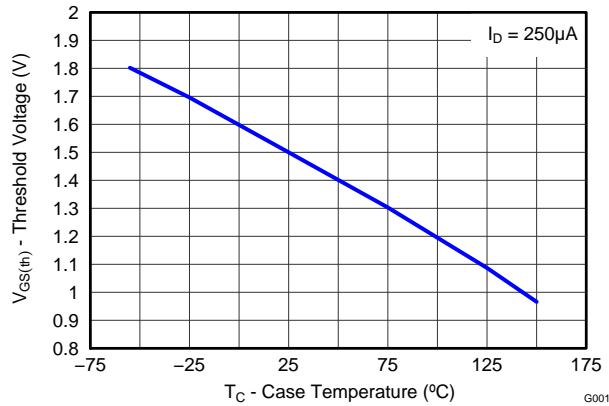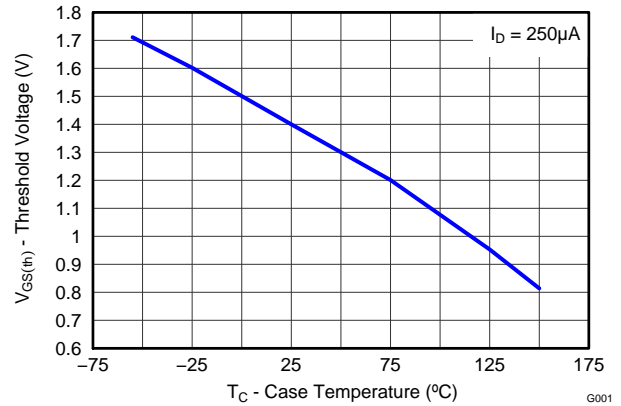

Figure 17. Control MOSFET $V_{GS(th)}$
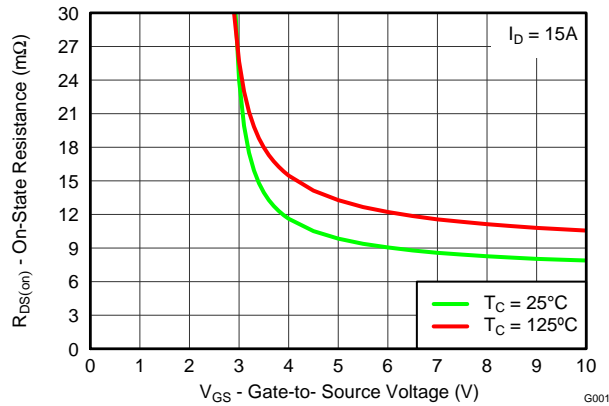

Figure 18. Sync MOSFET $V_{GS(th)}$

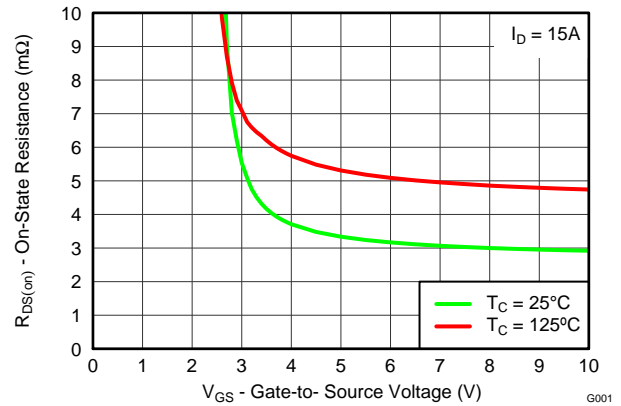**Figure 19. Control MOSFET $R_{DS(on)}$ vs V_{GS}**

Figure 20. Sync MOSFET $R_{DS(on)}$ vs V_{GS}

TYPICAL POWER BLOCK MOSFET CHARACTERISTICS (continued)
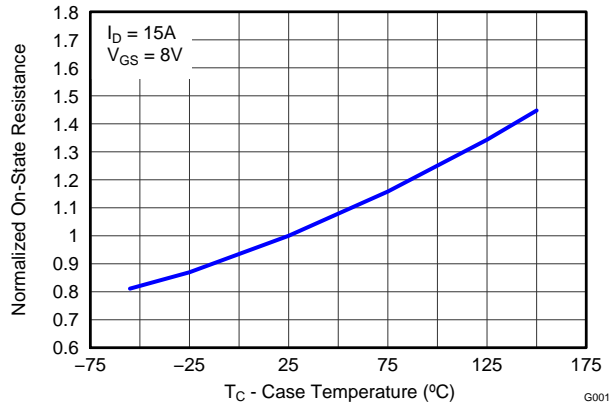
T_A = 25°C, unless stated otherwise.
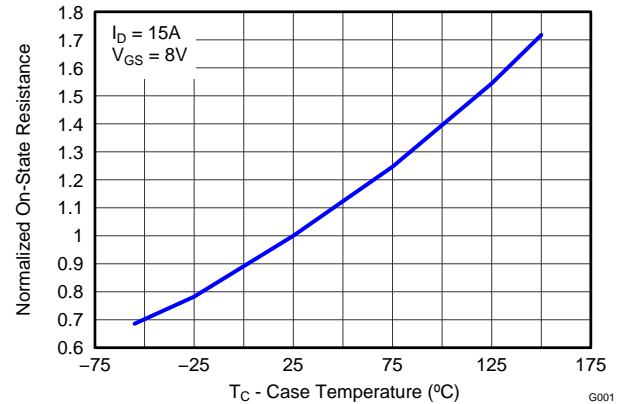

Figure 21. Control MOSFET Normalized R_DS(on)
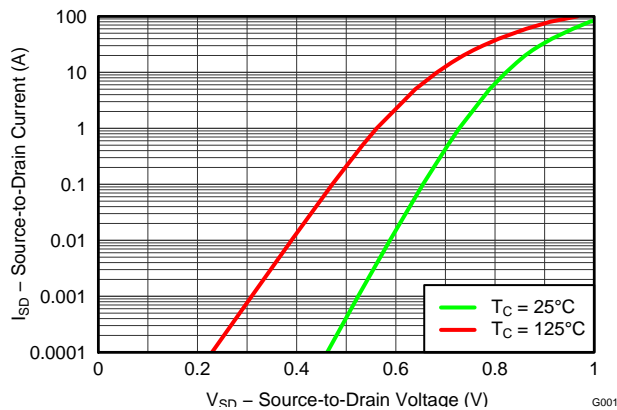

Figure 22. Sync MOSFET Normalized R_DS(on)
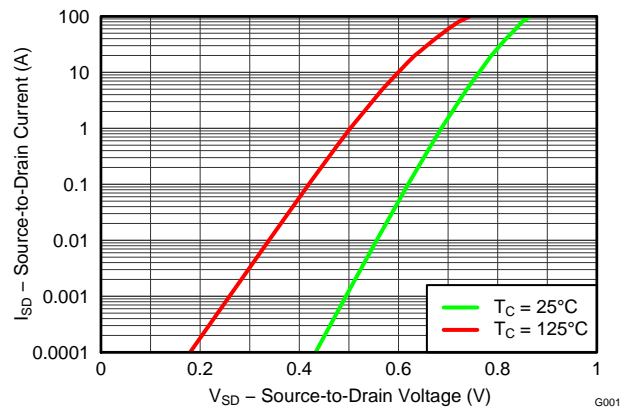

Figure 23. Control MOSFET Body Diode

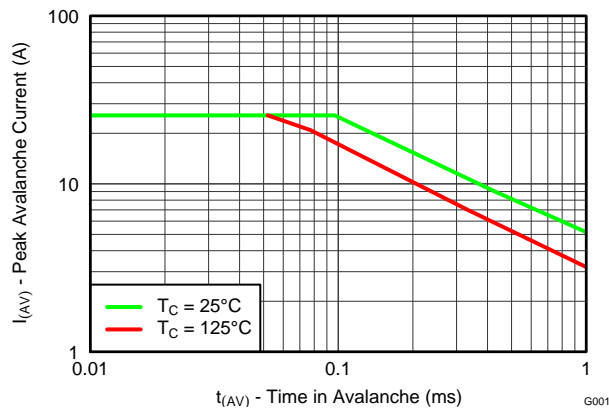**Figure 24. Sync MOSFET Body Diode**

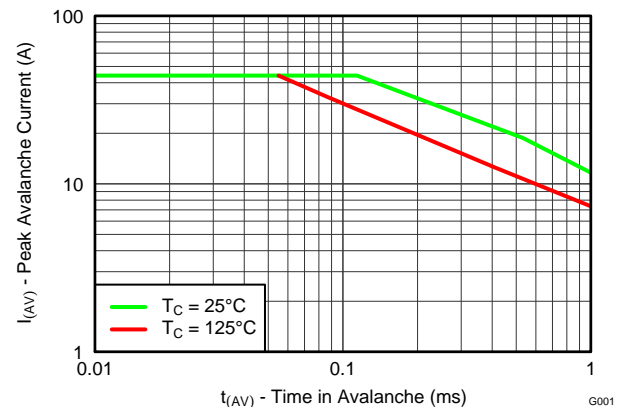**Figure 25. Control MOSFET Unclamped Inductive Switching**

Figure 26. Sync MOSFET Unclamped Inductive Switching

The CSD87588N NexFET™ power block is an optimized design for synchronous buck applications using 5V gate drive. The Control FET and Sync FET silicon are parametrically tuned to yield the lowest power loss and highest system efficiency. As a result, a new rating method is needed which is tailored towards a more systems centric environment. System level performance curves such as Power Loss, Safe Operating Area, and normalized graphs allow engineers to predict the product performance in the actual application.

Power Loss Curves

MOSFET centric parameters such as $R_{DS(ON)}$ and Q_{gd} are needed to estimate the loss generated by the devices. In an effort to simplify the design process for engineers, Texas Instruments has provided measured power loss performance curves. Figure 1 plots the power loss of the CSD87588N as a function of load current. This curve is measured by configuring and running the CSD87588N as it would be in the final application (see Figure 27).The measured power loss is the CSD87588N loss and consists of both input conversion loss and gate drive loss. Equation 1 is used to generate the power loss curve.

$$(V_{IN} \times I_{IN}) + (V_{DD} \times I_{DD}) - (V_{SW\_AVG} \times I_{OUT}) = \text{Power Loss} \qquad (1)$$

The power loss curve in Figure 1 is measured at the maximum recommended junction temperatures of 125°C under isothermal test conditions.

Safe Operating Curves (SOA)

The SOA curves in the CSD87588N data sheet provides guidance on the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. Figure 3 to Figure 4 outline the temperature and airflow conditions required for a given load current. The area under the curve dictates the safe operating area. All the curves are based on measurements made on a PCB design with dimensions of 4" (W) x 3.5" (L) x 0.062" (T) and 6 copper layers of 1 oz. copper thickness.

Normalized Curves

The normalized curves in the CSD87588N data sheet provides guidance on the Power Loss and SOA adjustments based on their application specific needs. These curves show how the power loss and SOA boundaries will adjust for a given set of systems conditions. The primary Y-axis is the normalized change in power loss and the secondary Y-axis is the change is system temperature required in order to comply with the SOA curve. The change in power loss is a multiplier for the Power Loss curve and the change in temperature is subtracted from the SOA curve.
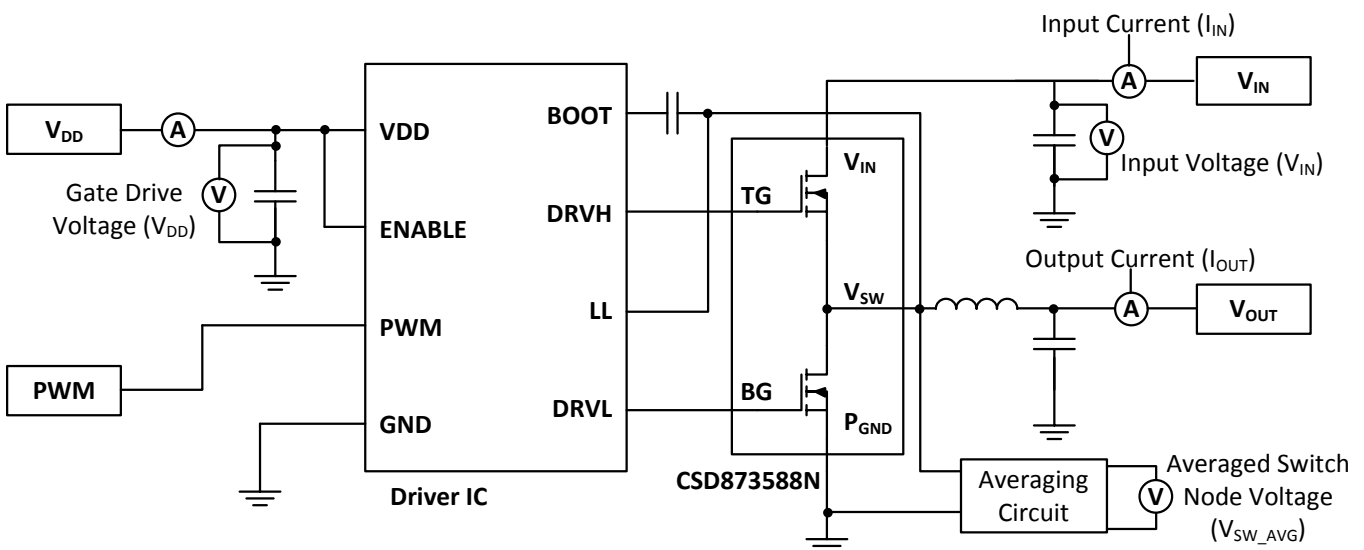

Figure 27. Typical Application

Calculating Power Loss and SOA

The user can estimate product loss and SOA boundaries by arithmetic means (see Design Example). Though the Power Loss and SOA curves in this data sheet are taken for a specific set of test conditions, the following procedure will outline the steps the user should take to predict product performance for any set of system conditions.

Design Example

Operating Conditions:
- Output Current = 15A
- Input Voltage = 7V
- Output Voltage = 1V
- Switching Frequency = 800kHz
- Inductor = 0.2μH

Calculating Power Loss

- Power Loss at 15A = 2.75W (Figure 1)
- Normalized Power Loss for input voltage ≈ 1.03 (Figure 6)
- Normalized Power Loss for output voltage ≈ 0.94 (Figure 7)
- Normalized Power Loss for switching frequency ≈ 1.08 (Figure 5)
- Normalized Power Loss for output inductor ≈ 1.03 (Figure 8)
- **Final calculated Power Loss = 2.75W x 1.05 x 0.95 x 1.05 x 1.05 ≈ 3.02W**

Calculating SOA Adjustments

- SOA adjustment for input voltage ≈ 0.3ºC (Figure 6)
- SOA adjustment for output voltage ≈ -0.5ºC (Figure 7)
- SOA adjustment for switching frequency ≈ 0.7ºC (Figure 5)
- SOA adjustment for output inductor ≈ 0.3ºC (Figure 8)
- **Final calculated SOA adjustment = 0.3 + (-0.5) + 0.7 + 0.3 ≈ 0.8ºC**

In the design example above, the estimated power loss of the CSD87588N would increase to 3.02W. In addition, the maximum allowable board and/or ambient temperature would have to decrease by 0.8ºC. Figure 28 graphically shows how the SOA curve would be adjusted accordingly.

1. Start by drawing a horizontal line from the application current to the SOA curve.
2. Draw a vertical line from the SOA curve intercept down to the board/ambient temperature.
3. Adjust the SOA board/ambient temperature by subtracting the temperature adjustment value.

In the design example, the SOA temperature adjustment yields a reduction in allowable board/ambient temperature of 0.8ºC. In the event the adjustment value is a negative number, subtracting the negative number would yield an increase in allowable board/ambient temperature.
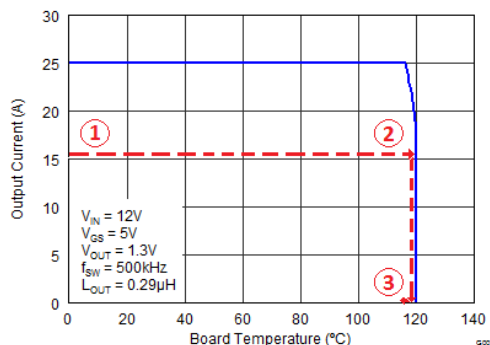

Figure 28. Power Block SOA

RECOMMENDED PCB DESIGN OVERVIEW

There are two key system-level parameters that can be addressed with a proper PCB design: Electrical and Thermal performance. Properly optimizing the PCB layout will yield maximum performance in both areas. A brief description on how to address each parameter is provided.

Electrical Performance

The CSD87588N has the ability to switch voltages at rates greater than 10kV/µs. Special care must be then taken with the PCB layout design and placement of the input capacitors, inductor, and output capacitors.

- The placement of the input capacitors relative to VIN and PGND pins of CSD87588N device should have the highest priority during the component placement routine. It is critical to minimize these node lengths. As such, ceramic input capacitors need to be placed as close as possible to the VIN and PGND pins (see Figure 5). The example in Figure 5 uses 1x10nF 0402 25V and 4 x 10µF 1206 25V ceramic capacitors (TDK Part # C3216X5R1C106KT or equivalent). Notice there are ceramic capacitors on both sides of the board with an appropriate amount of vias interconnecting both layers. In terms of priority of placement next to the Power Stage C21, C5, C8, C19, and C18 should follow in order.
- The switching node of the output inductor should be placed relatively close to the Power Block II CSD87588N VSW pins. Minimizing the VSW node length between these two components will reduce the PCB conduction losses and actually reduce the switching noise level.see Figure 29 [1]

[1] Keong W. Kam, David Pommerenke, "EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis", University of Missouri – Rolla

Thermal Performance

The CSD87588N has the ability to utilize the PGND planes as the primary thermal path. As such, the use of thermal vias is an effective way to pull away heat from the device and into the system board. Concerns of solder voids and manufacturability problems can be addressed by the use of three basic tactics to minimize the amount of solder attach that will wick down the via barrel:

- Intentionally space out the vias from each other to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed in your design. The example in Figure 29 uses vias with a 10 mil drill hole and a 16 mil capture pad.
- Tent the opposite side of the via with solder-mask.

In the end, the number and drill size of the thermal vias should align with the end user's PCB design rules and manufacturing capabilities.
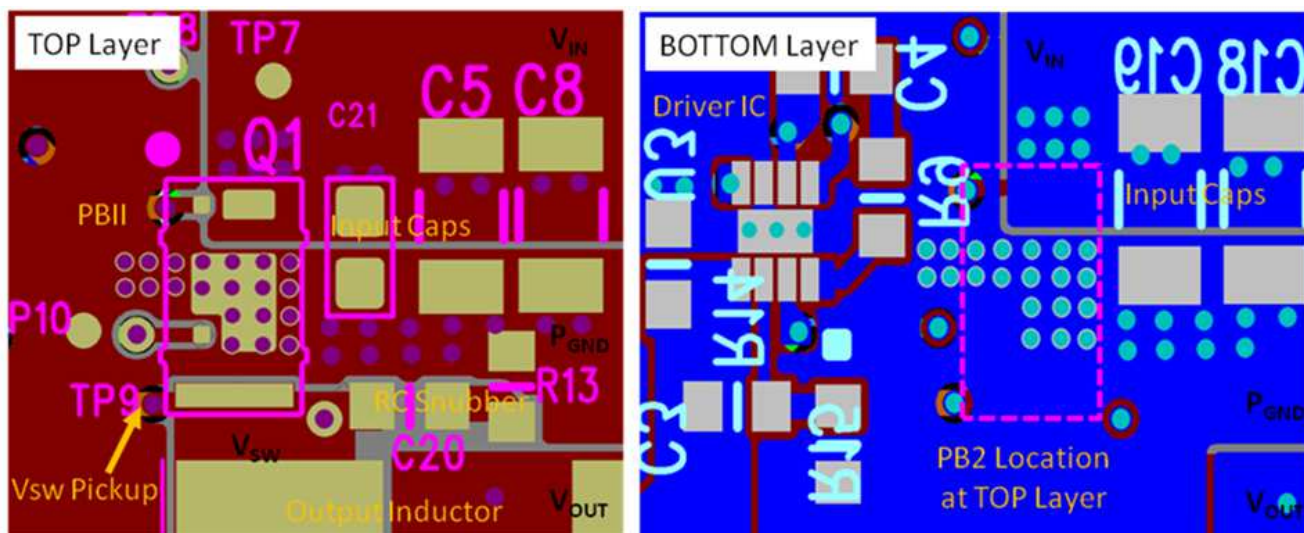

Figure 29. Recommended PCB Layout (Top Down View)
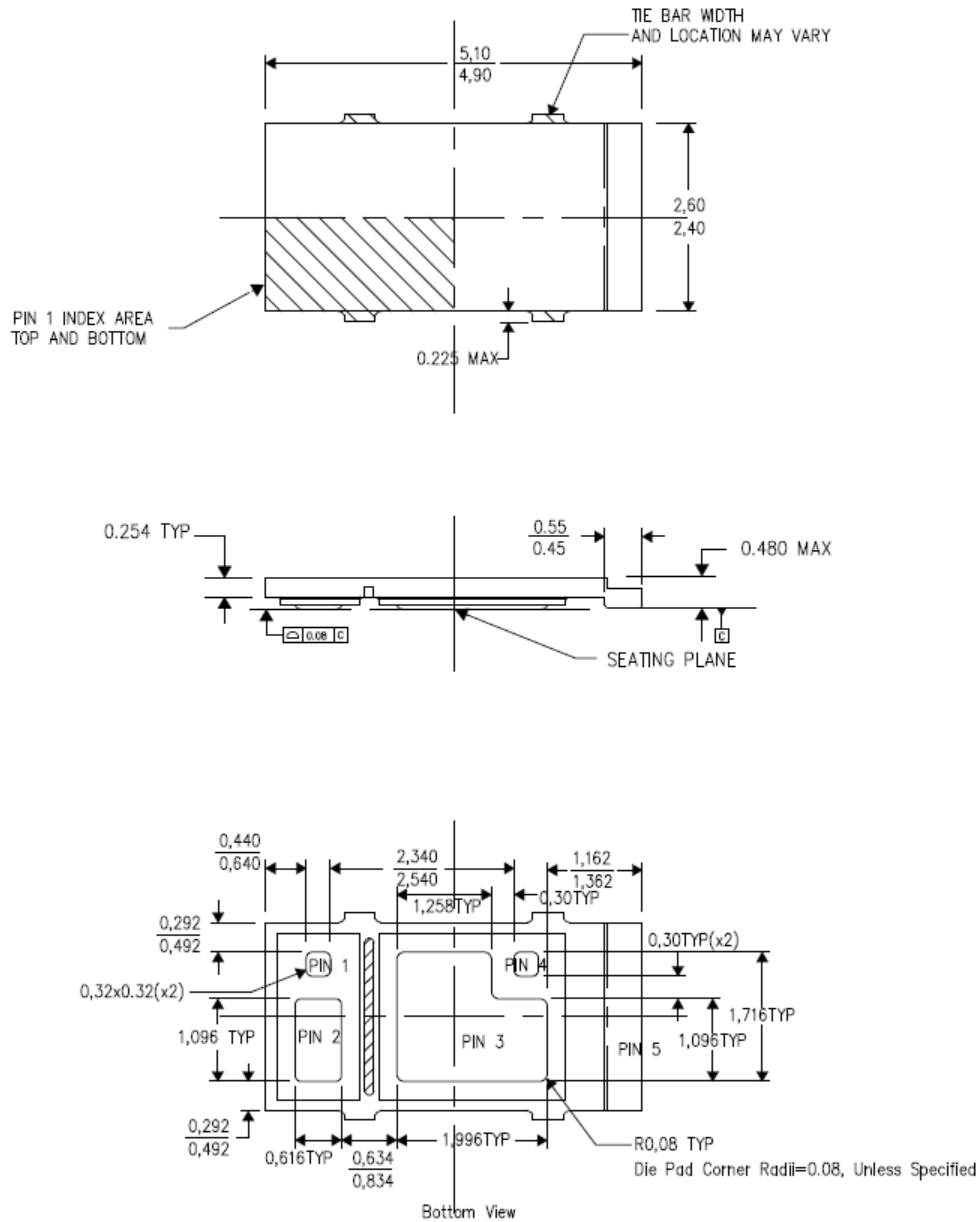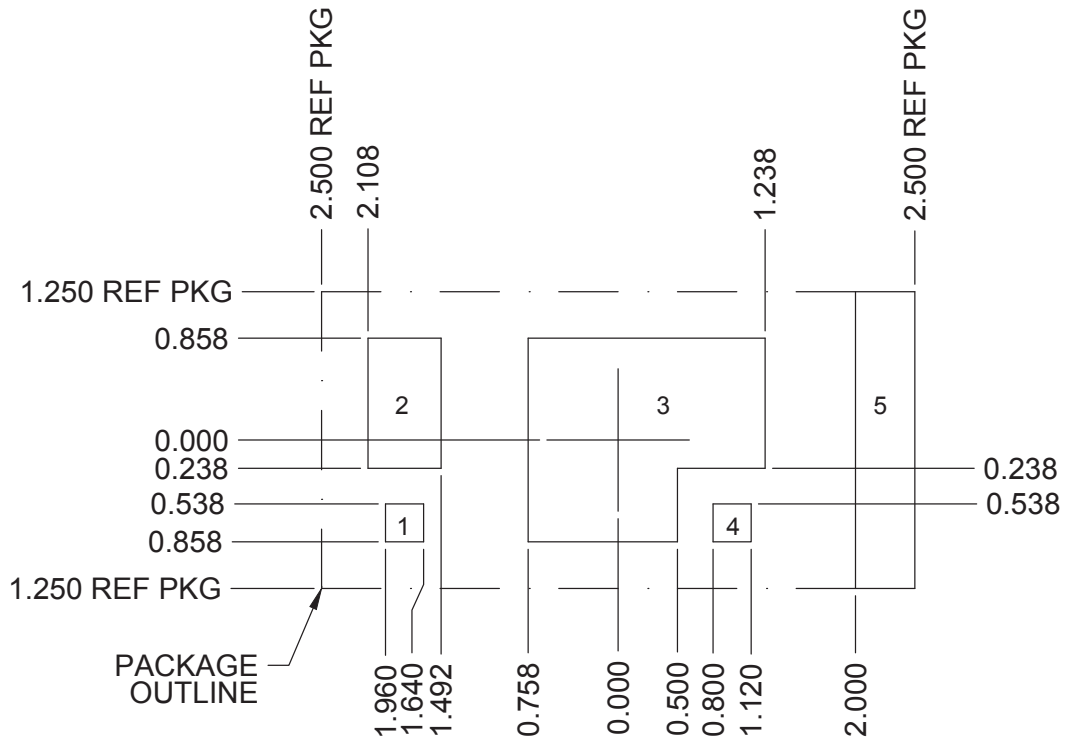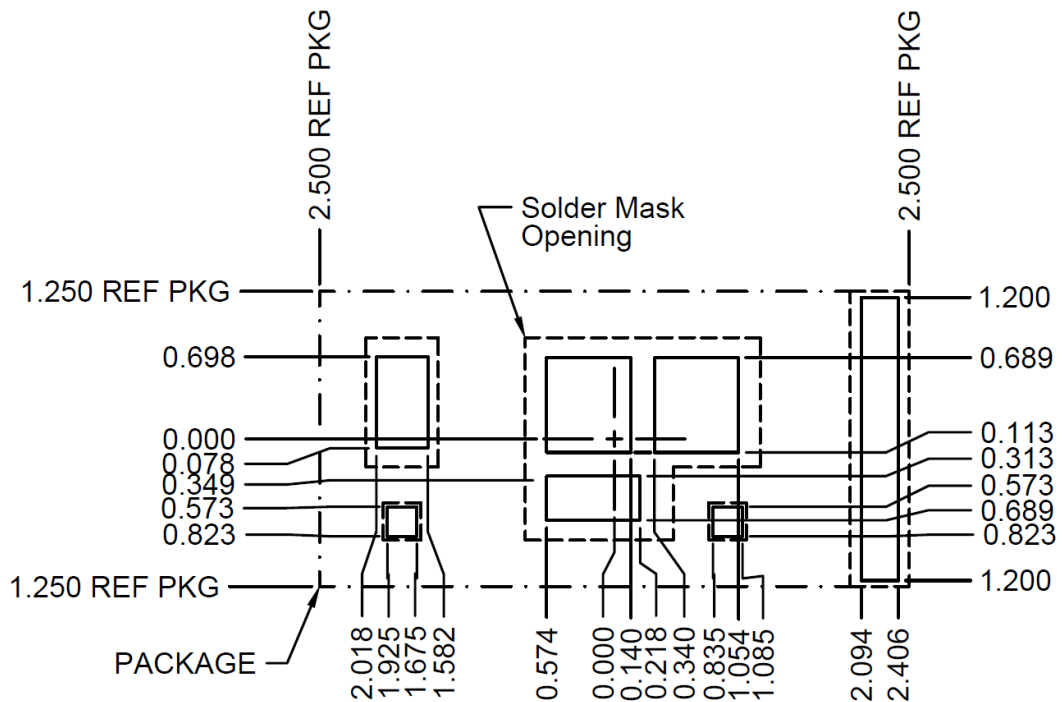
MECHANICAL DATA

CSD87588N Package Dimensions

Table 1. Pin Configuration

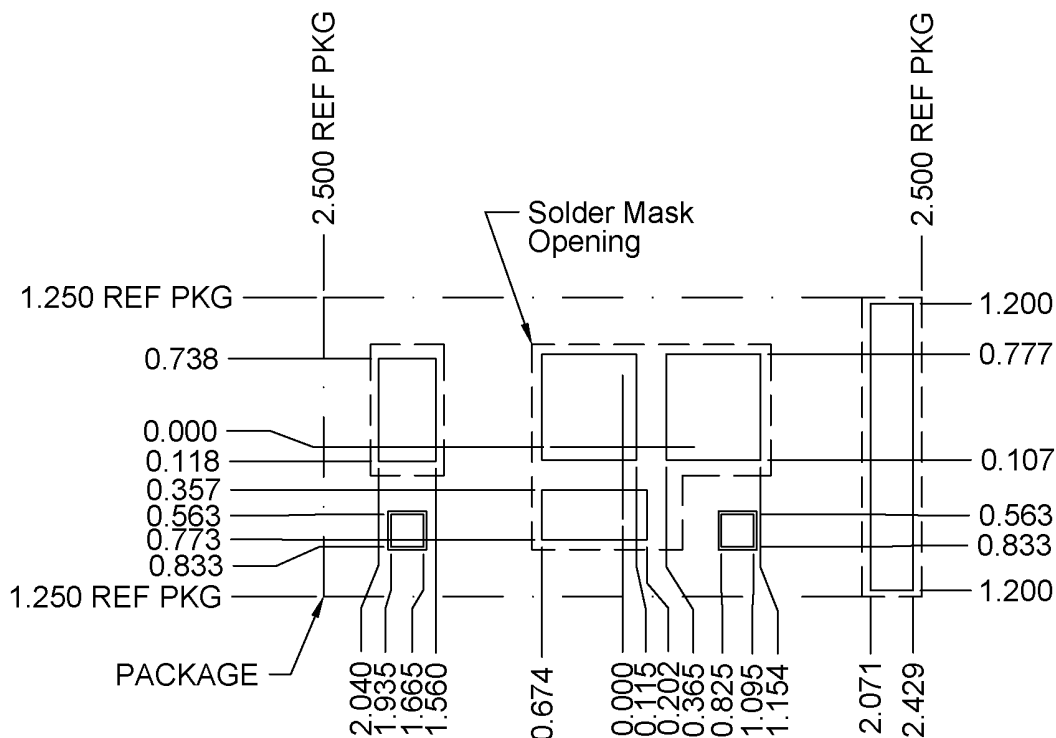| Position	Designation
Pin 1	TG
Pin 2	V_{IN}
Pin 3	P_{GND}
Pin 4	BG
Pin 5	V_{SW}

Land Pattern Recommendation

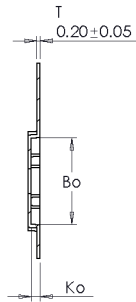**Stencil Recommendation (100 µm)**

Stencil Recommendation (125 μm)

For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.
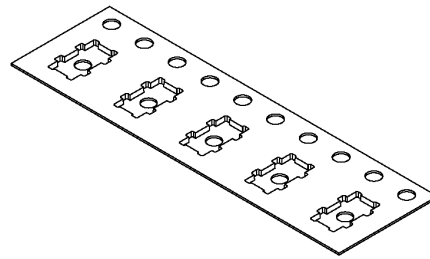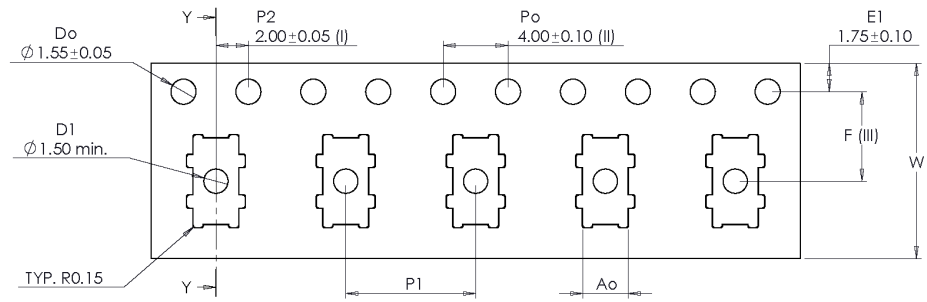
Pin Drawing

CSD87588N Embossed Carrier Tape Dimensions

SECTION Y-Y
SCALE 3.5 : 1

Ao	2.80	+/- 0.10
Bo	5.30	+/- 0.10
Ko	0.55	+/- 0.05
F	5.50	+/- 0.05
P1	8.00	+/- 0.10
W	12.00	+/- 0.30

Forming format : Press Form - 17
Estimated max. length : 278 meter/22B3 reel

(I) 　Measured from centreline of sprocket hole
　　 to centreline of pocket.
(II) 　Cumulative tolerance of 10 sprocket
　　 holes is ± 0.20 .
(III) 　Measured from centreline of sprocket
　　 hole to centreline of pocket.
(IV) 　Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

(1) Pin 1 will be oriented in the top left quadrant of the tape enclosure (closest to the carrier tape sprocket holes).

REVISION HISTORY

Changes from Original (March 2013) to Revision A　　　　　　　　　　　　　　　　　**Page**

- Changed $R_{\theta JC\text{-}PCB}$ To: $R_{\theta JC}$ in the THERMAL INFORMATION table 3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CSD87588N	ACTIVE	PTAB	MPA	5	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 150	87588N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD87588N	PTAB	MPA	5	2500	330.0	12.4	2.8	5.3	0.55	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD87588N	PTAB	MPA	5	2500	367.0	367.0	35.0

IMPORTANT NOTICE

Products		Applications	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		