16-BIT, QUAD CHANNEL, ULTRA-LOW GLITCH, VOLTAGE OUTPUT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **Relative Accuracy: 4LSB**
- **Glitch Energy: 0.15nV-s**
- ***Micro*Power Operation: 150μA per Channel at 2.7V**
- **Power-On Reset to Zero-Scale or Midscale**
- **Power Supply: +2.7V to +5.5V**
- **16-Bit Monotonic Over Temperature**
- **Settling Time: 10μs to ±0.003% FSR**
- **Ultra-Low AC Crosstalk: –100dB Typ**
- **Low-Power SPI™-Compatible Serial Interface with Schmitt-Triggered Inputs: Up to 50MHz**
- **On-Chip Output Buffer Amplifier with Rail-to-Rail Operation**
- **Double Buffered Input Architecture**
- **Simultaneous or Sequential Output Update and Power-Down**
- **Binary and 2's Complement Capability**
- **Asynchronous Clear to Zero-Scale and Midscale**
- **1.8V to 5.5V Logic Compatibility**
- **Available in a TSSOP-16 Package**

APPLICATIONS

- **Portable Instrumentation**
- **Closed-Loop Servo-Control**
- **Process Control**
- **Data Acquisition Systems**
- **Programmable Attenuation**
- **PC Peripherals**

DESCRIPTION

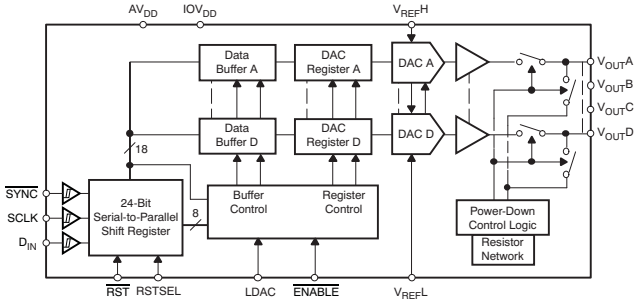
The DAC8555 is a 16-bit, quad channel, voltage output digital-to-analog converter (DAC) offering low-power operation and a flexible serial host interface. It offers monotonicity, good linearity, and exceptionally low glitch. Each on-chip precision output amplifier allows rail-to-rail output swing to be achieved over the supply range of 2.7V to 5.5V. The device supports a standard 3-wire serial interface capable of operating with input data clock frequencies up to 50MHz for IOV_{DD} = 5V.

The DAC8555 requires an external reference voltage to set the output range of each DAC channel. Also incorporated into the device is a power-on reset circuit, which can be programmed to ensure that the DAC outputs power up at zero-scale or midscale and remain there until a valid write takes place. The device also has the capability to function in both binary and 2's complement mode. The DAC8555 provides a per channel power-down feature, accessed over the serial interface, that reduces the current consumption to 175nA per channel at 5V.

The low-power consumption of this device in normal operation makes it ideally suited to portable battery-operated equipment and other low-power applications. The power consumption is 5mW at 5V, reducing to 4μW in power-down mode.

The DAC8555 is available in a TSSOP-16 package with a specified operating temperature range of –40°C to +105°C.

FUNCTIONAL BLOCK DIAGRAM



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGING/ORDERING INFORMATION(1)

PRODUCT	MAXIMUM RELATIVE ACCURACY (LSB)	MAXIMUM DIFFERENTIAL NONLINEARITY (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC8555	±12	±1	TSSOP-16	PW	–40°C to +105°C	D8555	DAC8555IPW	Tube, 90
							DAC8555IPWR	Tape and Reel, 2000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

	UNIT
AV_{DD}, IOV_{DD} to GND	–0.3V to 6V
Digital input voltage to GND	–0.3V to $+AV_{DD}$ + 0.3V
$V_{O(A)}$ to $V_{O(D)}$ to GND	–0.3V to $+AV_{DD}$ + 0.3V
Operating temperature range	–40°C to +105°C
Storage temperature range	–65°C to +150°C
Junction temperature range (T_J max)	+150°C
Power dissipation	$(T_J \text{ max} - T_A)/\theta_{JA}$
θ_{JA} Thermal impedance	118°C/W
θ_{JC} Thermal impedance	29°C/W

(1) Stresses above those listed under *absolute maximum ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V_{DD} = 2.7V to 5.5V, all specifications –40°C to +105°C (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE(1)					
Resolution		16			Bits
Relative accuracy	Measured by line passing through codes 485 and 64741		±4	±12	LSB
Differential nonlinearity	16-bit Monotonic		±0.25	±1	LSB
Zero-scale error	Measured by line passing through codes 485 and 64741		±2	±12	mV
Zero-scale error drift			±5		µV/°C
Full-scale error	Measured by line passing through codes 485 and 64741, (AV_{DD} = 5V, V_{REF} = 4.99V) and (AV_{DD} = 2.7V, V_{REF} = 2.69V)		±0.3	±0.5	% of FSR
Gain error			±0.05	±0.15	% of FSR
Gain temperature coefficient			±1		ppm of FSR/°C
PSRR Power-Supply Rejection Ratio	R_L = 2kΩ, C_L = 200pF		0.75		mV/V
OUTPUT CHARACTERISTICS(2)					
Output voltage range		0		$V_{REF}H$	V
Output voltage settling time	To ±0.003% FSR, 0200h to FD00h, R_L = 2kΩ, 0pF < C_L < 200pF		8	10	µs
	R_L = 2kΩ, C_L = 500pF		12		µs
Slew rate			1.8		V/µs
Capacitive load stability	R_L = ∞		470		pF
	R_L = 2kΩ		1000		pF

(1) Linearity calculated using a reduced code range of 485 to 64741; output unloaded.
(2) Ensured by design and characterization; not production tested.

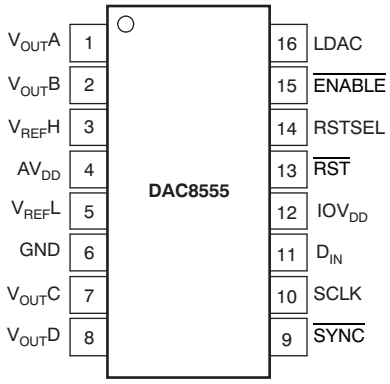
ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = 2.7V to 5.5V, all specifications –40°C to +105°C (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Code change glitch impulse	1LSB change around major carry		0.15		nV-s
Digital feedthrough			0.15		
DC crosstalk	Full-scale swing on adjacent channel. AV_{DD} = 5V, V_{REF} = 4.096V		0.25		LSB
AC crosstalk	1kHz sine wave		–100		dB
DC output impedance	At mid-point input		1		Ω
Short-circuit current	AV_{DD} = 5V		50		mA
	AV_{DD} = 3V		20		
Power-up time	Coming out of power-down mode, AV_{DD} = 5V		2.5		µs
	Coming out of power-down mode, AV_{DD} = 3V		5		
AC PERFORMANCE					
SNR	BW = 20kHz, AV_{DD} = 5V, f_{OUT} = 1kHz, 1st 19 harmonics removed for SNR calculation		95		dB
THD			–85		
SFDR			87		
SINAD			84		
REFERENCE INPUT					
$V_{REF}H$ Voltage	$V_{REF}L < V_{REF}H$, $AV_{DD} – (V_{REF}H + V_{REF}L)/2 > 1.2V$	0		AV_{DD}	V
$V_{REF}L$ Voltage	$V_{REF}L < V_{REF}H$, $AV_{DD} – (V_{REF}H + V_{REF}L)/2 > 1.2V$	0		$AV_{DD}/2$	V
Reference input current	$V_{REF}L$ = GND, $V_{REF}H = AV_{DD}$ = 5V		180	250	µA
	$V_{REF}L$ = GND, $V_{REF}H = AV_{DD}$ = 3V		120	200	µA
Reference input impedance	$V_{REF}L < V_{REF}H$		31		kΩ
LOGIC INPUTS(3)					
V_{IL} Logic input LOW voltage	2.7V ≤ IOV_{DD} ≤ 5.5V			$0.3 \times IOV_{DD}$	V
	1.8V ≤ IOV_{DD} ≤ 2.7V			$0.1 \times IOV_{DD}$	
V_{IH} Logic input HIGH voltage	2.7 ≤ IOV_{DD} ≤ 5.5V	$0.7 \times IOV_{DD}$			V
	1.8 ≤ IOV_{DD} < 2.7V	$0.95 \times IOV_{DD}$			
Pin capacitance				3	pF
POWER REQUIREMENTS					
AV_{DD}		2.7		5.5	V
IOV_{DD}		1.8		5.5	
I_{DD} (normal mode)	Input code = 32768, no load, reference current not included				
IOI_{DD}	$V_{IH} = IOV_{DD}$ and V_{IL} = GND		10	20	µA
AV_{DD} = 3.6V to 5.5V			0.65	0.95	mA
AV_{DD} = 2.7V to 3.6V			0.6	0.9	
I_{DD} (all power-down modes)	$V_{IH} = IOV_{DD}$ and V_{IL} = GND				
AV_{DD} = 3.6V to 5.5V			0.7	2	µA
AV_{DD} = 2.7V to 3.6V			0.4	2	
POWER EFFICIENCY					
I_{OUT}/I_{DD}	I_L = 2mA, AV_{DD} = 5V		89		%
TEMPERATURE RANGE					
Specified performance		–40		+105	°C

(3) Ensured by design and characterization; not production tested.

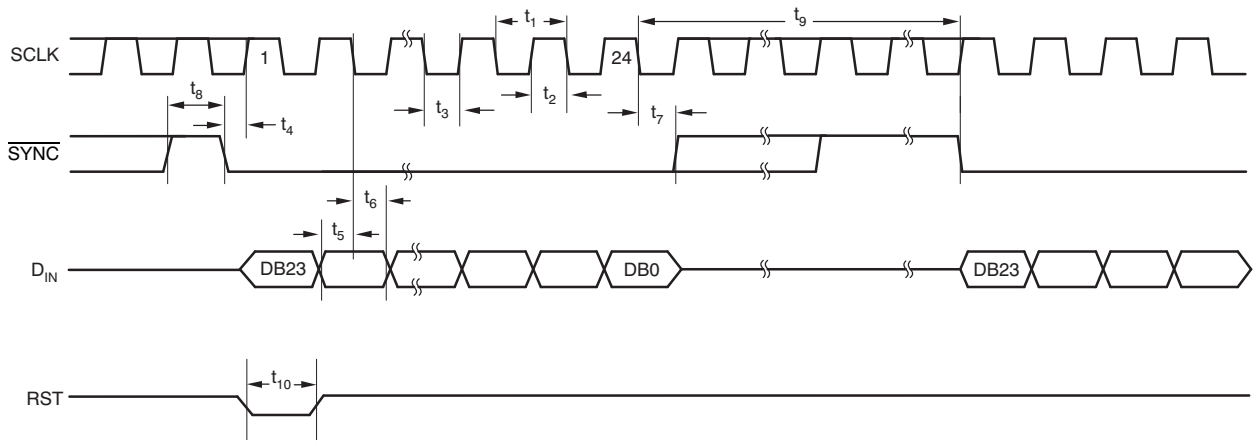
PIN CONFIGURATION



PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	$V_{OUT}A$	Analog output voltage from DAC A.
2	$V_{OUT}B$	Analog output voltage from DAC B.
3	$V_{REF}H$	Positive reference voltage input.
4	AV_{DD}	Power supply input, 2.7V to 5.5V.
5	$V_{REF}L$	Negative reference voltage input.
6	GND	Ground reference point for all circuitry on the device.
7	$V_{OUT}C$	Analog output voltage DAC C.
8	$V_{OUT}D$	Analog output voltage DAC D.
9	$\overline{SYNC}$	Level-triggered control input (active LOW). This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes LOW, it enables the input shift register and data is transferred in on the falling edges of the following clocks. The DAC is updated following the 24th clock (unless $\overline{SYNC}$ is taken HIGH before this edge, in which case the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the DAC8555). Schmitt-Trigger logic input.
10	SCLK	Serial clock input. Data can be transferred at rates up to 50MHz. Schmitt-Trigger logic input.
11	D_{IN}	Serial data input. Data is clocked into the 24-bit input shift register on each falling edge of the serial clock input. Schmitt-Trigger logic input.
12	IOV_{DD}	Digital input-output power supply
13	$\overline{RST}$	Asynchronous reset. Active low. If $\overline{RST}$ is low, all DAC channels reset either to zero-scale (RSTSEL = 0) or to midscale (RSTSEL = 1).
14	RSTSEL	Reset select. If RSTSEL is low, input coding is binary; if high = 2's complement.
15	$\overline{ENABLE}$	Active LOW, $\overline{ENABLE}$ LOW connects the SPI interface to the serial port.
16	LDAC	Load DACs, rising edge triggered loads all DAC registers.

SERIAL WRITE OPERATION



TIMING REQUIREMENTS(1)(2)

AV_{DD} = 2.7V to 5.5V, all specifications –40°C to +105°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1(3)	SCLK cycle time	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	40			ns
		IOV_{DD} = AV_{DD} = 3.6V to 5.5V	20			
t_2	SCLK HIGH time	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	20			ns
		IOV_{DD} = AV_{DD} = 3.6V to 5.5V	10			
t_3	SCLK LOW time	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	20			ns
		IOV_{DD} = AV_{DD} = 3.6V to 5.5V	10			
t_4	$\overline{SYNC}$ falling edge to SCLK rising edge setup time	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	0			ns
		IOV_{DD} = AV_{DD} = 3.6V to 5.5V	0			
t_5	Data setup time	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	5			ns
		IOV_{DD} = AV_{DD} = 3.6V to 5.5V	5			
t_6	Data hold time	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	4.5			ns
		IOV_{DD} = AV_{DD} = 3.6V to 5.5V	4.5			
t_7	24th SCLK falling edge to $\overline{SYNC}$ rising edge	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	0			ns
		IOV_{DD} = AV_{DD} = 3.6V to 5.5V	0			
t_8	Minimum $\overline{SYNC}$ HIGH time	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	40			ns
		IOV_{DD} = AV_{DD} = 3.6V to 5.5V	20			
t_9	24th $\overline{SCLK}$ falling edge to SYNC falling edge	IOV_{DD} = AV_{DD} = 2.7V to 5.5V	130			ns
t_{10}	Miniumum $\overline{RST}$ low time	IOV_{DD} = AV_{DD} = 2.7V to 3.5V	40			ns
		IOV_{DD} = AV_{DD} = 3.6V to 5.5V	20			

(1) All input signals are specified with t_R = t_F = 3ns (10% to 90% of AV_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.
(2) See Serial Write Operation timing diagram.
(3) Maximum SCLK frequency is 50MHz at IOV_{DD} = AV_{DD} = 3.6V to 5.5V and 25 MHz at IOV_{DD} = AV_{DD} = 2.7V to 3.6V.

TYPICAL CHARACTERISTICS: V_{DD} = 5V

At T_A = +25°C, unless otherwise noted.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

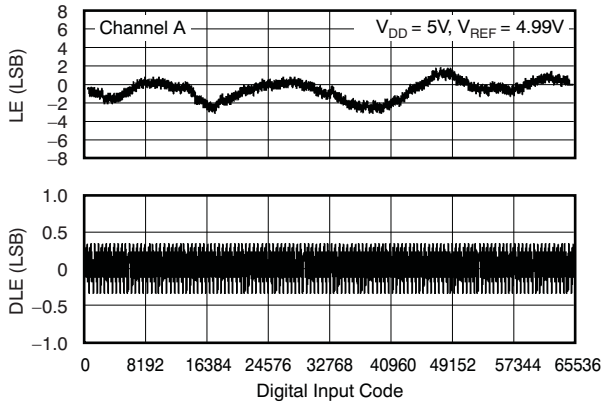


Figure 1.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

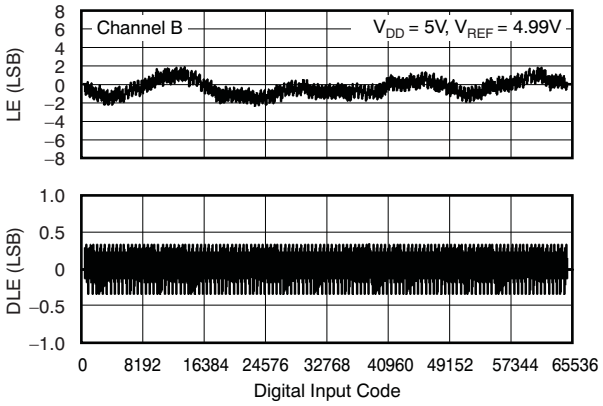


Figure 2.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

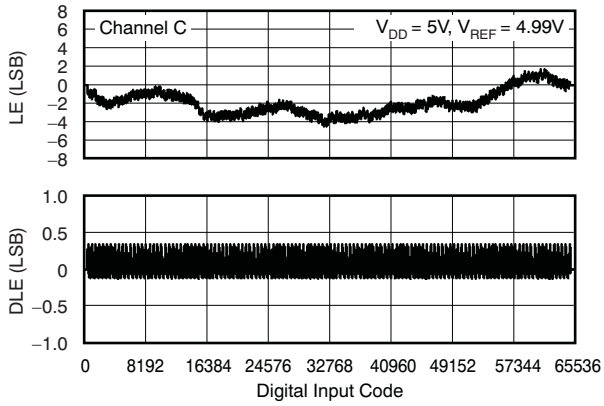


Figure 3.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

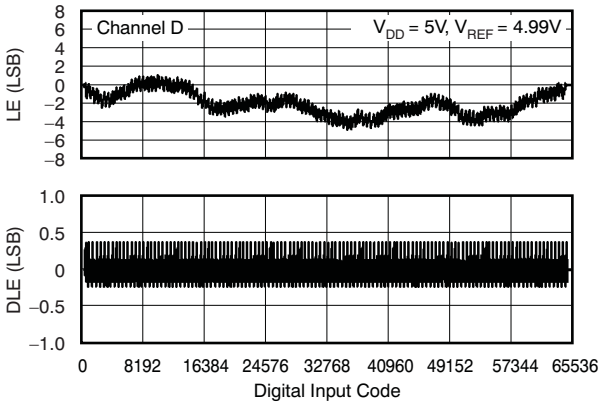


Figure 4.

ZERO-SCALE ERROR vs TEMPERATURE

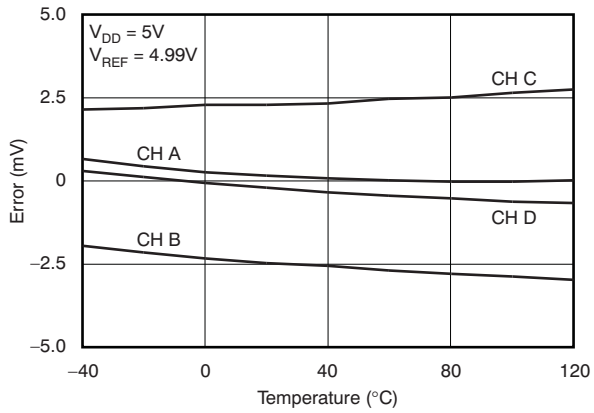


Figure 5.

FULL-SCALE ERROR vs TEMPERATURE

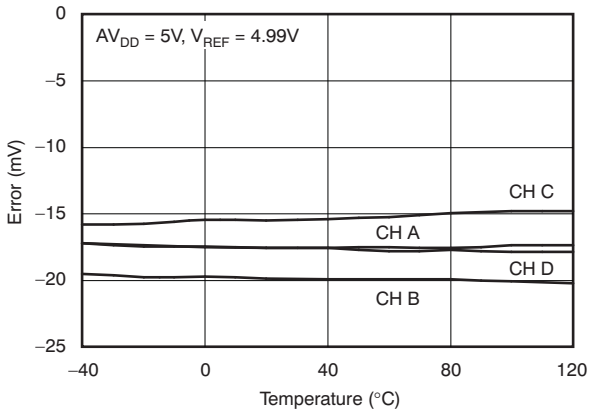


Figure 6.

TYPICAL CHARACTERISTICS: V_{DD} = 5V (continued)

At T_A = +25°C, unless otherwise noted.

SOURCE CURRENT CAPABILITY (ALL CHANNELS)

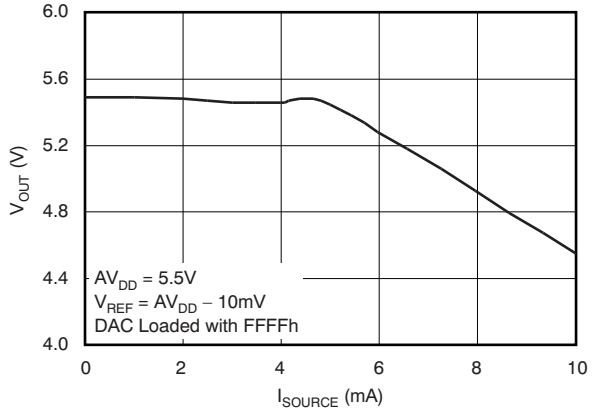


Figure 7.

SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

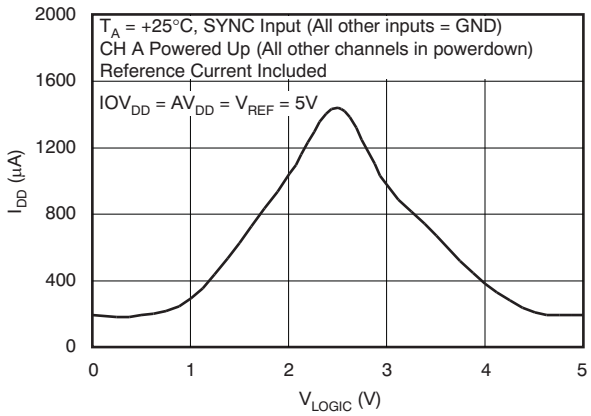


Figure 8.

POWER SPECTRAL DENSITY

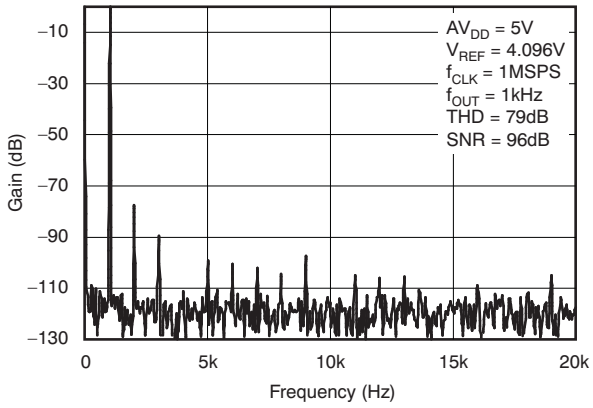


Figure 9.

TOTAL HARMONIC DISTORTION vs OUTPUT FREQUENCY

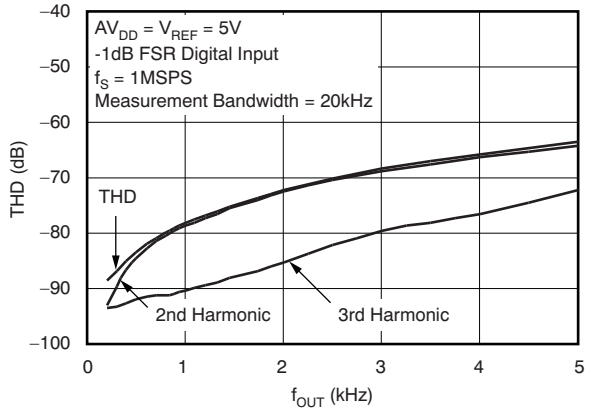


Figure 10.

FULL-SCALE SETTLING TIME: 5V RISING EDGE

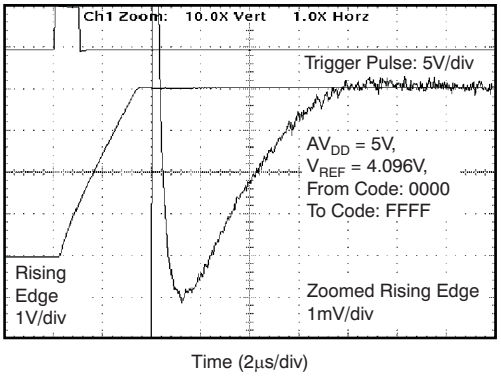


Figure 11.

FULL-SCALE SETTLING TIME: 5V FALLING EDGE

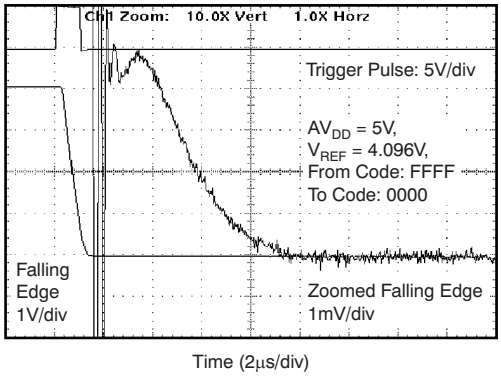


Figure 12.

TYPICAL CHARACTERISTICS: V_{DD} = 5V (continued)

At T_A = +25°C, unless otherwise noted.

HALF-SCALE SETTLING TIME: 5V RISING EDGE

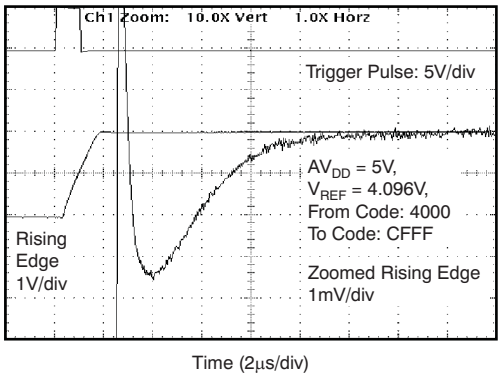


Figure 13.

HALF-SCALE SETTLING TIME: 5V FALLING EDGE

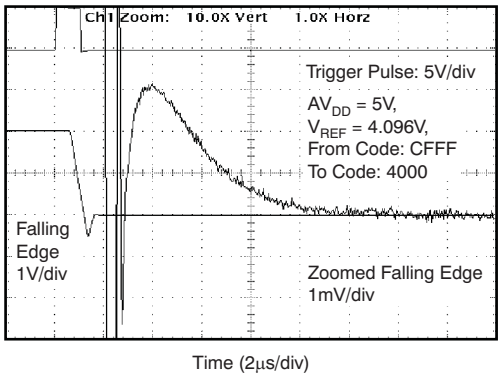


Figure 14.

GLITCH ENERGY: 5V, 1LSB STEP, RISING EDGE

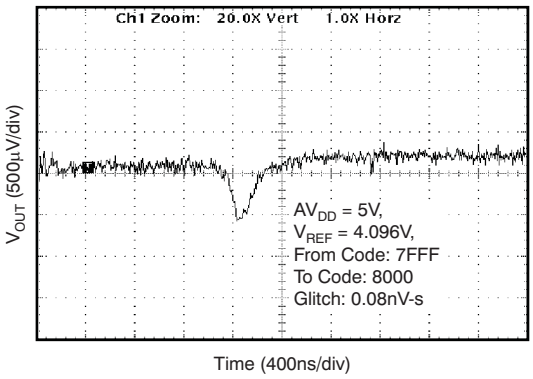


Figure 15.

GLITCH ENERGY: 5V, 1LSB STEP, FALLING EDGE

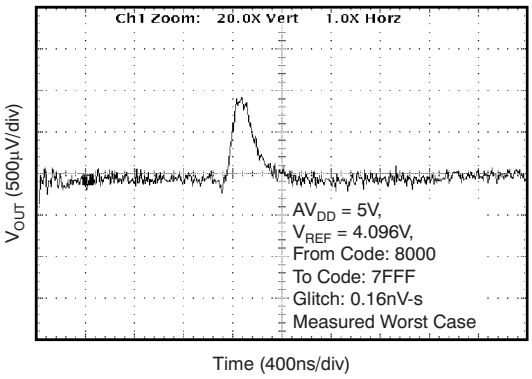


Figure 16.

GLITCH ENERGY: 5V, 16LSB STEP, RISING EDGE

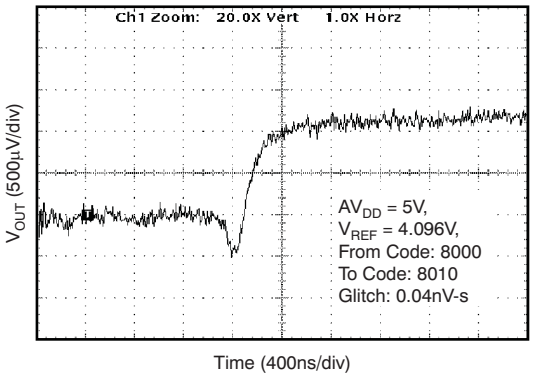


Figure 17.

GLITCH ENERGY: 5V, 16LSB STEP, FALLING EDGE

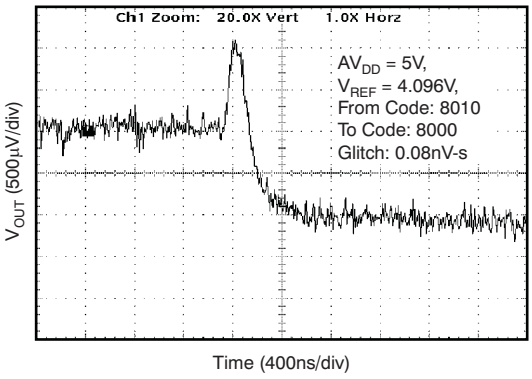


Figure 18.

TYPICAL CHARACTERISTICS: V_{DD} = 5V (continued)

At T_A = +25°C, unless otherwise noted.

GLITCH ENERGY: 5V, 256LSB STEP, RISING EDGE

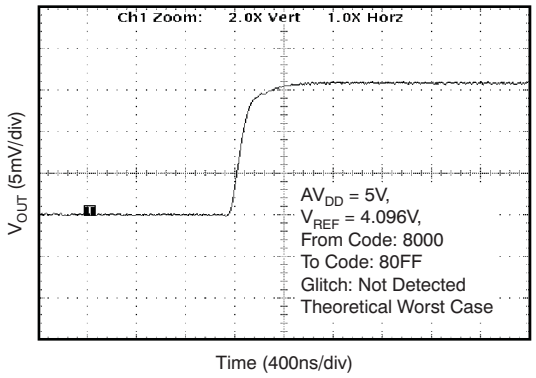


Figure 19.

GLITCH ENERGY: 5V, 256LSB STEP, FALLING EDGE

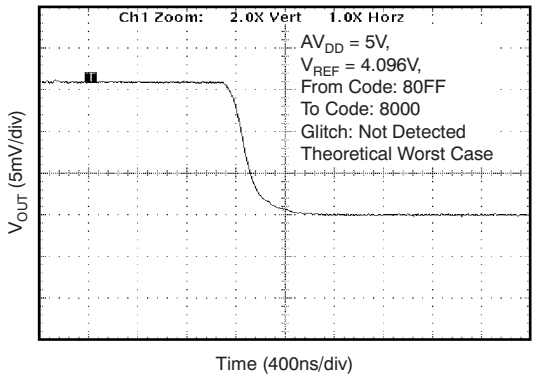


Figure 20.

OUTPUT NOISE DENSITY

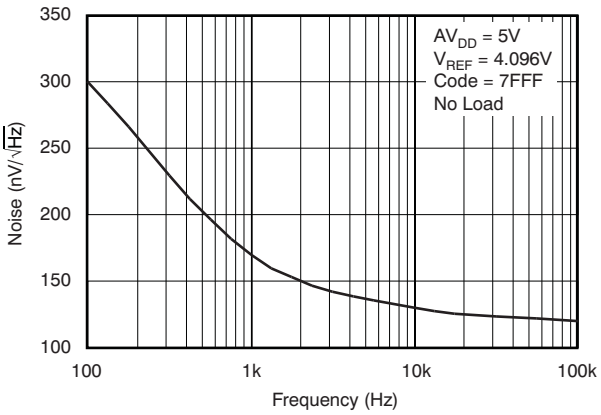


Figure 21.

SIGNAL-TO-NOISE RATIO vs OUTPUT FREQUENCY

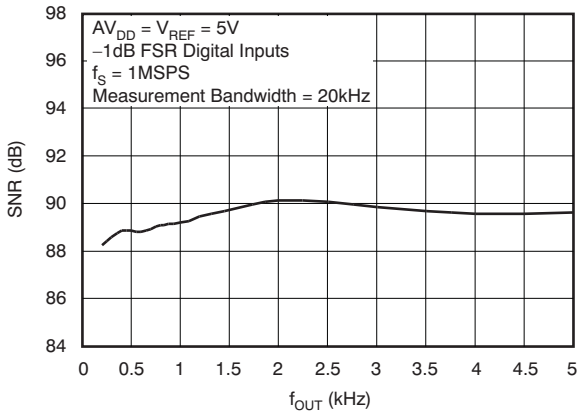


Figure 22.

TYPICAL CHARACTERISTICS: V_{DD} = 2.7V

At T_A = +25°C, unless otherwise noted.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

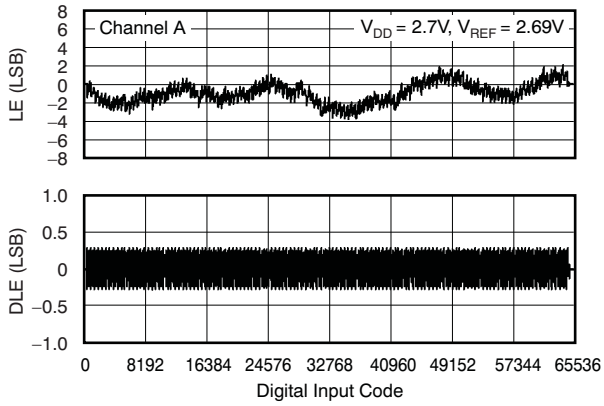


Figure 23.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

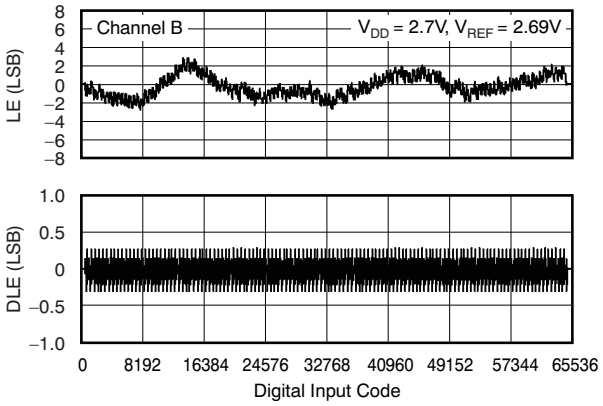


Figure 24.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

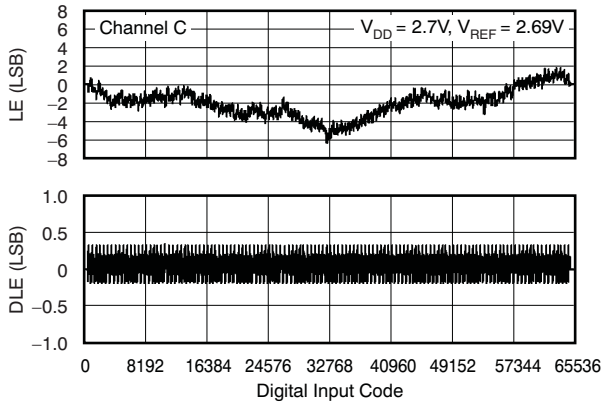


Figure 25.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

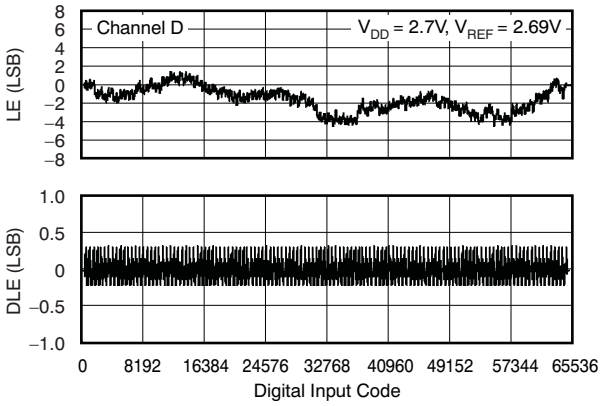


Figure 26.

ZERO-SCALE ERROR vs TEMPERATURE

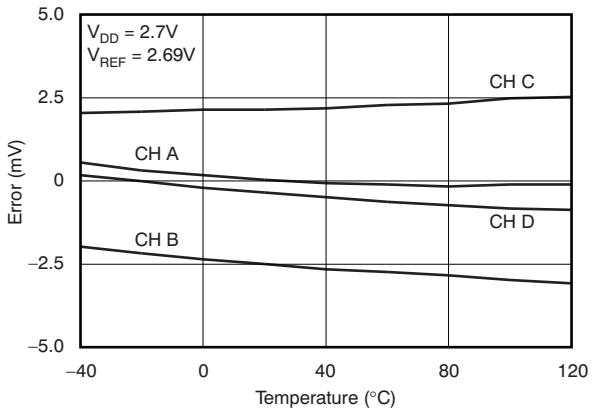


Figure 27.

FULL-SCALE ERROR vs TEMPERATURE

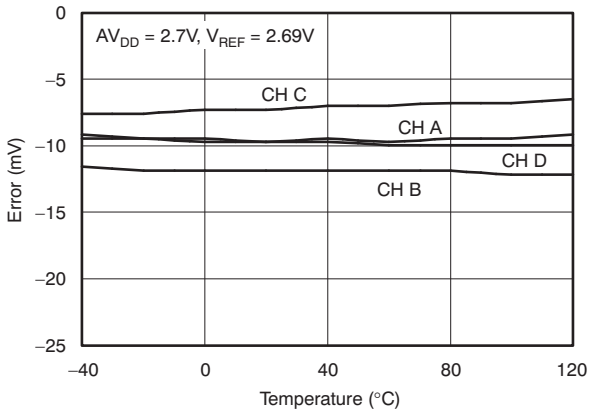


Figure 28.

TYPICAL CHARACTERISTICS: V_{DD} = 2.7V (continued)

At T_A = +25°C, unless otherwise noted.

SOURCE CURRENT CAPABILITY (ALL CHANNELS)

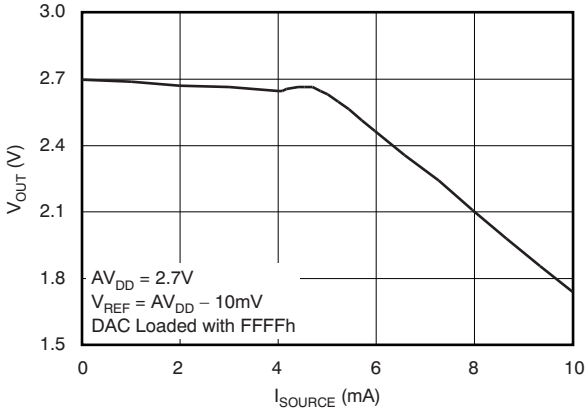


Figure 29.

SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

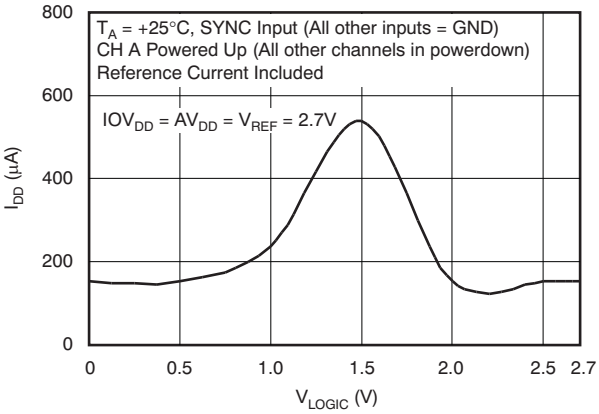


Figure 30.

FULL-SCALE SETTLING TIME: 2.7V RISING EDGE

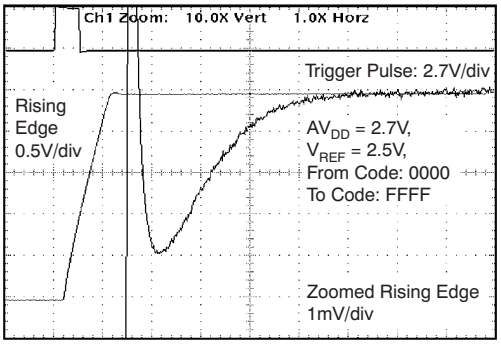


Figure 31.

FULL-SCALE SETTLING TIME: 2.7V FALLING EDGE

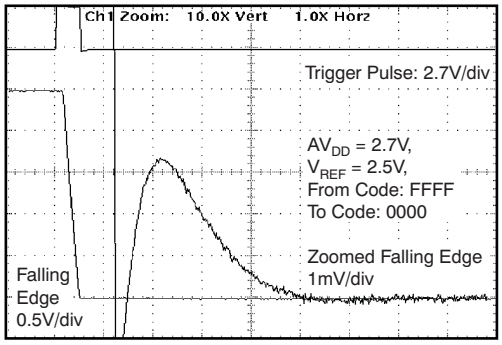


Figure 32.

HALF-SCALE SETTLING TIME: 2.7V RISING EDGE

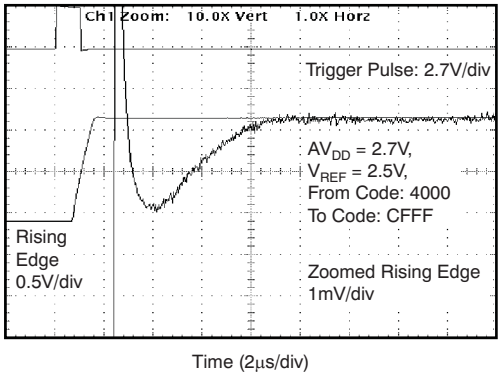


Figure 33.

HALF-SCALE SETTLING TIME: 2.7V FALLING EDGE

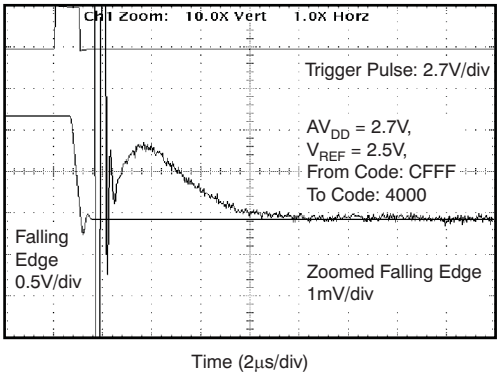


Figure 34.

TYPICAL CHARACTERISTICS: V_{DD} = 2.7V (continued)

At T_A = +25°C, unless otherwise noted.

GLITCH ENERGY: 2.7V, 1LSB STEP, RISING EDGE

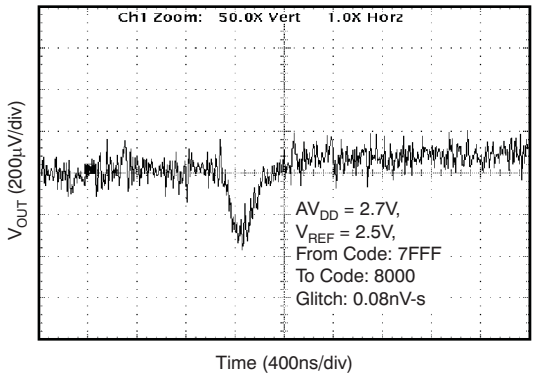


Figure 35.

GLITCH ENERGY: 2.7V, 1LSB STEP, FALLING EDGE

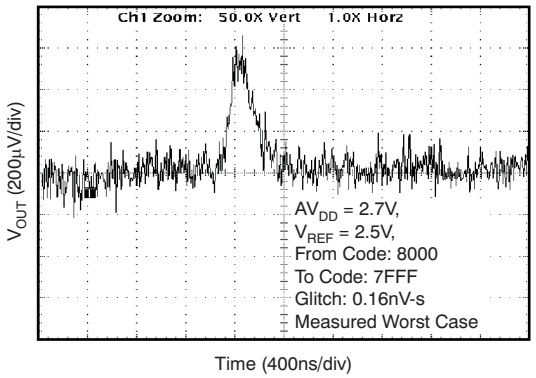


Figure 36.

GLITCH ENERGY: 2.7V, 16LSB STEP, RISING EDGE

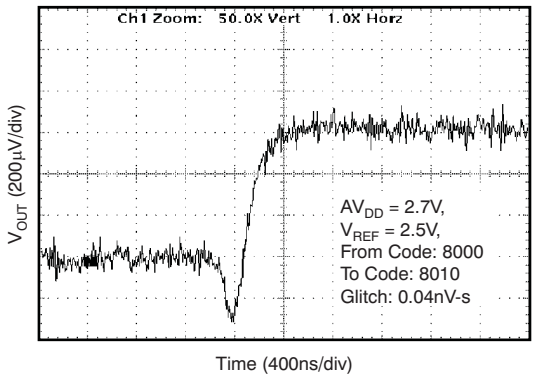


Figure 37.

GLITCH ENERGY: 2.7V, 16LSB STEP, FALLING EDGE

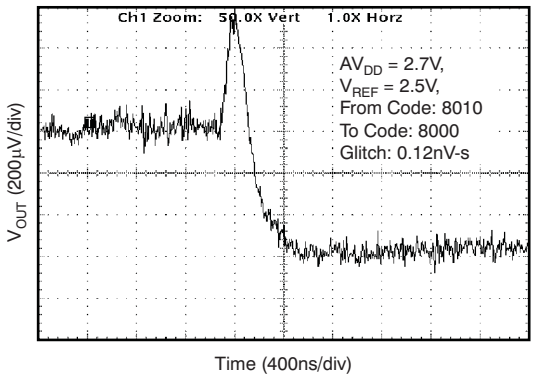


Figure 38.

GLITCH ENERGY: 2.7V, 256LSB STEP, RISING EDGE

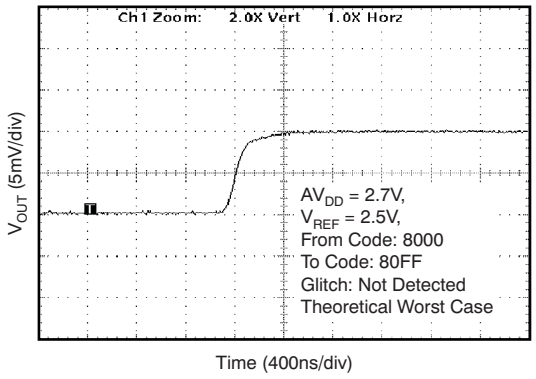


Figure 39.

GLITCH ENERGY: 2.7V, 256LSB STEP, FALLING EDGE

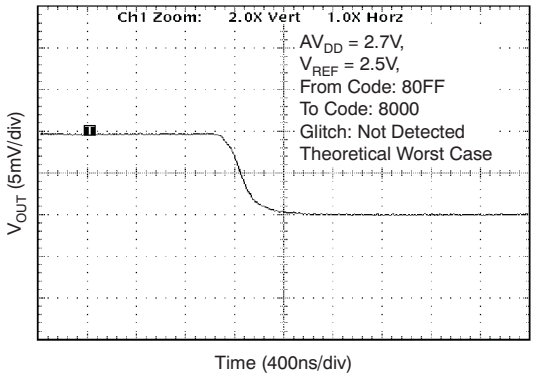


Figure 40.

TYPICAL CHARACTERISTICS: V_{DD} = 5V and 2.7V

At T_A = +25°C, unless otherwise noted.

SINK CURRENT CAPABILITY (ALL CHANNELS)

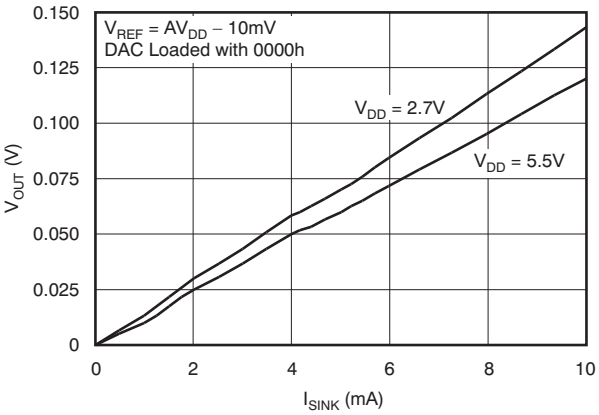


Figure 41.

SUPPLY CURRENT vs DIGITAL INPUT CODE

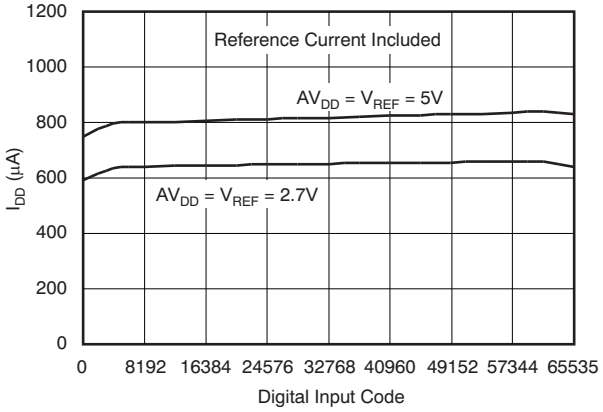


Figure 42.

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

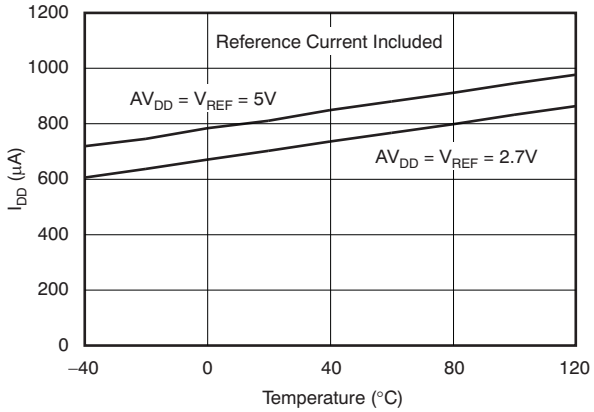


Figure 43.

SUPPLY CURRENT vs SUPPLY VOLTAGE

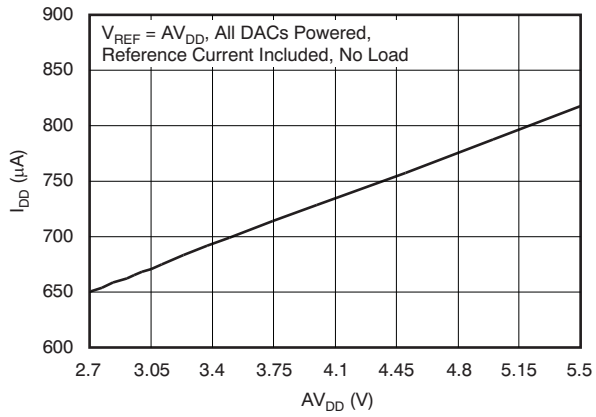


Figure 44.

THEORY OF OPERATION

DAC SECTION

The architecture of each channel of the DAC8555 consists of a resistor-string DAC followed by an output buffer amplifier. Figure 45 shows a simplified block diagram of the DAC architecture.

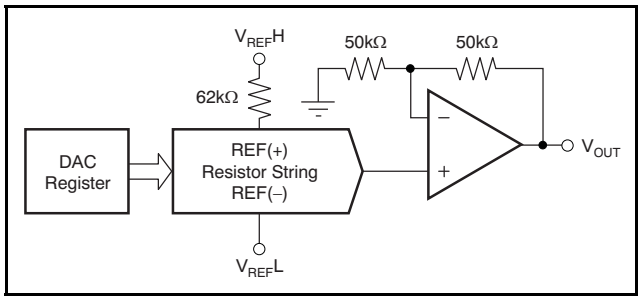


Figure 45. DAC8555 Architecture

The input coding for each device can be 2's complement or unipolar straight binary, so the ideal output voltage is given by:

$$V_{OUT}X = 2 \times V_{REF}L + \left(V_{REF}H - V_{REF}L\right) \times \frac{D_{IN}}{65536}$$

where D_{IN} = decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 65535.

RESISTOR STRING

The resistor string section is shown in Figure 46. It is simply a divide-by-2 resistor followed by a string of resistors. The code loaded into the DAC register determines at which node on the string the voltage is tapped off. This voltage is then applied to the output amplifier by closing one of the switches connecting the string to the amplifier.

OUTPUT AMPLIFIER

Each output buffer amplifier is capable of generating rail-to-rail voltages on its output that approaches an output range of 0V to AV_{DD} (gain and offset errors must be taken into account). Each buffer is capable of driving a load of 2kΩ in parallel with 1000pF to GND. The source and sink capabilities of the output amplifier can be seen in the Typical Characteristics.

SERIAL INTERFACE

The DAC8555 uses a 3-wire serial interface ($\overline{SYNC}$, SCLK, and D_{IN}), which is compatible with SPI, QSPI™, and Microwire™ interface standards, as well as most DSPs. See the Serial Write Operation timing diagram for an example of a typical write sequence.

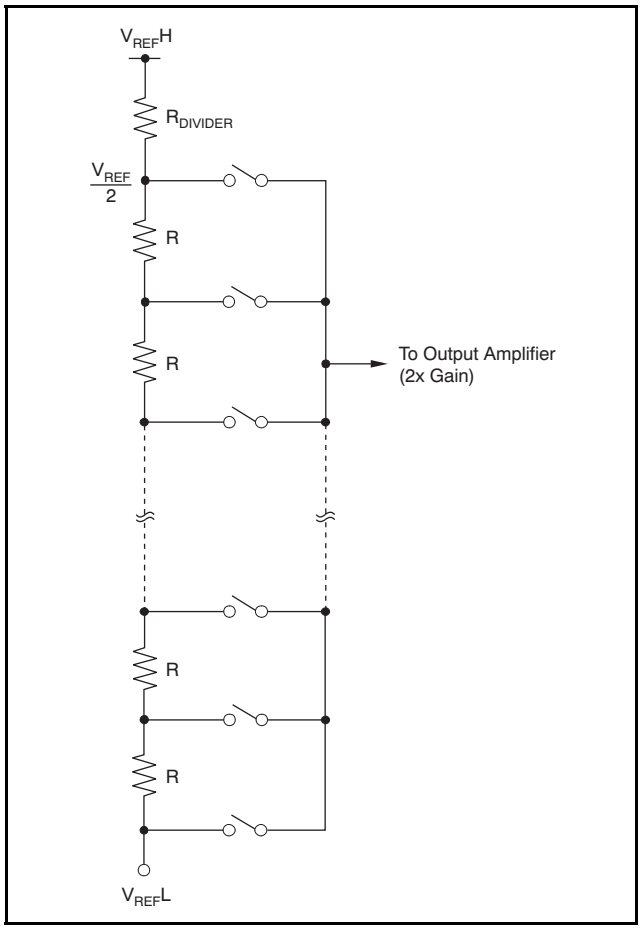


Figure 46. Resistor String

The write sequence begins by bringing the $\overline{SYNC}$ line LOW. Data from the D_{IN} line are clocked into the 24-bit shift register on each falling edge of SCLK. The serial clock frequency can be as high as 50MHz, making the DAC8555 compatible with high-speed DSPs. On the 24th falling edge of the serial clock, the last data bit is clocked into the shift register and the shift register gets locked. Further clocking does not change the shift register data. Once 24 bits are locked into the shift register, the eight MSBs are used as control bits and the 16 LSBs are used as data. After receiving the 24th falling clock edge, the DAC8555 decodes the eight control bits and 16 data bits to perform the required function, without waiting for a $\overline{SYNC}$ rising edge. A new SPI sequence starts at the next falling edge of $\overline{SYNC}$. A rising edge of $\overline{SYNC}$ before the 24-bit sequence is complete resets the SPI interface; no data transfer occurs.

After the 24th falling edge of SCLK is received, the $\overline{SYNC}$ line may be kept LOW or brought HIGH. In either case, the minimum delay time from the 24th falling SCLK edge to the next falling $\overline{SYNC}$ edge must be met in order to properly begin the next cycle.

To assure the lowest power consumption of the device, care should be taken that the levels are as close to each rail as possible. (Refer to the *Typical Characteristics* section for Figure 41, the *Supply Current vs Logic Input Voltage* transfer characteristic curve.)

IOV_{DD} AND VOLTAGE TRANSLATORS

The IOV_{DD} pin powers the the digital input structures of the DAC8555. For single-supply operation, it can be tied to AV_{DD}. For dual-supply operation, the IOV_{DD} pin provides interface flexibility with various CMOS logic families and should be connected to the logic supply of the system. Analog circuits and internal logic of the DAC8555 use AV_{DD} as the supply voltage. The external logic high inputs get translated to AV_{DD} by level shifters. These level shifters use the IOV_{DD} voltage as a reference to shift the incoming logic HIGH levels to AV_{DD}. IOV_{DD} is ensured to operate from 2.7V to 5.5V regardless of the AV_{DD} voltage, which ensures compatibility with various logic families. Although specified down to 2.7V, IOV_{DD} will operate at as low as 1.8V with degraded timing and temperature performance. For lowest power consumption, logic V_{IH} levels should be as close as possible to IOV_{DD}, and logic V_{IL} levels should be as close as possible to GND voltages.

ASYNCHRONOUS CLEAR

The DAC8555 output is asynchronously set to zero-scale voltage or midscale voltage (depending on RSTSEL) immediately after the $\overline{RST}$ pin is brought low. The $\overline{RST}$ signal resets all internal registers, and therefore, behaves like the Power-On Reset. The $\overline{RST}$ pin must be brought back to high before a write sequence is started.

If the RSTSEL pin is high, $\overline{RST}$ signal going low resets all outputs to midscale. If the RSTSEL pin is low, $\overline{RST}$ signal going low resets all outputs to zero-scale. RSTSEL should be set at power up.

INPUT SHIFT REGISTER

The input shift register (SR) of the DAC8555 is 24 bits wide, as shown in Figure 47, and is made up of eight control bits (DB23–DB16) and 16 data bits (DB15–DB0). DB23 and DB22 should always be '0'.

LD1 (DB21) and LD0 (DB20) control the updating of each analog output with the specified 16-bit data value or power-down command. Bit DB19 is a *don't care* bit that does not affect the operation of the DAC8555, and can be '1' or '0'. The DAC channel select bits (DB18, DB17) control the destination of the data (or power-down command) from DAC A through DAC D. The final control bit, PD0 (DB16), selects the power-down mode of the DAC8555 channels.

DB23 DB12

0	0	LD1	LD0	X	DAC Select 1	DAC Select 0	PD0	D15	D14	D13	D12

DB11 DB0

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Figure 47. DAC8555 Data Input Register Format

The DAC8555 also supports a number of different load commands. The load commands can be summarized as follows:

DB21 = 0 and DB20 = 0: Single-channel store. The temporary register (data buffer) corresponding to a DAC selected by DB18 and DB17 is updated with the contents of SR data (or power-down).

DB21 = 0 and DB20 = 1: Single-channel update. The temporary register and DAC register corresponding to a DAC selected by DB18 and DB17 are updated with the contents of SR data (or power-down).

DB21 = 1 and DB20 = 0: Simultaneous update. A channel selected by DB18 and DB17 gets updated with the SR data, and simultaneously, all the other channels get updated with previous stored data (or power-down) from temporary registers.

DB21 = 1 and DB20 = 1: Broadcast update. If DB18 = 0, then SR data gets ignored, all channels get updated with previously stored data (or power-down). If DB18 = 1, then SR data (or power-down) updates all channels.

DB16 is a power-down flag. If this flag is set, then DB15 and DB14 select one of the four power-down modes of the device as described in Table 1. If DB16 = 1, DB15 and DB14 no longer represent the two MSBs of data, but represent a power-down condition described in Table 1. Similar to data, power-down conditions can be stored at the temporary registers of each DAC. It is possible to update DACs simultaneously either with data, power-down, or a combination of both.

Refer to Table 2 for more information.

Table 1. DAC8555 Power-Down Modes

PD0 (DB16)	PD1 (DB15)	PD2 (DB14)	OPERATING MODE
1	0	0	Output high impedance
1	0	1	Output typically 1kΩ to GND
1	1	0	Output typically 100kΩ to GND
1	1	1	Output high impedance

Power-down/data selection is as follows:

Table 2. Control Matrix

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13-DB0	DESCRIPTION
0	0	LD 1	LD 0	Don't Care	DAC Sel 1	DAC Sel 0	PD0	MSB	MSB-1	MSB-2...LSB	
		0	0	X	0	0	0	Data			Write to buffer A with data
		0	0	X	0	1	0	Data			Write to buffer B with data
		0	0	X	1	0	0	Data			Write to buffer C with data
		0	0	X	1	1	0	Data			Write to buffer D with data
		0	0	X	(00, 01, 10, or 11)		1	See Table 1		0	Write to buffer (selected by DB17 and DB18) with power-down command
		0	1	X	(00, 01, 10, or 11)		0	Data			Write to buffer with data and load DAC (selected by DB17 and DB18)
		0	1	X	(00, 01, 10, or 11)		1	See Table 1		0	Write to buffer with power-down command and load DAC (selected by DB17 and DB18)
		1	0	X	(00, 01, 10, or 11)		0	Data			Write to buffer with data (selected by DB17 and DB18) and then load all DACs simultaneously from their corresponding buffers.
		1	0	X	(00, 01, 10, or 11)		1	See Table 1		0	Write to buffer with power-down command (selected by DB17 and DB18) and then load all DACs simultaneously from their corresponding buffers.
Broadcast Modes											
X	X	1	1	X	0	X	X	X			Simultaneously update all channels of DAC8555 with data stored in each channels temporary register.
X	X	1	1	X	1	X	0	Data			Write to all channels and load all DACs with SR data
X	X	1	1	X	1	X	1	See Table 1		0	Write to all channels and load all DACs with power-down command in SR.

$\overline{\text{SYNC}}$ INTERRUPT

In a normal write sequence, the $\overline{\text{SYNC}}$ line is kept LOW for at least 24 falling edges of SCLK and the addressed DAC register is updated on the 24th falling edge. However, if $\overline{\text{SYNC}}$ is brought HIGH before the 24th falling edge, it acts as an interrupt to the write sequence; the shift register is reset and the write sequence is discarded. Neither an update of the data buffer contents, DAC register contents, nor a change in the operating mode occurs (see Figure 48).

POWER-ON RESET TO ZERO-SCALE/MIDSCALE

The DAC8555 contains a power-on reset circuit that controls the output voltage during power-up. Depending on RSTSEL signal, on power-up, the DAC registers are reset and the output voltages are set to zero-scale (RSTSEL = 0) or midscale (RSTSEL = 1); they remain that way until a valid write sequence and load command are made to the respective DAC channel. The power-on reset is useful in applications where it is important to know the state of the output of each DAC while the device is in the process of powering up.

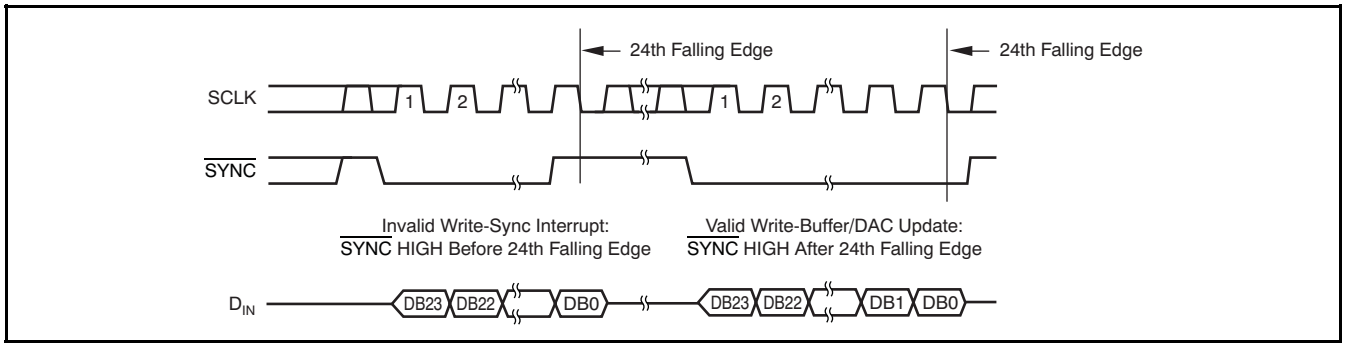


Figure 48. Interrupt and Valid $\overline{\text{SYNC}}$ Timing

POWER-DOWN MODES

The DAC8555 uses four modes of operation. These modes are accessed by setting three bits (PD2, PD1, and PD0) in the shift register and performing a *Load* action to the DACs. The DAC8555 offers a very flexible power-down interface based on channel register operation. A channel consists of a single 16-bit DAC with power-down circuitry, a temporary storage register (TR), and a DAC register (DR). TR and DR are both 18 bits wide. Two MSBs represent a power-down condition and 16 LSBs represent data for TR and DR. By adding bits 17 and 18 to TR and DR, a power-down condition can be temporarily stored and used as data. Internal circuits ensure that DB15 and DB14 are transferred to TR17 and TR16 (DR17 and DR16), when DB16 = '1'.

The DAC8555 treats the power-down condition as data; all the operational modes are still valid for power-down. It is possible to broadcast a power-down condition to all the DAC8555s in a system, or it is possible to simultaneously power-down a channel while updating data on other channels.

DB16, DB15, and DB14 = '100' (or '111') represent a power-down condition with Hi-Z output impedance for a selected channel. '101' represents a power-down condition with 1kΩ output impedance and '110' represents a power-down condition with 100kΩ output impedance.

Individual channels can be separately powered down, reducing the total power consumption. When all channels are powered down, the DAC8555 power consumption drops below 2μA. There is no power-up command. When a channel is updated with data, it automatically exits power-down. All channels exit power-down simultaneously after a broadcast data update. The time to exit power-down is approximately 5μs. See Table 1 and Table 2 for power-down operation details.

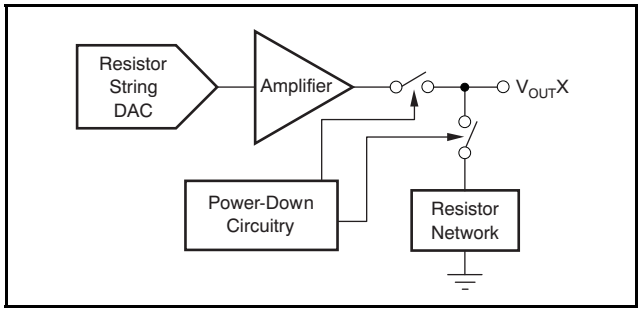


Figure 49. Output Stage During Power-Down (High-Impedance)

OPERATION EXAMPLES

Example 1: Write to Data Buffer A Through Buffer D; Load DAC A Through DAC D Simultaneously

- 1st — Write to data buffer A:

DB23	DB22	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	—	DB1	DB0
0	0	0	0	X	0	0	0	D15	—	D1	D0

- 2nd — Write to data buffer B:

DB23	DB22	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	—	DB1	DB0
0	0	0	0	X	0	1	0	D15	—	D1	D0

- 3rd — Write to data buffer C:

DB23	DB22	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	—	DB1	DB0
0	0	0	0	X	1	0	0	D15	—	D1	D0

- 4th — Write to data buffer D and simultaneously update all DACs:

DB23	DB22	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	—	DB1	DB0
0	0	1	0	X	1	1	0	D15	—	D1	D0

The DAC A, DAC B, DAC C, and DAC D analog outputs simultaneously settle to the specified values upon completion of the 4th write sequence. (The DAC voltages update simultaneously after the 24th SCLK falling edge of the 4th write cycle).

Example 2: Load New Data to DAC A Through DAC D Sequentially

- 1st — Write to data buffer A and load DAC A: DAC A output settles to specified value upon completion:

DB23	DB22	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	—	DB1	DB0
0	0	0	1	X	0	0	0	D15	—	D1	D0

- 2nd — Write to data buffer B and load DAC B: DAC B output settles to specified value upon completion:

DB23	DB22	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	—	DB1	DB0
0	0	0	1	X	0	1	0	D15	—	D1	D0

- 3rd — Write to data buffer C and load DAC C: DAC C output settles to specified value upon completion:

DB23	DB22	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	—	DB1	DB0
0	0	0	1	X	1	0	0	D15	—	D1	D0

- 4th — Write to data buffer D and load DAC D: DAC D output settles to specified value upon completion:

DB23	DB22	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	—	DB1	DB0
0	0	0	1	X	1	1	0	D15	—	D1	D0

After completion of each write cycle, DAC analog output settles to the voltage specified.

Example 3: Power Down DAC A and DAC B to 1kΩ and Power Down DAC C and DAC D to 100kΩ Simultaneously

- Write power-down command to data buffer A: DAC A to 1kΩ.

DB23	DB22	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	DB14	DB13	—
0	0	0	0	X	0	0	1	0	1	X	—

- Write power-down command to data buffer B: DAC B to 1kΩ.

DB23	DB22	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	DB14	DB13	—
0	0	0	0	X	0	1	1	0	1	X	—

- Write power-down command to data buffer C: DAC C to 1kΩ.

DB23	DB22	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	DB14	DB13	—
0	0	0	0	X	1	0	1	1	0	X	—

- Write power-down command to data buffer D: DAC D to 100kΩ and simultaneously update all DACs.

DB23	DB22	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	DB14	DB13	—
0	0	1	0	X	1	1	1	1	0	X	—

The DAC A, DAC B, DAC C, and DAC D analog outputs simultaneously power down to each respective specified mode upon completion of the 4th write sequence.

Example 4: Power Down DAC A Through DAC D to High-Impedance Sequentially:

- Write power-down command to data buffer A and load DAC A: DAC A output = Hi-Z:

DB23	DB22	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	DB14	DB13	—
0	0	0	1	X	0	0	1	1	1	X	—

- Write power-down command to data buffer B and load DAC B: DAC B output = Hi-Z:

DB23	DB22	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	DB14	DB13	—
0	0	0	1	X	0	1	1	1	1	x	—

- Write power-down command to data buffer C and load DAC C: DAC C output = Hi-Z:

DB23	DB22	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	DB14	DB13	—
0	0	0	1	X	1	0	1	1	1	X	—

- Write power-down command to data buffer D and load DAC D: DAC D output = Hi-Z:

DB23	DB22	LD1	LD0	DC	DAC Sel 1	DAC Sel 0	PD0	DB15	DB14	DB13	—
0	0	0	1	X	1	1	1	1	1	X	—

The DAC A, DAC B, DAC C, and DAC D analog outputs sequentially power down to high-impedance upon completion of the 1st, 2nd, 3rd, and 4th write sequences, respectively.

LDAC FUNCTIONALITY

The DAC8555 offers both a software and hardware simultaneous update function. The DAC8555 double-buffered architecture has been designed so that new data can be entered for each DAC without disturbing the analog outputs. The software simultaneous update capability is controlled by the load 1 (LD1) and load 0 (LD0) control bits. By setting load 1 = 1 all of the DAC registers will be updated on the falling edge of the 24th clock signal. When the new data has been entered into the device, all of the DAC outputs can be updated simultaneously and synchronously with the clock.

DAC8555 data updates are *synchronized* with the falling edge of the 24th SCLK cycle, which follows a falling edge of SYNC. For such *synchronous* updates, the LDAC pin is not required and it must be connected to GND permanently. The LDAC pin is used as a positive edge triggered timing signal for *asynchronous* DAC updates. Data buffers of all channels must be loaded with desired data before LDAC is triggered. After a low-to-high LDAC transition, all DACs are simultaneously updated with the contents of the corresponding data buffers. If the contents of a data buffer are not changed by the serial interface, the corresponding DAC output will remain unchanged after the LDAC trigger.

ENABLE PIN

For normal operation, the enable pin must be tied to a logic low. If the enable pin is tied high, the DAC8555 stops listening to the serial port. This feature can be useful for applications that share the same serial port.

MICROPROCESSOR INTERFACING

DAC8555 to 8051 Interface

See Figure 50 for a serial interface between the DAC8555 and a typical 8051-type microcontroller. The setup for the interface is as follows: TXD of the 8051 drives SCLK of the DAC8555, while RXD drives the serial data line of the device. The $\overline{\text{SYNC}}$ signal is derived from a bit-programmable pin on the port of the 8051. In this case, port line P3.3 is used. When data are to be transmitted to the DAC8555, P3.3 is taken LOW. The 8051 transmits data in 8-bit bytes; thus, only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left LOW after the first eight bits are transmitted, then a second and third write cycle are initiated to transmit the remaining data. P3.3 is taken HIGH following the completion of the third write cycle. The 8051 outputs the serial data in a format that presents the LSB first, while the DAC8555 requires data with the MSB as the first bit received. The 8051 transmit routine must therefore take this into account, and *mirror* the data as needed.

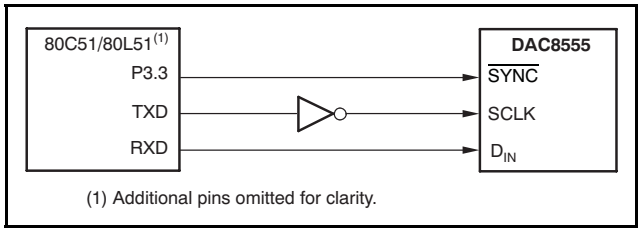


Figure 50. DAC8555 to 80C51/80L51 Interface

DAC8555 to Microwire Interface

Figure 51 shows an interface between the DAC8555 and any Microwire-compatible device. Serial data are shifted out on the falling edge of the serial clock and is clocked into the DAC8555 on the rising edge of the SK signal.

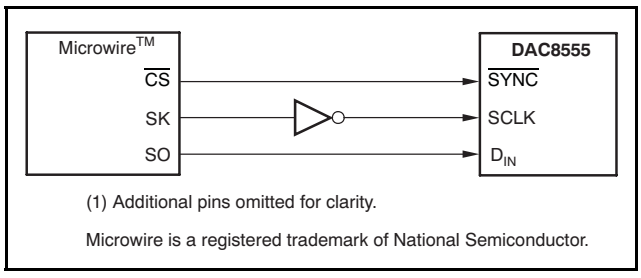


Figure 51. DAC8555 to Microwire Interface

DAC8555 to 68HC11 Interface

Figure 52 shows a serial interface between the DAC8555 and the 68HC11 microcontroller. SCK of the 68HC11 drives the SCLK of the DAC8555, while the MOSI output drives the serial data line of the DAC. The SYNC signal is derived from a port line (PC7), similar to the 8051 diagram.

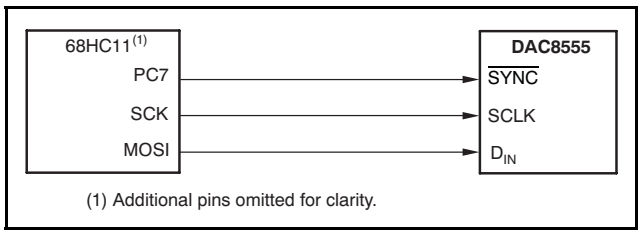


Figure 52. DAC8555 to 68HC11 Interface

The 68HC11 should be configured so that its CPOL bit is '0' and its CPHA bit is '1'. This configuration causes data appearing on the MOSI output to be valid on the falling edge of SCLK. When data are being transmitted to the DAC, the $\overline{\text{SYNC}}$ line is held LOW (PC7). Serial data from the 68HC11 are transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. (Data are transmitted MSB first.) In order to load data to the DAC8555, PC7 is left LOW after the first eight bits are transferred, then a second and third serial write operation are performed to the DAC. PC7 is taken HIGH at the end of this procedure.

DAC8555 to TMS320 DSP Interface

Figure 53 shows the connections between the DAC8555 and a TMS320 Digital Signal Processor (DSP). A single DSP can control up to four DAC8555s without any interface logic.

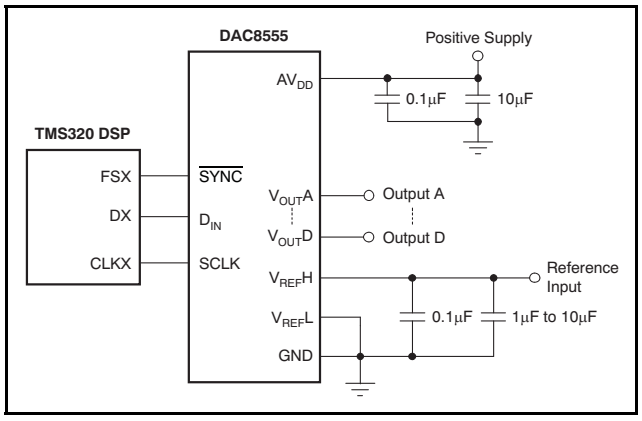


Figure 53. DAC8555 to TMS320 DSP

APPLICATION INFORMATION

CURRENT CONSUMPTION

The DAC8555 typically consumes 208µA at AV_{DD} = 5V and 180µA at AV_{DD} = 3V for each active channel, including reference current consumption. Additional current consumption can occur at the digital inputs if V_{IH} << IOV_{DD}. For most efficient power operation, CMOS logic levels are recommended at the digital inputs to the DAC.

In power-down mode, typical current consumption is 175nA per channel. A delay time of 10ms to 20ms after a power-down command is issued to the DAC is typically sufficient for the power-down current to drop below 10µA.

DRIVING RESISTIVE AND CAPACITIVE LOADS

The DAC8555 output stage is capable of driving loads of up to 1000pF while remaining stable. Within the offset and gain error margins, the DAC8555 can operate rail-to-rail when driving a capacitive load. Resistive loads of 2kΩ can be driven by the DAC8555 while achieving good load regulation. When the outputs of the DAC are driven to the positive rail under resistive loading, the PMOS transistor of each Class-AB output stage can enter into the linear region. When this scenario occurs, the added IR voltage drop deteriorates the linearity performance of the DAC. This deterioration only occurs within approximately the top 100mV of the DAC output voltage characteristic. Under resistive loading conditions, good linearity is preserved as long as the output voltage is at least 100mV below the AV_{DD} voltage.

CROSSTALK AND AC PERFORMANCE

The DAC8555 architecture uses separate resistor strings for each DAC channel in order to achieve ultra-low crosstalk performance. DC crosstalk seen at one channel during a full-scale change on the neighboring channel is typically less than 0.5LSBs. The AC crosstalk measured (for a full-scale, 1kHz sine wave output generated at one channel, and measured at the remaining output channel) is typically under –100dB.

In addition, the DAC8555 can achieve typical AC performance of 95dB signal-to-noise ratio (SNR) and –85dB total harmonic distortion (THD), making the DAC8555 a solid choice for applications requiring high SNR at output frequencies at or below 10kHz.

OUTPUT VOLTAGE STABILITY

The DAC8555 exhibits excellent temperature stability of 5ppm/°C typical output voltage drift over the specified temperature range of the device. This stability enables the output voltage of each channel to stay within a ±25µV window for a ±1°C ambient temperature change.

Good power-supply rejection ratio (PSRR) performance reduces supply noise present on AV_{DD} from appearing at the outputs to well below 10µV-s. Combined with good dc noise performance and true 16-bit differential linearity, the DAC8555 becomes a perfect choice for closed-loop control applications.

SETTLING TIME AND OUTPUT GLITCH PERFORMANCE

The DAC8555 settles to ±0.003% of its full-scale range within 10µs, driving a 200pF 2kΩ load. For good settling performance, the outputs should not approach the top and bottom rails. Small signal settling time is under 1µs, enabling data update rates exceeding 1MSPS for small code changes.

Many applications are sensitive to undesired transient signals such as glitch. The DAC8555 has a proprietary, ultra-low glitch architecture addressing such applications. Code-to-code glitches rarely exceed 1mV and they last under 0.3µs. Typical glitch energy is an outstanding 0.15nV-s. Theoretical worst-case glitch should occur during a 256LSB step, but it is so low, it cannot be detected.

DIFFERENTIAL AND INTEGRAL NONLINEARITY

The DAC8555 uses precision thin film resistors to achieve monotonicity and good linearity. Typical linearity error is ±4LSBs, with a ±0.3mV error for a 5V range. Differential linearity is typically ±0.25LSBs, with a ±19µV error for a consecutive code change.

USING THE REF02 AS A POWER SUPPLY FOR THE DAC8555

Due to the extremely low supply current required by the DAC8555, a possible configuration is to use a REF02 +5V precision voltage reference to supply the required voltage to the DAC8555 supply input as well as the reference input, as shown in Figure 54. This is especially useful if the power supply is quite noisy or if the system supply voltages are at some value other than 5V. The REF02 will output a steady supply voltage for the DAC8555. If the REF02 is used, the current it needs to supply to the DAC8555 is 0.85mA typical for AV_{DD} = 5V. When a DAC output is loaded, the REF02 also needs to supply the current to the load. The total typical current required (with a 5kΩ load on a given DAC output) is:

0.85mA + (5V/5kΩ) = 1.85mA

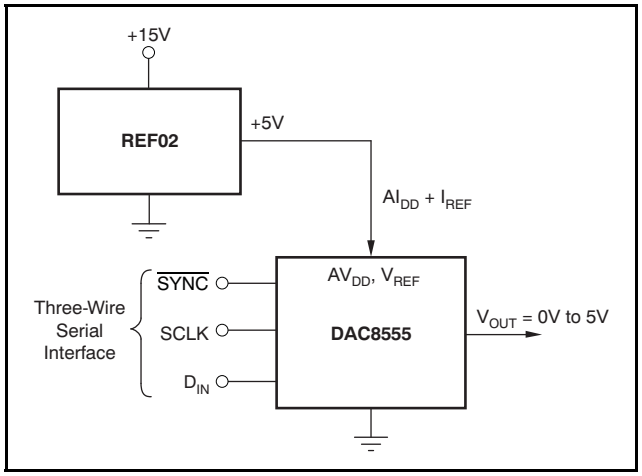


Figure 54. REF02 as a Power Supply to the DAC8555

BIPOLAR OPERATION USING THE DAC8555

The DAC8555 has been designed for single-supply operation, but a bipolar output range is also possible using the circuit in Figure 55. The circuit shown will give an output voltage range of $\pm V_{REF}$. Rail-to-rail operation at the amplifier output is achievable using an amplifier such as the OPA703, as shown in Figure 55.

The output voltage for any input code can be calculated as follows:

$$V_{OUT}X = \left[V_{REF} \times \left(\frac{D}{65536} \right) \times \left(\frac{R_1 + R_2}{R_1} \right) - V_{REF} \times \left(\frac{R_2}{R_1} \right) \right]$$

where D represents the input code in decimal (0–65535).

With V_{REF} = 5V, $R_1 = R_2$ = 10kΩ.

$$V_{OUT}X = \left(\frac{10 \times D}{65536} \right) - 5V$$

Using this example, an output voltage range of ±5V with 0000h corresponding to a –5V output and FFFFh corresponding to a 5V output can be achieved. Similarly, using V_{REF} = 2.5V, a ±2.5V output voltage range can be achieved.

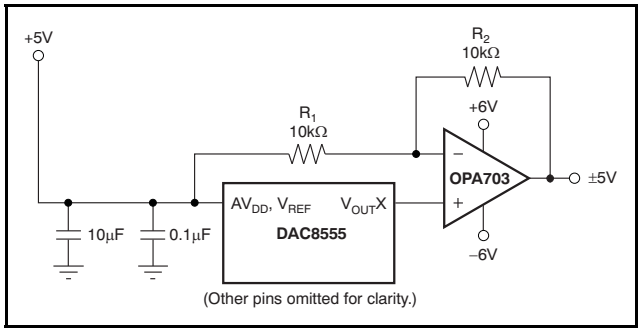


Figure 55. Bipolar Operation With the DAC8555

LAYOUT

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies.

The DAC8555 offers single-supply operation, and it will often be used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to keep digital noise from appearing at the output.

Due to the single ground pin of the DAC8555, all return currents, including digital and analog return currents for the DAC, must flow through a single point. Ideally, GND would be connected directly to an analog ground plane. This plane would be separate from the ground connection for the digital components until they were connected at the power-entry point of the system.

The power applied to AV_{DD} should be well-regulated and low-noise. Switching power supplies and DC/DC converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.

As with the GND connection, AV_{DD} should be connected to a positive power-supply plane or trace that is separate from the connection for digital logic until they are connected at the power-entry point. In addition, a 1µF to 10µF capacitor in parallel with a 0.1µF bypass capacitor is strongly recommended. In some situations, additional bypassing may be required, such as a 100µF electrolytic capacitor or even a *Pi* filter made up of inductors and capacitors—all designed to essentially low-pass filter the supply, removing the high-frequency noise.

Up to four DAC8555 devices can be used on a single SPI bus without any glue logic to create a high channel count solution. Special attention is required to avoid digital signal integrity problems when using multiple DAC8555s on the same SPI bus. Signal integrity of $\overline{SYNC}$, SCLK, and D_{IN} lines will not be an issue as long as the rise times of these digital signals are longer than six times the propagation delay between any two DAC8555 devices. Propagation speed is approximately six inches/ns on standard printed circuit boards (PCBs). Therefore, if the digital signal rise time is 1ns, the distance between any two DAC8555s has to be further apart on the PCB, and the signal rise times should be reduced by placing series resistors at the drivers for $\overline{SYNC}$, SCLK, and D_{IN} lines. If the largest distance between any two DAC8555s must be six inches, the rise time should be reduced to 6ns with an RC network formed by the series resistor at the digital driver and the total trace and input capacitance on the PCB.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC8555IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	D8555	Samples
DAC8555IPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	D8555	Samples

(1) The marketing status values are defined as follows:
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LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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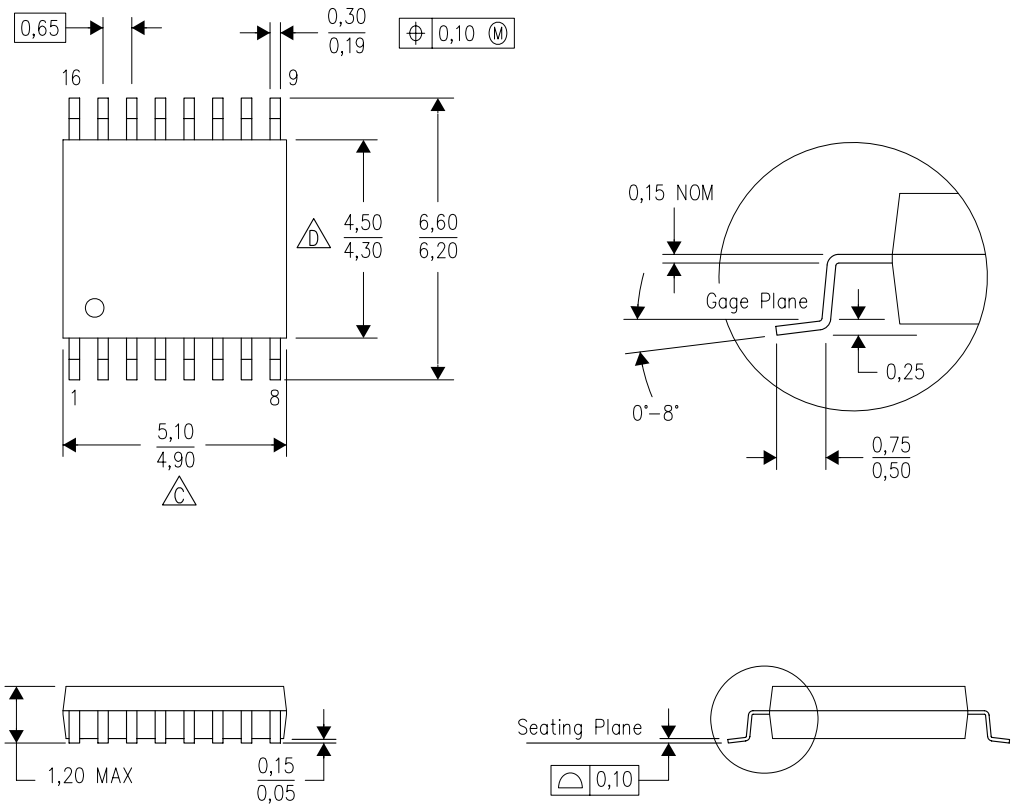
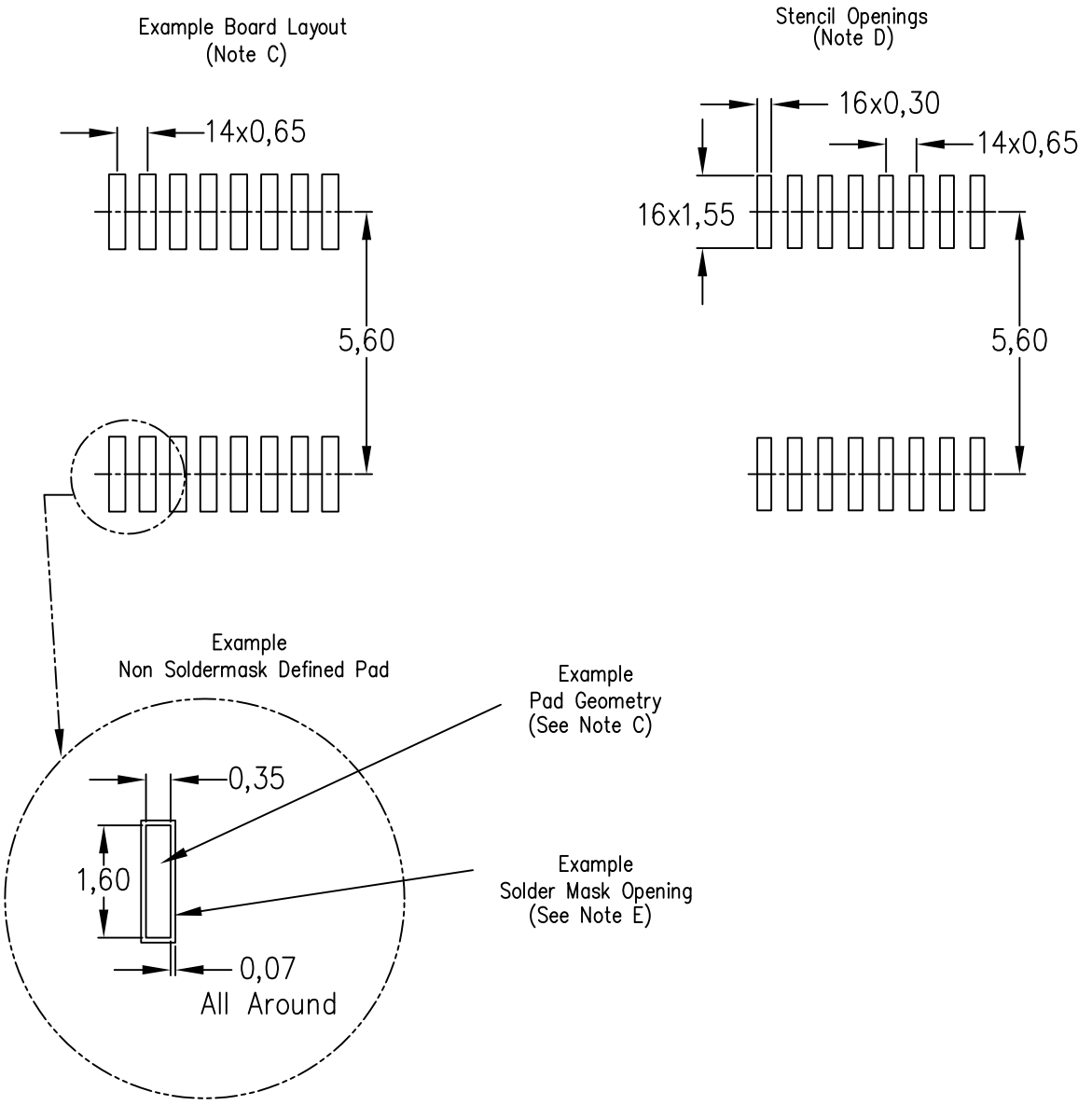


4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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