

# 512MB DDR SDRAM SoDIMM

## 200 PIN SO-DIMM

SDN06464D1BJ1SA-xx(W)R

512MByte in FBGA Technology

RoHS compliant

Options:

- |                                    |               |
|------------------------------------|---------------|
| ▪ Data Rate / Latency              | Marking       |
| DDR 400 MT/s CL3                   | -50           |
| DDR 333 MT/s CL2.5                 | -60           |
| ▪ Module density                   |               |
| 512MB with 8 dies and 1 rank       |               |
| ▪ Standard Grade (T <sub>A</sub> ) | 0°C to 70°C   |
| W-Grade (T <sub>A</sub> )          | -40°C to 85°C |

\*) The refresh rate has to be doubled when 85°C < T<sub>c</sub> < 95°C

## Environmental Requirements:

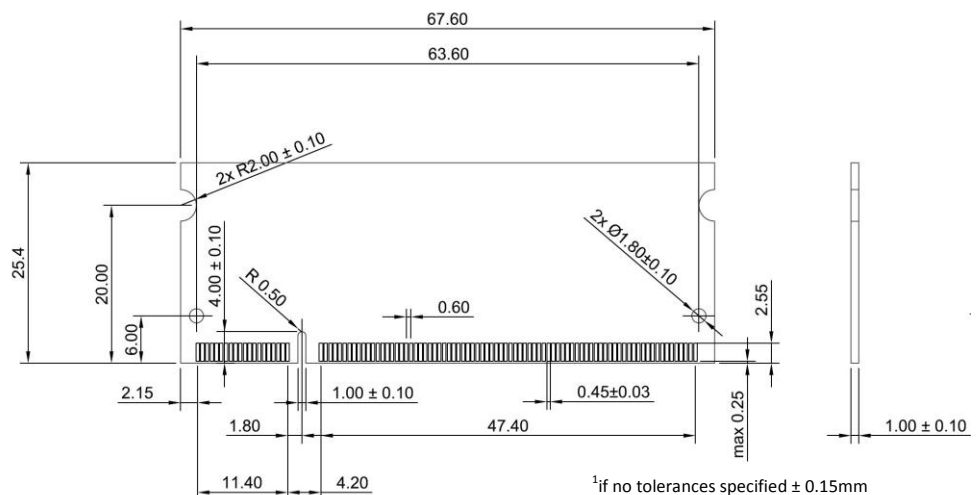
- Operating temperature (ambient)
 

|                |               |
|----------------|---------------|
| Standard Grade | 0°C to 70°C   |
| W-Grade        | -40°C to 85°C |
- Operating Humidity
- 10% to 90% relative humidity, noncondensing
- Operating Pressure
- 105 to 69 kPa (up to 10000 ft.)
- Storage Temperature
- 55°C to 100°C
- Storage Humidity
- 5% to 95% relative humidity, noncondensing
- Storage Pressure
- 1682 PSI (up to 5000 ft.) at 50°C

## Features:

- 200-pin 64-bit DDR1 Small Outline Dual-In-Line Double Data Rate Synchronous DRAM module
- Module organization: single rank 64M x 64
- V<sub>DD</sub> = 2.5V ±0.2V, V<sub>DDQ</sub> 2.5V ±0.2V
- V<sub>DD</sub> = 2.6V ±0.1V, V<sub>DDQ</sub> 2.6V ±0.1V (DDR400)
- 2.5V I/O ( SSTL\_2 compatible)
- Serial Presence Detect with EEPROM
- Gold-contact pads
- This module is fully pin and functional compatible to the JEDEC PC-3200 spec. and JEDEC- Standard MO-224. (see [www.jedec.org](http://www.jedec.org))
- The pcb and all components are manufactured according to the RoHS compliance specification [EU Directive 2002/95/EC Restriction of Hazardous Substances (RoHS)]
- **DDR1 - SDRAM component Samsung K4H510838J**
- 64Mx8 DDR1 SDRAM in 60-ball FBGA package
- Internal, pipelined double-data-rate (DDR)
- 2n pre-fetch architecture
- DLL to align DQ and DQS transitions with CK
- Bidirectional data strobe (DQS) transmitted/received with data, source-synchronous data capture
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- Four internal banks for concurrent operation
- Data mask (DM) for masking write data
- Programmable burst length: 2,4 or 8
- Adjustable data-output drive strength
- Auto Refresh (CBR) and Self Refresh, 8k Refresh every 64ms

Figure: mechanical dimensions<sup>1</sup>



This Swissbit module family is industry standard 200-pin 8-byte Double Data rate synchronous SDRAM Small Outline Dual-In-line Memory Modules (So-DIMMs), which are organized as x64 high speed memory arrays designed for use in non-parity applications. These So-DIMMs are assembled in FBGA Technology. The passive devices and the EEPROM are SMD components.

The So-DIMMs use serial presence detects (SPD) implemented via serial EEPROM using the two-pin-I<sup>2</sup>C protocol. The first 128 bytes are utilized by the So-DIMM manufacturer and the second 128 bytes are available to the end user.

All Swissbit DDR1 So-DIMMs provide a high performance, flexible 8-byte interface in a 67.6 mm long footprint.

All modules of the extended temperature grade have seen special tests during the manufacturing process to ensure proper operation according to the field of operation as stated in the environmental conditions.

### Module Configuration

| Organization | DDR SDRAMs used | Row Addr. | Bank Select | Col. Addr. | Refresh | Module Dimensions in mm |
|--------------|-----------------|-----------|-------------|------------|---------|-------------------------|
| 64M x 64     | 8 x 64M x 8     | 13        | BA0, BA1    | 11         | 8k      | 67.60 x 25,4 x 3.80 max |

### Product Spectrum

| Part Number            | Module Density | Transfer Rate | Clock Cycle/Data bit rate | Latency |
|------------------------|----------------|---------------|---------------------------|---------|
| SDN06464D1BJ1SA-50[W]R | 512MB          | 3.2 GB/s      | 5.0ns/400MT/s             | 3.0-3-3 |
| SDN06464D1BJ1SA-60[W]R | 512MB          | 2.7 GB/s      | 6.0ns/333MT/s             | 2.5-3-3 |

### Pin Name

|                 |                             |
|-----------------|-----------------------------|
| A0-9, A11 – A12 | Address Inputs              |
| A10/AP          | Address Input/Autoprecharge |
| BA0, BA1        | Bank Selects                |
| DQ0 – DQ63      | Data Input/Output           |
| DM0-DM7         | Data Masks                  |
| RAS#            | Row Address Strobe          |
| CAS#            | Column Address Strobe       |
| WE#             | Read / Write Enable         |
| CKE0            | Clock Enable                |
| CK0             | Clock Inputs, positive line |
| CK0#            | Clock Inputs, negative line |
| DQS0- DQS7      | Data strobes                |

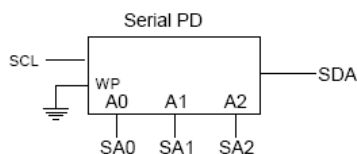
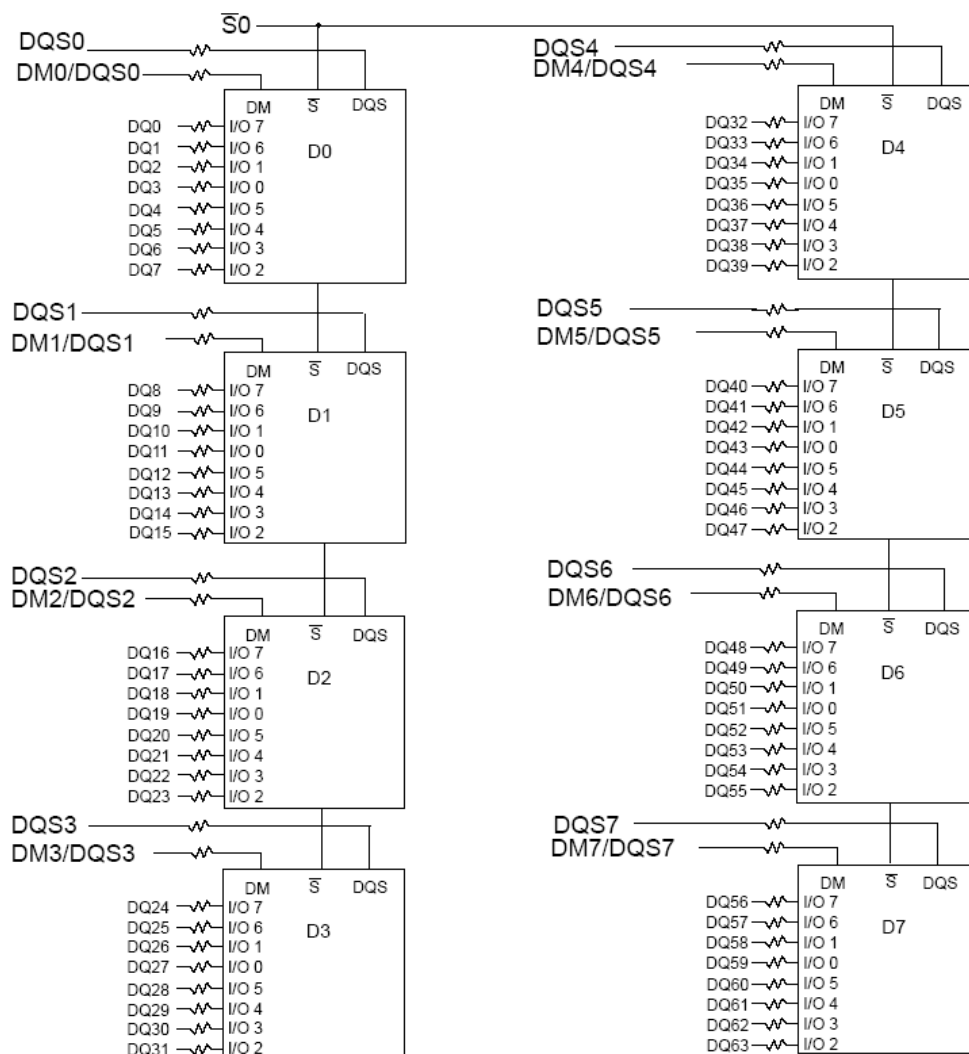
|                    |                                                    |
|--------------------|----------------------------------------------------|
| S0#                | Chip Select                                        |
| V <sub>DD</sub>    | Power (2.5V± 0.2V)                                 |
| V <sub>DDQ</sub>   | Power (2.5V±0.2V)                                  |
| V <sub>DDID</sub>  | V <sub>DD</sub> , V <sub>DDQ</sub> level detection |
| V <sub>DDSPD</sub> | SPD Power                                          |
| V <sub>REF</sub>   | Input/Output Reference                             |
| V <sub>SS</sub>    | Ground                                             |
| SCL                | Clock for Serial Presence Detect                   |
| SDA                | Serial Data Out for Serial Presence Detect         |
| NC                 | No Connection                                      |

**Pin Configuration**

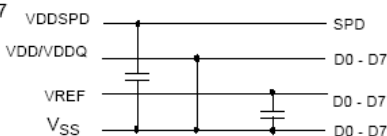
| PIN # | Front Side       | PIN # | Back Side        | PIN # | Front Side      | PIN # | Back Side       |
|-------|------------------|-------|------------------|-------|-----------------|-------|-----------------|
| 1     | V <sub>REF</sub> | 2     | V <sub>REF</sub> | 101   | A9              | 102   | A8              |
| 3     | V <sub>SS</sub>  | 4     | V <sub>SS</sub>  | 103   | V <sub>SS</sub> | 104   | V <sub>SS</sub> |
| 5     | DQ0              | 6     | DQ4              | 105   | A7              | 106   | A6              |
| 7     | DQ1              | 8     | DQ5              | 107   | A5              | 108   | A4              |
| 9     | V <sub>DD</sub>  | 10    | V <sub>DD</sub>  | 109   | A3              | 110   | A2              |
| 11    | DQS0             | 12    | DM0              | 111   | A1              | 112   | A0              |
| 13    | DQ2              | 14    | DQ6              | 113   | V <sub>DD</sub> | 114   | V <sub>DD</sub> |
| 15    | V <sub>SS</sub>  | 16    | V <sub>SS</sub>  | 115   | A10/AP          | 116   | BA1             |
| 17    | DQ3              | 18    | DQ7              | 117   | BA0             | 118   | RAS#            |
| 19    | DQ8              | 20    | DQ12             | 119   | WE#             | 120   | CAS#            |
| 21    | V <sub>DD</sub>  | 22    | V <sub>DD</sub>  | 121   | S0#             | 122   | NC/S1#          |
| 23    | DQ9              | 24    | DQ13             | 123   | NC/(A13)        | 124   | NC              |
| 25    | DQS1             | 26    | DM1              | 125   | V <sub>SS</sub> | 126   | V <sub>SS</sub> |
| 27    | V <sub>SS</sub>  | 28    | V <sub>SS</sub>  | 127   | DQ32            | 128   | DQ36            |
| 29    | DQ10             | 30    | DQ14             | 129   | DQ33            | 130   | DQ37            |
| 31    | DQ11             | 32    | DQ15             | 131   | V <sub>DD</sub> | 132   | V <sub>DD</sub> |
| 33    | V <sub>DD</sub>  | 34    | V <sub>DD</sub>  | 133   | DQS4            | 134   | DM4             |
| 35    | CK0              | 36    | V <sub>DD</sub>  | 135   | DQ34            | 136   | DQ38            |
| 37    | CK0#             | 38    | V <sub>SS</sub>  | 137   | V <sub>SS</sub> | 138   | V <sub>SS</sub> |
| 39    | V <sub>SS</sub>  | 40    | V <sub>SS</sub>  | 139   | DQ35            | 140   | DQ39            |
| 41    | DQ16             | 42    | DQ20             | 141   | DQ40            | 142   | DQ44            |
| 43    | DQ17             | 44    | DQ21             | 143   | V <sub>DD</sub> | 144   | V <sub>DD</sub> |
| 45    | V <sub>DD</sub>  | 46    | V <sub>DD</sub>  | 145   | DQ41            | 146   | DQ45            |
| 47    | DQS2             | 48    | DM2              | 147   | DQS5            | 148   | DM5             |
| 49    | DQ18             | 50    | DQ22             | 149   | V <sub>SS</sub> | 150   | V <sub>SS</sub> |
| 51    | V <sub>SS</sub>  | 52    | V <sub>SS</sub>  | 151   | DQ42            | 152   | DQ46            |

| PIN # | Front Side      | PIN # | Back Side       | PIN # | Front Side          | PIN # | Back Side       |
|-------|-----------------|-------|-----------------|-------|---------------------|-------|-----------------|
| 53    | DQ19            | 54    | DQ23            | 153   | DQ43                | 154   | DQ47            |
| 55    | DQ24            | 56    | DQ28            | 155   | V <sub>DD</sub>     | 156   | V <sub>DD</sub> |
| 57    | V <sub>DD</sub> | 58    | V <sub>DD</sub> | 157   | V <sub>DD</sub>     | 158   | CK1#            |
| 59    | DQ25            | 60    | DQ29            | 159   | V <sub>SS</sub>     | 160   | CK1             |
| 61    | DQS3            | 62    | DM3             | 161   | V <sub>SS</sub>     | 162   | V <sub>SS</sub> |
| 63    | V <sub>SS</sub> | 64    | V <sub>SS</sub> | 163   | DQ48                | 164   | DQ52            |
| 65    | DQ26            | 66    | DQ30            | 165   | DQ49                | 166   | DQ53            |
| 67    | DQ27            | 68    | DQ31            | 167   | V <sub>DD</sub>     | 168   | V <sub>DD</sub> |
| 69    | V <sub>DD</sub> | 70    | V <sub>DD</sub> | 169   | DQS6                | 170   | DM6             |
| 71    | NC/CB0          | 72    | NC/(CB4)        | 171   | DQ50                | 172   | DQ54            |
| 73    | NC/CB1          | 74    | NC/(CB5)        | 173   | V <sub>SS</sub>     | 174   | V <sub>SS</sub> |
| 75    | V <sub>SS</sub> | 76    | V <sub>SS</sub> | 175   | DQ51                | 176   | DQ55            |
| 77    | NC/(DQS8)       | 78    | NC/(DM8)        | 177   | DQ56                | 178   | DQ60            |
| 79    | NC/(CB2)        | 80    | NC/(CB6)        | 179   | V <sub>DD</sub>     | 180   | V <sub>DD</sub> |
| 81    | V <sub>DD</sub> | 82    | V <sub>DD</sub> | 181   | DQ57                | 182   | DQ61            |
| 83    | NC/(CB3)        | 84    | NC/(CB7)        | 183   | DQS7                | 184   | DM7             |
| 85    | NC              | 86    | NC/(RESET)      | 185   | V <sub>SS</sub>     | 186   | V <sub>SS</sub> |
| 87    | V <sub>SS</sub> | 88    | V <sub>SS</sub> | 187   | DQ58                | 188   | DQ62            |
| 89    | NC/(CK2)        | 90    | V <sub>SS</sub> | 189   | DQ59                | 190   | DQ63            |
| 91    | NC/(CK2#)       | 92    | V <sub>DD</sub> | 191   | V <sub>DD</sub>     | 192   | V <sub>DD</sub> |
| 93    | V <sub>DD</sub> | 94    | V <sub>DD</sub> | 193   | SDA                 | 194   | SA0             |
| 95    | NC/(CKE1)       | 96    | CKE0            | 195   | SCL                 | 196   | SA1             |
| 97    | NC              | 98    | NC/(BA2)        | 197   | V <sub>DD_SPD</sub> | 198   | SA2             |
| 99    | A12             | 100   | A11             | 199   | V <sub>DD_ID</sub>  | 200   | NC              |

FUNCTIONAL BLOCK DIAGRAMM 512MB DDR SDRAM SODIMM 1RANK; NON-ECC



BA0 - BA1 ———— BA0-BA1: SDRAMs D0 - D7  
A0 - A13 ———— A0-A13: SDRAMs D0 - D7  
RAS ———— RAS: SDRAMs D0 - D7  
CAS ———— CAS: SDRAMs D0 - D7  
CKE0 ———— CKE: SDRAMs D0 - D7  
WE ———— WE: SDRAMs D0 - D7



# DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(0°C ≤ T<sub>A</sub> ≤ + 70°C; V<sub>DDQ</sub> = +2.5V ± 0.2V, V<sub>DD</sub> = +2.5V ± 0.2V) see Note 1 on Page 9

| PARAMETER/ CONDITION                                                                                                                                                  | SYMBOL               | MIN                     | MAX                     | UNITS |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|-------------------------|-------------------------|-------|
| Supply Voltage                                                                                                                                                        | V <sub>DD</sub>      | 2.3                     | 2.7                     | V     |
| I/O Supply Voltage                                                                                                                                                    | V <sub>DDQ</sub>     | 2.3                     | 2.7                     | V     |
| I/O Reference Voltage                                                                                                                                                 | V <sub>REF</sub>     | 0.49 x V <sub>DDQ</sub> | 0.51x V <sub>DDQ</sub>  | V     |
| I/O Termination Voltage (system)                                                                                                                                      | V <sub>TT</sub>      | V <sub>REF</sub> - 0.04 | V <sub>REF</sub> + 0.04 | V     |
| Input High (Logic 1) Voltage                                                                                                                                          | V <sub>IH (DC)</sub> | V <sub>REF</sub> + 0.15 | V <sub>DD</sub> + 0.3   | V     |
| Input Low (Logic 0) Voltage                                                                                                                                           | V <sub>IL (DC)</sub> | -0.3                    | V <sub>REF</sub> - 0.15 | V     |
| INPUT LEAKAGE CURRENT<br>Any input 0V ≤ V <sub>IN</sub> ≤ V <sub>DD</sub> , V <sub>REF</sub> pin 0V ≤ V <sub>IN</sub> ≤ 1.35V<br>(All other pins not under test = 0V) | I <sub>I</sub>       | -16                     | 16                      | μA    |
| OUTPUT LEAKAGE CURRENT<br>(DQ <sub>S</sub> are disabled; 0V ≤ V <sub>OUT</sub> ≤ V <sub>DDQ</sub> )                                                                   | I <sub>OZ</sub>      | -40                     | 40                      | μA    |
| OUTPUT LEVELS:<br>High Current (V <sub>OUT</sub> = V <sub>DDQ</sub> -0.373V, minimum V <sub>REF</sub> , minimum V <sub>TT</sub> )                                     | I <sub>OH</sub>      | -16.8                   | -                       | mA    |
| Low Current (V <sub>OUT</sub> = 0.373V, maximum V <sub>REF</sub> , maximum V <sub>TT</sub> )                                                                          | I <sub>OL</sub>      | 16.8                    | -                       | mA    |

# AC INPUT OPERATING CONDITIONS

(0°C ≤ T<sub>A</sub> ≤ + 70°C; V<sub>DDQ</sub> = +2.5V ± 0.2V, V<sub>DD</sub> = +2.5V ± 0.2V) see Note 1 on Page 9

| PARAMETER/ CONDITION         | SYMBOL               | MIN                      | MAX                      | UNITS |
|------------------------------|----------------------|--------------------------|--------------------------|-------|
| Input High (Logic 1) Voltage | V <sub>IH (AC)</sub> | V <sub>REF</sub> + 0.310 | -                        | V     |
| Input Low (Logic 0) Voltage  | V <sub>IL (AC)</sub> | -                        | V <sub>REF</sub> - 0.310 | V     |
| I/O Reference Voltage        | V <sub>REF(AC)</sub> | 0.49 x V <sub>DDQ</sub>  | 0.51x V <sub>DDQ</sub>   | V     |

# CAPACITANCE

| PARAMETER                              | SYMBOL          | MIN  | MAX  | UNITS |
|----------------------------------------|-----------------|------|------|-------|
| Input/Output Capacitance: DQ, DQS      | C <sub>10</sub> | 4.0  | 5.0  | pF    |
| Input Capacitance: Command and Address | C <sub>11</sub> | 18.0 | 27.0 | pF    |
| Input Capacitance: /S 0,1              | C <sub>11</sub> | 18.0 | 27.0 | pF    |
| Input Capacitance: CK, /CK             | C <sub>12</sub> | 10.0 | 14.0 | pF    |
| Input Capacitance: CKE                 | C <sub>13</sub> | 18.0 | 27.0 | pF    |

# I<sub>DD</sub> Specifications AND CONDITIONS

(0°C ≤ T<sub>A</sub> ≤ + 70°C; V<sub>DDQ</sub> = +2.5V ± 0.2V, V<sub>DD</sub> = +2.5V ± 0.2V) see Note 1 on Page 9

| Parameter<br>& Test Condition                                                                                                                                                                                                                                                                                                     | Symbol                      | max.       |            | Unit |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|------------|------------|------|
|                                                                                                                                                                                                                                                                                                                                   |                             | 3200-3.033 | 2700-2.533 |      |
| <b>OPERATING CURRENT; *)</b> : One device bank; Active-Precharge;<br>t <sub>RC</sub> = t <sub>RC</sub> (Min); t <sub>CK</sub> = t <sub>CK</sub> (Min); DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles                                                       | I <sub>DD0</sub>            | 520        | 480        | mA   |
| <b>OPERATING CURRENT;*)</b><br>One device bank; Active-Read-Precharge;<br>Burst = 2; t <sub>RC</sub> = t <sub>RC</sub> (Min);<br>t <sub>CK</sub> = t <sub>CK</sub> (Min); I <sub>OUT</sub> = 0mA;<br>Address and control inputs changing once per clock cycle                                                                     | I <sub>DD1</sub>            | 600        | 560        | mA   |
| <b>PRECHARGE POWER-DOWN STANDBY CURRENT;</b><br>All device banks idle;<br>Power-down mode;<br>t <sub>CK</sub> = t <sub>CK</sub> (Min); CKE = (LOW)                                                                                                                                                                                | I <sub>DD2P</sub>           | 40         | 40         | mA   |
| <b>IDLE STANDBY CURRENT;</b> CS# = HIGH; All device banks idle;<br>t <sub>CK</sub> = t <sub>CK</sub> (Min); CKE = HIGH; Address and other control inputs changing once per clock cycle.<br>V <sub>IN</sub> = V <sub>REF</sub> for DQ, DQS, and DM                                                                                 | I <sub>DD2F</sub>           | 184        | 184        | mA   |
| <b>PRECHARGE QUIET STANDBY CURRENT;</b><br>CS# > V <sub>IH</sub> (min); All banks idle;<br>CKE >= V <sub>IH</sub> (min); t <sub>CK</sub> =6ns for DDR333, 5ns for DDR400;<br>Address and other control inputs stable at >=V <sub>IH</sub> (min) or <= V <sub>IL</sub> (max); V <sub>IN</sub> =V <sub>REF</sub> for DQ, DQS and DM | I <sub>DD2Q</sub>           | 160        | 160        | mA   |
| <b>ACTIVE POWER-DOWN STANDBY CURRENT;</b> One device bank active; Power-down mode; t <sub>CK</sub> = t <sub>CK</sub> (Min); CKE = LOW                                                                                                                                                                                             | I <sub>DD3P</sub>           | 120        | 120        | mA   |
| <b>ACTIVE STANDBY CURRENT;</b> CS# = HIGH; CKE = HIGH;<br>One device bank; Active-Precharge; t <sub>RC</sub> = t <sub>RAS</sub> (Max); t <sub>CK</sub> = t <sub>CK</sub> (Min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle                              | I <sub>DD3N</sub>           | 280        | 280        | mA   |
| <b>OPERATING CURRENT;</b><br>Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; t <sub>CK</sub> = t <sub>CK</sub> (Min);<br>I <sub>OUT</sub> = 0mA                                                                                                                    | I <sub>DD4R</sub>           | 800        | 720        | mA   |
| <b>OPERATING CURRENT;</b> Burst = 2; Writes; Continuous burst;<br>One device bank active; Address and control inputs changing once per clock cycle; t <sub>CK</sub> = t <sub>CK</sub> (Min); DQ, DM, and DQS inputs changing twice per clock cycle                                                                                | I <sub>DD4W</sub>           | 720        | 640        | mA   |
| <b>AUTO REFRESH CURRENT;</b> t <sub>RC</sub> = t <sub>RC</sub> (Min)                                                                                                                                                                                                                                                              | I <sub>DD5</sub>            | 960        | 800        | mA   |
| <b>SELF REFRESH CURRENT;</b> CKE ≤ 0.2V; External clock on;<br>T <sub>ck</sub> =6ns for DDR333, 5ns for DDR400                                                                                                                                                                                                                    | I <sub>DD6(normal)</sub>    | 40         | 40         | mA   |
|                                                                                                                                                                                                                                                                                                                                   | I <sub>DD6(Low power)</sub> | 24         | 24         | mA   |
| <b>OPERATING CURRENT – FOUR BANK OPERATION;</b> Four bank interleaving with BL=4                                                                                                                                                                                                                                                  | I <sub>DD7A</sub>           | 1600       | 1440       | mA   |

\*) Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.

# DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T<sub>A</sub> ≤ +70°C; V<sub>DDQ</sub> = +2.5V ± 0.2V, V<sub>DD</sub> = +2.5V ± 0.2V) see Note 1 on Page 9

| AC CHARACTERISTICS                                        |                    | 3200-3.0-3-3                         |       | 2700-2.5-3-3                         |       | Unit            |
|-----------------------------------------------------------|--------------------|--------------------------------------|-------|--------------------------------------|-------|-----------------|
| PARAMETER                                                 | SYMBOL             | MIN                                  | MAX   | MIN                                  | MAX   |                 |
| Access window of DQ <sub>S</sub> CK/CK#                   | t <sub>AC</sub>    | -0.65                                | +0.65 | -0.65                                | +0.65 | ns              |
| CK high-level width                                       | t <sub>CH</sub>    | 0.45                                 | 0.55  | 0.45                                 | 0.55  | t <sub>CK</sub> |
| CK low-level width                                        | t <sub>CL</sub>    | 0.45                                 | 0.55  | 0.45                                 | 0.55  | t <sub>CK</sub> |
| Clock cycle time                                          | CL=2.0             | t <sub>CK(2.0)</sub>                 | 7.5   | 13.0                                 | 7.5   | ns              |
|                                                           | CL=2.5             | t <sub>CK(2.5)</sub>                 | 6.0   | 13.0                                 | 6.0   |                 |
|                                                           | CL=3.0             | t <sub>CK(3.0)</sub>                 | 5.0   | 13.0                                 |       |                 |
| DQ and DM input hold time relative to DQS                 | t <sub>DH</sub>    | 0.40                                 | -     | 0.45                                 | -     | ns              |
| DQ and DM input setup time relative to DQS                | t <sub>DS</sub>    | 0.40                                 | -     | 0.45                                 | -     | ns              |
| DQ and DM input pulse width ( for each input )            | t <sub>DIPW</sub>  | 1.75                                 | -     | 1.75                                 | -     | ns              |
| Access window of DQS from CK/CK#                          | t <sub>DQSCK</sub> | -0.6                                 | +0.6  | -0.6                                 | +0.6  | ns              |
| DQS input high pulse width                                | t <sub>DQSH</sub>  | 0.35                                 | -     | 0.35                                 | -     | t <sub>CK</sub> |
| DQS input low pulse width                                 | t <sub>DQSL</sub>  | 0.35                                 | -     | 0.35                                 | -     | t <sub>CK</sub> |
| DQS –DQ skew, DQS to last DQ valid, per group, per access | t <sub>DQSQ</sub>  |                                      | 0.40  | -                                    | 0.45  | ns              |
| Write command to first DQS latching transition            | t <sub>DQSS</sub>  | 0.72                                 | 1.28  | 0.75                                 | 1.25  | t <sub>CK</sub> |
| DQS falling edge to CK rising- setup time                 | t <sub>DSS</sub>   | 0.2                                  | -     | 0.2                                  | -     | t <sub>CK</sub> |
| DQS falling edge from CK rising- hold time                | t <sub>DSH</sub>   | 0.2                                  | -     | 0.2                                  | -     | t <sub>CK</sub> |
| Half clock period                                         | t <sub>HP</sub>    | t <sub>ch</sub> ,<br>t <sub>cl</sub> | -     | t <sub>ch</sub> ,<br>t <sub>cl</sub> | -     | ns              |
| Data-out high-impedance window from CK/CK#                | t <sub>HZ</sub>    | -0.7                                 | +0.7  | -0.7                                 | +0.7  | ns              |
| Data-out low-impedance window from CK/CK#                 | t <sub>LZ</sub>    | -0.7                                 | +0.7  | -0.7                                 | +0.7  | ns              |
| Address and control input hold time ( fast slew rate )    | t <sub>IHF</sub>   | 0.6                                  | -     | 0.75                                 | -     | ns              |
| Address and control input setup time ( fast slew rate )   | t <sub>ISF</sub>   | 0.6                                  | -     | 0.75                                 | -     | ns              |
| Address and control input hold time ( slow slew rate )    | t <sub>IHS</sub>   | 0.7                                  | -     | 0.8                                  | -     | ns              |
| Address and control input setup time ( slow slew rate )   | t <sub>ISS</sub>   | 0.6                                  | -     | 0.8                                  | -     | ns              |
| LOAD MODE REGISTER command cycle time                     | t <sub>MRD</sub>   | 10                                   | -     | 12                                   | -     | ns              |
| Adress and control input pulse width (for each input)     | t <sub>IPW</sub>   | 2.2                                  | -     | 2.2                                  | -     | ns              |
| DQ-DQS hold, DQS to first DQ to go non-valid, per access  | t <sub>QH</sub>    | t <sub>HP</sub> - t <sub>QHS</sub>   |       | t <sub>HP</sub> - t <sub>QHS</sub>   |       | ns              |
| Data hold skew factor                                     | t <sub>QHS</sub>   | -                                    | 0.5   | -                                    | 0.6   | ns              |

| AC CHARACTERISTICS                                                               |                | 3200-3.0-3-3        |        | 2700-2.5-3-3        |        |          |
|----------------------------------------------------------------------------------|----------------|---------------------|--------|---------------------|--------|----------|
| PARAMETER                                                                        | SYMBOL         | MIN                 | MAX    | MIN                 | MAX    | Unit     |
| ACTIVE to PRECHARGE command                                                      | $t_{RAS}$      | 40                  | 70.000 | 42                  | 70.000 | ns       |
| ACTIVE to READ with Auto precharge command                                       | $t_{RAP}$      | 15                  | -      | 15                  | -      | ns       |
| ACTIVE to ACTIVE/AUTO REFRESH command period                                     | $t_{RC}$       | 55                  | -      | 60                  | -      | ns       |
| AUTO REFRESH command period                                                      | $t_{RFC}$      | 70                  | -      | 72                  | -      | ns       |
| ACTIVE to READ or WRITE delay                                                    | $t_{RCD}$      | 15                  | -      | 18                  | -      | ns       |
| PRECHARGE command period                                                         | $t_{RP}$       | 15                  | -      | 18                  | -      | ns       |
| DQS read preamble                                                                | $t_{RPRE}$     | 0.9                 | 1.1    | 0.9                 | 1.1    | $t_{CK}$ |
| DQS read postamble                                                               | $t_{RPST}$     | 0.4                 | 0.6    | 0.4                 | 0.6    | $t_{CK}$ |
| ACTIVE bank <i>a</i> to ACTIVE bank <i>b</i> command                             | $t_{RRD}$      | 10                  | -      | 12                  | -      | ns       |
| DQS write preamble                                                               | $t_{WPREH}$    | 0.25                | -      | 0.25                | -      | $t_{CK}$ |
| DQS write preamble setup time                                                    | $t_{WPRES}$    | 0                   | -      | 0                   | -      | ns       |
| DQS write postamble                                                              | $t_{WPST}$     | 0.4                 | 0.6    | 0.4                 | 0.6    | $t_{CK}$ |
| Write recovery time                                                              | $t_{WR}$       | 15                  | -      | 15                  | -      | ns       |
| Internal WRITE to READ command delay                                             | $t_{WTR}$      | 2                   | -      | 1                   | -      | $t_{CK}$ |
| Data valid output window                                                         | N/A            | $t_{QH} - t_{DQSQ}$ |        | $t_{QH} - t_{DQSQ}$ |        | ns       |
| REFRESH to REFRESH command interval                                              | $t_{REFC}$     | -                   | 70.3   | -                   | 70.3   | $\mu s$  |
| Average periodic refresh interval<br>$0^{\circ}C \leq T_{CASE} \leq 85^{\circ}C$ | $t_{REFI}$     | -                   | 7.8    | -                   | 7.8    | $\mu s$  |
| 85 $^{\circ}C < T_{CASE} \leq 95^{\circ}C$                                       | $t_{REFI(IT)}$ | -                   | 3.9    | -                   | 3.9    |          |
| Terminating voltage delay to $V_{DD}$                                            | $t_{VTD}$      | 0                   | -      | 0                   | -      | ns       |
| Exit SELF REFRESH to non-READ command                                            | $t_{XSNR}$     | 70                  | -      | 75                  | -      | ns       |
| Exit SELF REFRESH to READ command                                                | $t_{XSRD}$     | 200                 | -      | 200                 | -      | $t_{CK}$ |

Note 1: Values for AC timing, IDD, and electrical AC and DC characteristics might have been collected within the standard temperature range and at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified and for the corresponding field of operation according to the actual temperature grade of the module (extended E, I or W; refer to the environmental conditions for more details).

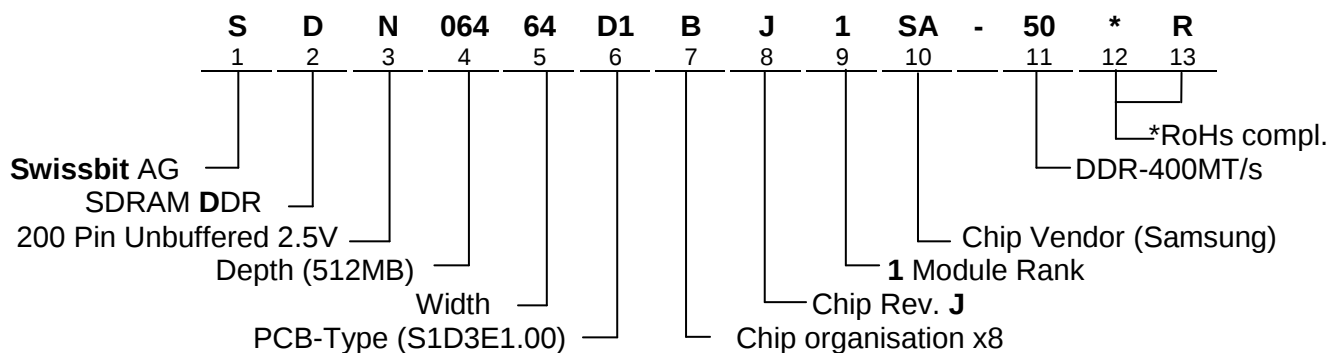
# SERIAL PRESENCE-DETECT MATRIX

| BYTE  | DESCRIPTION                                                                                  | 3200-3.0-3-3 | 2700-2.5-3-3 |
|-------|----------------------------------------------------------------------------------------------|--------------|--------------|
| 0     | NUMBER OF SPD BYTES USED                                                                     | 0x80         |              |
| 1     | TOTAL NUMBER OF BYTES IN SPD DEVICE                                                          | 0x08         |              |
| 2     | FUNDAMENTAL MEMORY TYPE                                                                      | 0x07         |              |
| 3     | NUMBER OF ROW ADDRESSES ON ASSEMBLY                                                          | 0x0D         |              |
| 4     | NUMBER OF COLUMN ADDRESSES ON ASSEMBLY                                                       | 0x0B         |              |
| 5     | NUMBER OF PHYSICAL BANKS ON DIMM                                                             | 0x01         |              |
| 6     | MODULE DATA WIDTH                                                                            | 0x40         |              |
| 7     | MODULE DATA WIDTH (continued)                                                                | 0x00         |              |
| 8     | MODULE VOLTAGE INTERFACE LEVELS (V <sub>DDQ</sub> )                                          | 0x04         |              |
| 9     | SDRAM CYCLE TIME, (t <sub>CK</sub> )<br>(CAS LATENCY =2.5 (2700, 2100) ; CL=3* (3200))       | 0x50         | 0x60         |
| 10    | SDRAM ACCESS FROM CLOCK, (t <sub>AC</sub> )<br>(CAS LATENCY =2.5 (2700, 2100); CL=3* (3200)) | 0x65         |              |
| 11    | MODULE CONFIGURATION TYPE                                                                    | 0x00         |              |
| 12    | REFRESH RATE/ TYPE                                                                           | 0x82         |              |
| 13    | SDRAM DEVICE WIDTH (PRIMARY SDRAM)                                                           | 0x08         |              |
| 14    | ERROR- CHECKING SDRAM DATA WIDTH                                                             | 0x00         |              |
| 15    | MINIMUM CLOCK DELAY, BACK- TO- BACK<br>RANDOM COLUMN ACCESS                                  | 0x01         |              |
| 16    | BURST LENGTHS SUPPORTED                                                                      | 0x0E         |              |
| 17    | NUMBER OF BANKS ON SDRAM DEVICE                                                              | 0x04         |              |
| 18    | CAS LATENCIES SUPPORTED                                                                      | 0x1C         | 0x0C         |
| 19    | CS LATENCY                                                                                   | 0x01         |              |
| 20    | WE LATENCY                                                                                   | 0x02         |              |
| 21    | SDRAM MODULE ATTRIBUTES                                                                      | 0x20         |              |
| 22    | SDRAM DEVICE ATTRIBUTES: GENERAL                                                             | 0xC1         |              |
| 23    | SDRAM CYCLE TIME, (t <sub>CK</sub> )<br>(CAS LATENCY=2(2700, 2100) CL=2.5*(3200))            | 0x60         | 0x75         |
| 24    | SDRAM ACCESS FROM CK, (t <sub>AC</sub> )<br>(CAS LATENCY=2(2700, 2100) CL=2.5*(3200))        | 0x70         |              |
| 25    | SDRAM CYCLE TIME, (t <sub>CK</sub> )<br>(CAS LATENCY=1.5(2700, 2100) CL=2*(3200))            | 0x75         | 0x00         |
| 26    | SDRAM ACCESS FROM CK, (t <sub>AC</sub> )<br>(CAS LATENCY=1.5(2700, 2100) CL=2*(3200))        | 0x75         | 0x00         |
| 27    | MINIMUM ROW PRECHARGE TIME, (t <sub>RP</sub> )                                               | 0x3C         | 0x48         |
| 28    | MINIMUM ROW ACTIVE TO ROW ACTIVE, (t <sub>RRD</sub> )                                        | 0x28         | 0x30         |
| 29    | MINIMUM RAS# TO CAS# DELAY, (t <sub>RCD</sub> )                                              | 0x3C         | 0x48         |
| 30    | MINIMUM RAS# PULSE WIDTH, (t <sub>RAS</sub> )                                                | 0x28         | 0x2A         |
| 31    | MODULE BANK DENSITY                                                                          | 0x80         |              |
| 32    | ADDRESS AND COMMAND SETUP TIME, (t <sub>IS</sub> )                                           | 0x60         | 0x75         |
| 33    | ADDRESS AND COMMAND HOLD TIME, (t <sub>IH</sub> )                                            | 0x60         | 0x75         |
| 34    | DATA/DATA MASK INPUT SETUP TIME, (t <sub>DS</sub> )                                          | 0x40         | 0x45         |
| 35    | DATA/DATA MASK INPUT HOLD TIME, (t <sub>DH</sub> )                                           | 0x40         | 0x45         |
| 36-40 | RESERVED                                                                                     | 0x00         |              |
| 41    | MIN ACTIVE AUTO REFRESH TIME (t <sub>RC</sub> )                                              | 0x37         | 0x3C         |
| 42    | MINIMUM AUTO REFRESH TO ACTIVE/<br>AUTO REFRESH COMMAND PERIOD, (t <sub>RFC</sub> )          | 0x46         | 0x48         |
| 43    | SDRAM DEVICE MAX CYCLE TIME (t <sub>CKMAX</sub> )                                            | 0x28         | 0x30         |
| 44    | SDRAM DEVICE MAX DQS-DQ SKEW TIME<br>(t <sub>DQSQ</sub> )                                    | 0x28         | 0x2D         |
| 45    | SDRAM DEVICE MAX READ DATA HOLD SKEW FACTOR<br>(t <sub>QHS</sub> )                           | 0x50         | 0x55         |

## SERIAL PRESENCE-DETECT MATRIX (continued)

| BYTE   | DESCRIPTION                             | 3200-3.0-3-3         | 2700-2.5-3-3         |
|--------|-----------------------------------------|----------------------|----------------------|
| 46-61  | RESERVED                                | 0x00                 |                      |
| 62     | SPD REVISION                            | 0x11                 |                      |
| 63     | CHECKSUM FOR BYTES 0-62                 | 0xAE                 | 0x48                 |
| 64     | MANUFACTURER'S JEDEC ID CODE            | 7F                   |                      |
| 65     | MANUFACTURER'S JEDEC ID CODE(continued) | 7F                   |                      |
| 66     | MANUFACTURER'S JEDEC ID CODE(continued) | 7F                   |                      |
| 67     | MANUFACTURER'S JEDEC ID CODE(continued) | DA                   |                      |
| 72     | MANUFACTURING LOCATION                  | 0x01 = CH            | 0x02 = GE 0x03 = USA |
| 73-90  | MODULE PART NUMBER (ASCII)              | "SDN06464D1BJ1SA-xx" |                      |
| 91     | PCB IDENTIFICATION CODE                 | X                    |                      |
| 92     | PCB IDENTIFICATION CODE (continued)     | X                    |                      |
| 93     | YEAR OF MANUFACTURE IN BCD              | X                    |                      |
| 94     | WEEK OF MANUFACTURE IN BCD              | X                    |                      |
| 95-98  | MODULE SERIAL NUMBER                    | X                    |                      |
| 99-127 | MANUFACTURER-SPECIFIC DATA (RSVD)       | X                    |                      |

## Part Number Code



\* optional / additional information

| Revision History |                                                                               |            |
|------------------|-------------------------------------------------------------------------------|------------|
| Revision         | Changes                                                                       | Date       |
| 1.0              | Initial Revision                                                              | 31.10.2012 |
| 1.1              | New I <sub>DD</sub> -Values added, Extended Temperature-Grade (W-Grade) added | 20.11.2012 |

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# CE Declaration of Conformity

We

**Manufacturer:** Swissbit AG  
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CH-9552 Bronschhofen  
Switzerland

declare under our sole responsibility that the product

**Product Type:** 512MB DDR1 SODIMM  
**Brand Name:** SWISSMEMORY™  
**Product Series:** DDR1 SODIMM  
**Part Number:** SDN06464D1BJ1SA-xxxR

to which this declaration relates is in conformity with the following directives:

**2002/96/EC Category 3 (WEEE)**

following the provisions of Directive

**Restriction of the use of certain hazardous substances**

**2011/65/EU**

Swissbit AG, November 2012



Manuela Kögel  
Head of Quality Management