DS8922/DS8922A/DS8923A TRI-STATE RS-422 Dual Differential Line Driver and Receiver Pairs

Check for Samples: DS8922, DS8922A, DS8923A

FEATURES

- **12 ns Typical Propagation Delay**
- **Output Skew—±0.5 ns Typical**
- **Meets the Requirements of EIA Standard RS-422**
- **Complementary Driver Outputs**
- **High Differential or Common-Mode Input Voltage Ranges of ±7V**
- **±0.2V Receiver Sensitivity over the Input Voltage Range**
- **Receiver Input Fail-Safe Circuitry**
- **Receiver Input Hysteresis—70 mV typical**
- **Glitch Free Power Up/Down**
- **TRI-STATE Outputs**

DESCRIPTION

The DS8922/22A and DS8923A are Dual Differential Line Driver and Receiver pairs. These devices are designed specifically for applications meeting the ST506, ST412 and ESDI Disk Drive Standards. In addition, the devices meet the requirements of the EIA Standard RS-422.

These devices offer an input sensitivity of 200 mV over a ±7V common mode operating range. Hysteresis is incorporated (typically 70 mV) to improve noise margin for slowly changing input waveforms. An input fail-safe circuit is provided such that if the receiver inputs are open the output assumes the logical one state.

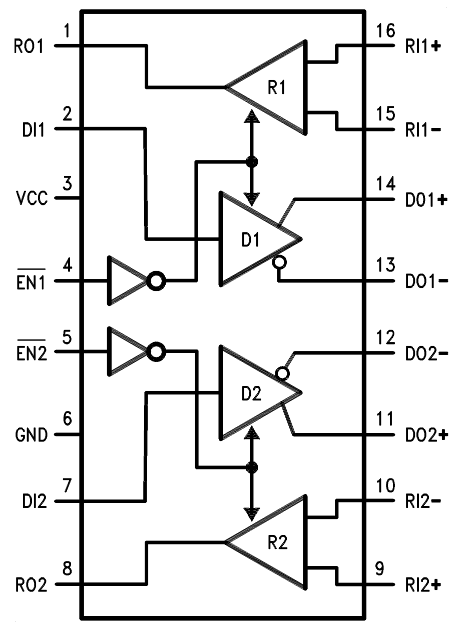
The DS8922A and DS8923A drivers are designed to provide unipolar differential drive to twisted pair or parallel wire transmission lines. Complementary outputs are logically ANDed and provide an output skew of 0.5 ns (typ.) with propagation delays of 12 ns.

Both devices feature TRI-STATE outputs. The DS8922/22A have independent control functions common to a driver and receiver pair. The DS8923A has separate driver and receiver control functions.

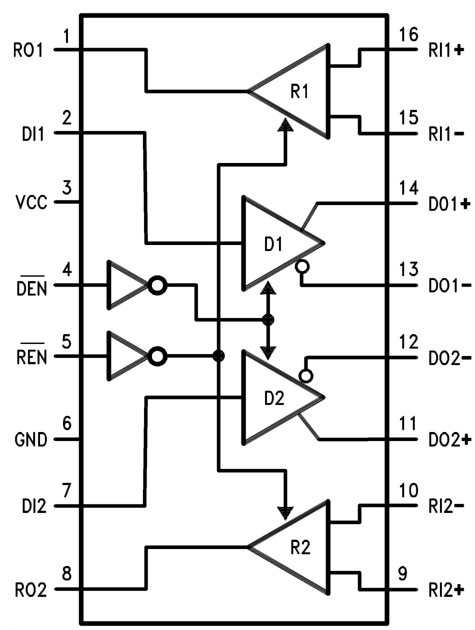
Power up/down circuitry is featured which will TRI-STATE the outputs and prevent erroneous glitches on the transmission lines during system power up or power down operation.

The DS8922/22A and DS8923A are designed to be compatible with TTL and CMOS.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



DS8922A Dual-In-Line
Top View
See Package Number D (R-PDSO-G16) or NFG0016E



DS8923A Dual-In-Line
Top View
See Package Number D (R-PDSO-G16) or NFG0016E

DS8922/22A

$\overline{EN1}$	$\overline{EN2}$	RO1	RO2	DO1	DO2
0	0	ACTIVE	ACTIVE	ACTIVE	ACTIVE
1	0	HI-Z	ACTIVE	HI-Z	ACTIVE
0	1	ACTIVE	HI-Z	ACTIVE	HI-Z
1	1	HI-Z	HI-Z	HI-Z	HI-Z

DS8923A

$\overline{DEN}$	$\overline{REN}$	RO1	RO2	DO1	DO2
0	0	ACTIVE	ACTIVE	ACTIVE	ACTIVE
1	0	ACTIVE	ACTIVE	HI-Z	HI-Z
0	1	HI-Z	HI-Z	ACTIVE	ACTIVE
1	1	HI-Z	HI-Z	HI-Z	HI-Z

Absolute Maximum Ratings (1)(2)

Supply Voltage	7V
Drive Input Voltage	−0.5V to +7V
Output Voltage	5.5V
Receiver Output Sink Current	50 mA
Receiver Input Voltage	±10V
Differential Input Voltage	±12V
Maximum Package Power Dissipation @ +25°C	
D Package	1300 mW
NFG Package	1450 mW
Derate D Package 10.4 mW/°C above +25°C	
Derate NFG Package 11.6 mW/°C above +25°C	
Storage Temperature Range	−65°C to +165°C
Lead Temp. (Soldering, 4 seconds)	260°C
ESD Rating (HBM)	2000V+

(1) “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits. The Table of Electrical Characteristics provides conditions for actual device operation.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage	4.5	5.5	V
Temperature (T_A)	0	70	°C

DS8922/22A and DS8923A Electrical Characteristics[(1)(2)(3)]

Symbol	Conditions		Min	Typ	Max	Units
RECEIVER						
V_{TH}	$-7V \le V_{CM} \le +7V$		−200	±35	+200	mV
V_{HYST}	$-7V \le V_{CM} \le +7V$		15	70		mV
R_{IN}	V_{IN} = −7V, +7V (Other Input = GND)		4.0	6.0		kΩ
I_{IN}	V_{IN} = 10V				3.25	mA
	V_{IN} = −10V				−3.25	mA
V_{OH}	V_{CC} = MIN, I_{OH} = − 400 µA		2.5			V
V_{OL}	V_{CC} = MAX, I_{OL} = 8 mA				0.5	V
I_{SC}	V_{CC} = MAX, V_{OUT} = 0V		−15		−100	mA
DRIVER						
V_{OH}	V_{CC} = MIN, I_{OH} = −20 mA		2.5			V
V_{OL}	V_{CC} = MIN, I_{OL} = +20 mA				0.5	V
I_{OFF}	V_{CC} = 0V, V_{OUT} = 5.5V				100	µA
$\lvert VT \rvert - \lvert \overline{VT} \rvert$					0.4	V
VT			2.0			V
$\lvert V_{OS} - \overline{V_{OS}} \rvert$					0.4	V
I_{SC}	V_{CC} = MAX, V_{OUT} = 0V		−30		−150	mA
DRIVER and RECEIVER						
I_{OZ}		V_{OUT} = 2.5V			50	µA
TRI-STATE	V_{CC} = MAX	V_{OUT} = 0.4V			−50	µA
Leakage						
I_{CC}	V_{CC} = MAX	ACTIVE			76	mA
		TRI-STATE			78	mA
DRIVER and ENABLE INPUTS						
V_{IH}			2.0			V
V_{IL}					0.8	V
I_{IL}	V_{CC} = MAX, V_{IN} = 0.4V			−40	−200	µA
I_{IH}	V_{CC} = MAX, V_{IN} = 2.7V				20	µA
I_I	V_{CC} = MAX, V_{IN} = 7.0V				100	µA
V_{CL}	V_{CC} = MIN, I_{IN} = −18 mA				−1.5	V

(1) All currents into device pins are shown as positive values; all currents out of the device are shown as negative; all voltages are referenced to ground unless otherwise specified. All values shown as max or min are classified on absolute value basis.
(2) All typical values are V_{CC} = 5V, T_A = 25°C.
(3) Only one output at a time should be shorted.

Receiver Switching Characteristics (Figure 1) (Figure 2) (Figure 2)

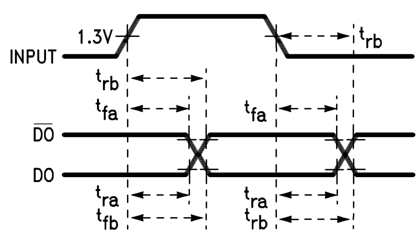
Parameter	Conditions	Min	Typ	Max		Units
				8922	**8922A/23A**	
T_{pLH}	CL = 30 pF		12	22.5	20	ns
T_{pHL}	CL = 30 pF		12	22.5	20	ns
$\lvert T_{pLH} - T_{pHL} \rvert$	CL = 30 pF		0.5	5	3.5	ns
Skew (Channel to Channel)	CL = 30 pF		0.5	3.0	2.0	ns
T_{pLZ}	CL = 15 pF S2 Open		15			ns
T_{pHZ}	CL = 15 pF S1 Open		15			ns
T_{pZL}	CL = 30 pF S2 Open		20			ns
T_{pZH}	CL = 30 pF S1 Open		20			ns

Driver Switching Characteristics

Parameter	Conditions	Min	Typ	Max		Units
				8922	8922A/23A	
SINGLE ENDED CHARACTERISTICS (Figure 4, Figure 5, Figure 6, and Figure 8)						
T_{pLH}	CL = 30 pF		12	15	15	ns
T_{pHL}	CL = 30 pF		12	15	15	ns
T_{TLH}	CL = 30 pF		5	10	10	ns
T_{THL}	CL = 30 pF		5	10	10	ns
$\|T_{pLH}–T_{pHL}\|$	CL = 30 pF		0.5			ns
Skew	CL = 30 pF [(1)]		0.5	5	3.5	ns
Skew (Channel to Channel)			0.5	3.0	2.0	ns
T_{pLZ}	CL = 30 pF		15			ns
T_{pHZ}	CL = 30 pF		15			ns
T_{pZL}	CL = 30 pF		20			ns
T_{pZH}	CL = 30 pF		20			ns
DIFFERENTIAL SWITCHING CHARACTERISTICS [(2)], (Figure 4)						
T_{pLH}	CL = 30 pF		12	15	15	ns
T_{pHL}	CL = 30 pF		12	15	15	ns
$\|T_{pLH}–T_{pHL}\|$	CL = 30 pF		0.5	6.0	2.75	ns

(1) Difference between complementary outputs at the 50% point.
(2) Differential Delays are defined as calculated results from single ended rise and fall time measurements. This approach in establishing AC performance specifications has been taken due to limitations of available Automatic Test Equipment (ATE). The calculated ATE results assume a linear transition between measurement points and are a result of the following equations: $Tcp = \frac{(Tfb \times Trb) - (Tra \times Tfa)}{Trb - Tra - Tfa + Tfb}$ Where: Tcp = Crossing Point Tra, Trb, Tfa and Tfb are time measurements with respect to the input.

Switching Time Waveforms



AC Test Circuits and Switching Waveforms

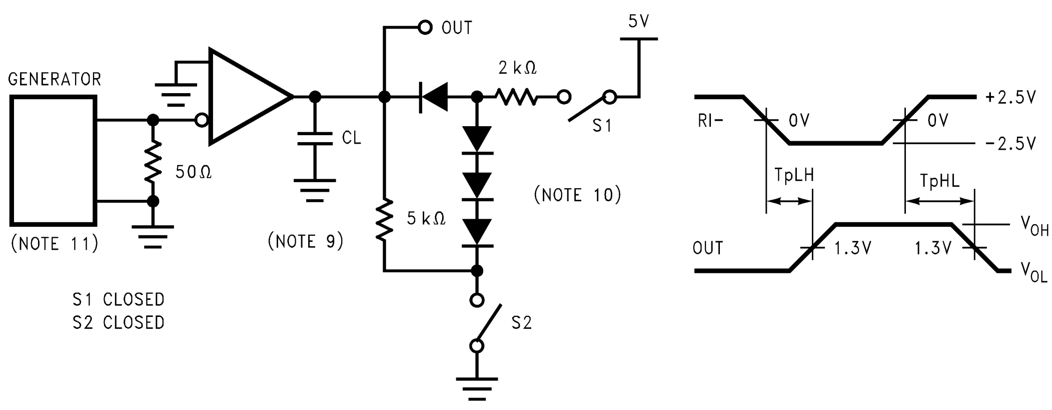


Figure 1.

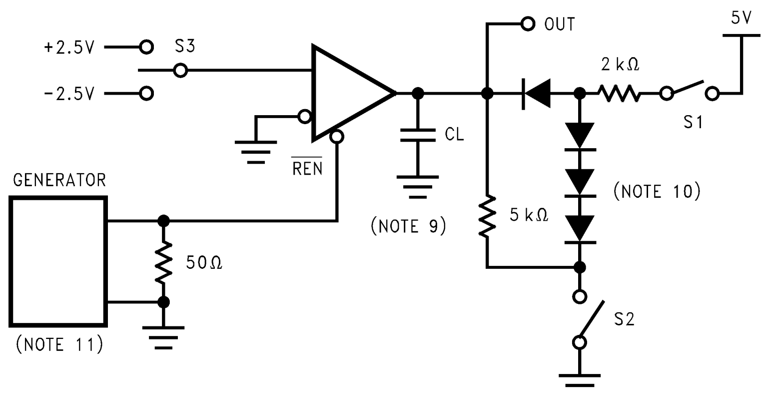


Figure 2.

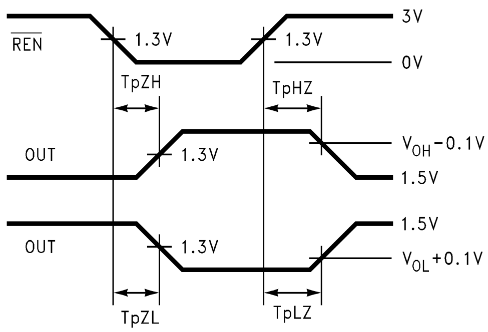
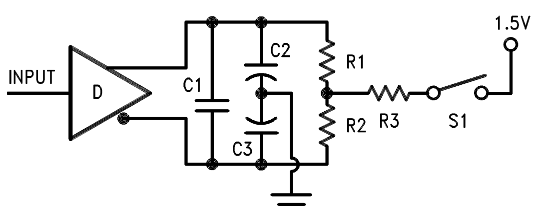


Figure 3.

	S1	S2	S3
T_{PLZ}	Closed	Open	+2.5V
T_{PHZ}	Open	Closed	−2.5V
T_{PZL}	Closed	Open	+2.5V
T_{PZH}	Open	Closed	−2.5V



NOTE: C1=C2=C3=30 pF, R1=R2=50 Ω, R3=500 Ω

Figure 4.

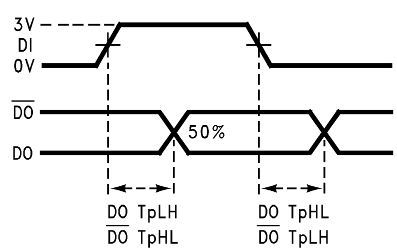


Figure 5.

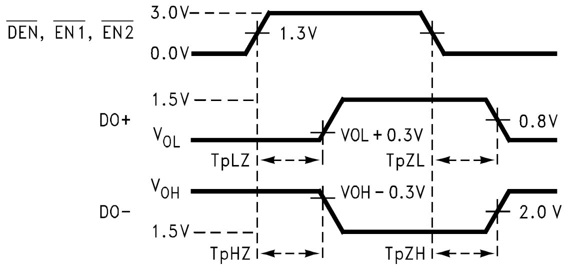


Figure 6.

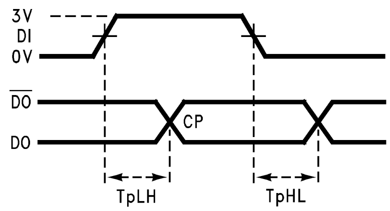


Figure 7.

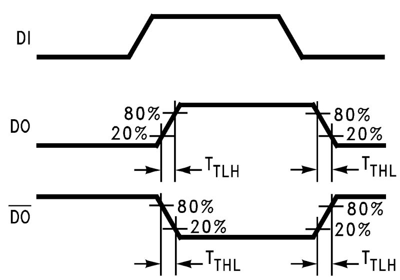


Figure 8.

Typical Performance Characteristics

(DS8923A)

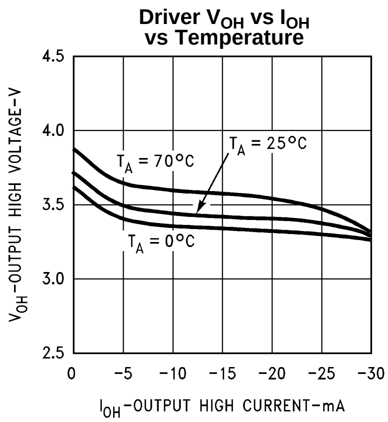


Figure 9.

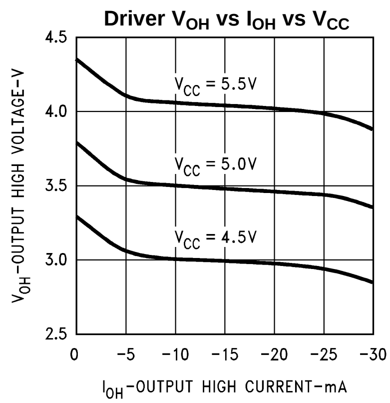


Figure 10.

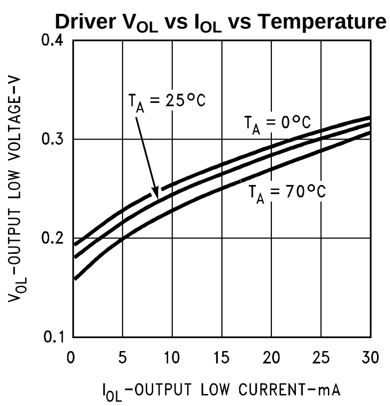


Figure 11.

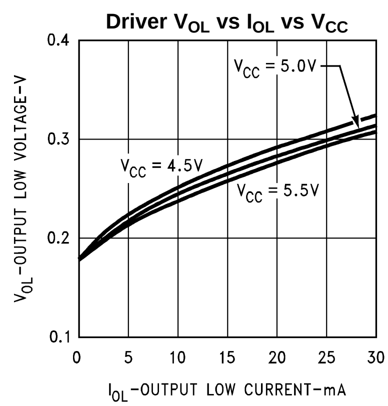


Figure 12.

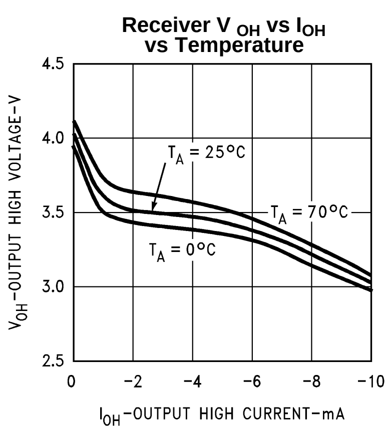


Figure 13.

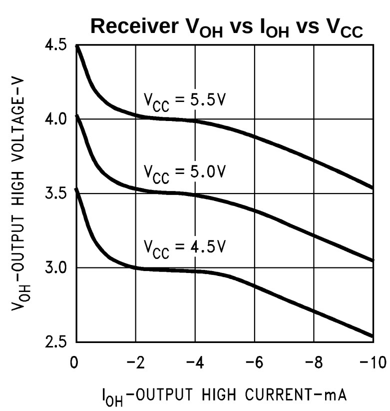


Figure 14.

Typical Performance Characteristics (continued)

(DS8923A)

Receiver V_{OL} vs I_{OL} vs Temperature

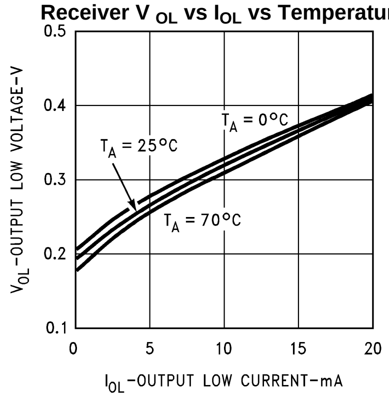


Figure 15.

Receiver V_{OL} vs I_{OL} vs V_{CC}

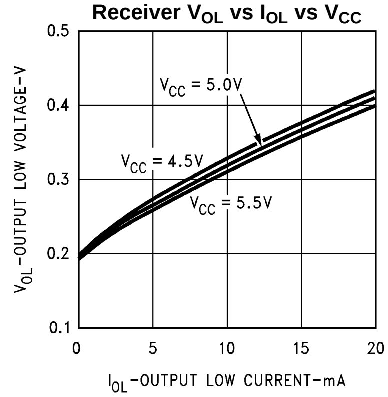


Figure 16.

Driver Differential Propagation Delay vs Temperature

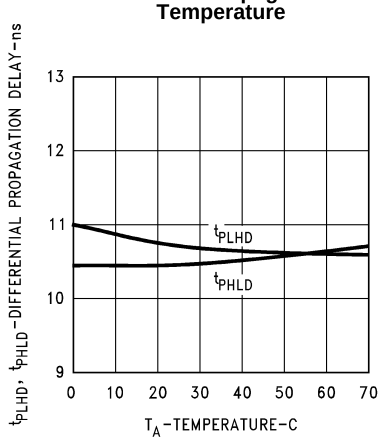


Figure 17.

Driver Differential Propagation Delay vs V_{CC}

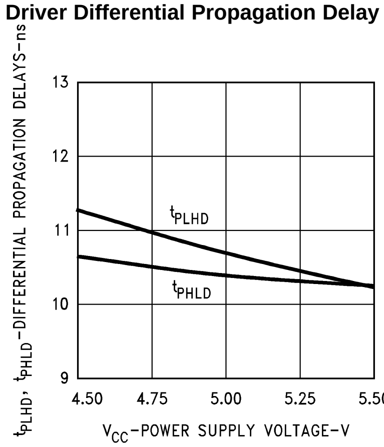


Figure 18.

Receiver Propagation Delay vs Temperature

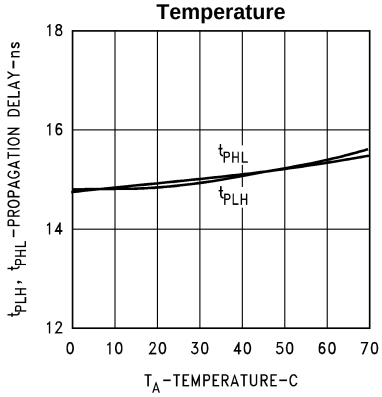


Figure 19.

Receiver Propagation Delay vs V_{CC}

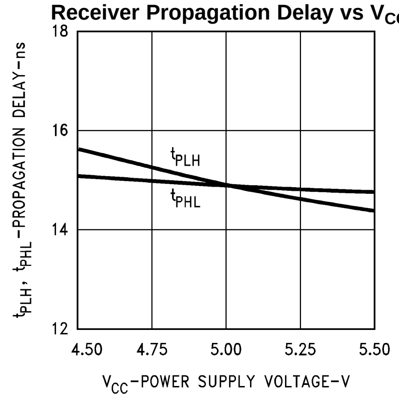


Figure 20.

Typical Performance Characteristics (continued)

(DS8923A)

Driver V_{OD} vs Temperature

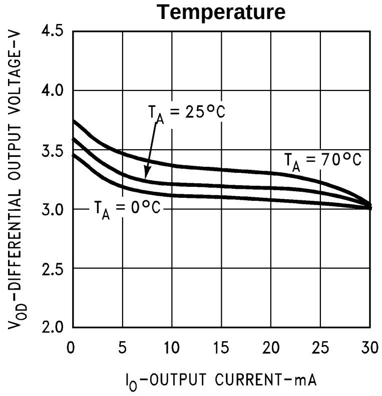


Figure 21.

Driver V_{OD} vs V_{CC}

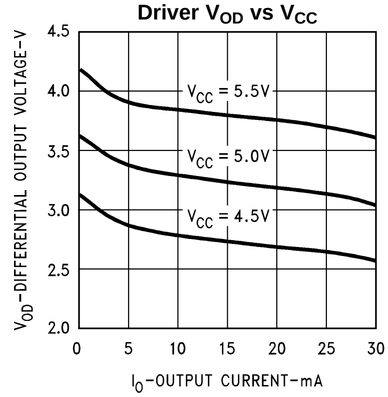


Figure 22.

Driver V_{OD} vs R_L

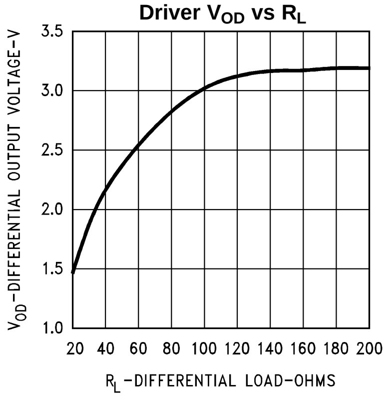


Figure 23.

Driver Differential Transition Time vs Temperature

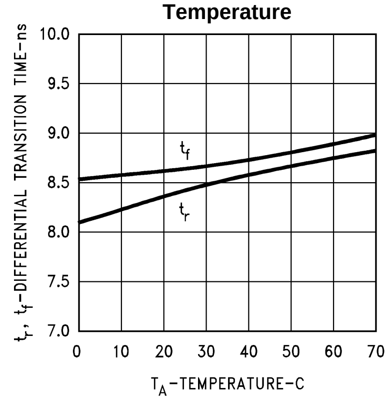


Figure 24.

Driver Differential Transition Time vs V_{CC}

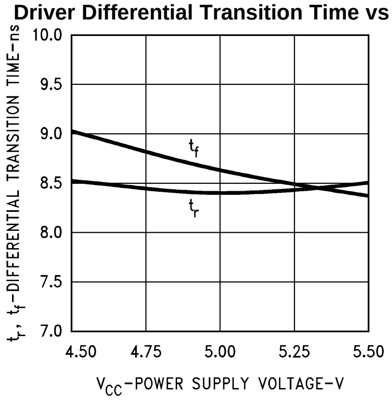


Figure 25.

Supply Current vs Temperature

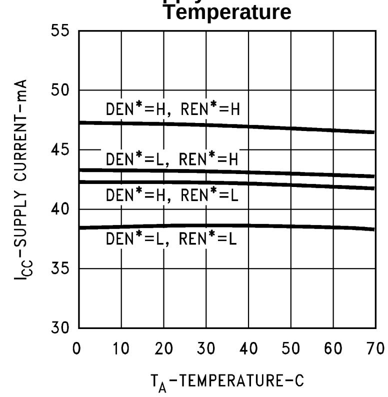


Figure 26.

Typical Performance Characteristics (continued)

(DS8923A)

Supply Current vs V_{CC}

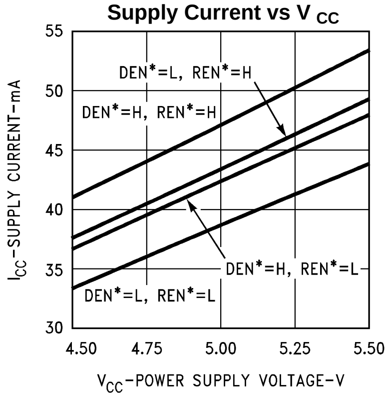


Figure 27.

I_{CC} vs Driver Switching Frequency

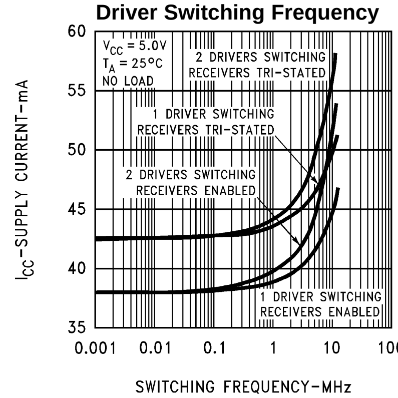


Figure 28.

Driver Short Circuit Current vs Temperature

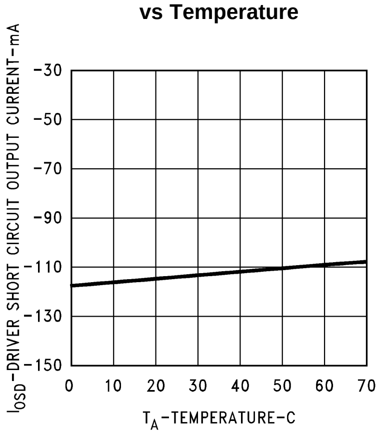


Figure 29.

Driver Short Circuit Current vs V_{CC}

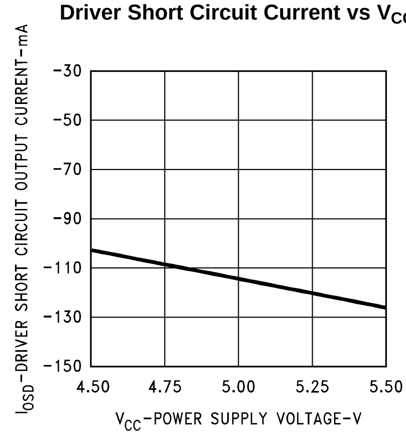


Figure 30.

Receiver Short Circuit Current vs Temperature

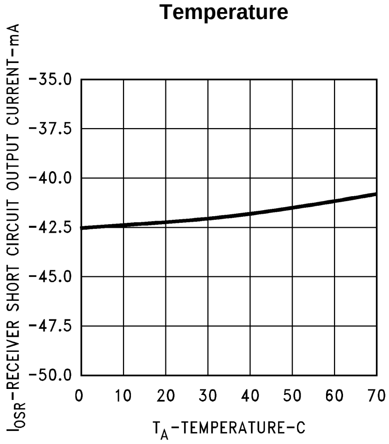


Figure 31.

Receiver Short Circuit Current vs V_{CC}

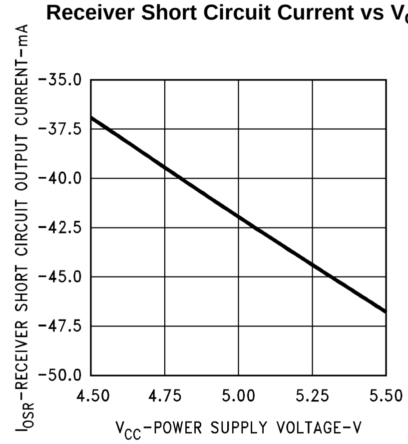


Figure 32.

TYPICAL APPLICATIONS

Figure 33. ESDI Application

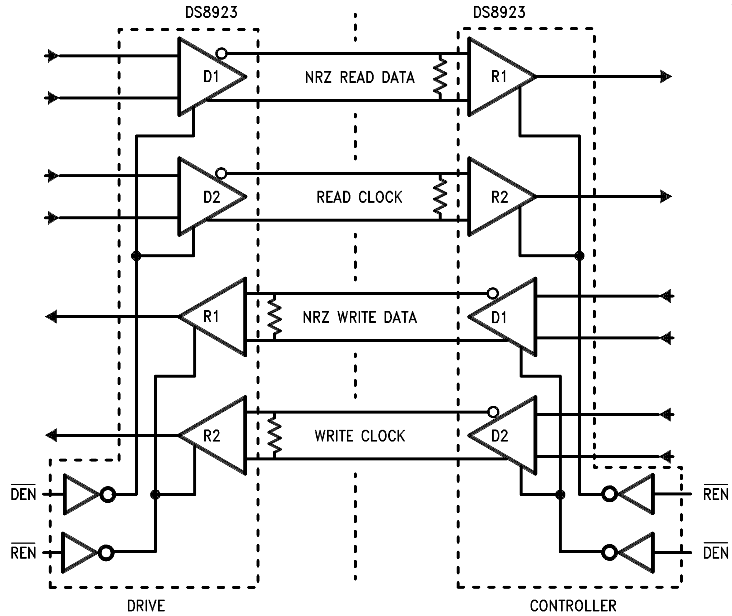


Figure 34.

Figure 35. ST504 and ST412 Applications

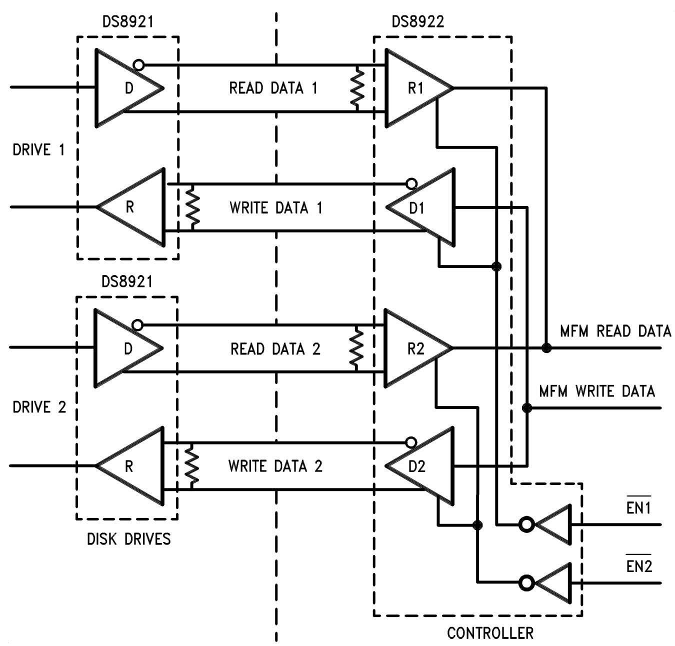


Figure 36.

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DS8922AM	ACTIVE	SOIC	D	16	48	TBD	Call TI	Call TI	0 to 70	DS8922AM	Samples
DS8922AM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	DS8922AM	Samples
DS8922AMX	ACTIVE	SOIC	D	16	2500	TBD	Call TI	Call TI	0 to 70	DS8922AM	Samples
DS8922AMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	DS8922AM	Samples
DS8923AM	ACTIVE	SOIC	D	16	48	TBD	Call TI	Call TI	0 to 70	DS8923AM	Samples
DS8923AM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	DS8923AM	Samples
DS8923AN	ACTIVE	PDIP	NFG	16	25	TBD	Call TI	Call TI	0 to 70	DS8923AN	Samples
DS8923AN/NOPB	ACTIVE	PDIP	NFG	16	25	Pb-Free (RoHS)	SN	Level-1-NA-UNLIM	0 to 70	DS8923AN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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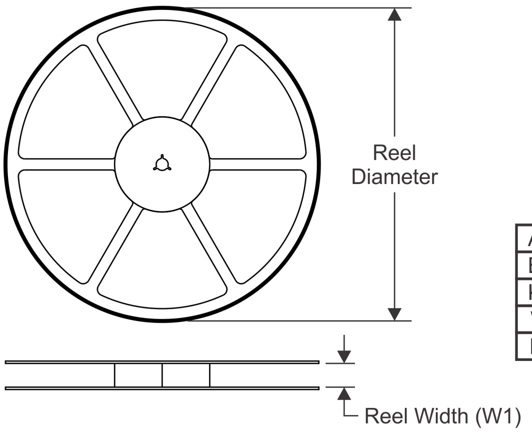
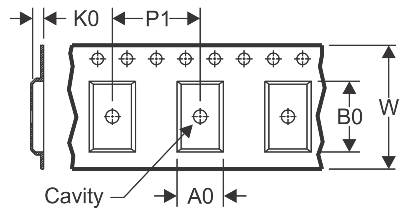
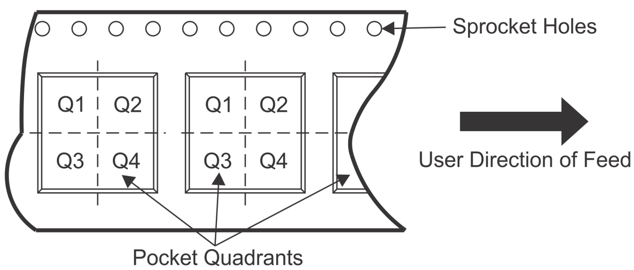
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

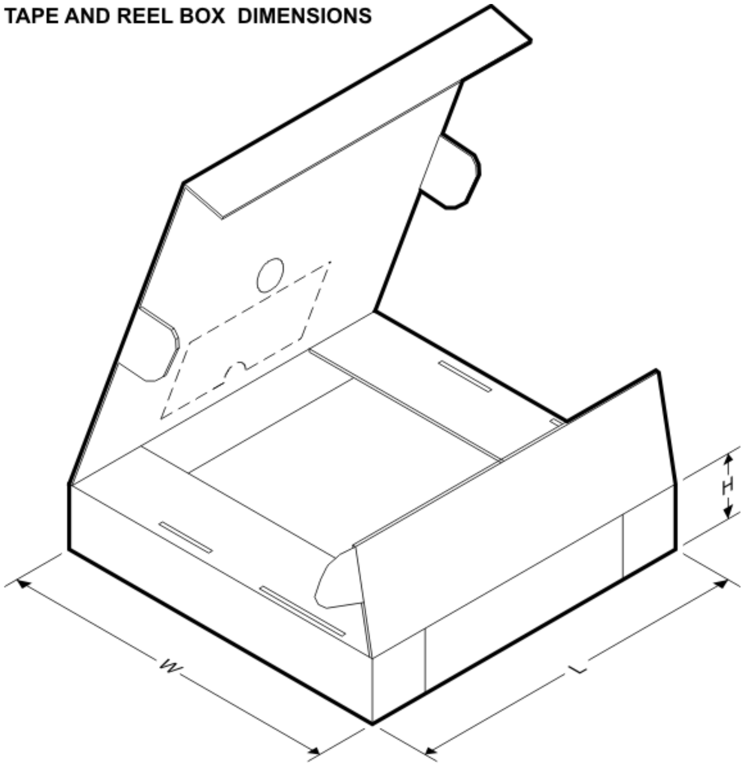
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS8922AMX	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
DS8922AMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

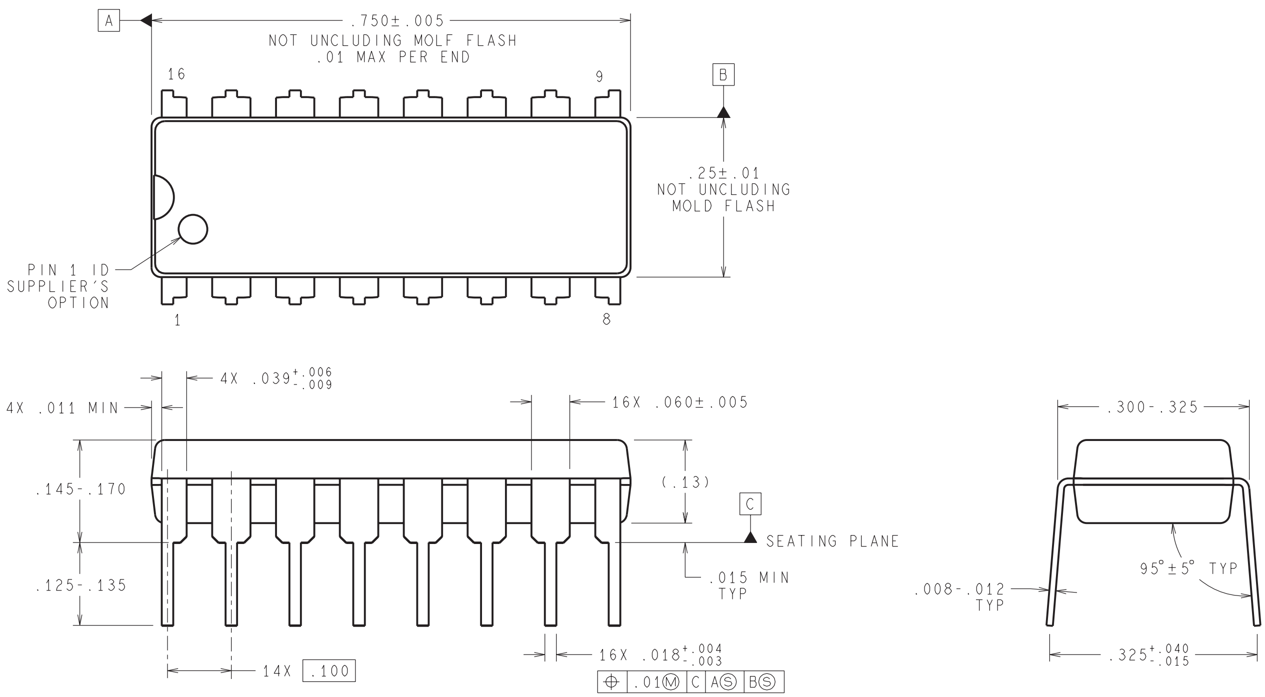
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS8922AMX	SOIC	D	16	2500	367.0	367.0	35.0
DS8922AMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

NFG0016E

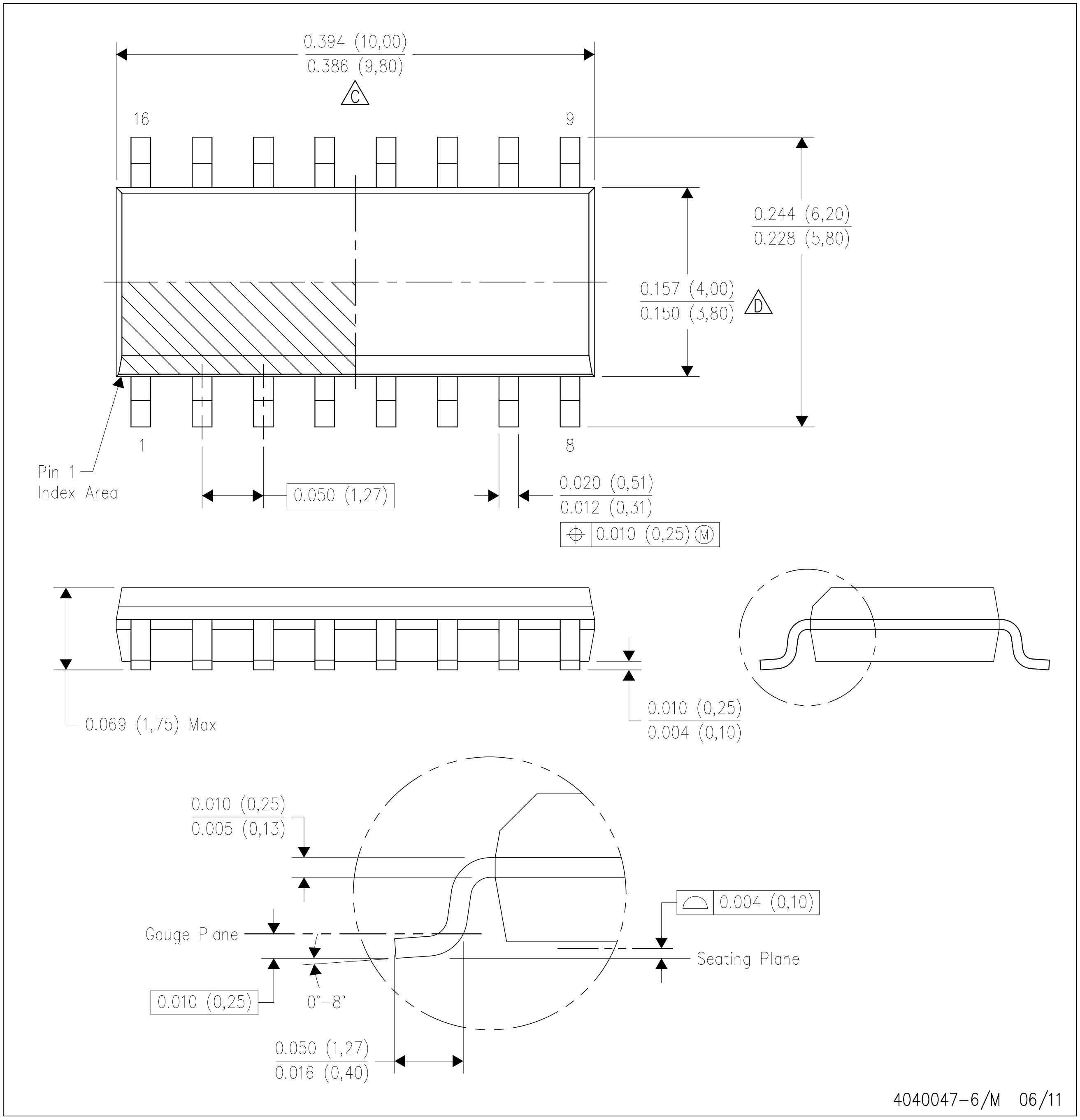


DIMENSIONS ARE IN INCHES

DIMENSIONS IN ( ) FOR REFERENCE ONLY

N16E (Rev G)

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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