Low-Voltage, Low R_{ON}, Dual DPDT Analog Switch

DESCRIPTION

The DG2017 is a dual DPDT (double-pole/double-throw), optimized for high performance analog switching, and specifically designed to benefit portable audio applications.

One pair of double-throw switches is sub 1 Ω for low impedance speaker performance while the second pair of double-throw switches is suitable for microphone applications.

With the DPDT configuration, the DG2017 provides the flexibility for stereo-single-end or differential BTL output structures with a fully integrated differential microphone switching solution.

The DG2017 is an integrated monolithic device in a QFN-16 (4 mm x 4 mm) package that provides a space saving solution over the use of multiple single SPDT devices as well as providing the advantage of on-resistance flatness and matching that single SPDT devices cannot offer.

The DG2017 provides low charge injection (2 pC), fast switching time (t_{ON} and t_{OFF} less than 100 ns), excellent Off-Isolation and Crosstalk (- 70 dB at 100 kHz). During operation, continuous current through any or all switches is rated at ± 200 mA, ideal for portable audio applications.

Built on Vishay Siliconix's low voltage CMOS process, the DG2017 contains an epitaxial layer that prevents latchup. Break-before-make is guaranteed. When on, each switch conducts equally well in both directions, and block up to the power supply level when off.

FEATURES

- Low voltage operation (2 V to 5.5 V)
- Low on-resistance at 2.7 V - R_{ON}:
  SW_1, SW_2 - 3.2 Ω
  SW_3, SW_4 - 0.64 Ω
- Fast switching: t_{ON} = 46 ns
  t_{OFF} = 21 ns
- QFN-16 (4 mm x 4 mm) package
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS COMPLIANT
HALOGEN FREE

BENEFITS

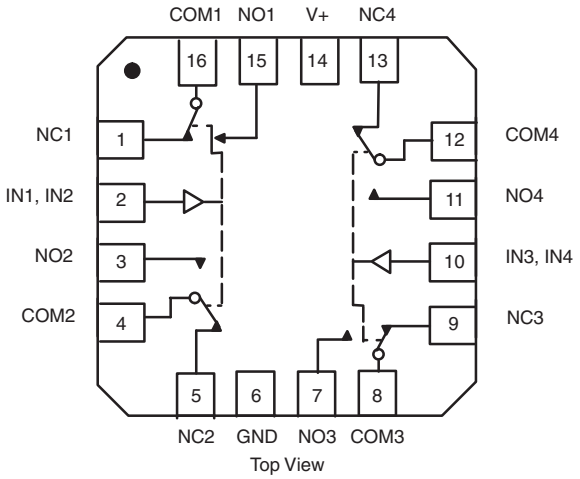
- Space saving solution
- Low power consumption
- Guaranteed low voltage operation
- Low voltage logic compatible

APPLICATIONS

- Cellular Phones
- Integrated Speaker Switching
- Audio and Video Signal Routing
- PCMCIA Cards
- Battery Operated Systems

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

QFN-16 (4 x 4)



Top View

TRUTH TABLE		
Logic	**NC1, 2, 3 and 4**	**NO1, 2, 3 and 4**
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION		
Temp Range	**Package**	**Part Number**
- 40 °C to 85 °C	16-pin QFN (4 x 4 mm) (Variation 1)	DG2017DN-T1-E4

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)			
Parameter		**Limit**	**Unit**
Reference V+ to GND		- 0.3 to + 6	V
IN, COM, NC, NO[a]		- 0.3 to (V+ + 0.3)	
Current (Any terminal except NO, NC or COM)		30	mA
Continuous Current (NO, NC, or COM)		± 200	
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 300	
Storage Temperature (D Suffix)		- 65 to 150	°C
Package Solder Reflow Conditions[d]	16-pin QFN (4 mm x 4 mm)	240	
Power Dissipation (Packages)[b]	QFN-16 (4 mm x 4 mm)	1880	mW

Notes:
a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 23.5 mW/°C above 70 °C.
d. Manual soldering with iron is not recommended for leadless components. The QFN is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

SPECIFICATIONS (V+ = 3 V)							
Parameter	**Symbol**	**Test Conditions Otherwise Unless Specified** V+ = 3 V, ± 10 %, V_{IN} = 0.4 V or 1.6 V[e]	**Temp.[a]**	**Limits - 40 °C to 85 °C Min.[b]**	**Typ.[c]**	**Max.[b]**	**Unit**
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC} V_{COM}		Full	0		V+	V
DC Characteristics							
On-Resistance	R_{ON} (SW_1, SW_2)	V+ = 2.7 V, V_{COM} = 0.2 V/1.5 V, I_{NO}, I_{NC} = 10 mA	Room Full		3.2	3.7 4.3	Ω
	R_{ON} (SW_3, SW_4)	V+ = 2.7 V, V_{COM} = 0.2 V/1.5 V, I_{NO}, I_{NC} = 100 mA	Room Full		0.67	1.1 1.2	
R_{ON} Flatness[d]	R_{ON} (SW_1, SW_2)	V+ = 2.7 V, V_{COM} = 0.2 V/1.5 V, I_{NO}, I_{NC} = 10 mA	Room Full		1.4	2	
	R_{ON} (SW_3, SW_4)	V+ = 2.7 V, V_{COM} = 0.2 V/1.5 V, I_{NO}, I_{NC} = 100 mA	Room Full		0.12	0.3	
R_{ON} Match[d]	ΔR_{ON} (SW_1, SW_2)	V+ = 2.7 V, V_{COM} = 0.2 V/1.5 V, I_{NO}, I_{NC} = 10 mA	Room Full			0.3	
	ΔR_{ON} (SW_3, SW_4)	V+ = 2.7 V, V_{COM} = 0.2 V/1.5 V, I_{NO}, I_{NC} = 100 mA	Room Full			0.3	
Switch Off Leakage Current	$I_{NO(off)}$ $I_{NC(off)}$	V+ = 3.3 V V_{NO}, V_{NC} = 0.3 V/3 V, V_{COM} = 0.3 V/3 V	Room Full	- 0.5 5		0.5 5	nA
	$I_{COM(off)}$		Room Full	- 0.5 5		0.5 5	
Channel-On Leakage Current	$I_{COM(on)}$	V+ = 3.3 V, V_{NO} = V_{NC}, V_{COM} = 0.3 V/3 V	Room Full	- 0.5 5		0.5 5	
Digital Control							
Input High Voltage	V_{INH}		Full	1.6			V
Input Low Voltage	V_{INL}		Full			0.4	
Input Capacitance	C_{in}		Full		6		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 V or V+	Full	- 1		1	µA

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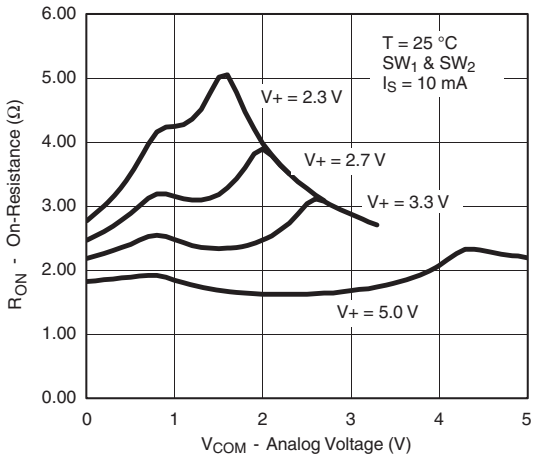
SPECIFICATIONS (V+ = 3 V)							
Parameter	**Symbol**	**Test Conditions Otherwise Unless Specified** V+ = 3 V, ± 10 %, V_{IN} = 0.4 V or 1.6 V[e]	**Temp.[a]**	**Limits - 40 °C to 85 °C Min.[b]**	**Typ.[c]**	**Max.[b]**	**Unit**
Dynamic Characteristics							
Turn-On Time	t_{ON} (SW_1, SW_2)	V_{NO} or V_{NC} = 2 V, R_L = 300 Ω, C_L = 35 pF (fig. 1, 2)	Room Full		62	85 91	ns
	t_{ON} (SW_3, SW_4)		Room Full		46	74 79	
Turn-Off Time	t_{ON} (SW_1, SW_2)		Room Full		12	35 36	
	t_{ON} (SW_3, SW_4)		Room Full		21	46 48	
Break-Before-Make Time	t_d (SW_1, SW_2)		Full	5	45		
	t_d (SW_3, SW_4)		Full	5	26		
Charge Injection[d]	Q_{INJ} (SW_1, SW_2)	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω (fig. 3)	Room		2		pC
	Q_{INJ} (SW_3, SW_4)				1		
Off-Isolation[d]	OIRR (SW_1, SW_2)	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz (fig. 4)	Room		- 68		dB
	OIRR (SW_3, SW_4)				- 51		
Crosstalk[d]	X_{TALK} (SW_1, SW_2)				- 69		
	X_{TALK} (SW_3, SW_4)				- 51		
N_O, N_C Off Capacitance[d]	C_{OFF} (SW_1, SW_2)	V_{IN} = 0 V or V+, f = 1 MHz	Room		12		pF
	C_{OFF} (SW_3, SW_4)				43		
Channel-On Capacitance[d]	C_{ON} (SW_1, SW_2)				86		
	C_{ON} (SW_3, SW_4)				283		
Power Supply							
Power Supply Range	V+			2		5.5	V
Power Supply Current	I+	V_{OE} = 0 V or V+				1	µA

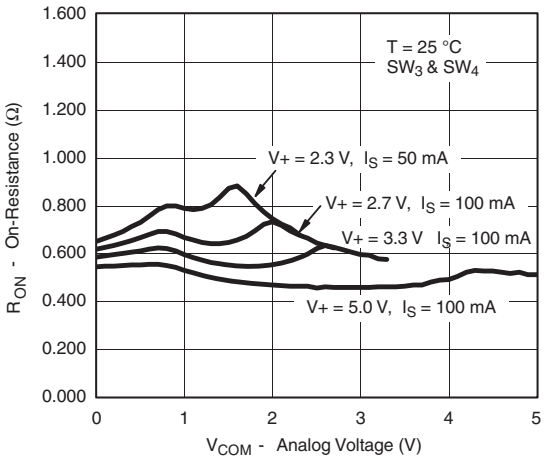
Notes:
a. Room = 25 °C, full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guarantee by design, nor subjected to production test.
e. VIN = input voltage to perform proper function.
f. Guaranteed by 5 V leakage testing, not production tested.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

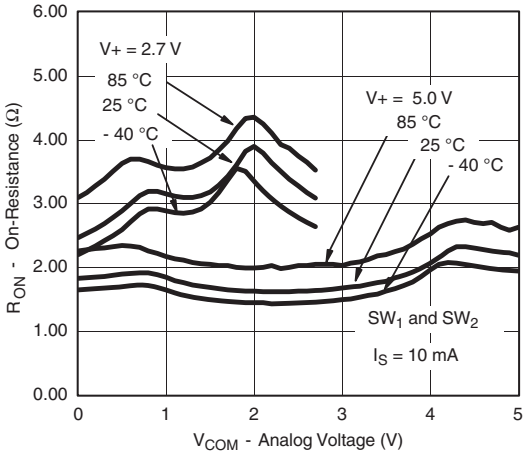
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



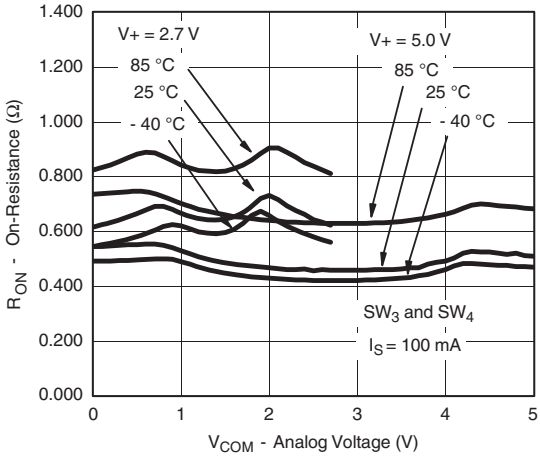
R_{ON} vs. V_{COM} and Single Supply Voltage



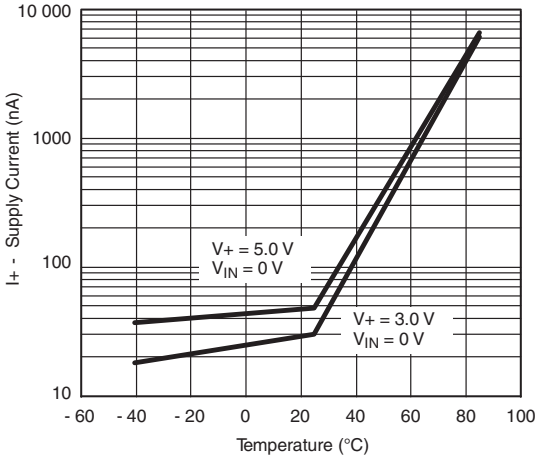
R_{ON} vs. V_{COM} and Single Supply Voltage



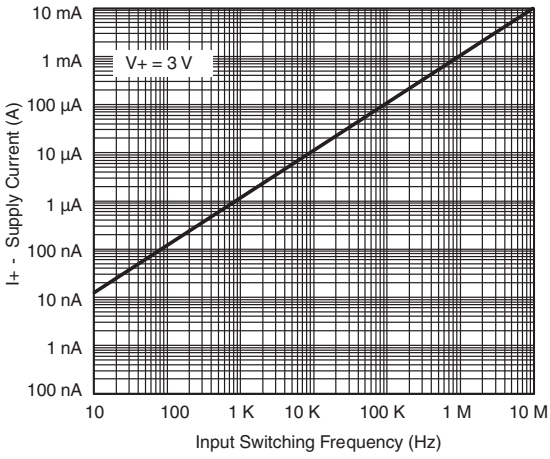
R_{ON} vs. Analog Voltage and Temperature



R_{ON} vs. Analog Voltage and Temperature



Supply Current vs. Temperature



Supply Current vs. Input Switching Frequency

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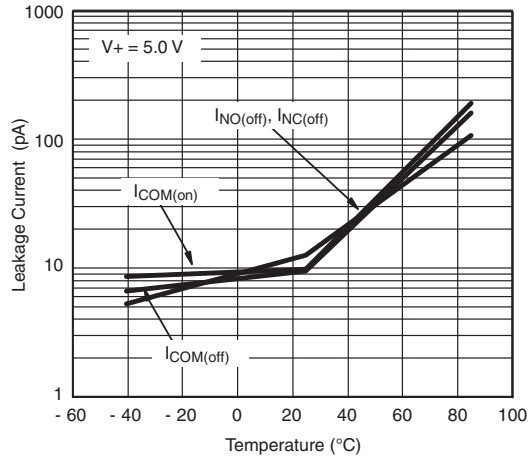
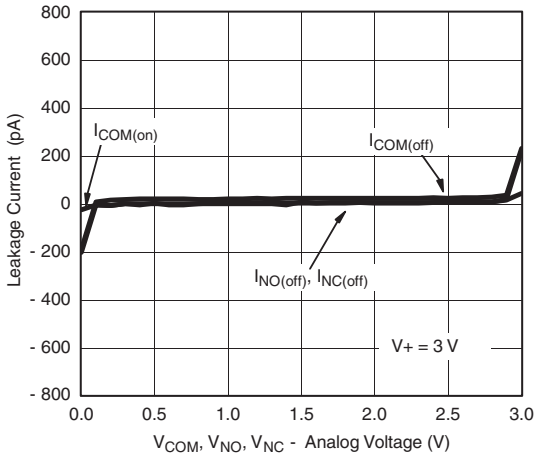
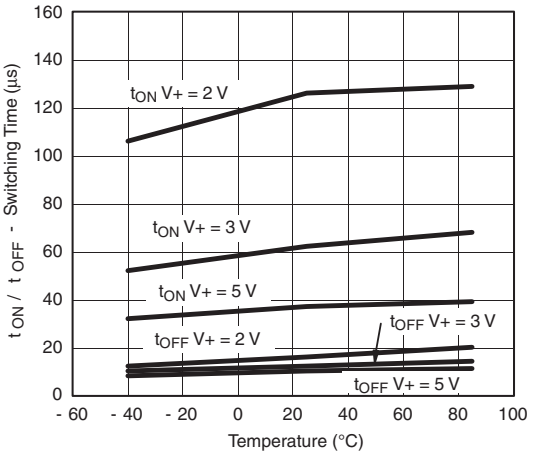
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



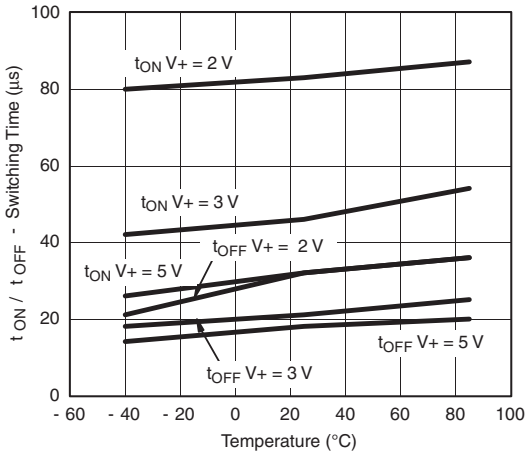
Leakage Current vs. Temperature



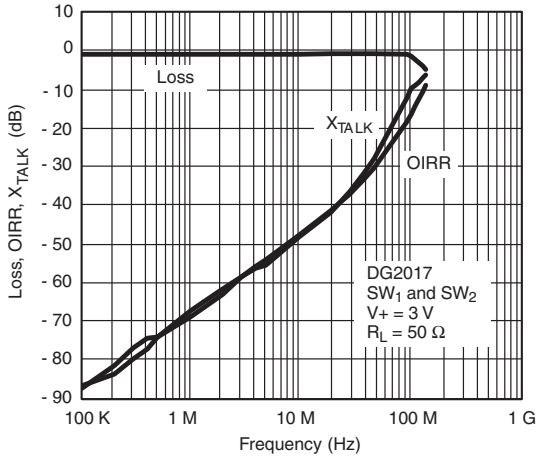
Leakage vs. Analog Voltage



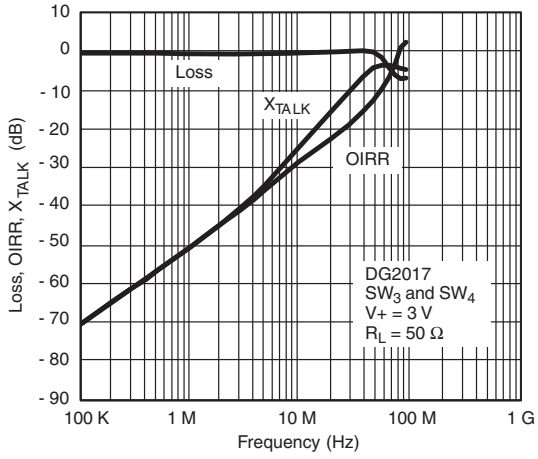
Switching Time vs. Temperature



Switching Time vs. Temperature

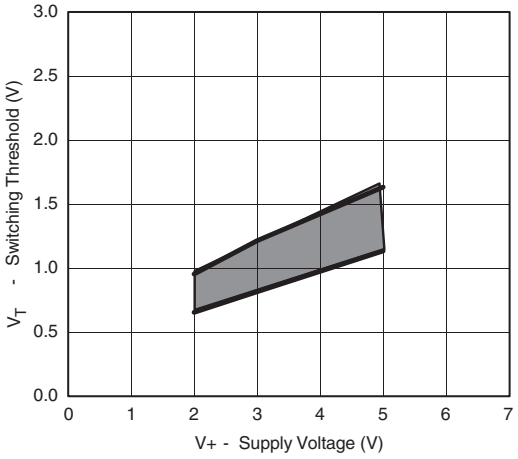


Insertion Loss, Off-Isolation Crosstalk vs. Frequency

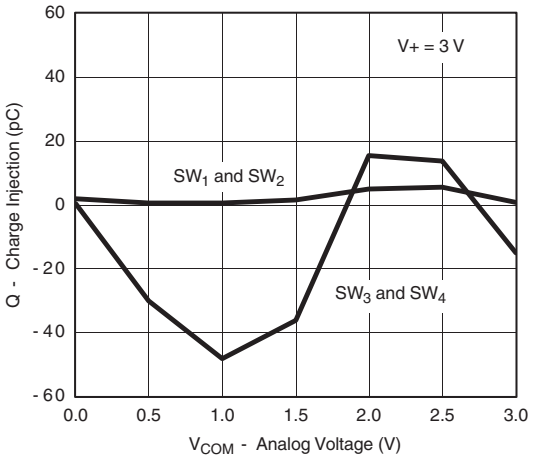


Insertion Loss, Off-Isolation, Crosstalk vs. Frequency

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

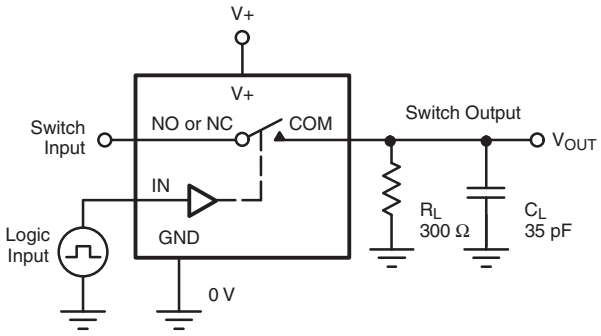


Switching Threshold vs. Supply Voltage



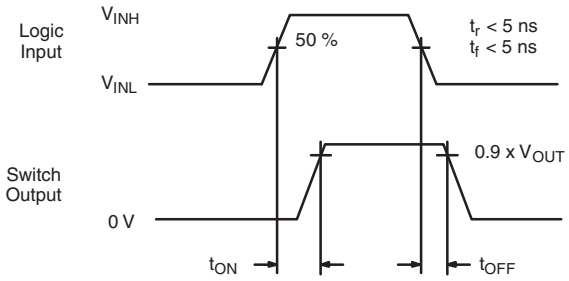
Charge Injection vs. Analog Voltage

TEST CIRCUITS



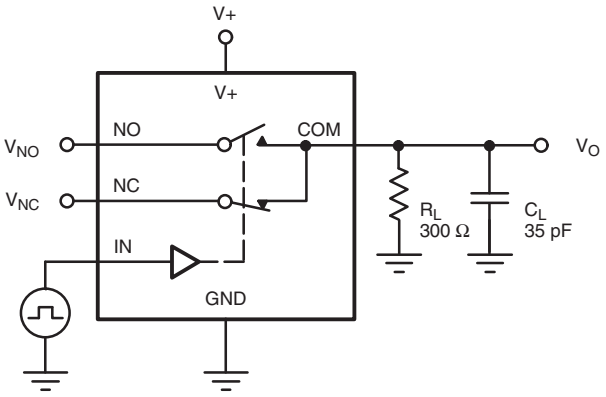
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time



C_L (includes fixture and stray capacitance)

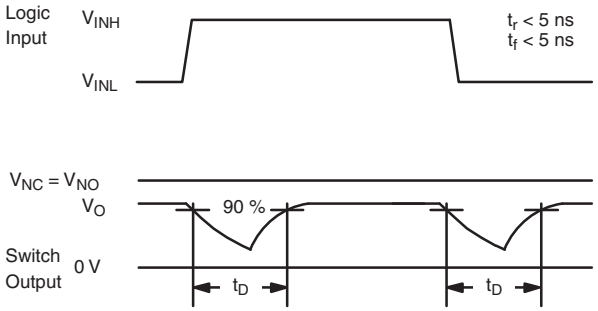


Figure 2. Break-Before-Make Interval

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TEST CIRCUITS

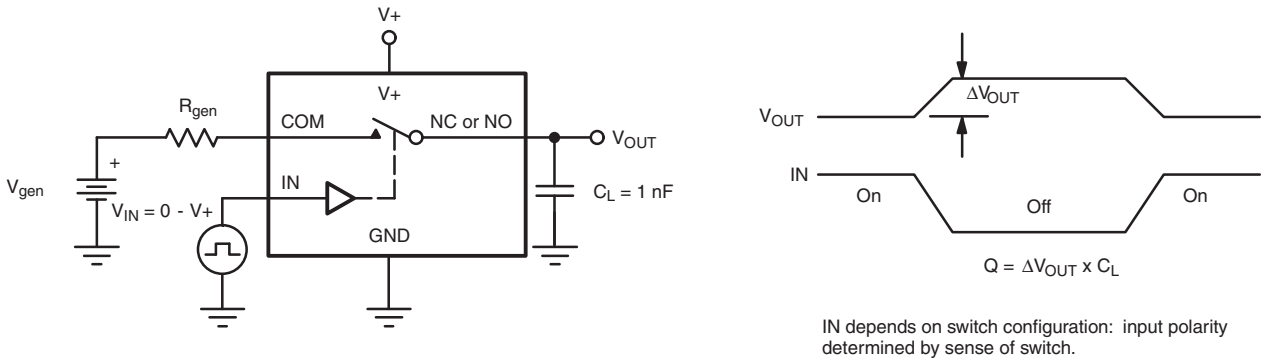


Figure 3. Charge Injection

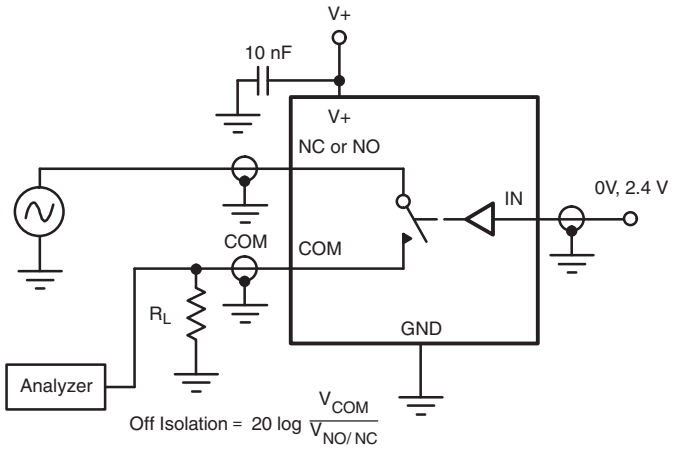


Figure 4. Off-Isolation

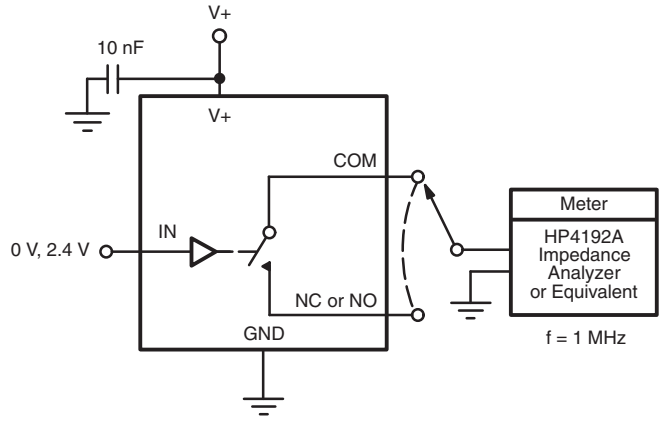
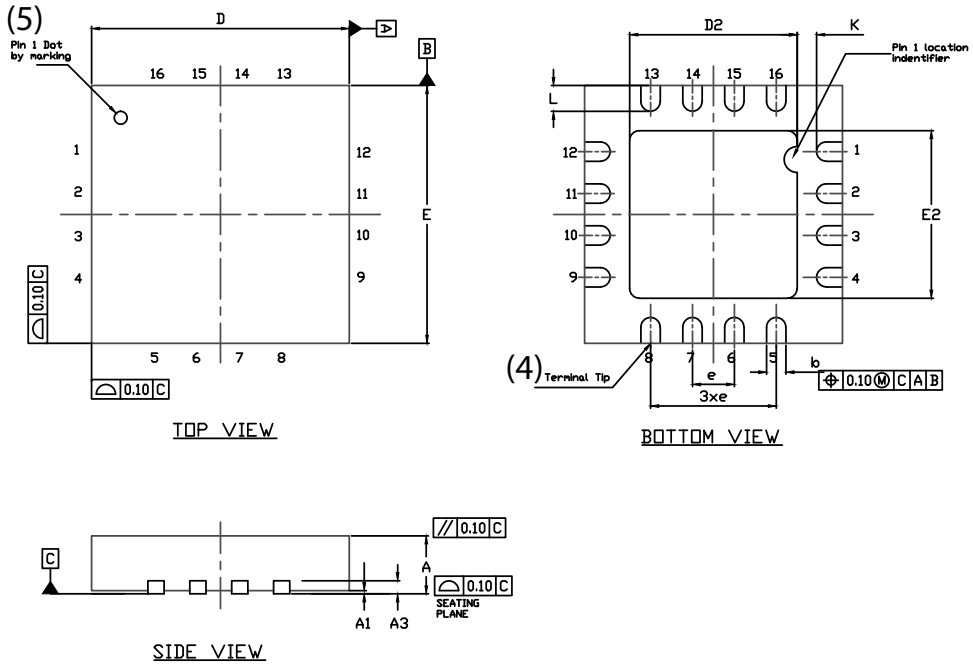


Figure 5. Channel Off/On Capacitance

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?72228.

QFN 4x4-16L Case Outline



DIM	VARIATION 1						VARIATION 2					
	MILLIMETERS[1]			INCHES			MILLIMETERS[1]			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.75	0.85	0.95	0.029	0.033	0.037	0.75	0.85	0.95	0.029	0.033	0.037
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
A3	0.20 ref.			0.008 ref.			0.20 ref.			0.008 ref.		
b	0.25	0.30	0.35	0.010	0.012	0.014	0.25	0.30	0.35	0.010	0.012	0.014
D	4.00 BSC			0.157 BSC			4.00 BSC			0.157 BSC		
D2	2.0	2.1	2.2	0.079	0.083	0.087	2.5	2.6	2.7	0.098	0.102	0.106
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
E	4.00 BSC			0.157 BSC			4.00 BSC			0.157 BSC		
E2	2.0	2.1	2.2	0.079	0.083	0.087	2.5	2.6	2.7	0.098	0.102	0.106
K	0.20 min.			0.008 min.			0.20 min.			0.008 min.		
L	0.5	0.6	0.7	0.020	0.024	0.028	0.3	0.4	0.5	0.012	0.016	0.020
N[3]	16			16			16			16		
Nd[3]	4			4			4			4		
Ne[3]	4			4			4			4		

Notes

(1) Use millimeters as the primary measurement.
(2) Dimensioning and tolerances conform to ASME Y14.5M. - 1994.
(3) N is the number of terminals. Nd and Ne is the number of terminals in each D and E site respectively.
(4) Dimensions b applies to plated terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.
(5) The pin 1 identifier must be existed on the top surface of the package by using identification mark or other feature of package body.
(6) Package warpage max. 0.05 mm.

ECN: S13-0893-Rev. B, 22-Apr-13
DWG: 5890

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