

Fault-Protected Single 8-Ch/Differential 4-Ch Analog Multiplexers

DESCRIPTION

The DG458 and DG459 are 8-channel single-ended and 4-channel differential analog multiplexers, respectively, incorporating fault protection. A series n-p-n MOSFET structure provides device and signal-source protection in the event of power loss or overvoltages. Under fault conditions the multiplexer input (or output) appears as an open circuit and only a few nanoamperes of leakage current will flow. This protects not only the multiplexer and the circuitry following it, but also protects the sensors or signal sources which drive the multiplexer.

The DG458 and DG459 can withstand continuous overvoltage inputs up to ± 35 V. All digital inputs have TTL compatible logic thresholds. Break-before-make operation prevents channel-to-channel interference.

The DG458 and DG459 are improved pin-compatible replacements for HI-508A/509A and MAX358/359 multiplexers.

FEATURES

- Fault and Overvoltage Protection
- All Channels Off When Power Off
- Latchup-Proof
- Fast Switching - t_A : 200 ns
- Break-Before-Make Switching
- Low On-Resistance: 180 Ω
- Low Power Consumption: 3 mW
- TTL and CMOS Compatible Inputs



RoHS*
COMPLIANT

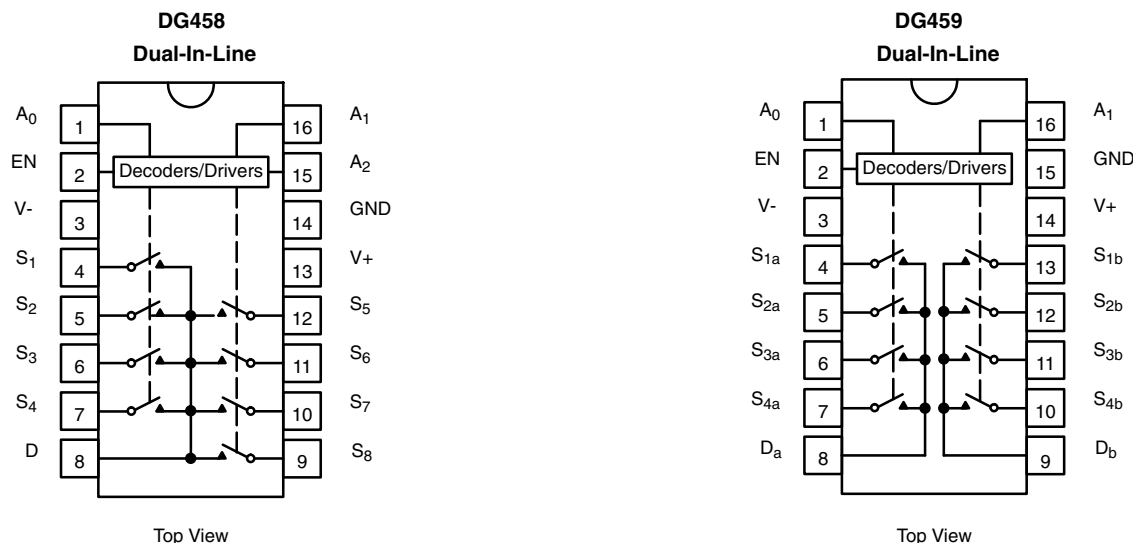
BENEFITS

- Improved Ruggedness
- Power Loss Protection
- Prevents Adjacent Channel Crosstalk
- Standard Logic Interface
- Superior Accuracy
- Fast Settling Time

APPLICATIONS

- Data Acquisition Systems
- Industrial Process Control Systems
- Avionics Test Equipment
- High-Rel Control Systems
- Telemetry

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



* Pb containing terminations are not RoHS compliant, exemptions may apply

THRU TABLES AND ORDERING INFORMATION

TRUTH TABLE - DG458				
A ₂	A ₁	A ₀	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

TRUTH TABLE - DG459			
A ₁	A ₀	EN	On Switch
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Logic "0" = $V_{AL} \leq 0.8 \text{ V}$

Logic "1" = $V_{AH} \geq 2.4 \text{ V}$

X = Don't Care

ORDERING INFORMATION		
Temp Range	Package	Part Number
- 40 to 85 °C	16-pin Plastic DIP	DG458DJ DG458DJ-E3
		DG459DJ DG459DJ-E3

ABSOLUTE MAXIMUM RATINGS			
Parameter		Limit	Unit
V ₊ to V ₋		44	V
V ₊ to GND		22	
V ₋ to GND		- 25	
V _{EN} , V _A Digital Input		(V ₋) - 4 to (V ₊) + 4	
V _S , Analog Input Overvoltage with Power On		(V ₋) - 20 to (V ₊) + 20	
V _S , Analog Input Overvoltage with Power Off		- 35 to + 35	
Continuous Current, S or D		20	mA
Peak Current, S or D (Pulsed at 1 ms, 10 % duty cycle max)		40	
Storage Temperature	(AK Suffix)	- 65 to 150	°C
	(DJ Suffix)	- 65 to 125	
Power Dissipation (Package) ^a	16-pin Plastic DIP ^B	600	mW
	16-pin CerDIP ^C	1000	
	LCC-20 ^d	1000	

Notes:

a. All leads soldered or welded to PC board.

b. Derate 6.3 mW/°C above 75 °C.

c. Derate 12 mW/°C above 75 °C.

d. Derate 10 mW/°C above 75 °C.



SPECIFICATIONS ^a										
Parameter	Symbol	Test Conditions Unless Otherwise Specified V ₊ = 15 V, V ₋ = - 15 V V _{AL} = 0.8 V, V _{AH} = 2.4 V ^f		Temp. ^b	Typ. ^c	A Suffix - 55 °C to 125 °C		D Suffix - 40 °C to 85 °C		Unit
						Min. ^d	Max. ^d	Min. ^d	Max. ^d	
Analog Switch										
Analog Signal Range ^e	V _{ANALOG}			Full		- 10	10	- 10	10	V
Drain-Source On-Resistance	R _{DS(on)}	V _D = ± 9.5 V, I _S = - 400 μA		Room Full	0.45		1.2 1.5		1.5 1.8	kΩ
		V _D = ± 5 V, I _S = - 400 μA		Room	180		400		400	Ω
R _{DS(on)} Matching Between Channels ^h	ΔR _{DS(on)}	V _D = 0 V, I _S = - 400 μA		Room	6					%
Source Off Leakage Current	I _{S(off)}	V _{EN} = 0 V, V _D = ± 10 V V _S = ± 10 V		Room Full	0.03	- 0.5 - 50	0.5 50	- 1 - 20	1 20	nA
Drain Off Leakage Current	I _{D(off)}	V _{EN} = 0 V V _D = ± 10 V V _S = ± 10 V	DG458	Room Full	0.1	- 1 - 200	1 200	- 1 - 50	1 50	
			DG459	Room Full	0.1	- 1 - 100	1 100	- 2 - 25	2 25	
Differential Off Drain Leakage Current	I _{DIFF}	DG459 Only		Room		- 50	50	- 20	20	
Drain On Leakage Current	I _{D(on)}	V _S = V _D = ± 10 V	DG458	Room Full	0.1	- 2 - 200	2 200	- 5 - 50	5 50	
			DG459	Room Full	0.05	- 2 - 100	2 100	- 5 - 25	5 25	
Fault										
Output Leakage Current (with Overvoltage)	I _{D(off)}	V _S = ± 33 V, V _D = 0 V See Figure 1		Room	0.02					nA
Input Leakage Current (with Overvoltage)	I _{S(off)}	V _S = ± 25 V, V _D = 10 V, See Figure 1		Room	0.005	- 5	5	- 10	10	μA
Input Leakage Current (with Power Supplies Off)		V _S = ± 25 V, V _{SUPS} = 0 V V _D = A ₀ , A ₁ , A ₂ , EN = 0 V		Room	0.001	- 2	2	- 5	5	
Digital Control										
Input Low Threshold	V _{AI}			Full			0.8		0.8	V
Input Low Threshold	V _{AL}			Full		2.4		2.4		
Logic Input Control	I _A	V _A = 2.4 V or 0.8 V		Full		- 1	1	- 1	1	μA

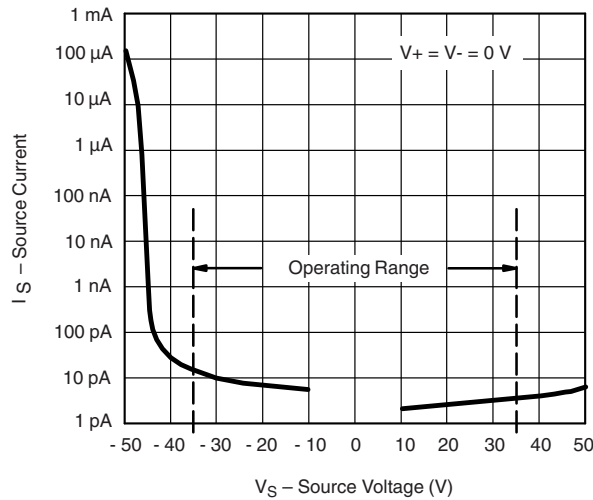
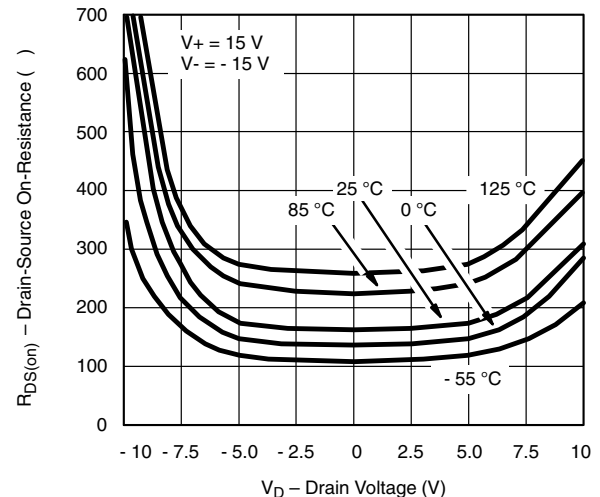
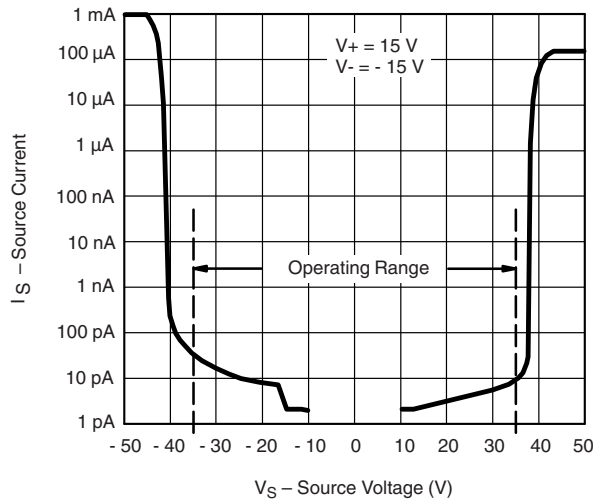
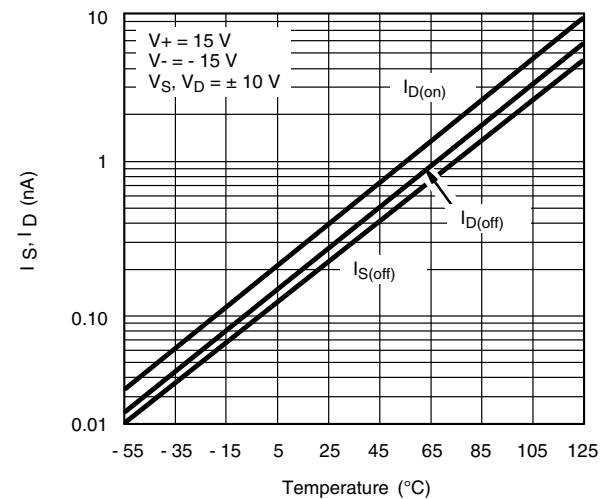
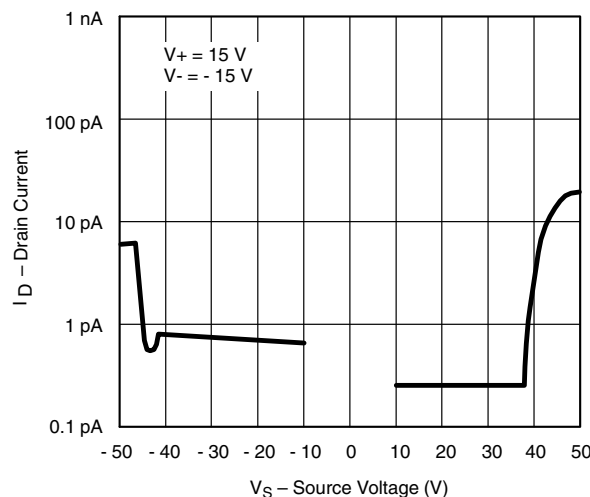
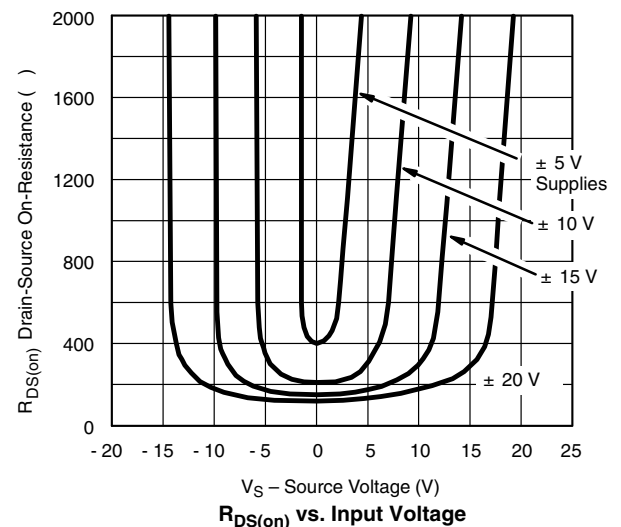
SPECIFICATIONS ^a										
Parameter	Symbol	Test Conditions Unless Otherwise Specified V ₊ = 15 V, V ₋ = - 15 V V _{AL} = 0.8 V, V _{AH} = 2.4 V ^f		Temp. ^b	Typ. ^c	A Suffix - 55 °C to 125 °C		D Suffix - 40 °C to 85 °C		Unit
						Min. ^d	Max. ^d	Min. ^d	Max. ^d	
Dynamic Characteristics										
Transition Time	t _A	See Figure 3		Room	200		500		500	ns
Break-Before-Make Interval	t _{OPEN}	See Figure 4		Room	45	10		10		
Enable Turn-On Time	t _{ON(EN)}	See Figure 5		Room Full	140		250 500		250 500	
Enable Turn-Off Time	t _{OFF(EN)}			Room Full	50		250 500		250 500	
Settling Time	t _s	To 0.1 %		Room	0.5					μs
		To 0.01 %		Room	1.5					
Off Isolation	OIRR	V _{EN} = 0 V, R _L = 1 kΩ C _L = 15 pF, V _S = 3 V _{RMS} f = 100 kHz		Room	90					dB
Logic Input Capacitance	C _{In}	f = 1 MHz		Room	5					pF
Source Off Capacitance	C _{S(off)}			Room	5					
Drain Off Capacitance	C _{D(off)}		DG458	Room	15					
			DG459	Room	10					
Drain On Capacitance	C _{D(on)}		DG458	Room	40					
			DG459	Room	35					
Power Supplies										
Positive Supply Current	I ₊	V _{EN} = 5 or 0 V, V _A = 0 V		Room Full	0.05		0.1 0.2		0.1 0.2	mA
Negative Supply Current	I ₋			Room Full	- 0.01	- 0.1 - 0.2		- 0.1 - 0.2		
Power Supply Range for Continuous Operation				Room		± 4.5	± 18	± 4.5	± 18	V

Notes:

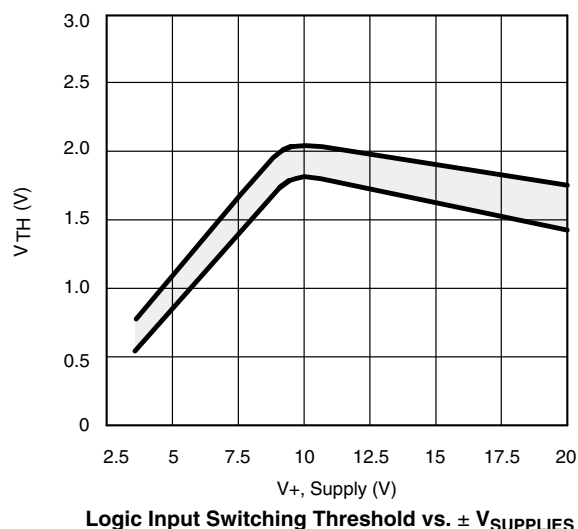
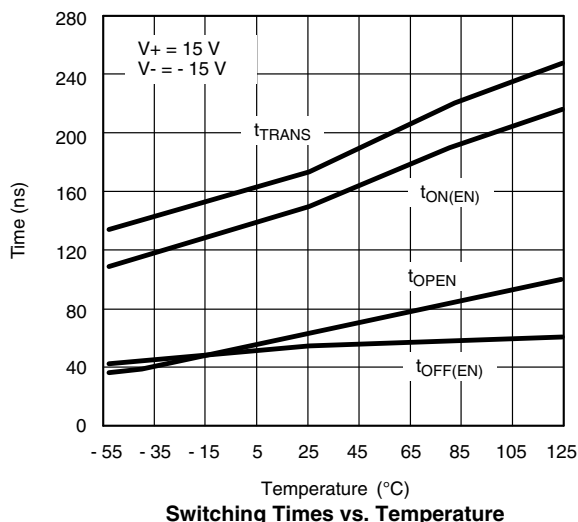
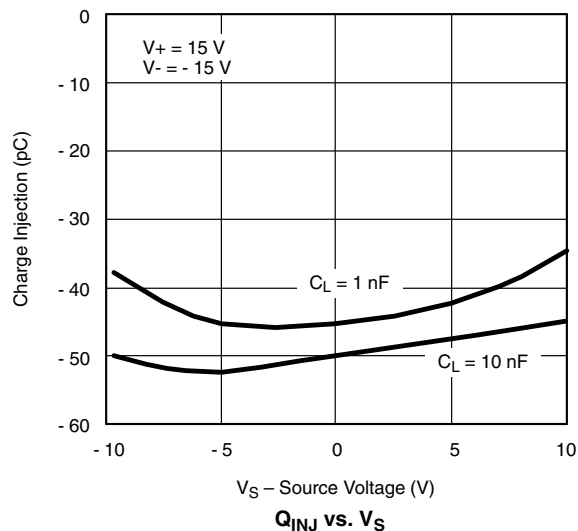
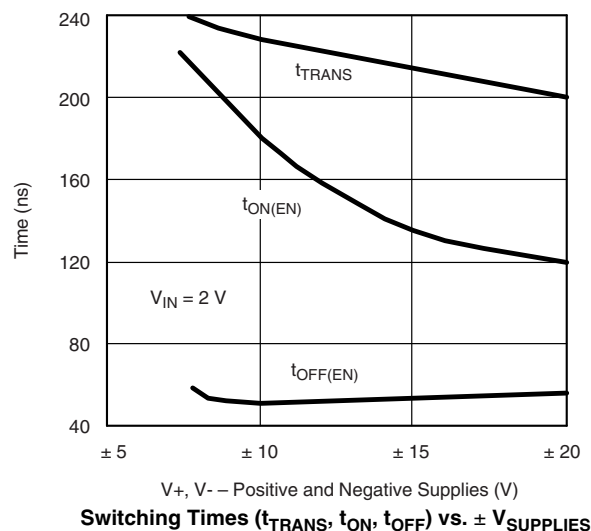
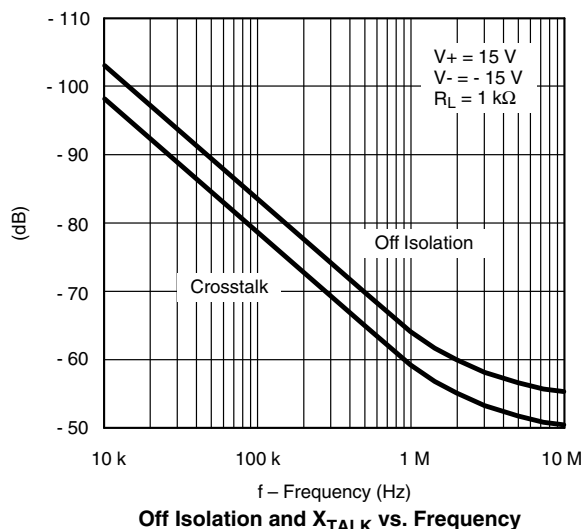
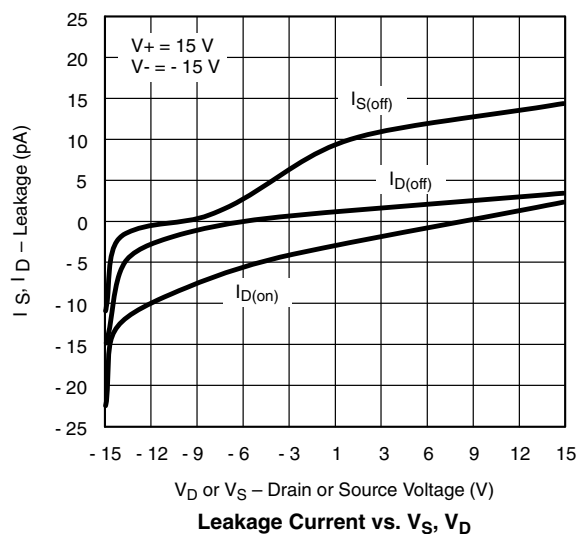
- Refer to PROCESS OPTION FLOWCHART.
- Room = 25 °C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- V_{IN} = input voltage to perform proper function.
- When the analog signal exceeds the + 13.5 V or - 12 V, R_{DS(on)} starts to rise until only leakage currents flow.

$$h. \Delta R_{DS(on)} = \left(\frac{R_{DS(on) \text{ MAX}} - R_{DS(on) \text{ MIN}}}{R_{DS(on) \text{ AVE}}} \right) \times 100 \%$$

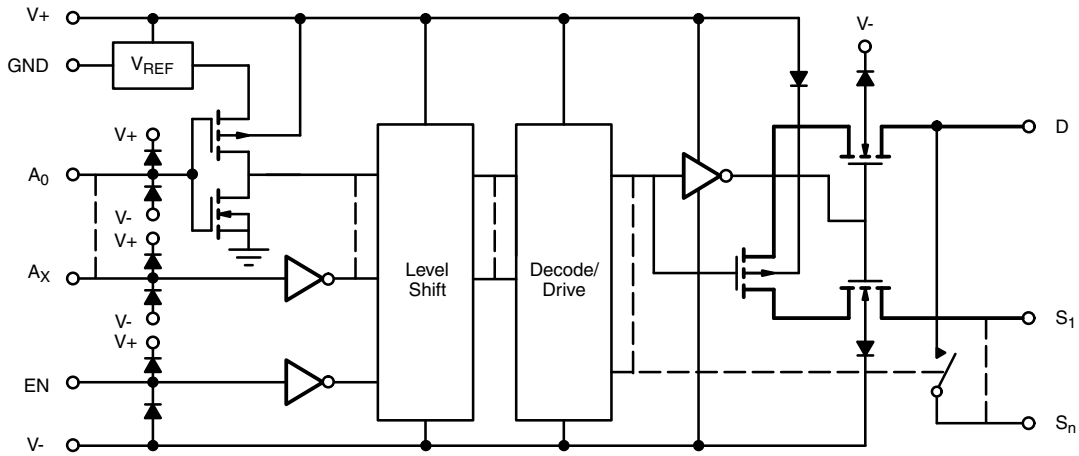
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Input Leakage vs. Input Voltage

 $R_{DS(on)}$ vs. V_D and Temperature

Off-Channel Leakage Currents vs. Input Voltage

Leakage Currents vs. Temperature

Output Leakage vs. Off-Channel Overvoltage

 $R_{DS(on)}$ vs. Input Voltage

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



SCHEMATIC DIAGRAM (TYPICAL CHANNEL)



TEST CIRCUITS

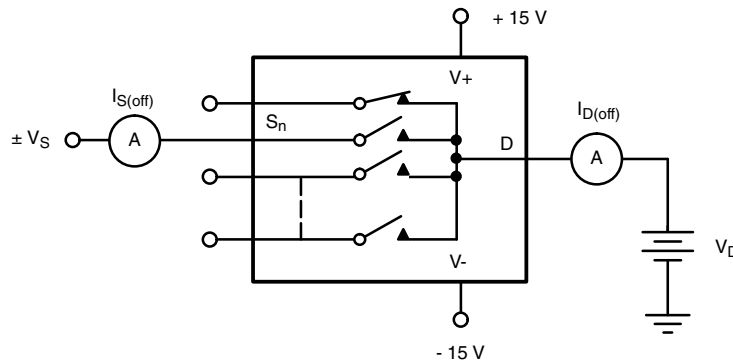


Figure 2. Analog Input Overvoltage

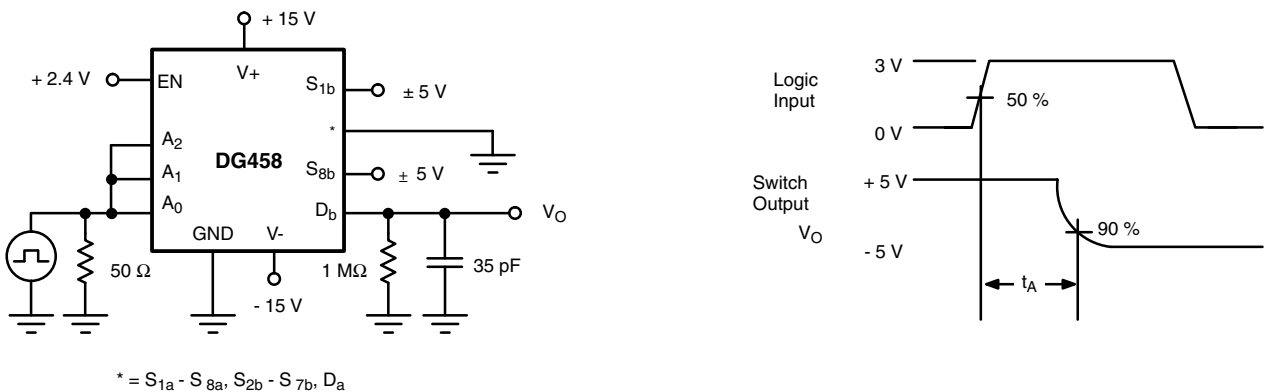


Figure 3. Transition Time

TEST CIRCUITS

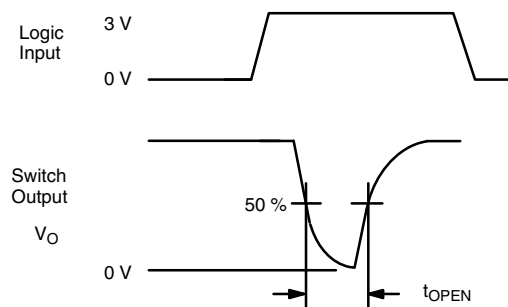
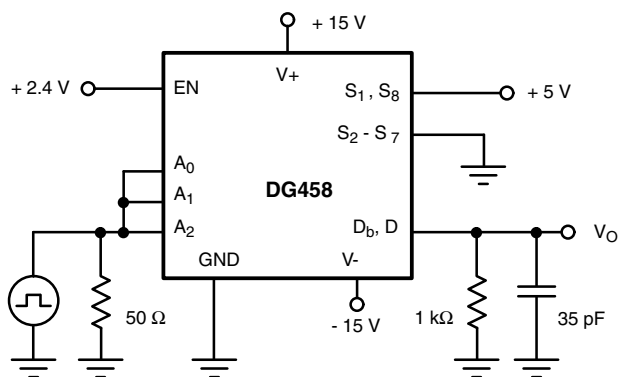


Figure 4. Break-Before-Make Time

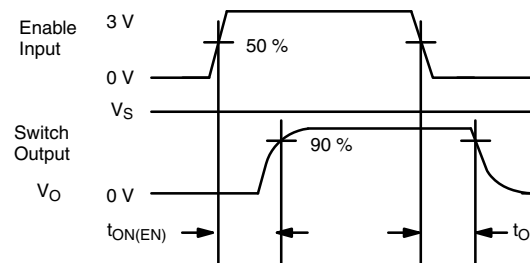
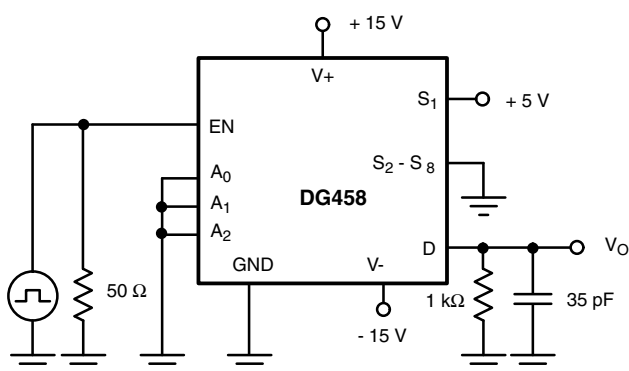


Figure 5. Enable Delay

DETAILED DESCRIPTION

The Vishay Siliconix DG458 and DG459 multiplexers are fully fault- and overvoltage-protected for continuous input voltages up to ± 35 V whether or not voltage is applied to the power supply pins ($V+$, $V-$). These multiplexers are built on a high-voltage junction-isolated silicon-gate CMOS process. Two n-channel and one p-channel MOSFETs are connected in series to form each channel (Figure 1).

Within the normal analog signal range (± 10 V), the $R_{DS(on)}$ variation as a function of analog signal voltage is comparable to that of the classic parallel N-MOS and P-MOS switches.

When the analog signal approaches or exceeds either supply rail, even for an on-channel, one of the three series MOSFETs gets cut-off, providing inherent protection against overvoltages even if the multiplexer power supply voltages are lost. This protection is good up to the breakdown voltage of the respective series MOSFETs. Under fault conditions only sub microamp leakage currents can flow in or out of the multiplexer. This not only provides protection for the multiplexer and succeeding circuitry, but it allows normal, undisturbed operation of all other channels. Additionally, in case of power loss to the multiplexer, the loading caused on the transducers and signal sources is insignificant, therefore redundant multiplexers can be used on critical applications such as telemetry and avionics.

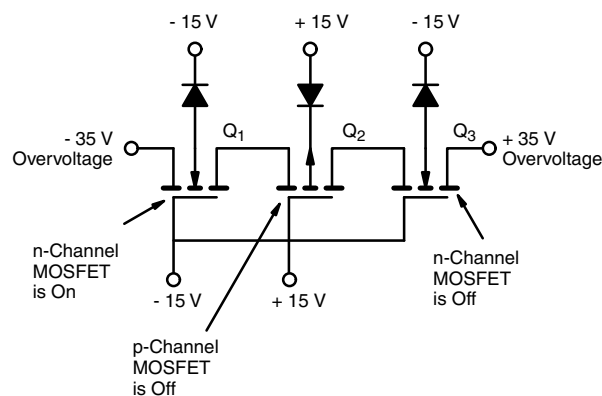
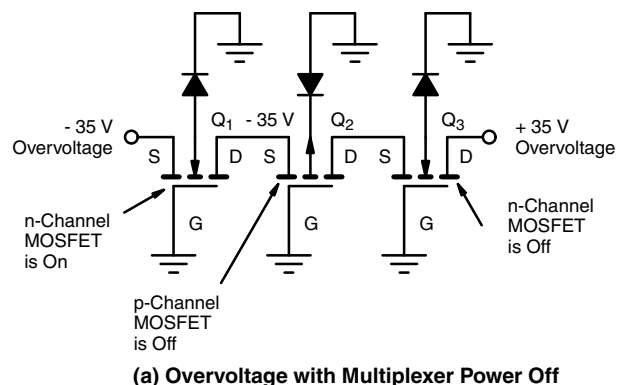


Figure 5. Overvoltage Protection

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?70064>.



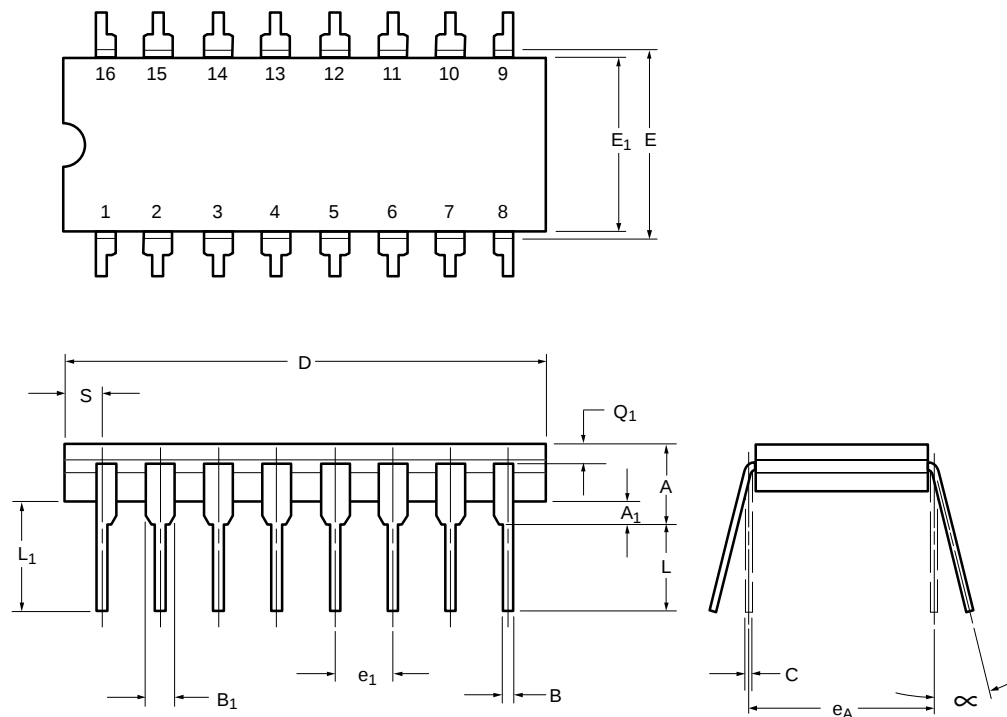
PDIP: 16-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A₁	0.38	1.27	0.015	0.050
B	0.38	0.51	0.015	0.020
B₁	0.89	1.65	0.035	0.065
C	0.20	0.30	0.008	0.012
D	18.93	21.33	0.745	0.840
E	7.62	8.26	0.300	0.325
E₁	5.59	7.11	0.220	0.280
e₁	2.29	2.79	0.090	0.110
e_A	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
Q₁	1.27	2.03	0.050	0.080
S	0.38	1.52	.015	0.060
ECN: S-03946—Rev. D, 09-Jul-01 DWG: 5482				



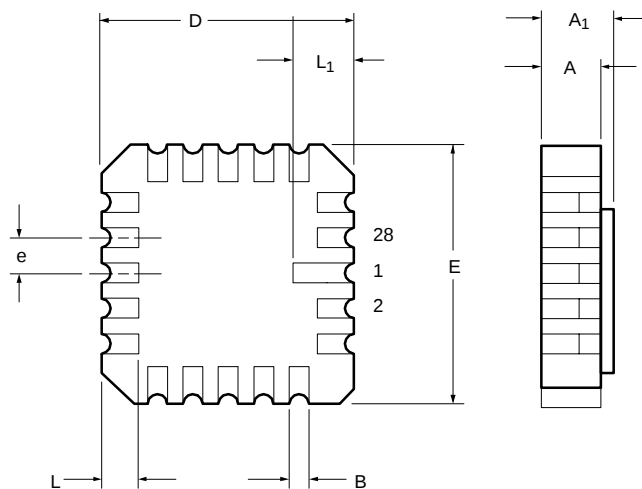
CERDIP: 16-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	4.06	5.08	0.160	0.200
A ₁	0.51	1.14	0.020	0.045
B	0.38	0.51	0.015	0.020
B ₁	1.14	1.65	0.045	0.065
C	0.20	0.30	0.008	0.012
D	19.05	19.56	0.750	0.770
E	7.62	8.26	0.300	0.325
E ₁	6.60	7.62	0.260	0.300
e ₁	2.54 BSC		0.100 BSC	
e _A	7.62 BSC		0.300 BSC	
L	3.18	3.81	0.125	0.150
L ₁	3.81	5.08	0.150	0.200
Q ₁	1.27	2.16	0.050	0.085
S	0.38	1.14	0.015	0.045
∞	0°	15°	0°	15°
ECN: S-03946—Rev. G, 09-Jul-01 DWG: 5403				



20-LEAD LCC



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.37	2.24	0.054	0.088
A₁	1.63	2.54	0.064	0.100
B	0.56	0.71	0.022	0.028
D	8.69	9.09	0.342	0.358
E	8.69	9.09	0.442	0.358
e	1.27 BSC		0.050 BSC	
L	1.14	1.40	0.045	0.055
L₁	1.96	2.36	0.077	0.093
ECN: S-03946—Rev. B, 09-Jul-01 DWG: 5321				



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