

0.5 pC Charge Injection, 100 pA Leakage, Dual SPDT Analog Switch

DESCRIPTION

The DG636 is an analog CMOS, dual SPDT switch, designed to operate from a + 2.7 V to + 12 V single supply or from ± 2.7 V to ± 5.0 V, dual supplies. The DG636 is fully specified at + 3 V, + 5 V and ± 5 V. All control logic inputs have guaranteed 2 V logic high limits when operating from + 5 V or ± 5 V supplies and 1.4 V when operating from a 3 V supply. The DG636 switches conduct equally well in both directions and offer rail to rail analog signal handling. < 1 pC low charge injection, coupled with very low switch capacitance and leakage current makes this product ideal for use in precision instrumentation applications. Operating temperature range is specified from - 40 °C to + 125 °C. The DG636 is available in 14 lead TSSOP and the space saving 1.8 mm x 2.6 mm miniQFN package.

FEATURES

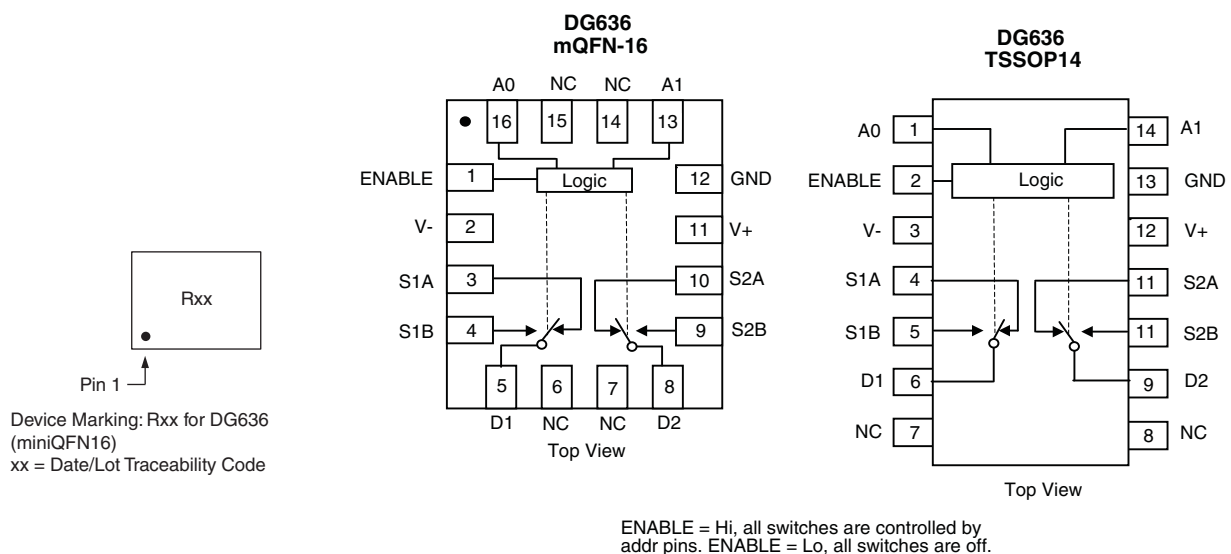
- Ultra low charge injection (± 0.5 pC, typ. over the full analog signal range)
- Leakage current < 0.5 nA max. at 85 °C (for DG636EQ-T1-E3)
- Low switch capacitance (C_{soff} , 2 pF typ.)
- Low $R_{\text{DS(on)}}$ - 115 Ω max.
- Fully specified with single supply operation at 3.0 V, 5.0 V and dual supplies at ± 5.0 V
- Low voltage, 2.5 V CMOS/TTL compatible
- 600 MHz, - 3 dB bandwidth
- Excellent isolation and crosstalk performance (typ. > - 60 dB at 10 MHz)
- Fully specified from - 40 °C to 85 °C and - 40 °C to + 125 °C
- 14 pin TSSOP and 16 pin miniQFN package (1.8 mm x 2.6 mm)
- Compliant to RoHS directive 2002/95/EC


RoHS
COMPLIANT

APPLICATIONS

- High-end data acquisition
- Medical instruments
- Precision instruments
- High speed communications applications
- Automated test equipment
- Sample and hold applications

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE

Enable Input	Selected Input		On Switches
	A1	A0	DG636
L	X	X	All Switches Open
H	L	L	D1 to S1A, D2 to S2A
H	L	H	D1 to S1B, D2 to S2A
H	H	L	D1 to S1A, D2 to S2B
H	H	H	D1 to S1B, D2 to S2B

ORDERING INFORMATION

Temp. Range	Package	Part Number
- 40 °C to 125 °C ^a	14 pin TSSOP	DG636EQ-T1-E3
	16 pin miniQFN	DG636EN-T1-E4

Notes:

a. - 40 °C to 85 °C datasheet limits apply.

ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ °C}$, unless otherwise noted)

Parameter	Limit	Unit
V+ to V-	14	V
GND to V-	7	
Digital Inputs ^a , V_S , V_D	(V-) - 0.3 to (V+) + 0.3 or 30 mA, whichever occurs first	
Continuous Current (Any Terminal)	30	mA
Peak Current, S or D (Pulsed 1 ms, 10 % Duty Cycle)	100	
Storage Temperature	- 65 to 150	°C
Power Dissipation (Package) ^b	14 pin TSSOP ^c	mW
	16 pin miniQFN ^{d, e}	
Thermal Resistance (Package) ^b	14 pin TSSOP	°C/W
	16 pin miniQFN	

Notes:

a. Signals on SX, DX, or INX exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

b. All leads welded or soldered to PC board.

c. Derate 5.6 mW/°C above 70 °C.

d. Derate 6.6 mW/°C above 70 °C.

e. Manual soldering with iron is not recommended for leadless components. The miniQFN-16 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

SPECIFICATIONS FOR DUAL SUPPLIES

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 5 V, V- = - 5 V VIN A0, A1 and ENABLE = 2.0 V, 0.8 V ^a	Temp. ^b	Typ. ^c	- 40 °C to 125 °C		- 40 °C to 85 °C		Unit
					Min. ^d	Max. ^d	Min. ^d	Max. ^d	
Analog Switch									
Analog Signal Range ^e	V _{ANALOG}		Full		- 5	5	- 5	5	V
On-Resistance	R _{DS(on)}	I _S = 1 mA, V _D = - 3 V, 0 V, + 3 V	Room Full	70		115 160		115 140	Ω
On-Resistance Match	ΔR _{ON}	I _S = 1 mA, V _D = ± 3 V	Room Full	1		5 6.5		5 6.5	
On-Resistance Flatness	R _{FLATNESS}	I _S = 1 mA, V _D = - 3 V, 0 V, + 3 V	Room Full	10		20 33		20 22	

SPECIFICATIONS FOR DUAL SUPPLIES									
		Test Conditions Unless Otherwise Specified V+ = 5 V, V- = - 5 V VIN A0, A1 and ENABLE = 2.0 V, 0.8 V ^a			- 40 °C to 125 °C		- 40 °C to 85 °C		
Parameter	Symbol		Temp. ^b	Typ. ^c	Min. ^d	Max. ^d	Min. ^d	Max. ^d	Unit
Analog Switch									
Analog Signal Range ^e	V _{ANALOG}		Full		- 5	5	- 5	5	V
On-Resistance	R _{DS(on)}	I _S = 1 mA, V _D = - 3 V, 0 V, + 3 V	Room Full	70		115 160		115 140	Ω
On-Resistance Match	ΔR _{ON}	I _S = 1 mA, V _D = ± 3 V	Room Full	1		5 6.5		5 6.5	
On-Resistance Flatness	R _{FLATNESS}	I _S = 1 mA, V _D = - 3 V, 0 V, + 3 V	Room Full	10		20 33		20 22	
Switch Off Leakage Current (for 14 pin TSSOP)	I _{S(off)}	V+ = 5.5 V, V- = - 5.5 V V _D = ± 4.5 V, V _S = ∓ 4.5 V	Room Full	± 0.01	- 0.1 - 18	0.1 18	- 0.1 - 0.5	0.1 0.5	nA
	I _{D(off)}		Room Full	± 0.01	- 0.1 - 18	0.1 18	- 0.1 - 0.5	0.1 0.5	
Channel On Leakage Current (for 14 pin TSSOP)	I _{D(on)}	V+ = 5.5 V, V- = - 5.5 V, V _S = V _D = ± 4.5 V	Room Full	± 0.01	- 0.1 - 18	0.1 18	- 0.1 - 0.5	0.1 0.5	
Switch Off Leakage Current (for 16 pin miniQFN)	I _{S(off)}	V+ = 5.5 V, V- = - 5.5 V V _D = ± 4.5 V, V _S = ∓ 4.5 V	Room Full	± 0.01	- 1 - 18	1 18	- 1 - 2	1 2	
	I _{D(off)}		Room Full	± 0.01	- 1 - 18	1 18	- 1 - 2	1 2	
Channel On Leakage Current (for 16 pin miniQFN)	I _{D(on)}	V+ = 5.5 V, V- = - 5.5 V, V _S = V _D = ± 4.5 V	Room Full	± 0.01	- 1 - 18	1 18	- 1 - 2	1 2	
Digital Control									
Input Current, V _{IN} Low	I _{IL}	V _{IN} A0, A1 and ENABLE Under Test = 0.8 V	Full	0.005	- 0.1	0.1	- 0.1	0.1	μA
Input Current, V _{IN} High	I _{IH}	V _{IN} A0, A1 and ENABLE Under Test = 2.0 V	Full	0.005	- 0.1	0.1	- 0.1	0.1	
Input Capacitance ^e	C _{IN}	f = 1 MHz	Room	3.4					pF
Dynamic Characteristics									
Transition Time	t _{TRANS}	V _{S(CLOSE)} = 3 V, V _{S(OPEN)} = 0.0 V, R _L = 300 Ω, C _L = 35 pF	Room Full	20		70 105		70 80	ns
Turn-On Time	t _{ON}	R _L = 300 Ω, C _L = 35 pF V _S = ± 3 V	Room Full	16		60 90		60 65	
Turn-Off Time	t _{OFF}		Room Full	15		52 76		52 56	
Break-Before-Make Time Delay	t _D	V _S = 3 V R _L = 300 Ω, C _L = 35 pF	Room Full	15	5		5		
Charge Injection ^e	Q	V _g = 0 V, R _g = 0 Ω, C _L = 1 nF	Room	0.1					pC
Off Isolation ^e	OIRR	R _L = 50 Ω, C _L = 5 pF, f = 10 MHz	Room	- 58					dB
Bandwidth ^e	BW	R _L = 50 Ω	Room	610					MHz
Channel-to-Channel Crosstalk ^e	X _{TALK}	R _L = 50 Ω, C _L = 5 pF, f = 10 MHz	Room	- 88					dB
Source Off Capacitance ^e	C _{S(off)}	f = 1 MHz	Room	2.1					pF
Drain Off Capacitance ^e	C _{D(off)}		Room	4.2					
Channel On Capacitance ^e	C _{D(on)}		Room	11.3					
Total Harmonic Distortion ^e	THD	Signal = 1 V _{RMS} , 20 Hz to 20 kHz, R _L = 600 Ω	Room	0.01					%

SPECIFICATIONS FOR DUAL SUPPLIES

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 5 V, V- = - 5 V VIN A0, A1 and ENABLE = 2.0 V, 0.8 V ^a	Temp. ^b	Typ. ^c	- 40 °C to 125 °C		- 40 °C to 85 °C		Unit
					Min. ^d	Max. ^d	Min. ^d	Max. ^d	
Power Supplies									
Power Supply Current	I+	VIN = 0 V, or V+	Room Full	0.001		0.5 1		0.5 1	µA
Negative Supply Current	I-		Room Full	- 0.001	- 0.5 - 1		- 0.5 - 1		
Ground Current	IGND		Room Full	- 0.001	- 0.5 - 1		- 0.5 - 1		

SPECIFICATIONS FOR SINGLE SUPPLY

Parameter	Symbol	Test Conditions Unless Otherwise Specified V ₊ = 5 V, V ₋ = 0 V V _{IN} A0, A1 and ENABLE = 2.0 V, 0.8 V ^a	Temp. ^b	Typ. ^c	- 40 °C to 125 °C		- 40 °C to 85 °C		Unit
					Min. ^d	Max. ^d	Min. ^d	Max. ^d	
Analog Switch									
Analog Signal Range ^e	V _{ANALOG}		Full			5		5	V
On-Resistance	R _{DS(on)}	I _S = 1 mA, V _D = + 3.5 V	Room Full	120		170 250		170 200	Ω
On-Resistance Match	ΔR _{ON}	I _S = 1 mA, V _D = + 3.5 V	Room Full	3		5 12		5 10	
Switch Off Leakage Current (for 14 pin TSSOP)	I _{S(off)}	V ₊ = 5.5 V, V ₋ = 0 V V _D = 1 V/4.5 V, V _S = 4.5 V/1 V	Room Full	± 0.01	- 0.1 - 18	0.1 18	- 0.1 - 0.5	0.1 0.5	nA
	I _{D(off)}		Room Full	± 0.01	- 0.1 - 18	0.1 18	- 0.1 - 0.5	0.1 0.5	
Channel On Leakage Current (for 14 pin TSSOP)	I _{D(on)}	V ₊ = 5.5 V, V ₋ = 0 V V _S = V _D = 1 V/4.5 V	Room Full	± 0.01	- 0.1 - 18	0.1 18	- 0.1 - 0.5	0.1 0.5	
Switch Off Leakage Current (for 16 pin miniQFN)	I _{S(off)}	V ₊ = 5.5 V, V ₋ = 0 V V _D = 1 V/4.5 V, V _S = 4.5 V/1 V	Room Full	± 0.01	- 1 - 18	1 18	- 1 - 2	1 2	
	I _{D(off)}		Room Full	± 0.01	- 1 - 18	1 18	- 1 - 2	1 2	
Channel On Leakage Current (for 16 pin miniQFN)	I _{D(on)}	V ₊ = 5.5 V, V ₋ = 0 V, V _S = V _D = 1 V/4.5 V	Room Full	± 0.01	- 1 - 18	1 18	- 1 - 2	1 2	
Digital Control									
Input Current, V _{IN} Low	I _L	V _{IN} A0, A1 and ENABLE Under Test = 0.8 V	Full	0.005	- 0.1	0.1	- 0.1	0.1	μA
Input Current, V _{IN} High	I _H	V _{IN} A0, A1 and ENABLE Under Test = 2.0 V	Full	0.005	- 0.1	0.1	- 0.1	0.1	
Input Capacitance	C _{IN}	f = 1 MHz	Room	4.3					pF
Dynamic Characteristics									
Transition Time	t _{TRANS}	V _{S(CLOSE)} = 3 V, V _{S(OPEN)} = 0.0 V, R _L = 300 Ω, C _L = 35 pF	Room Full	36		75 120		75 95	ns
Enable Turn-On Time	t _{ON(EN)}		Room Full	30		70 102		70 80	
Enable Turn-Off Time	t _{OFF(EN)}		Room Full	17		47 88		47 63	
Break-Before-Make-Time	t _{BMM}		Room Full	23	5		5		
Charge Injection	Q	C _L = 1 nF, R _{GEN} = 0 Ω, V _{GEN} = 0 V	Full	0.1					pC
Off-Isolation ^e	OIRR	f = 10 MHz, R _L = 50 Ω, C _L = 5 pF	Room	- 58					dB
Crosstalk ^e	X _{TALK}		Room	- 81					
Bandwidth ^e	BW	R _L = 50 Ω	Room	520					MHz

SPECIFICATIONS FOR SINGLE SUPPLY

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 5 V, V- = 0 V VIN A0, A1 and ENABLE = 2.0 V, 0.8 V ^a	Temp. ^b	Typ. ^c	- 40 °C to 125 °C		- 40 °C to 85 °C		Unit
					Min. ^d	Max. ^d	Min. ^d	Max. ^d	
Dynamic Characteristics									
Total Harmonic Distortion	THD	Signal = 1 V _{RMS} , 20 Hz to 20 kHz, R _L = 600 Ω	Room	0.009					%
Source Off Capacitance ^e	C _{S(off)}	f = 1 MHz	Room	2.5					pF
Drain Off Capacitance ^e	C _{D(off)}			6.4					
Channel On Capacitance ^e	C _{D(on)}			11.3					
Power Supplies									
Power Supply Current	I+	V _{IN} = 0 V, or V+	Room Full	0.001		0.5 1		0.5 1	μA
Negative Supply Current	I-		Room Full	- 0.001	- 0.5 - 1		- 0.5 - 1		
Ground Current	I _{GND}		Room Full	- 0.001	- 0.5 - 1		- 0.5 - 1		

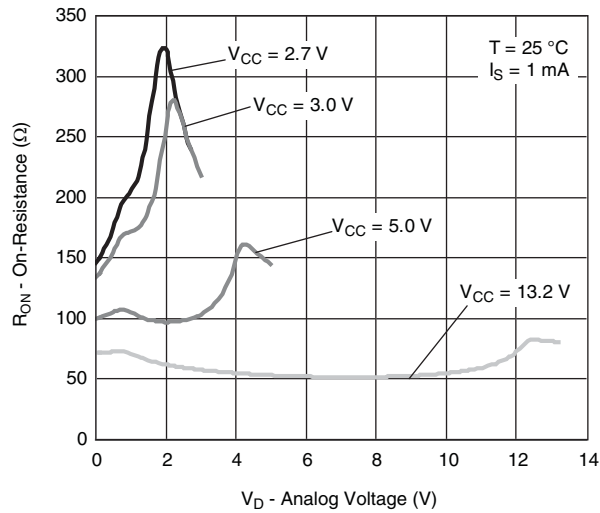
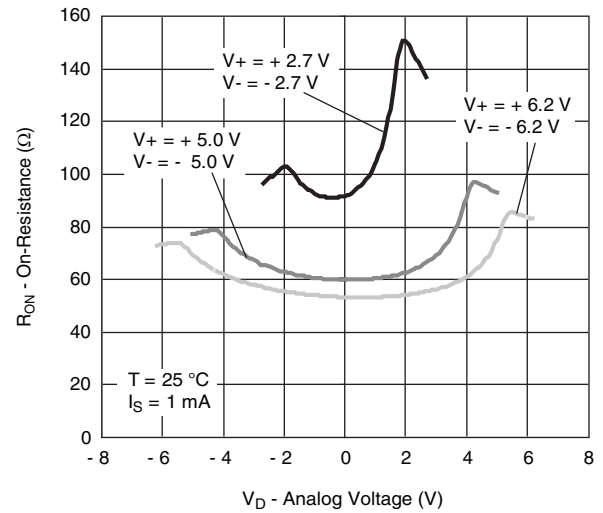
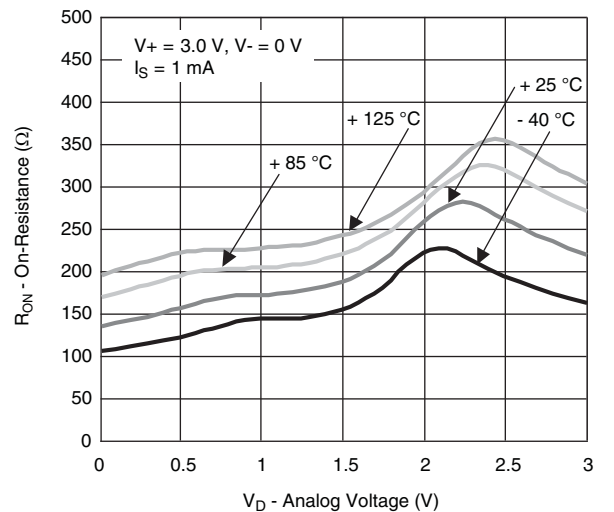
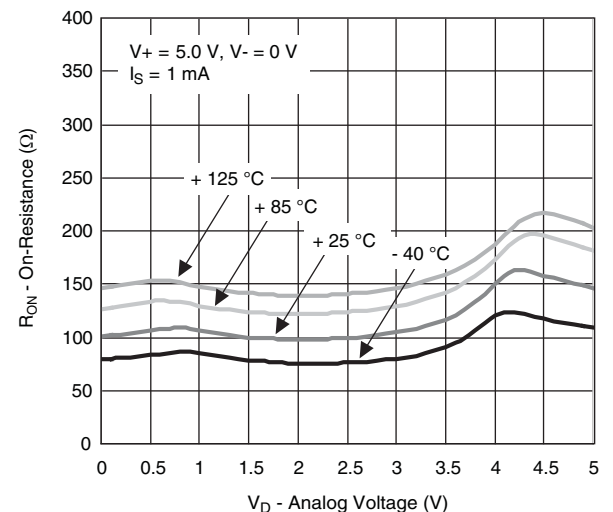
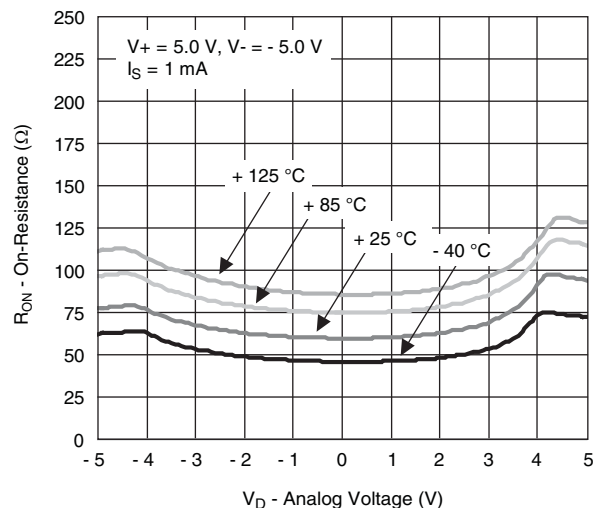
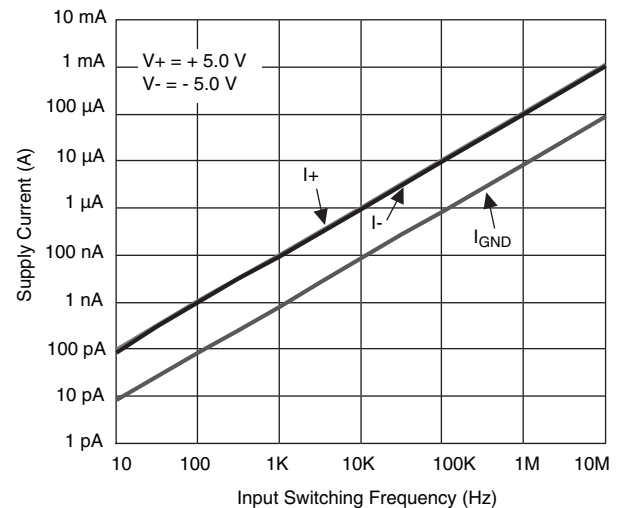
SPECIFICATIONS FOR SINGLE SUPPLY

Parameter	Symbol	Test Conditions Unless Otherwise Specified V ₊ = 3 V, V ₋ = 0 V V _{IN} A0, A1 and ENABLE = 1.4 V, 0.6 V ^a	Temp. ^b	Typ. ^c	- 40 °C to + 125 °C		- 40 °C to + 85 °C		Unit
					Min. ^d	Max. ^d	Min. ^d	Max. ^d	
Analog Switch									
Analog Signal Range ^e	V _{ANALOG}		Full			3		3	V
On-Resistance	R _{DS(ON)}	I _S = 1 mA, V _D = + 1.5 V	Room Full	200		245 325		245 290	Ω
On-Resistance Match	ΔR _{ON}	I _S = 1 mA, V _D = + 1.5 V	Room Full	5		6 13		11 6	
Switch Off Leakage Current (for 14 pin TSSOP)	I _{S(off)}	V ₊ = 3 V, V ₋ = 0 V V _D = 1 V/3 V, V _S = 3 V/1 V	Room Full	± 0.01	- 0.1 - 18	0.1 18	- 0.1 - 0.5	0.1 0.5	nA
	I _{D(off)}		Room Full	± 0.01	- 0.1 - 18	0.1 18	- 0.1 - 0.5	0.1 0.5	
Channel On Leakage Current (for 14 pin TSSOP)	I _{D(on)}	V ₊ = 3 V, V ₋ = 0 V V _S = V _D = 1 V/3 V	Room Full	± 0.01	- 0.1 - 18	0.1 18	- 0.1 - 0.5	0.1 0.5	
Switch Off Leakage Current (for 16 pin miniQFN)	I _{S(off)}	V ₊ = 3.3 V, V ₋ = 0 V V _D = 1 V/3 V, V _S = 3 V/1 V	Room Full	± 0.01	- 1 - 18	1 18	- 1 - 2	1 2	
	I _{D(off)}		Room Full	± 0.01	- 1 - 18	1 18	- 1 - 2	1 2	
Channel On Leakage Current (for 16 pin miniQFN)	I _{D(on)}	V ₊ = 3.3 V, V ₋ = 0 V, V _S = V _D = 1 V/3 V	Room Full	± 0.01	- 1 - 18	1 18	- 1 - 2	1 2	
Digital Control									
Input Current, V _{IN} Low	I _L	V _{IN} A0, A1 and ENABLE Under Test = 0.6 V	Full	0.005	- 1	1	- 1	1	μA
Input Current, V _{IN} High	I _H	V _{IN} A0, A1 and ENABLE Under Test = 1.4 V	Full	0.005	- 1	1	- 1	1	
Input Capacitance	C _{IN}	f = 1 MHz	Room	4.3					pF

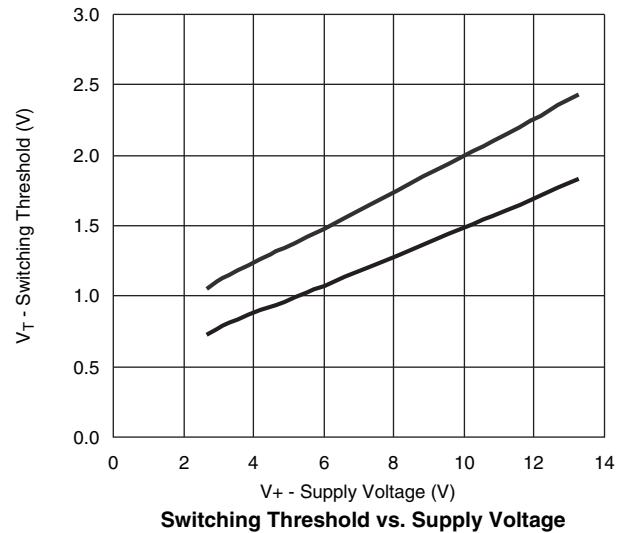
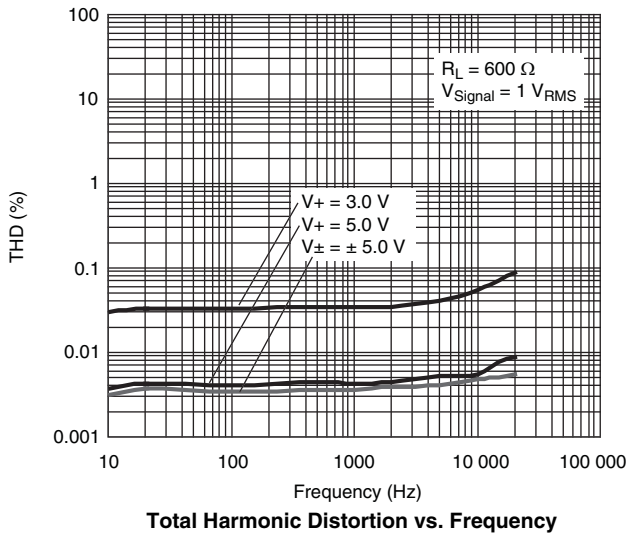
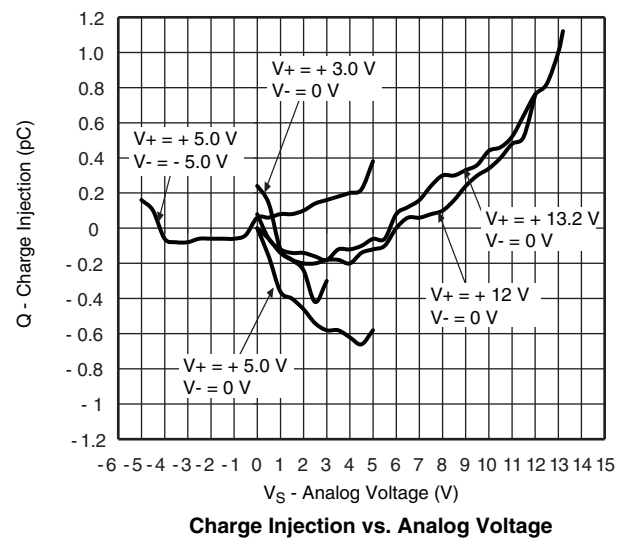
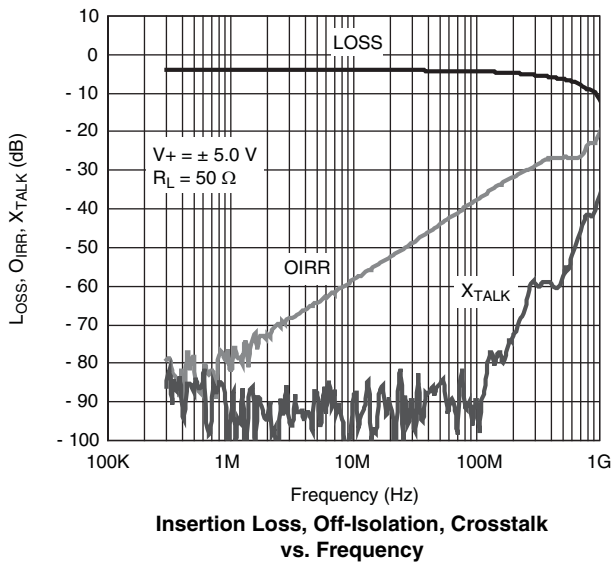
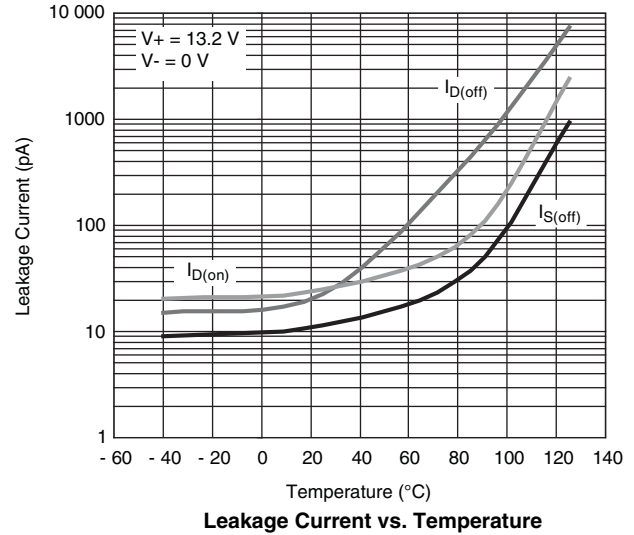
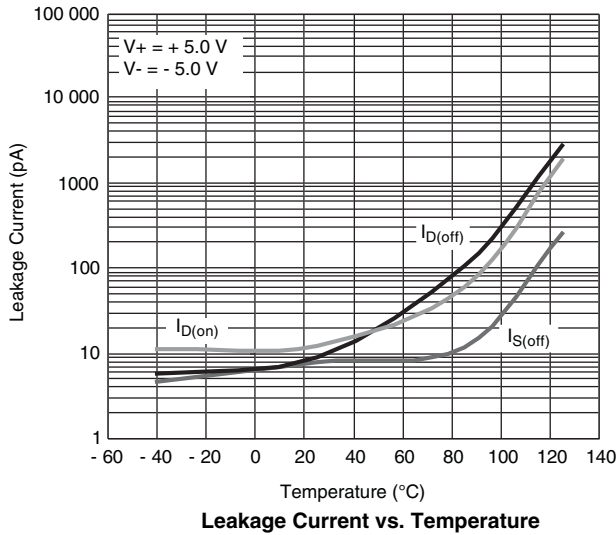
SPECIFICATIONS FOR SINGLE SUPPLY

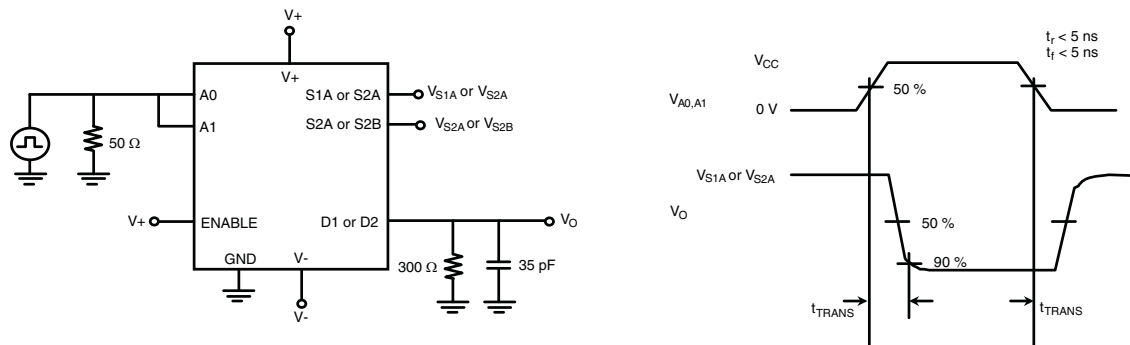
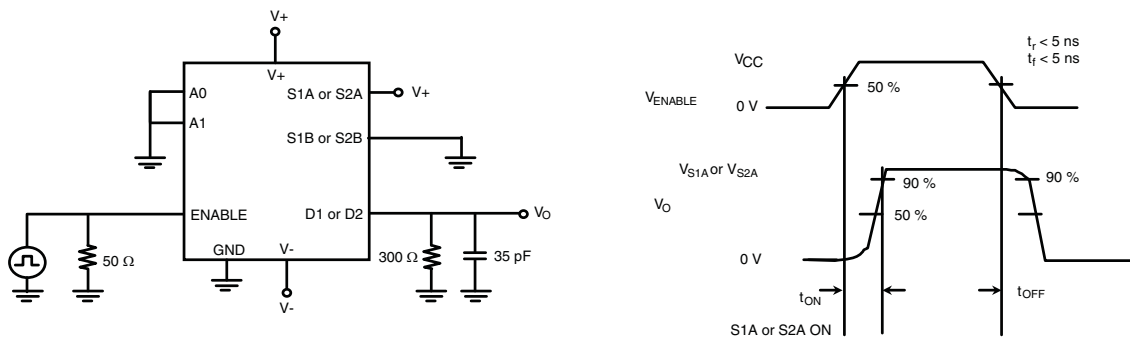
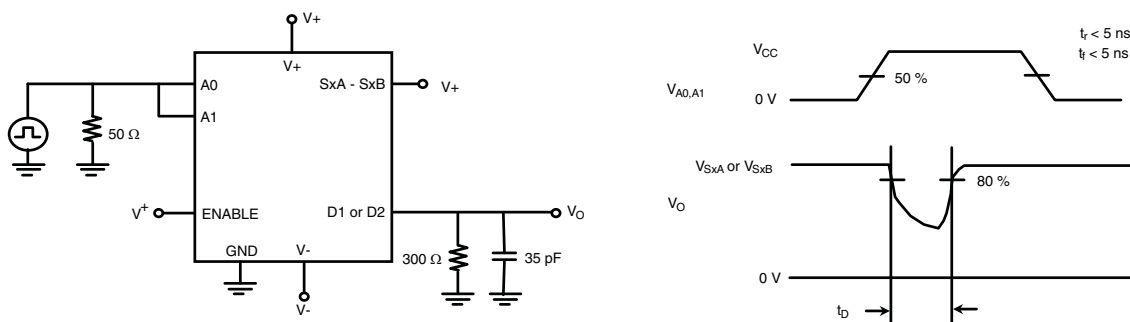
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 3 V, V- = 0 V VIN A0, A1 and ENABLE = 1.4 V, 0.6 V ^a	Temp. ^b	Typ. ^c	- 40 °C to + 125 °C		- 40 °C to + 85 °C		Unit
					Min. ^d	Max. ^d	Min. ^d	Max. ^d	
Dynamic Characteristics									
Transition Time	t _{TRANS}	V _{S(CLOSE)} = 3.0 V, V _{S(OPEN)} = 0.0 V, R _L = 300 Ω, C _L = 35 pF	Room Full	95		130 190		130 160	ns
Enable Turn-On Time	t _{ON(EN)}		Room Full	77		108 161		108 131	
Enable Turn-Off Time	t _{OFF(EN)}		Room Full	35		76 112		76 88	
Break-Before-Make-Time	t _{BMM}		Room Full	45	5		5		
Charge Injection	Q	C _L = 1 nF, R _{GEN} = 0 Ω, V _{GEN} = 0 V	Full	0.24					pC
Off-Isolation ^e	OIRR	f = 10 MHz, R _L = 50 Ω, C _L = 5 pF	Room	- 57					dB
Crosstalk ^e	X _{TALK}		Room	- 93					
Bandwidth ^e	BW	R _L = 50 Ω	Room	442					MHz
Total Harmonic Distortion	THD	Signal = 1 V _{RMS} , 20 Hz to 20 kHz, R _L = 600 Ω	Room	0.09					%
Source Off Capacitance ^e	C _{S(off)}	f = 1 MHz	Room	2.5					pF
Drain Off Capacitance ^e	C _{D(off)}			6.4					
Channel On Capacitance ^e	C _{D(on)}			11.7					
Power Supplies									
Power Supply Current	I+	V _{IN} = 0 V, or V+	Room Full	0.001		0.5 1		0.5 1	μA
Negative Supply Current	I-		Room Full	- 0.001	- 0.5 - 1		- 0.5 - 1		
Ground Current	I _{GND}		Room Full	- 0.001	- 0.5 - 1		- 0.5 - 1		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

On-Resistance vs. V_D (Single Supply Voltage)

On-Resistance vs. V_D (Dual Supply Voltage)

On-Resistance vs. Analog Voltage and Temperature

On-Resistance vs. Analog Voltage and Temperature

On-Resistance vs. Analog Voltage and Temperature

Supply Current vs. Input Switching Frequency

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



TEST CIRCUITS

Figure 1. Transition Time

Figure 2. Enable Switching Time

Figure 3. Break-Before-Make

TEST CIRCUITS

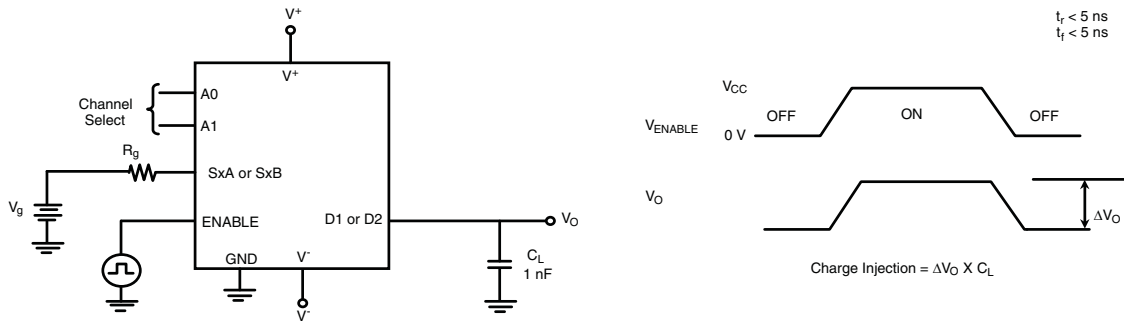


Figure 4. Charge Injection

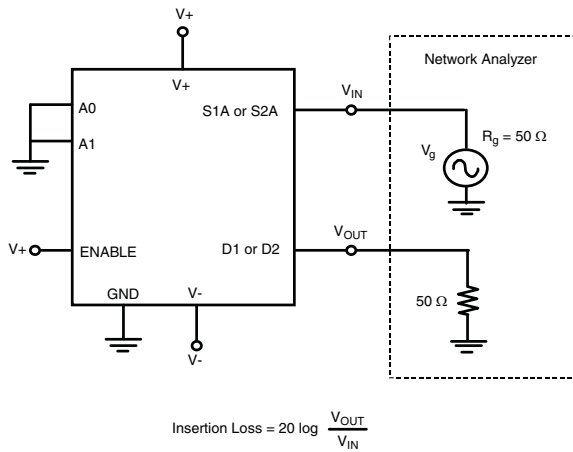


Figure 5. Insertion Loss

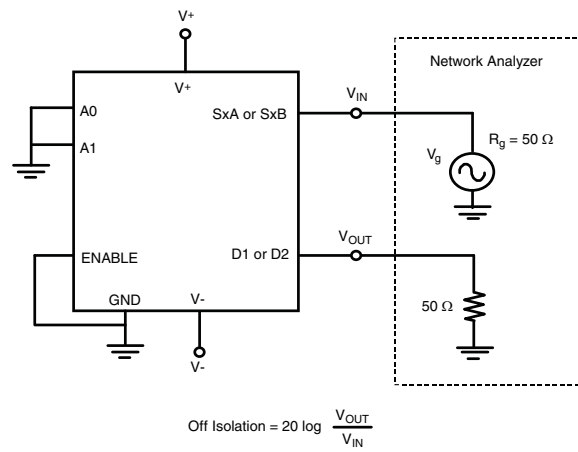


Figure 6. Off-Isolation

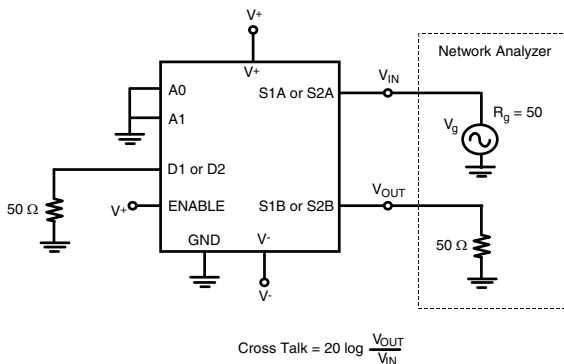


Figure 7. Crosstalk

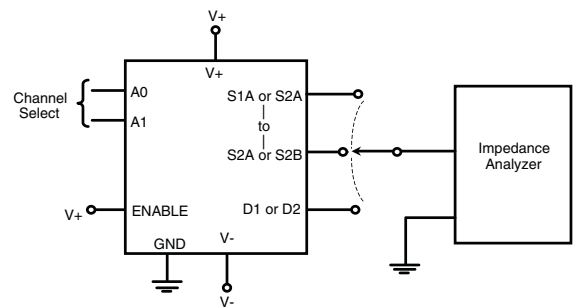
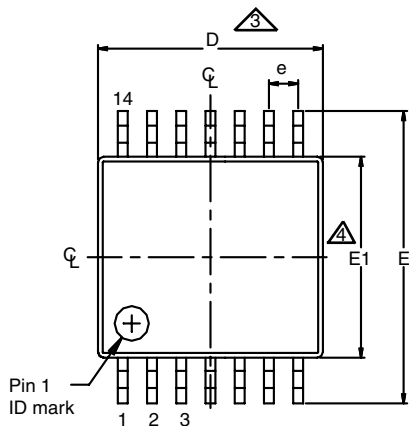


Figure 8. Source/Drain Capacitance

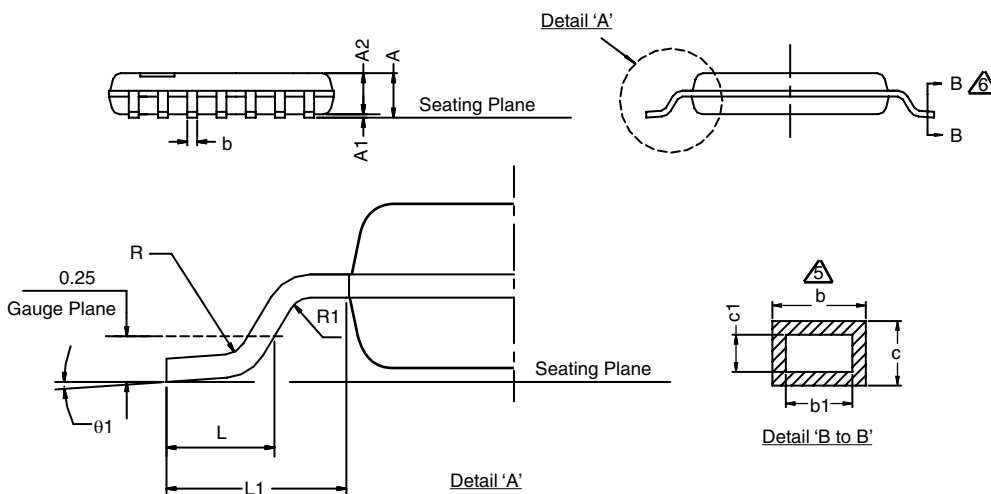
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg269901.

14L TSSOP



Notes:

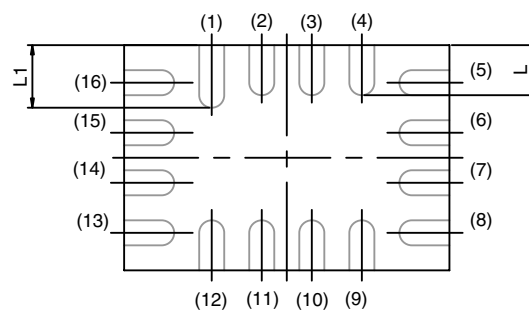
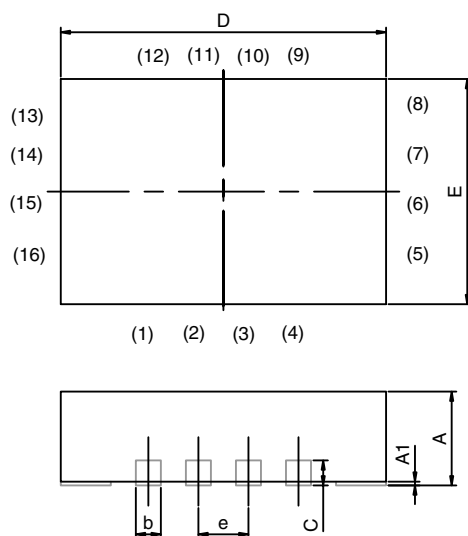
1. All dimensions are in millimeters (angles in degrees)
2. Dimensioning and tolerancing per ANSI Y14.5M-1982
3. Dimension 'D' does not include mold flash, protrusions or gate burrs
4. Dimension 'E1' does not include internal flash or protrusion
5. Dimension 'b' does not include dambar protrusion
6. Cross section B to B to be determined at 0.10 mm to 0.25 mm from the lead tip



SYMBOL	MINIMUM	NOMINAL	MAXIMUM
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	0.90	1.05
D	4.9	5.0	5.1
E1	4.3	4.4	4.5
E	6.2	6.4	6.6
L	0.45	0.60	0.75
R	0.09	-	-
R1	0.09	-	-
b	0.19	-	0.30
b1	0.19	0.22	0.25
c	0.09	-	0.20
c1	0.09	-	0.16
θ1	0°	-	8°
L1		1.0 ref.	
e		0.65 BSC	

ECN: T-07766-Rev. A, 14-Jan-08
DWG: 5962

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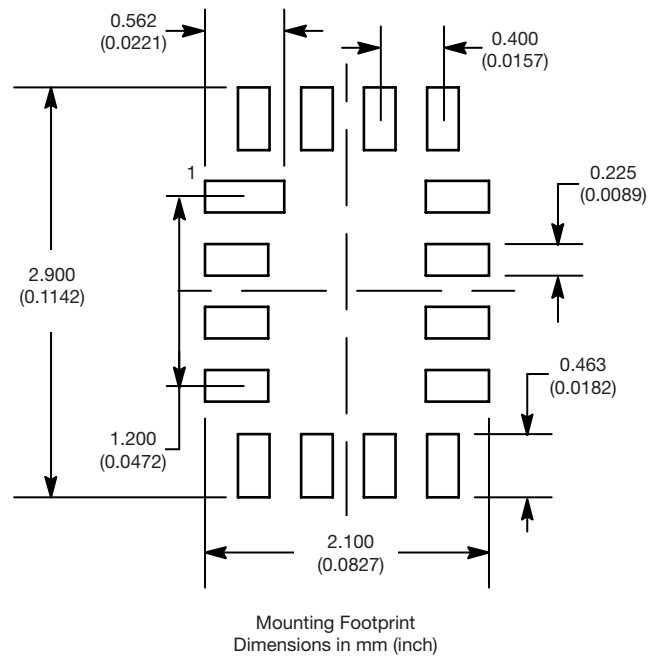


BACK SIDE VIEW

DIM	MILLIMETERS			INCHES		
	MIN.	NAM	MAX.	MIN.	NAM	MAX.
A	0.70	0.75	0.80	0.0275	0.0295	0.0315
A1	0	-	0.05	0	-	0.002
b	0.15	0.20	0.25	0.0059	0.0078	0.0098
C	0.15	0.20	0.25	0.0059	0.0078	0.0098
D	2.60 BSC			0.1023 BSC		
E	1.80 BSC			0.0708 BSC		
e	0.40 BSC			0.0157 BSC		
L	0.35	0.40	0.45	0.0137	0.0157	0.0177
L1	0.45	0.50	0.55	0.0177	0.0196	0.0216

ECN T-06380-Rev. A, 14-Aug-06
DWG: 5954

RECOMMENDED MINIMUM PADS FOR MINI QFN 16L





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