

Low-Voltage Single SPDT Analog Switch

DESCRIPTION

The DG9411 is a single-pole/double-throw monolithic CMOS analog switch designed for high performance switching of analog signals. Combining low power, high speed (t_{ON} : 9 ns, t_{OFF} : 5 ns), low on-resistance ($r_{DS(on)}$: 7 Ω) and small physical size (SC70), the DG9411 is ideal for portable and battery powered applications requiring high performance and efficient use of board space.

The DG9411 is built on Vishay Siliconix's low voltage J12 process. An epitaxial layer prevents latchup. Break-before-make is guaranteed for DG9411.

Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

FEATURES

- Low voltage operation (2.25 V to 5.5 V)
- Low on-resistance - $r_{DS(on)}$: 7 Ω
- Fast switching - t_{ON} : 9 ns, t_{OFF} : 5 ns
- Low charge injection - Q_{INJ} : 5 pC
- Low power consumption
- TTL/CMOS compatible
- 6-Pin SC70 package



Available
RoHS*
COMPLIANT

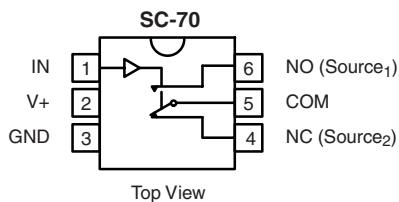
BENEFITS

- Reduced power consumption
- Simple logic interface
- High accuracy
- Reduce board space

APPLICATIONS

- Cellular phones
- Communication systems
- Portable test equipment
- Battery operated systems
- Sample and hold circuits

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Device Marking
● 4Dx or
● 4Dxy

TRUTH TABLE

Logic	NC	NO
0	ON	OFF
1	OFF	ON

Logic "0" \leq 0.8 V

Logic "1" \geq 2.4 V

ORDERING INFORMATION

Temp Range	Package	Part Number
- 40 to 85 °C	SC70-6	DG9411DL-T1 DG9411DL-T1-E3

* Pb containing terminations are not RoHS compliant, exemptions may apply.



ABSOLUTE MAXIMUM RATINGS			
Parameter		Limit	Unit
Reference V+ to GND		- 0.3 to + 6	V
IN, COM, NC, NO ^a		- 0.3 to (V+ + 0.3)	
Continuous Current (Any Terminal)		± 50	mA
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 200	
Storage Temperature		- 65 to 150	°C
Power Dissipation (Packages) ^b	6-Pin SC70 ^c	250	mW

Notes:

- a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC Board.
- c. Derate 3.1 mW/°C above 70 °C.

SPECIFICATIONS V+ = 2.5 V							
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 2.5 V, ± 10 % VIN = 0.4 or 2.0 V ^e	Temp ^a	Limits - 40 to 85 °C			Unit
				Min ^b	Typ ^c	Max ^b	
Analog Switch							
Analog Signal Range ^d	V _{NO} , V _{NC} V _{COM}		Full	0		V+	V
Drain-Source On-Resistance	r _{DS(on)}	V+ = 2.25 V, V _D = 1.0 V, I _S = 10 mA	Room Full ^d		26 29	35 40	Ω
r _{DS(on)} Flatness ^d	r _{DS(on)} Flatness	V+ = 2.5 V	Room		10		
Switch Off Leakage Current ^f	I _{S(off)}	V+ = 2.75 V, V _S = 0.5 V/1.5 V, V _D = 1.5 V/0.5 V	Room Full ^d	- 250 - 3.0		250 3.0	pA nA
	I _{D(off)}		Room Full ^d	- 250 - 3.0		250 3.0	pA nA
Channel-On Leakage Current ^f	I _{D(on)}	V+ = 2.75 V, V _S = V _D = 0.5 V/1.5 V	Room Full ^d	- 250 - 3.0		250 3.0	pA nA
Digital Control							
Input High Voltage	V _{INH}		Full	2			V
Input Low Voltage	V _{INL}		Full			0.4	
Input Capacitance ^d	C _{in}		Full		3		pF
Input Current	I _{INL} or I _{INH}	V _{IN} = 0 or V+	Full	- 1		1	μA
Dynamic Characteristics							
Turn-On Time	t _{ON}	V _D or V _S = 1.5 V, R _L = 300 Ω, C _L = 35 pF Figures 1 and 2	Room Full ^d		16	40 45	ns
Turn-Off Time	t _{OFF}		Room Full		7	23 28	
Break-Before-Make Time	t _d		Room ^d	1	12		
Charge Injection ^d	Q _{INJ}	C _L = 1 nF, V _{GEN} = 0 V, V _S = 0 V, R _{GEN} = 0 Ω, Figure 3	Room		5	10	pC
Off-Isolation ^d	OIRR	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz	Room		- 73		dB
Crosstalk ^d	X _{TALK}		Room		- 70		
Source-Off Capacitance ^d	C _{S(off)}	V _{IN} = 0 or V+, f = 1 MHz	Room		7		pF
Channel-On Capacitance ^d	C _{D(on)}		Room		20		
Drain-to-Source Capacitance ^d	C _{DS(off)}		Room		20		
Power Supply							
Power Supply Range	V+			2.25		2.75	V
Power Supply Current ^d	I+	V _{IN} = 0 or V+			0.01	1.0	μA
Power Consumption	P _C						0.3



SPECIFICATIONS $V_+ = 3\text{ V}$							
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 3\text{ V}, \pm 10\%$ $V_{IN} = 0.4\text{ or }2.0\text{ V}^e$	Temp ^a	Limits - 40 to 85 °C			Unit
				Min ^b	Typ ^c	Max ^b	
Analog Switch							
Analog Signal Range ^d	V_{NO}, V_{NC} V_{COM}		Full	0		V_+	V
Drain-Source On-Resistance ^d	$r_{DS(on)}$	$V_+ = 2.7\text{ V}, V_D = 1.5\text{ V}, I_S = 10\text{ mA}$	Room Full		15 19	25 30	Ω
$r_{DS(on)}$ Flatness ^d	$r_{DS(on)}$ Flatness	$V_S = 0\text{ to }V_+, I_S = 10\text{ mA}$	Room		7.5		
Switch Off Leakage Current ^f	$I_{S(off)}$	$V_+ = 3.3\text{ V}, V_S = 1\text{ V}/3\text{ V}, V_D = 3\text{ V}/1\text{ V}$	Room Full	- 500 - 4.0		500 4.0	pA nA
	$I_{D(off)}$		Room Full	- 500 - 4.0		500 4.0	pA nA
Channel-On Leakage Current ^f	$I_{D(on)}$	$V_+ = 3.3\text{ V}, V_S = V_D = 1\text{ V}/3\text{ V}$	Room Full	- 500 - 4.0		500 4.0	pA nA
Digital Control							
Input High Voltage	V_{INH}		Full	2			V
Input Low Voltage	V_{INL}		Full			0.8	
Input Capacitance ^d	C_{in}		Full		3		pF
Input Current	I_{INL} or I_{INH}	$V_{IN} = 0\text{ or }V_+$	Full	- 1		1	μA
Dynamic Characteristics							
Turn-On Time ^d	t_{ON}	$V_D\text{ or }V_S = 2.0\text{ V}, R_L = 300\ \Omega, C_L = 35\text{ pF}$ Figures 1 and 2	Room Full		12	15 20	ns
Turn-Off Time ^d	t_{OFF}		Room Full		6	8 10	
Break-Before-Make Time ^d	t_d		Room	1	7		
Charge Injection ^d	Q_{INJ}	$C_L = 1\text{ nF}, V_{GEN} = 0\text{ V}, V_S = 0\text{ V}, R_{GEN} = 0\ \Omega,$ Figure 3	Room		5	10	pC
Off-Isolation ^d	OIRR	$R_L = 50\ \Omega, C_L = 5\text{ pF}, f = 1\text{ MHz}$	Room		- 73		dB
Crosstalk ^d	X_{TALK}		Room		- 70		
Source-Off Capacitance ^d	$C_{S(off)}$	$V_{IN} = 0\text{ or }V_+, f = 1\text{ MHz}$	Room		7		pF
Channel-On Capacitance ^d	$C_{D(on)}$		Room		20		
Drain-to-Source Capacitance ^d	$C_{DS(off)}$		Room		20		
Power Supply							
Power Supply Range	V_+			2.7		3.3	V
Power Supply Current	I_+	$V_{IN} = 0\text{ or }V_+$			0.01	1.0	μA
Power Consumption	P_C						0.4



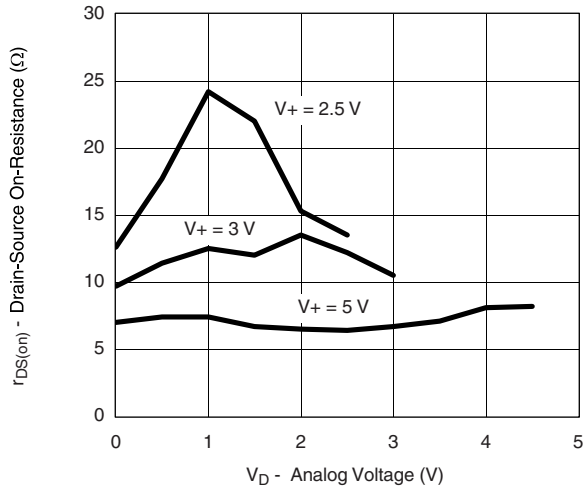
SPECIFICATIONS $V_+ = 5\text{ V}$							
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 5\text{ V}, \pm 10\%$ $V_{IN} = 0.8\text{ or }2.4\text{ V}^e$	Temp ^a	Limits - 40 to 85 °C			Unit
				Min ^b	Typ ^c	Max ^b	
Analog Switch							
Analog Signal Range ^d	V_{NO}, V_{NC} V_{COM}		Full	0		V_+	V
Drain-Source On-Resistance	$r_{DS(on)}$	$V_+ = 4.5\text{ V}, V_D = 3\text{ V}, I_S = 10\text{ mA}$	Room Full		7 10	12 16	Ω
$r_{DS(on)}$ Flatness ^d	$r_{DS(on)}$ Flatness	$V_+ = 2.5\text{ V}$	Room		2		
Switch Off Leakage Current	$I_{S(off)}$	$V_+ = 5.5\text{ V}, V_S = 1\text{ V}/4.5\text{ V}, V_D = 4.5\text{ V}/1\text{ V}$	Room Full	- 1.0 - 4.0		1.0 4.0	nA
	$I_{D(off)}$		Room Full	- 1.0 - 4.0		1.0 4.0	
Channel-On Leakage Current	$I_{D(on)}$	$V_+ = 5.5\text{ V}, V_S = V_D = 1\text{ V}/4.5\text{ V}$	Room Full	- 1.0 - 3.0		1.0 4.5	
Digital Control							
Input High Voltage	V_{INH}		Full	2.4			V
Input Low Voltage	V_{INL}		Full			0.8	
Input Capacitance	C_{in}		Full		3		pF
Input Current	I_{INL} or I_{INH}	$V_{IN} = 0$ or V_+	Full	- 1		1	μA
Dynamic Characteristics							
Turn-On Time ^d	t_{ON}	V_D or $V_S = 3\text{ V}, R_L = 300\ \Omega, C_L = 35\text{ pF}$ Figure 1 and 2	Room Full		9 11	15	ns
Turn-Off Time ^d	t_{OFF}		Room Full		5 7	9	
Break-Before-Make Time ^d	t_d		Room	1	4		
Charge Injection ^d	Q_{INJ}	$C_L = 1\text{ nF}, V_S = 0\text{ V}, V_{GEN} = 0\text{ V}, R_{GEN} = 0\ \Omega$ Figure 3	Room		5	10	pC
Off-Isolation ^d	OIRR	$R_L = 50\ \Omega, C_L = 5\text{ pF}, f = 1\text{ MHz}$	Room		- 73		dB
Crosstalk ^d	X_{TALK}		Room		- 70		
Source-Off Capacitance ^d	$C_{S(off)}$	$V_{IN} = 0$ or $V_+, f = 1\text{ MHz}$	Room		7		pF
Channel-On Capacitance ^d	$C_{D(on)}$		Room		20		
Drain-to-Source Capacitance ^d	$C_{DS(off)}$		Room		20		
Power Supply							
Power Supply Range	V_+			4.5		5.5	V
Power Supply Current	I_+	$V_{IN} = 0$ or V_+			0.01	1.0	μA
Power Consumption	P_C						0.6

Notes:

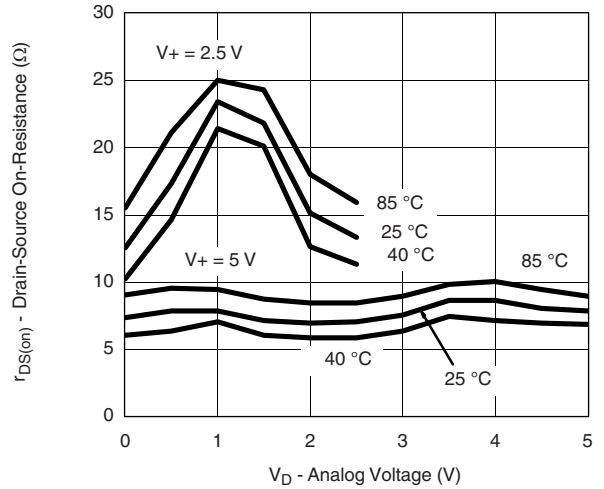
- Room = 25 °C, Full = as determined by the operating suffix.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
- Typical values are for design aid only, not guaranteed nor subject to production testing.
- Guarantee by design, nor subjected to production test.
- V_{IN} = input voltage to perform proper function.
- Guaranteed by 5 V leakage testing, not production tested.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

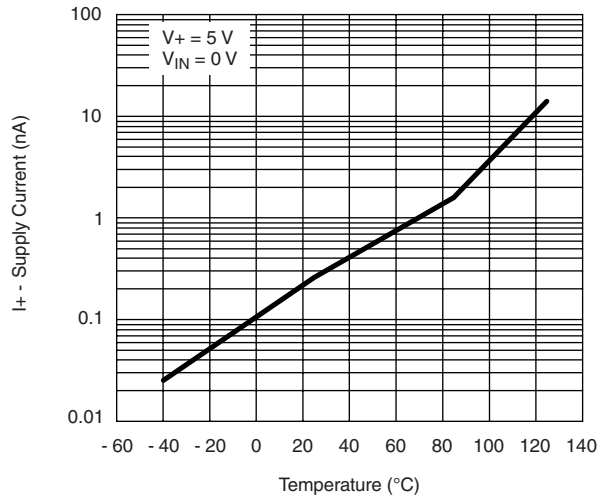
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



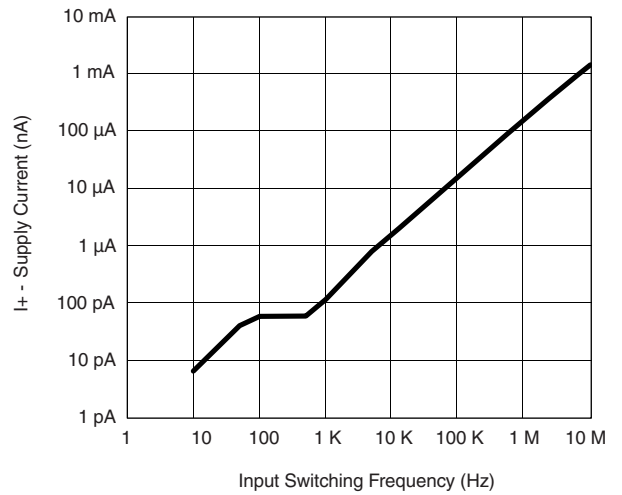
$r_{DS(on)}$ vs. Analog and Power Voltage



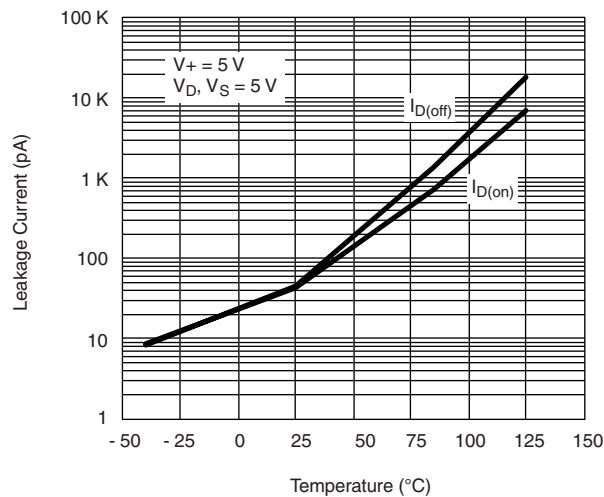
$r_{DS(on)}$ vs. Analog Voltage and Temperature



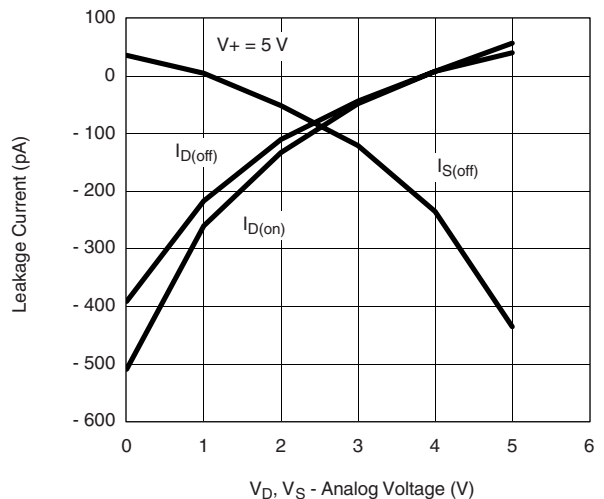
Supply Current vs. Temperature



Supply Current vs. Input Switching Frequency

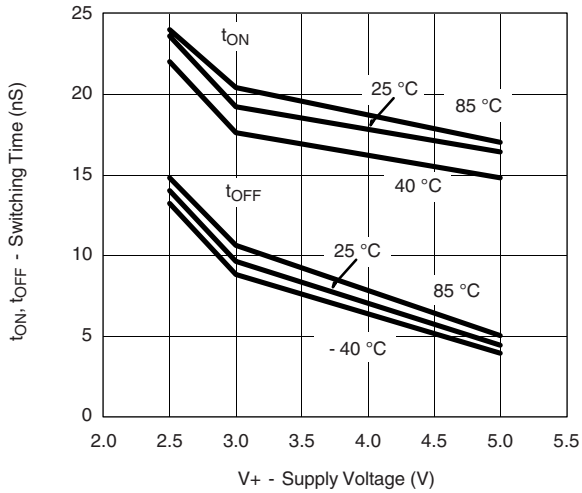


Leakage Current vs. Temperature

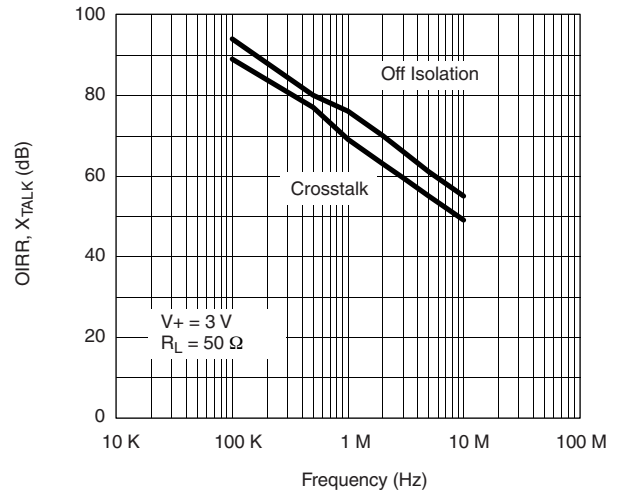


Leakage vs. Analog Voltage

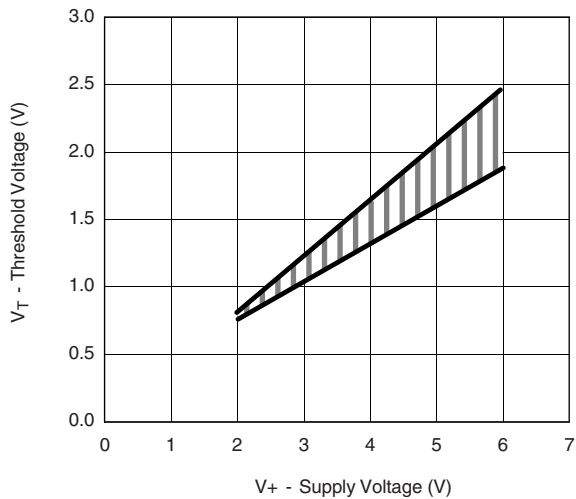
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



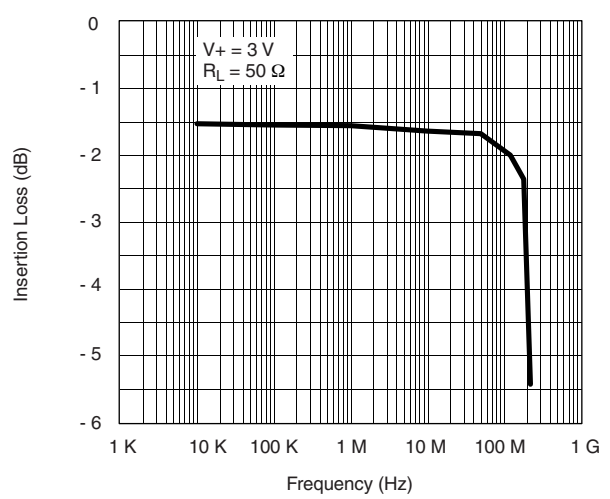
Switching Time vs. Temperature and Supply Voltage



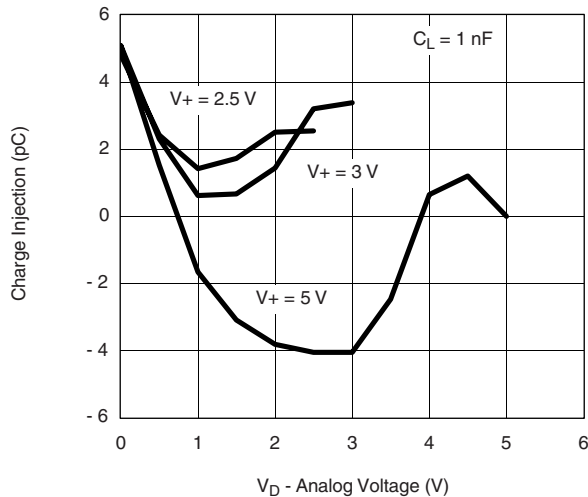
Crosstalk and Off Isolation vs. Frequency



Input Switching Threshold vs. Supply Voltage

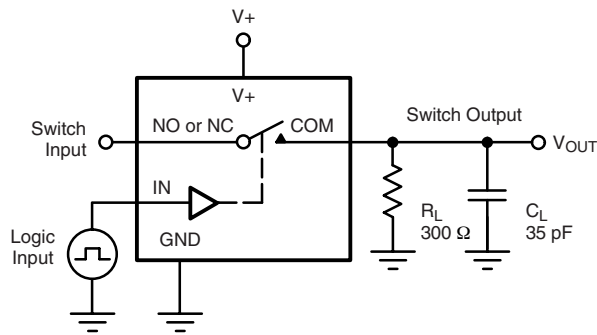


Insertion Loss vs. Frequency



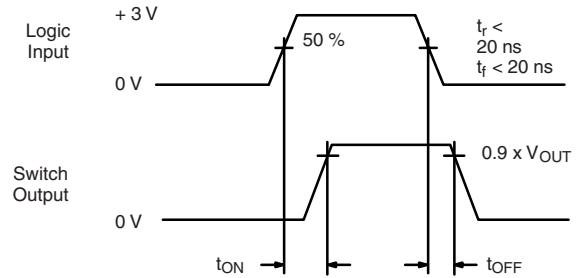
Charge Injection vs. Analog Voltage

TEST CIRCUITS



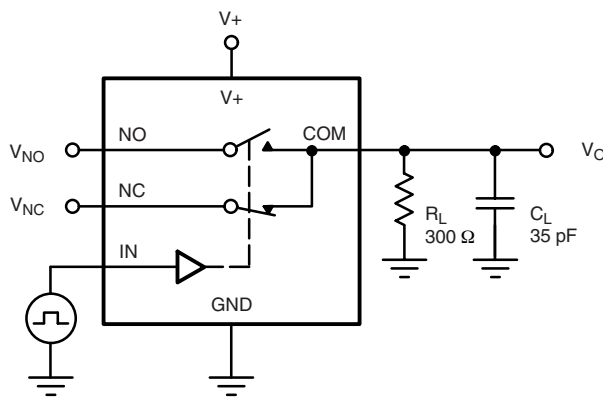
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM} \left(\frac{R_L}{R_L + R_{ON}} \right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time



C_L (includes fixture and stray capacitance)

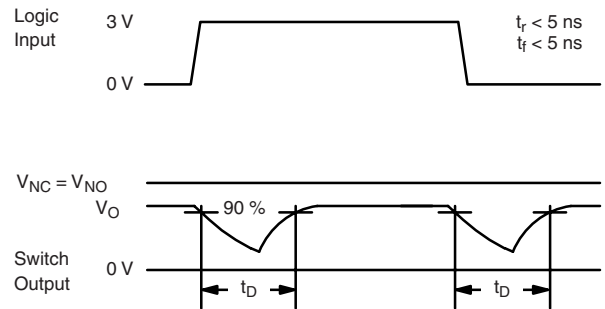
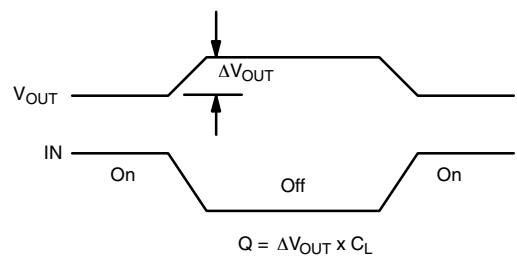
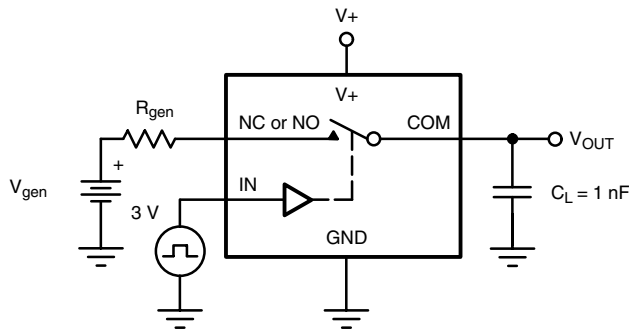


Figure 2. Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

TEST CIRCUITS

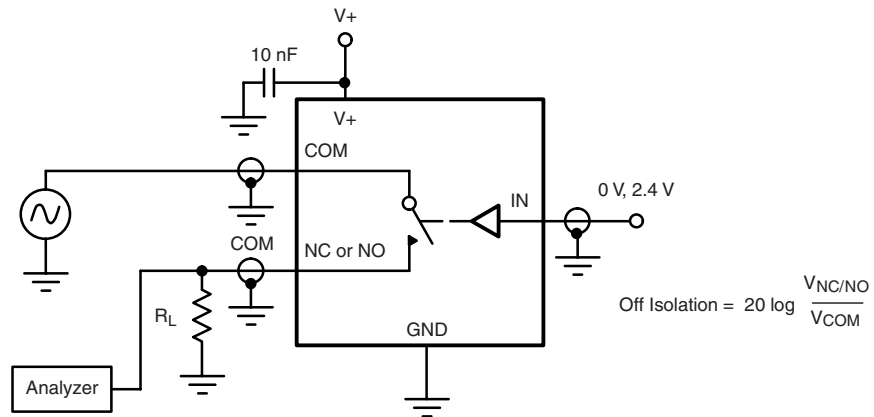


Figure 4. Off-Isolation

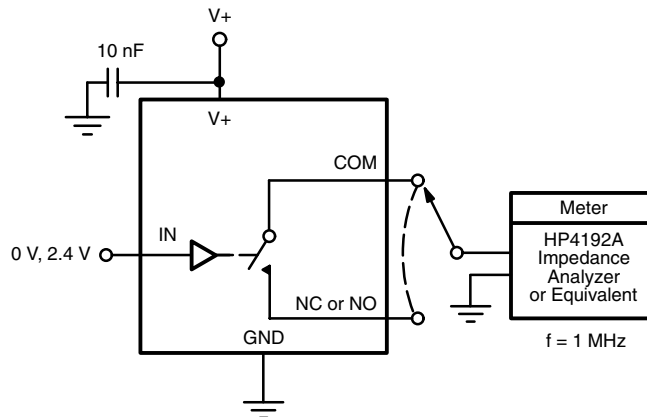
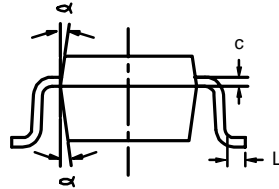
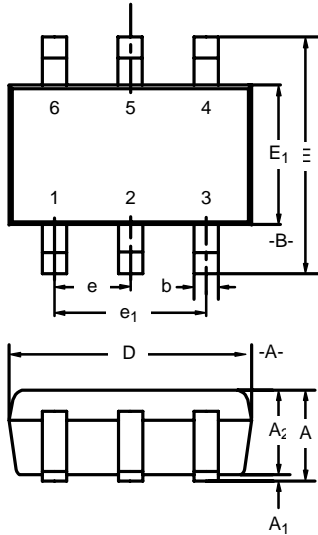


Figure 5. Channel Off/On Capacitance

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?71347>.

SC-70: 6-LEADS



Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.90	-	1.10	0.035	-	0.043
A ₁	-	-	0.10	-	-	0.004
A ₂	0.80	-	1.00	0.031	-	0.039
b	0.15	-	0.30	0.006	-	0.012
c	0.10	-	0.25	0.004	-	0.010
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E ₁	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65BSC			0.026BSC		
e ₁	1.20	1.30	1.40	0.047	0.051	0.055
L	0.10	0.20	0.30	0.004	0.008	0.012
α	7°Nom			7°Nom		

ECN: S-03946—Rev. B, 09-Jul-01
DWG: 5550



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