DLP® 0.17 HVGA DDR Series 210 DMD

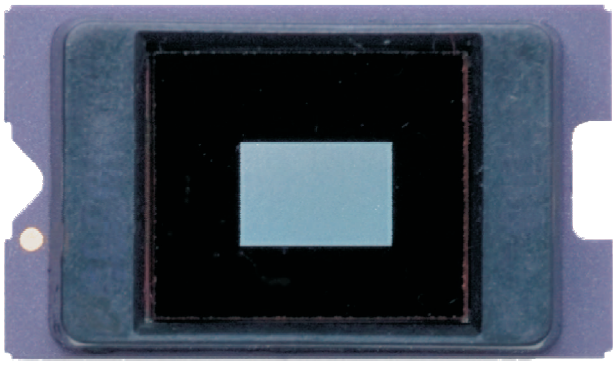
Check for Samples: DLP1700

FEATURES

- **0.17-Inch Micromirror Array Diagonal**
  - **480 × 320 Array of Aluminum, Micrometer-Sized Mirrors (Half-VGA Resolution)**
  - **7.6-µm Micromirror Pitch**
  - **±12° Micromirror Tilt Angle (Relative to Flat State)**
  - **Designed for Corner Illumination**
- **Designed for Use With Broadband Visible Light (420 nm–720 nm):**
  - **Window Transmission 97% (Single Pass, Through Two Window Surfaces)**
  - **Micromirror Reflectivity 88%**
  - **Array Diffraction Efficiency 86%**
  - **Array Fill Factor 92%**
- **10-Bit, Double Data Rate (DDR) Input Data Bus**
- **60 MHz Input Data Clock Rate**
- **Electrical Power Consumption as Low as 84 mW**
- **Built-In Reset Driver Circuitry**
- **15.5 mm by 9 mm Package Footprint**
- **Package Includes a 46-pin Board-to-Board Connector**
- **Package Mates to a PANASONIC AXK5L46347G Socket**

APPLICATIONS

- **Structured Light**
- **3D Optical Measurement Systems**
- **Augmented Reality**
- **Portable Embedded Displays**



DESCRIPTION

The DLP1700 Digital Micromirror Device (DMD) is a digitally controlled MOEMS (micro-opto-electromechanical system) spatial light modulator (SLM). When coupled to an appropriate optical system, the DLP1700 can be used to modulate the amplitude, direction, and/or phase of incoming (illumination) light.

Architecturally, the DLP1700 is a latchable, electrical-in/optical-out semiconductor device. This architecture makes the DLP1700 well suited for use in applications such as structured lighting, 3D optical metrology, augmented reality, microscopy, and spectroscopy. The compact physical size of the DLP1700 enables integration into portable equipment.

The DLP1700 is one of three components in the DLP 0.17 HVGA chip-set (see Figure 1). Proper function and operation of the DLP1700 requires that it be used in conjunction with the other components of the chip-set. Refer to DLP 0.17 HVGA chip-set data sheet (TI literature number DLPS017) for further details.

Electrically, the DLP1700 consists of a two-dimensional array of 1-bit CMOS memory cells, organized in a square grid of 480 memory cell columns by 320 memory cell rows. The CMOS memory array is written to on a column-by-column basis, over a 10-bit double data rate (DDR) bus. Row addressing is handled via a serial control bus. The specific CMOS memory access protocol is handled by the DLPC100 Digital Controller.

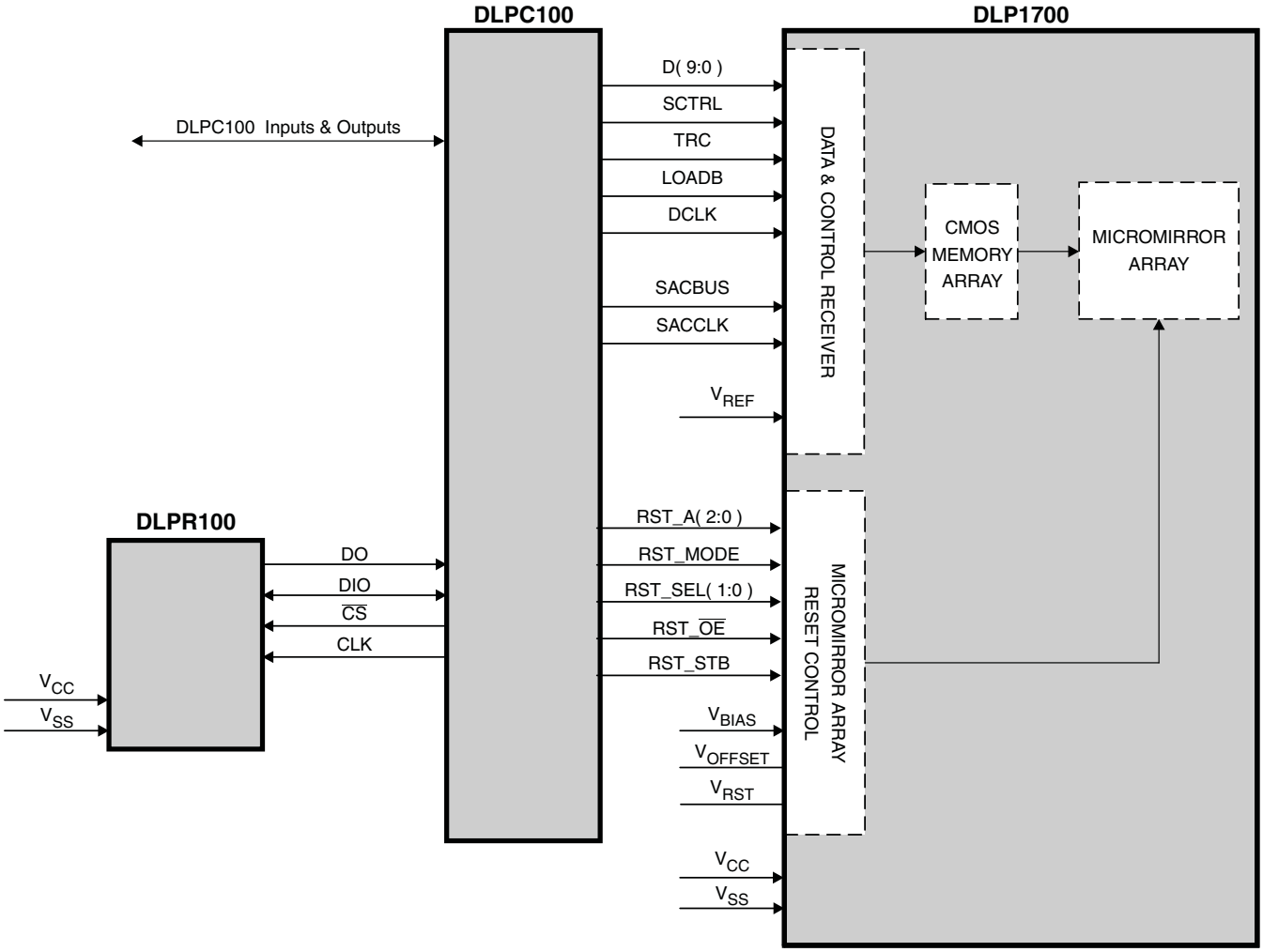


Figure 1. Block Diagram of 0.17 HVGA Chipset

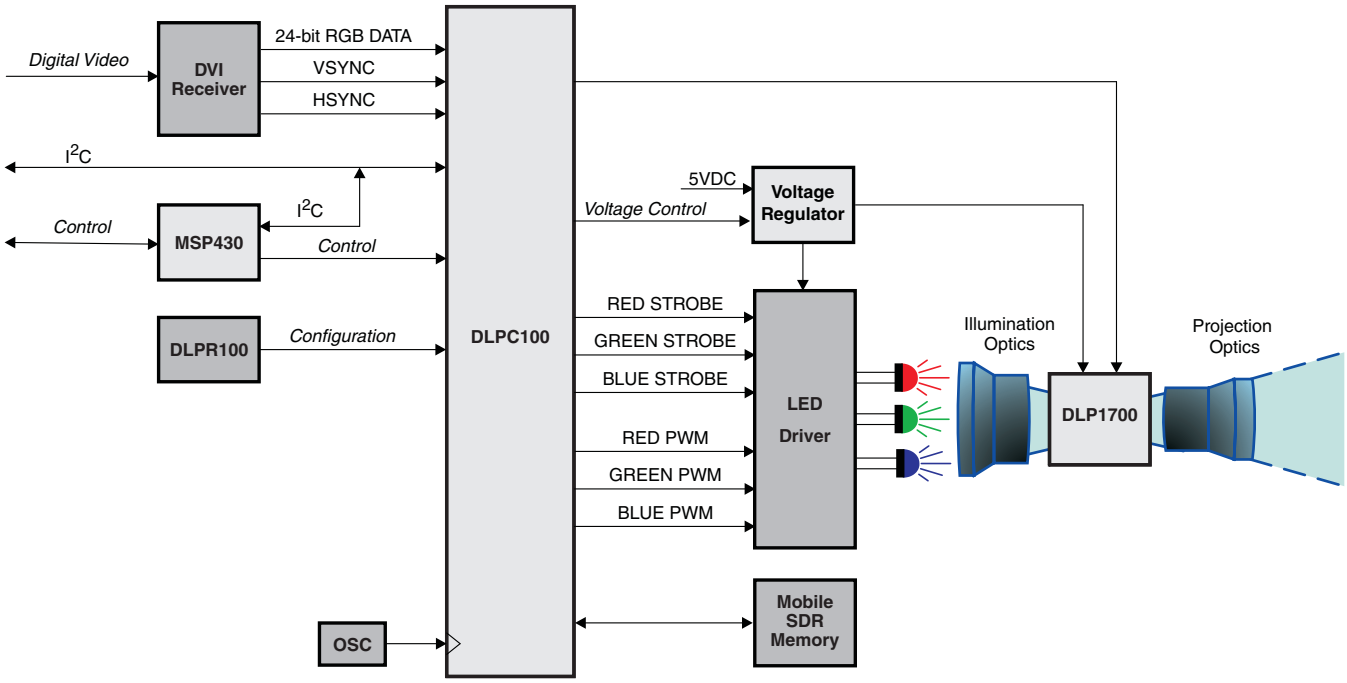


Figure 2. Typical Application

Optically, the DLP1700 consists of 153,600 highly reflective, digitally switchable, micrometer-sized mirrors ("micromirrors"), organized in a two-dimensional array of 480 micromirror columns by 320 micromirror rows (Figure 3). Each aluminum micromirror is approximately 7.6 microns in size (refer to "Micromirror Pitch" in Figure 3), and is switchable between two discrete angular positions: –12° and +12°. The angular positions are measured relative to a 0° "flat state", which is parallel to the array plane (see Figure 4). The tilt direction is perpendicular to the hinge-axis which is positioned diagonally relative to the overall array, with the "On State" landed position directed towards "Row 319, Column 0" corner of the device package (refer to "Micromirror Hinge-Axis Orientation" in Figure 3). In the field of visual displays, the 480 x 320 "pixel" resolution is referred to as "Half VGA" (HVGA).

Each individual micromirror is positioned over a corresponding CMOS memory cell. The angular position of a specific micromirror is determined by the binary state (logic 0 or 1) of the corresponding CMOS memory cell contents. Writing a logic 1 into a memory cell will result in the corresponding micromirror switching to a +12° position. Writing a logic 0 into a memory cell will result in the corresponding micromirror switching to a –12° position.

The angular position (–12° or +12°) of the individual micromirrors changes synchronously with a micromirror "clocking pulse" (rather than being synchronous with the CMOS memory cell data update). The micromirror "clocking pulse" is referred to as a Mirror Reset. Application of the Mirror Reset results in each micromirror being electro-mechanically "latched" into the angular position dictated by the contents of the corresponding CMOS memory cell.

Operationally, updating the angular position of the micromirror array consists of first updating the contents of the CMOS memory, followed by application of a Mirror Reset to all or a portion of the micromirror array (depending upon the configuration of the system). Mirror Reset pulses are generated internally by the DLP1700 DMD, with application of the pulses being coordinated by the DLPC100 controller. Refer to SWITCHING CHARACTERISTICS timing specifications.

Around the perimeter of the 480 x 320 array of micromirrors is a uniform band of "border" micromirrors. The border micromirrors are not user-addressable. The border micromirrors land in the –12° position once power has been applied to the device. There are 14 border micromirrors on each side of the 480 by 320 active array.

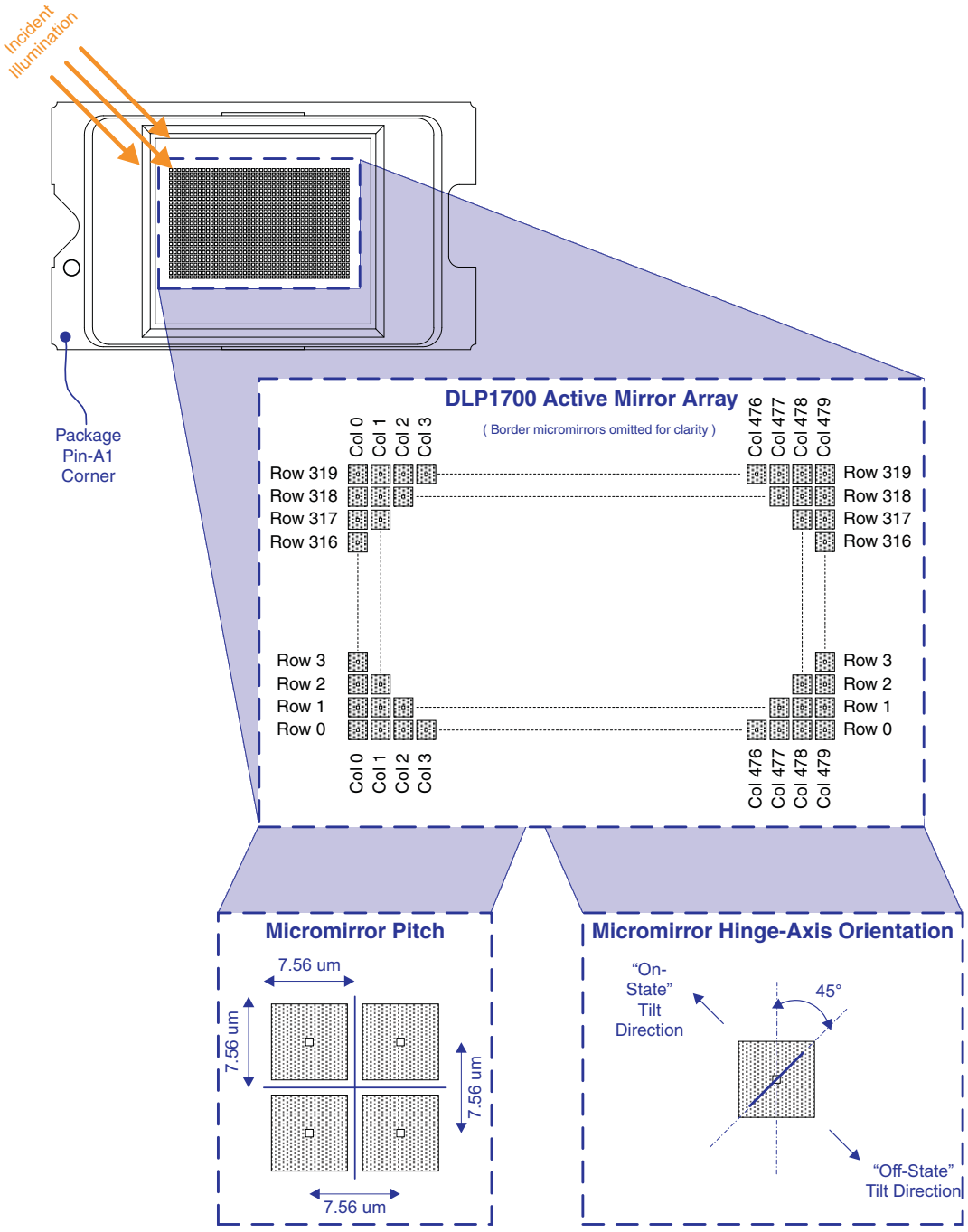


Figure 3. DMD Micromirror Array, Pitch, and Hinge-Axis Orientation

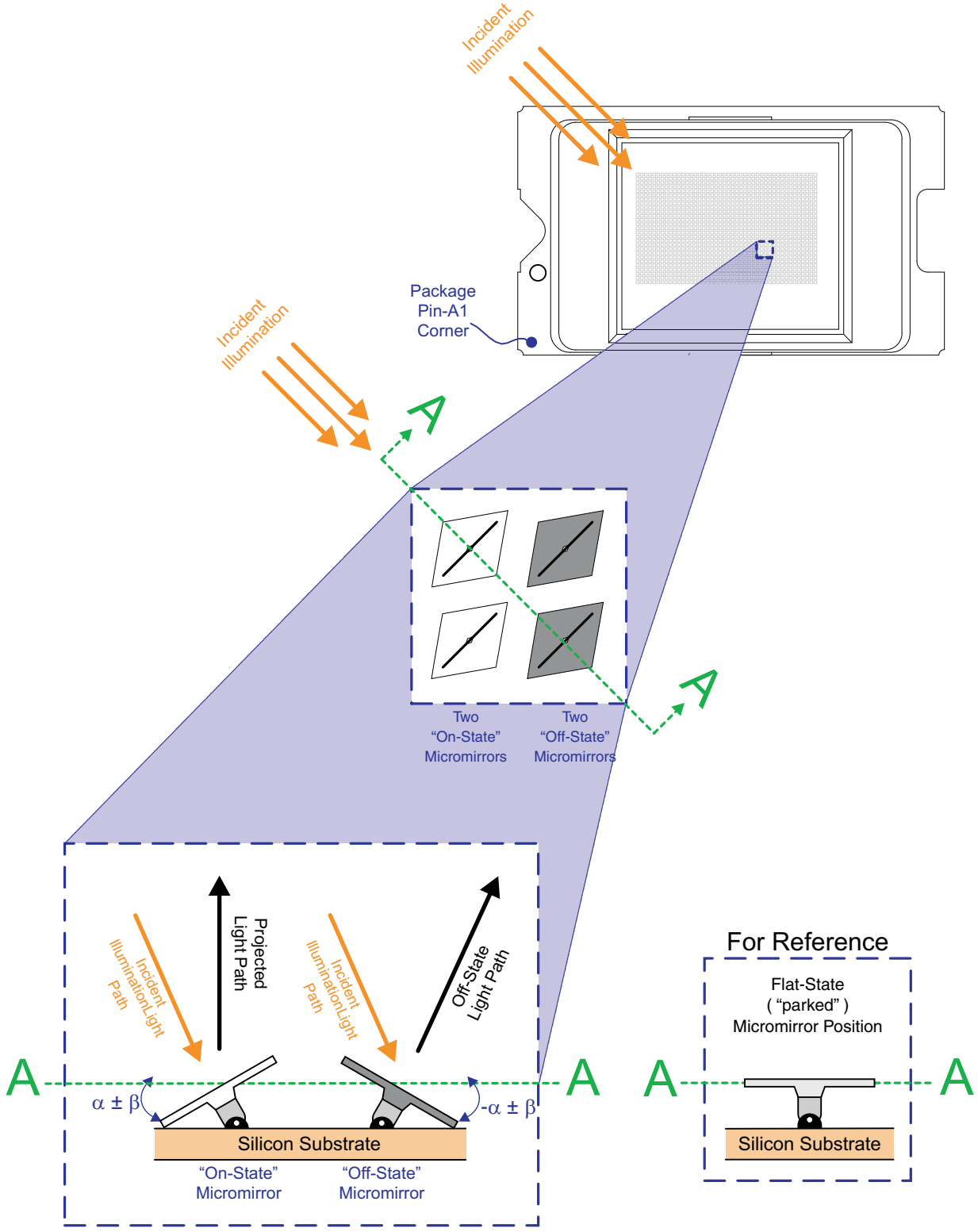


Figure 4. Micromirror Landed Positions and Light Paths

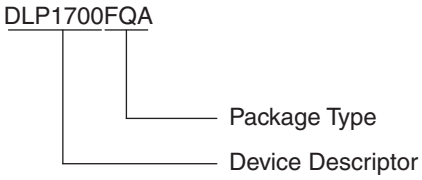
Related Documents

The following documents contain additional information related to the use of the DLP1700 device:

Table 1. Related Documents

DOCUMENT	TI LITERATURE NUMBER
DLP 0.17 HVGA Chip-Set data sheet	DLPS017
DLPC100 Digital Controller data sheet	DLPS019
DLPR100 Configurable PROM data sheet	DLPS020

Orderable Part Number



Device Marking

The device marking consists of the fields shown in Figure 5.

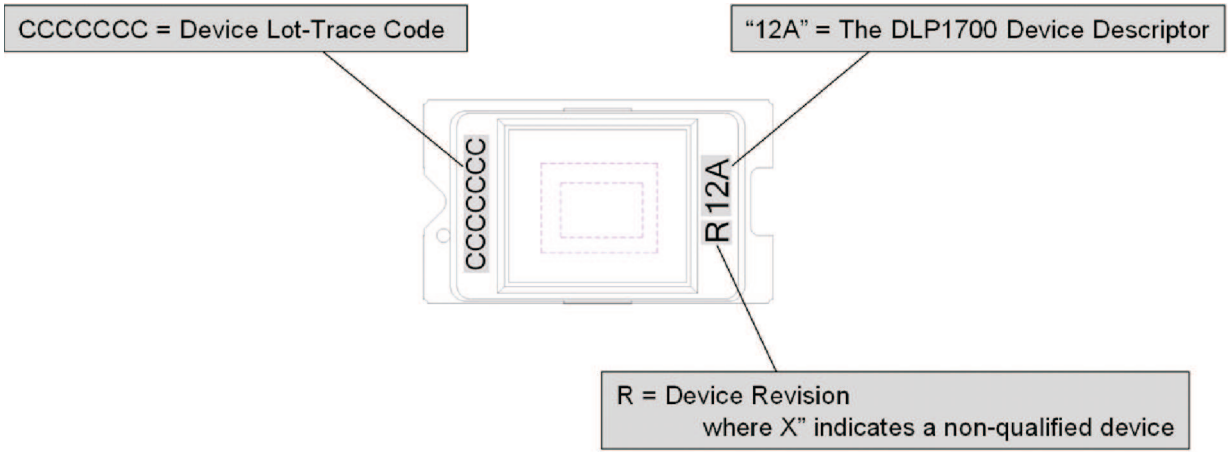


Figure 5. DMD Marking (Device Top View)

Device Terminals

Figure 6. Package Connector Signal Names (Device Bottom View)

Table 2. Terminal Characteristics

TERMINAL NAME	PIN	I/O/P	TYPE	INTERNAL TERMINATION	CLOCKED BY	DATA RATE	DESCRIPTION
Data Inputs							
D(0)	C3	Input	LVCMOS	None	DCLK	DDR	Input data bus
D(1)	C7	Input	LVCMOS	None	DCLK	DDR	
D(2)	C9	Input	LVCMOS	None	DCLK	DDR	
D(3)	C10	Input	LVCMOS	None	DCLK	DDR	
D(4)	C11	Input	LVCMOS	None	DCLK	DDR	
D(5)	D16	Input	LVCMOS	None	DCLK	DDR	
D(6)	D14	Input	LVCMOS	None	DCLK	DDR	
D(7)	D13	Input	LVCMOS	None	DCLK	DDR	
D(8)	D11	Input	LVCMOS	None	DCLK	DDR	
D(9)	D10	Input	LVCMOS	None	DCLK	DDR	
DCLK	D9	Input	LVCMOS	None	–	–	Input data bus clock
Data Control Inputs							
LOADB	D8	Input	LVCMOS	None	DCLK	DDR	Parallel data load enable
TRC	D3	Input	LVCMOS	None	DCLK	DDR	Input data toggle rate control
SCTRL	D6	Input	LVCMOS	None	DCLK	DDR	Serial control bus
SACBUS	D21	Input	LVCMOS	None	SACCLK	DDR	Serial SAC bus data
SACCLK	D19	Input	LVCMOS	None	–	–	Serial SAC bus clock
Mirror Reset Control Inputs							
RST_A0	C18	Input	LVCMOS	None	RST_STB	SDR	Reset block address select
RST_A1	C16	Input	LVCMOS	None	RST_STB	SDR	
RST_A2	C19	Input	LVCMOS	None	RST_STB	SDR	
RST_MODE	C13	Input	LVCMOS	None	RST_STB	SDR	Reset driver mode
RST_SEL0	D18	Input	LVCMOS	None	RST_STB	SDR	Reset driver output level select
RST_SEL1	C14	Input	LVCMOS	None	RST_STB	SDR	
RST_STB	C20	Input	LVCMOS	None	–	–	Reset driver input strobe
RST_$\overline{OE}$	C17	Input	LVCMOS	None	–	–	Reset driver output enable
Power							
V_{BIAS}	D20	Power	Analog	None	–	–	Mirror reset bias voltage
V_{OFFSET}	D4	Power	Analog	None	–	–	Mirror reset offset voltage
V_{RST}	C6	Power	Analog	None	–	–	Mirror reset voltage
V_{REF}	C4	Power	Analog	None	–	–	Power supply for double data rate low voltage CMOS logic terminals
V_{CC}	C5, C12, D5, D15	Power	Analog	None	–	–	Power supply for single data rate LVCMOS logic terminals
V_{SS}	C1, C2,C8, C15, C21, C22, C23, D1, D2, D7, D12, D17, D22, D23	Power	Analog	None	–	–	Common return for all power inputs
NO_CONNECT	A1–A15, B1–B15, E1–E15, F1–F15	–	–	–	–	–	No connection (Any connection to these terminals may result in undesirable effects)

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted). Stresses beyond those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. The Absolute Maximum Ratings are stress ratings only, and functional performance of the device at these or any other conditions beyond those indicated under " Recommended Operating Conditions" is not implied. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability.

PARAMETER		CONDITIONS	MIN	MAX	UNIT
Electrical					
V_{CC}	Voltage applied to V_{CC} (1)(2)		–0.5	4	V
V_{REF}	Voltage applied to V_{REF} (1)(2)		–0.5	4	V
V_{OFFSET}	Voltage applied to V_{OFFSET} (1)(2)(3)		–0.5	9	V
V_{BIAS}	Voltage applied to V_{BIAS} (1)(2)(3)		–0.5	17	V
V_{RST}	Voltage applied to V_{RST} (1)(2)		–11	0.5	V
	Delta supply voltage $\lvert V_{BIAS} - V_{OFFSET} \rvert$ (3)			9.0	V
	Voltage applied to all other input terminals (1)		–0.5	V_{REF} + 0.3	V
	Current required from a high-level output	V_{OH} = 2.4 V		–20	mA
	Current required from a low-level output	V_{OL} = 0.4 V		15	mA
Environmental					
T_C	Case temperature (4)	Operating	–10	70	°C
		Non-operating	–40	80	
	Device temperature gradient (5)	Operating		10	°C
	Local ambient relative humidity (6)	Operating		95	%
		Non-operating		95	
	Illumination power density (7)	< 400 nm		2	mW/cm^2
		400 to 700		See (8)	
		> 700 nm		10	
	Electrostatic discharge immunity (9)	All pins		2000	V

(1) All voltages referenced to V_{SS} (ground).
(2) Voltages V_{CC}, V_{REF}, V_{OFFSET}, V_{BIAS}, and V_{RST} are required for proper DMD operation.
(3) Exceeding the recommended allowable absolute voltage difference between V_{BIAS} and V_{OFFSET} may result in excess current draw.
(4) Case temperature as measured at the Thermal Test Point indicated in Figure 11.
(5) As measured between any two points on the exterior of the package, or as predicted between any two points inside the micromirror array cavity. Refer to the Thermal Characteristics for information related to calculating the micromirror array temperature.
(6) Non-condensing
(7) Total integrated illumination power density, above or below the indicated wavelength threshold.
(8) Limited only by the resulting case temperature.
(9) Tested in accordance with JESD22-A114-B Electrostatic Discharge (ESD) sensitivity testing Human Body Model (HBM).

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by the Recommended Operating Conditions. No level of performance is implied when operating the device above or below the Recommended Operating Conditions limits.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Electrical						
V_{REF}	LVCMOS interface supply voltage (1)(2)		1.65	1.8	1.95	V
V_{CC}	LVCMOS logic supply voltage (1)(2)		2.25	2.5	3.6	V
V_{OFFSET}	Mirror electrode and HVCMOS supply voltage (1)(2)(3)		8.25	8.5	8.75	V
V_{BIAS}	Mirror electrode voltage (1)(2)(3)		15.5	16	16.5	V
V_{RST}	Mirror electrode voltage (1)(2)		– 9.5	–10	–10.5	V
	Delta supply voltage $\lvert V_{BIAS} - V_{OFFSET} \rvert$ (3)				8.75	V
V_{T+}	Positive-going threshold voltage		0.4 × V_{REF}		0.7 × V_{REF}	V
$V_{T–}$	Negative-going threshold voltage		0.3 × V_{REF}		0.6 × V_{REF}	V
V_{hys}	Hysteresis voltage ($V_{T+} – V_{T–}$)		0.1 × V_{REF}		0.4 × V_{REF}	V
I_{OH}	High-level output current	V_{OH} = 2.4 V, V_{CC} ≥ 3.0 V			–20	mA
		V_{OH} = 1.7 V, V_{CC} ≥ 2.25 V			–15	
I_{OL}	Low-level output current	V_{OL} = 0.4 V, V_{CC} ≥ 3.0 V			15	mA
		V_{OL} = 0.4 V, V_{CC} ≥ 2.25 V			14	
f_{DCLK}	DCLK clock frequency		40		60	MHz
Mechanical						
	Static load applied to the package electrical connector area (4) (5)				45	N
	Static load applied to the DMD mounting area (6) (5)				100	N
Environmental						
T_C	Case Temperature (7)		0		70	°C

(1) All voltages referenced to V_{SS} (ground).
(2) Voltages V_{CC}, V_{REF}, V_{OFFSET}, V_{BIAS}, V_{RST} are required for proper DMD operation.
(3) Exceeding the recommended voltage difference between V_{BIAS} and V_{OFFSET} may result in excessive current draw. See the Absolute Maximum Ratings for further details.
(4) Load should be uniformly distributed across the entire connector area. Refer to the Package Mechanical Characteristics for size and location of the connector interface area.
(5) See Figure 7
(6) Load should be uniformly distributed across the 3 datum-A surfaces. Refer to the Package Mechanical Characteristics for size and location of the datum-A surfaces.
(7) Case temperature as measured at the Thermal Test Point indicated in Figure 11

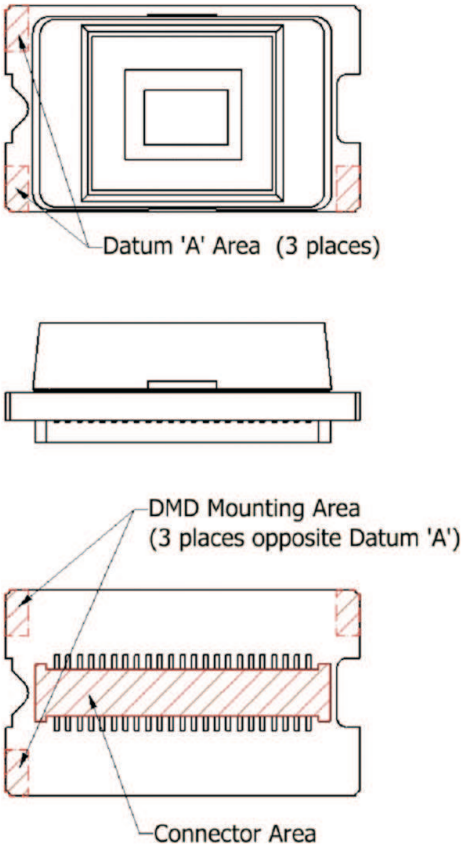


Figure 7. System Interface Loads

ELECTRICAL CHARACTERISTICS

over the range of recommended supply voltage and recommended case operating temperature (unless otherwise noted)

PARAMETER		CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage (1)	V_{CC} = 3.3 V,	I_{OH} = –34 mA	2.4		V
		V_{CC} = 2.5 V,	I_{OH} = –23 mA	1.7		
V_{OL}	Low-level output voltage (1)	V_{CC} = 3.3 V,	I_{OH} = 19 mA		0.4	V
		V_{CC} = 2.5 V,	I_{OH} = 16 mA		0.4	
I_{OZ}	High impedance output current (1)	V_{CC} = 3.6 V			10	µA
I_{IL}	Low-level input current (1)	V_{REF} = 1.95 V,	V_I = 0 V	–1.6		nA
I_{IH}	High-level input current (1)	V_{REF} = 1.95 V,	V_I = V_{REF}		1.9	nA
I_{REF}	Current into V_{REF} terminal	V_{REF} = 1.95 V,	f_{DCLK} = 40 MHz		0.4	
			f_{DCLK} = 60 MHz		0.61	
I_{CC}	Current into V_{CC} terminal	V_{CC} = 2.75 V,	f_{DCLK} = 40 MHz		20.6	mA
			f_{DCLK} = 60 MHz		30.8	
		V_{CC} = 3.6 V,	f_{DCLK} = 40 MHz		28	
			f_{DCLK} = 60 MHz		41.8	
I_{OFFSET}	Current into V_{OFFSET} terminal (2)	V_{OFFSET} = 8.75 V			0.77	mA
I_{BIAS}	Current into V_{BIAS} terminal (2)	V_{BIAS} = 17 V, 3 mirror resets in 200 µs	RST_$\overline{OE}$ = Low		0.77	mA
			RST_$\overline{OE}$ = High		2.1	
I_{RST}	Current into V_{RST} terminal	V_{RST} = –12 V, 3 mirror resets within 200 µs			0.44	mA
P_{REF}	Power into V_{REF} terminal (3)	V_{REF} = 1.95 V,	f_{DCLK} = 40 MHz		0.77	mW
			f_{DCLK} = 60 MHz		1.18	
P_{CC}	Power into V_{CC} terminal (3)	V_{CC} = 2.75 V,	f_{DCLK} = 40 MHz		56.6	mW
			f_{DCLK} = 60 MHz		84.7	
		V_{CC} = 3.6 V,	f_{DCLK} = 40 MHz		100	
			f_{DCLK} = 60 MHz		150	
P_{OFFSET}	Power into V_{OFFSET} terminal (3)	V_{OFFSET} = 8.75 V			6.7	mW
P_{BIAS}	Power into V_{BIAS} terminal (3)	V_{BIAS} = 17 V, 3 mirror resets within 200 µs	RST_$\overline{OE}$ = Low		14.2	mW
			RST_$\overline{OE}$ = High		35.5	
P_{RST}	Power into V_{RST} terminal (3)	V_{RST} = –12 V,			5.3	mW
C_I	Input capacitance (1)	f = 1 MHz			10	pF
C_O	Output capacitance (1)	f = 1 MHz			10	pF

(1) Applies to LVCMOS pins only.
(2) Exceeding the maximum allowable absolute voltage difference between V_{BIAS} and V_{OFFSET} may result in excesses current draw. (Refer to Absolute Maximum Ratings for details)
(3) In some applications, the total DMD heat load can be dominated by the amount of incident light energy absorbed. Refer to the Thermal Characteristics for further details.

SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
t_{s1}	Setup time: DATA before rising or falling edge of DCLK	1.5			ns
	Setup time: TRC before rising or falling edge of DCLK	1.5			
	Setup time: SCTRL before rising or falling edge of DCLK	1.5			
t_{s2}	Setup time: LOADB low before rising edge of DCLK	1.5			ns
t_{s3}	Setup time: SAC_BUS low before rising edge of SAC_CLK	1.5			ns
t_{h1}	Hold time: DATA after rising or falling edge of DCLK	1.5			ns
	Hold time: TRC after rising or falling edge of DCLK	1.5			
	Hold time: SCTRL after rising or falling edge of DCLK	1.5			
t_{h2}	Hold time: LOADB low after falling edge of DCLK	1.5			ns
t_{h3}	Hold time: SAC_BUS low after rising edge of SAC_CLK	1.5			ns
t_{c1}	Clock cycle: DCLK	16.67		25	ns
t_{c3}	Clock cycle: SAC_CLK	16.67		25	ns
t_{w1}	Pulse width high or low: DCLK	6.67			ns
t_{w2}	Pulse width low: LOADB	6.67			ns
t_{w3}	Pulse width high or low: SAC_CLK	6.67			ns
t_r	Rise time (20% – 80%): DCLK / SAC_CLK			2.5	ns
	Rise time (20% – 80%): DATA / TRC / SCTRL / LOADB			2.5	
t_f	Fall time (20% – 80%): DCLK / SAC_CLK			2.5	ns
	Fall time (20% – 80%): DATA / TRC / SCTRL / LOADB			2.5	

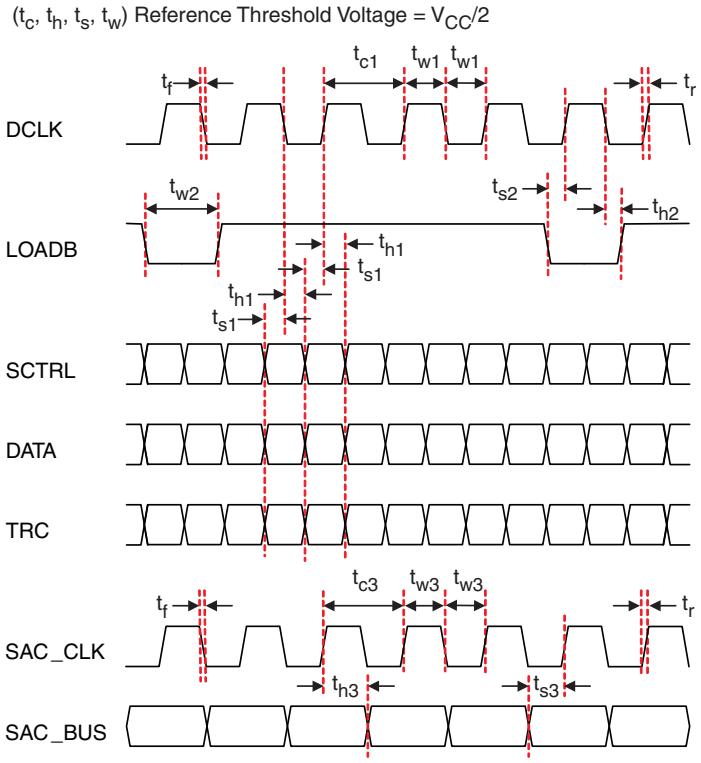


Figure 8. Switching Characteristics

LOAD CIRCUIT

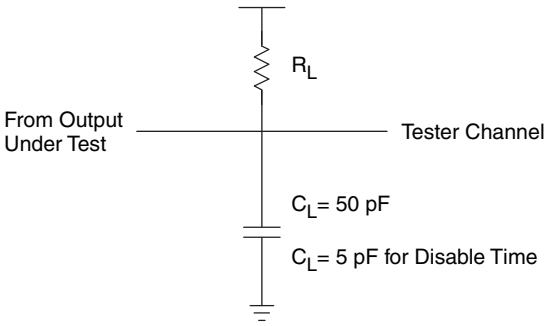


Figure 9. LVCMOS Output Test Load

POWER-UP AND POWER-DOWN PROCEDURES

CAUTION

Reliable performance of the DMD requires that the following conditions be met:

1) That the VCC, VREF, VOFFSET, VBIAS, and VRESET power supply inputs all be present during operation
2) That the VCC, VREF, VOFFSET, VBIAS, and VRESET power supplies be sequence on and off in the manner perscribed below.

Repeated failure to adhere to the prescribed power-up and power-down procedures may affect device reliability

DMD Power Supply Power-Up Procedure

Step 1: Power-Up V_{CC} and V_{REF} in any order

Step 2: Wait for V_{CC} and V_{REF} to each reach a stable level within their respective recommended operating ranges.

Step 3: Power-Up V_{BIAS}, V_{OFFSET}, and V_{RESET} in any order, provided that the maximum delta-voltage between V_{BIAS} and V_{OFFSET} is not exceeded (Refer to Absolute Maximum Ratings for details)

Note 1: ***During the Power-Up procedure, the DMD's LVCMOS inputs should not be driven high until after Step 2 has been completed***

Note 2: ***Power supply slew rates during Power-Up are unrestricted, provided that all other conditions are met***

DMD Power Supply Power-Down Procedure

Step 1: Command the Chip-Set Controller to execute a "mirror parking sequence". Refer to the Controller data sheet (listed in Related Documents) for details.

Step 2: Powerdown V_{BIAS}, V_{OFFSET}, and V_{RST} in any order, provided that the maximum delta voltage between V_{BIAS} and V_{OFFSET} is not exceeded. (Refer to Absolute Maximum Ratings for details)

Step 3: Wait for V_{BIAS}, V_{OFFSET}, and V_{RST} to each discharge to a stable level within 4 V of the reference ground.

Step 4: Powerdown V_{CC} and V_{REF} in any order.

Note 1: ***During the Power-Down procedure, the DMD's LVCMOS inputs should be held at a level less than V_{REF} + 0.3 volts***

Note 2: ***Power supply slew rates during Power-Down are unrestricted, provided that all other conditions are met***

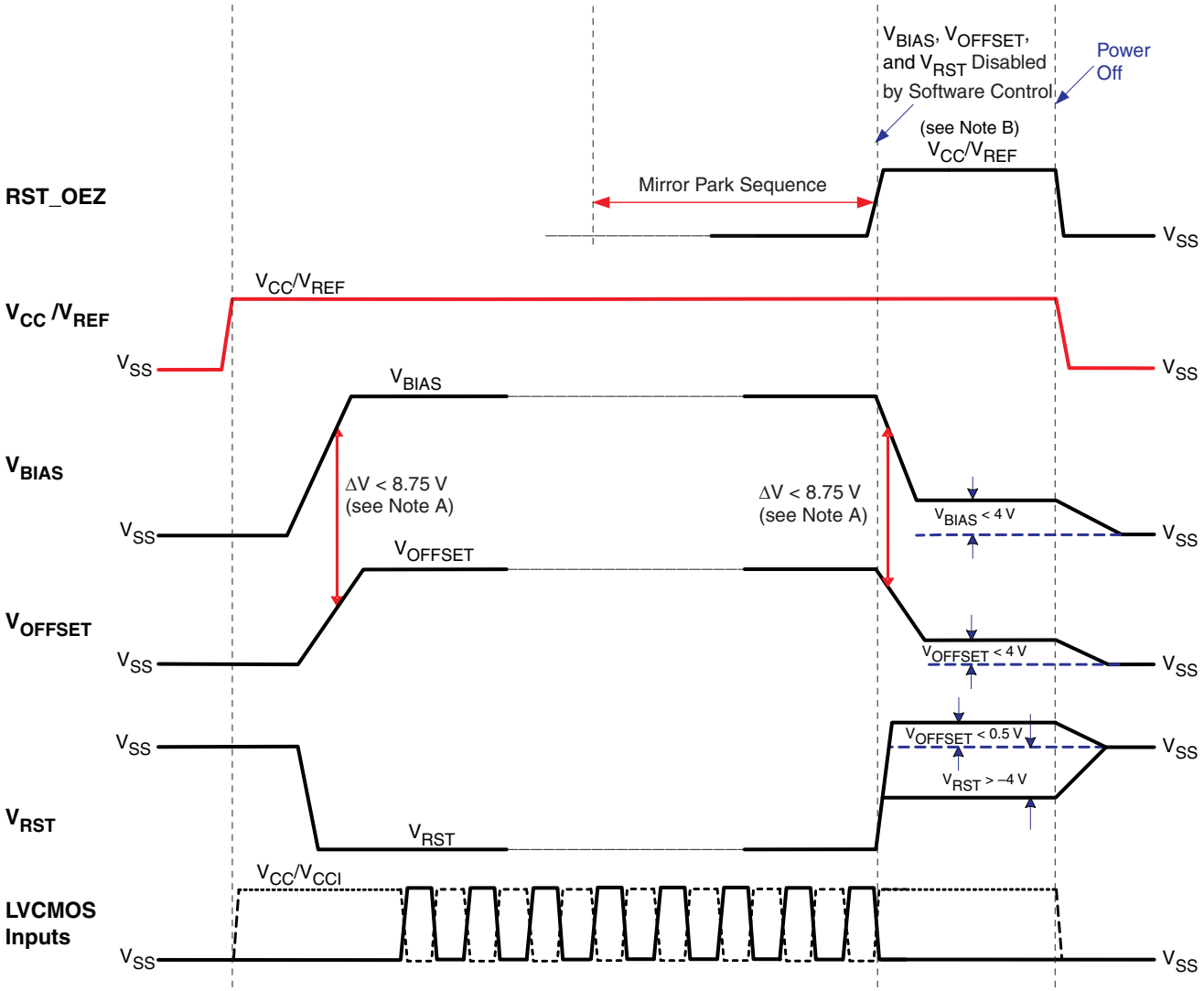


Figure 10. Power-Up / Power-Down Timing

Micromirror Array Physical Characteristics

Physical characteristics of the micromirror array are provided in Table 3. Additional details are provided in the Package Mechanical Characteristics section.

Table 3. Micromirror Array Physical Characteristics

PARAMETER	VALUE	UNITS
Number of active micromirror columns (1)	480	micromirrors
Number of active micromirror rows (1)	320	micromirrors
Micromirror pitch (1)	7.56	microns
Micromirror active array height (1)	320	micromirrors
	2419.2	microns
Micromirror active array width (1)	480	micromirrors
	3628.8	microns
Micromirror array border (2)	14	mirrors/side

(1) See Figure 3
(2) The mirrors that form the array border are hard-wired to tilt in the –12° (“Off”) direction once power is applied to the DMD (see Figure 3 and Figure 4).

Micromirror Array Optical Characteristics

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Refer to the related Application Notes (listed in Related Documents) for guidelines.

Table 4. Micromirror Array Optical Characteristics

	PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
α	Micromirror tilt angle	DMD "parked" state(1)(2)(3), see Figure 4		0		degrees
		DMD "landed" state(1)(4)(5), see Figure 4		12		
β	Micromirror tilt angle variation (1)(4)(6)(7)(8)	See Figure 4	–1		1	
	Orientation of the micromirror axis-of-rotation(9)	See Figure 3		45		
	Micromirror axis-of-rotation orientation variation(9)			See(10)		
	Micromirror array optical efficiency(11)(12)	420 nm to 700 nm, with all micromirrors in the ON state		68		%
	Window material			Corning Eagle XG		
	Window refractive index	at 546.1 nm		1.5119		
	Window flatness(13)	per 25 µm			4	fringes
	Window aperture			See (14)		

(1) Measured relative to the plane formed by the overall micromirror array
(2) "Parking" the micromirror array returns all of the micromirrors to an essentially flat (0˚) state (as measured relative to the plane formed by the overall micromirror array).
(3) When the micromirror array is "parked", the tilt angle of each individual micromirror is uncontrolled.
(4) Additional variation exists between the micromirror array and the package datums, as shown in the Package Mechanical Characteristics section.
(5) When the micromirror array is "landed", the tilt angle of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of "1" will result in a micromirror "landing" in an nominal angular position of "+12 degrees". A binary value of 0 will result in a micromirror "landing" in an nominal angular position of "-12 degrees".
(6) Represents the "landed" tilt angle variation relative to the Nominal "landed" tilt angle.
(7) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
(8) For some applications, it is critical to account for the micromirror tilt angle variation in the overall System Optical Design. With some System Optical Designs, the micromirror tilt angle varation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some System Optical Designs, the micromirror tilt angle variation between devices may result in colorimetry variations and/or system contrast varations.
(9) Measured relative to the package datums "B" and "C", shown in the Package Mechanical Characteristics section.
(10) Variation of the micromirror axis-of-rotation is subject to the location tolerance of the active array, as shown in the Package Mechanical Characteristics section.
(11) The minimum or maximum DMD optical efficiency observed in a specific application depends on numerous application-specific design variables, such as:
  (a) Illumination wavelength, bandwidth/line-width, degree of coherence
  (b) Illumination angle, plus angle tolerance
  (c) Illumination and projection aperture size, and location in the system optical path
  (d) IIllumination overfill of the DMD micromirror array
  (e) Aberrations present in the illumination source and/or path
  (f) Aberrations present in the projection path
  (g) Etc.

  The specified nominal DMD optical efficiency is based on the following use conditions:
  (a) Visible illumination (420 nm – 700 nm)
  (b) Input illumination optical axis oriented at 24° relative to the window normal
  (c) Projection optical axis oriented at 0° relative to the window normal
  (d) f/3.0 illumination aperture
  (e) f/2.4 projection aperture

  Based on these use conditions, the nominal DMD optical efficiency results from the following four components:
  (a) Micromirror array fill factor: nominally 92.5%
  (b) Micromirror array diffraction efficiency: nominally 86%
  (c) Micromirror surface reflectivity: nominally 88%
  (d) Window transmission: nominally 97% (single pass, through two surface transitions)
(12) Does not account for the effect of micromirror switching duty cycle, which is application dependant. Micromirror switching duty cycle represents the percentage of time that the micromirror is actually reflecting light from the optical illumination path to the optical projection path. This duty cycle depends on the illumination aperture size, the projection aperture size, and the micromirror array update rate.
(13) At a wavelength of 632.8 nm.
(14) Refer to the Package Mechanical Characteristics for details regarding the size and location of the window aperture.

Thermal Characteristics

Achieving optimal DMD performance requires proper management of the maximum DMD case temperature, the maximum temperature of any individual micromirror in the active array, the maximum temperature of the window aperture, and the temperature gradient between any two points on or within the package.

Refer to the Absolute Maximum Ratings and Recommended Operation Conditions for applicable temperature limits.

Case Temperature

The temperature of the DMD case can be measured directly. For consistency, a Thermal Test Point location is defined, as shown in Figure 11.

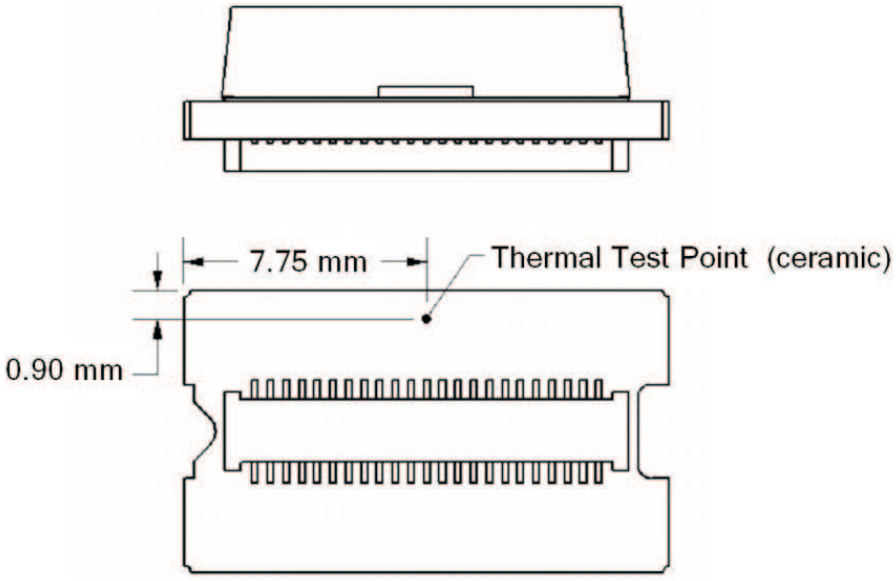


Figure 11. Thermal Test Point Location

Package Electrical Characteristics

The package interconnect trace lengths are provided in Table 5. Refer to the DLP 0.17 HVGA Chip-Set Data Sheet (TI literature number DLPS017) for details regarding signal integrity considerations for end-equipment designs.

Table 5. Package Trace Length Data

PIN NO.	PIN NAME	PACKAGE TRACE LENGTH (μm)
C1	V_{SS}	–
C2	V_{SS}	–
C3	D(0)	776
C4	V_{REF}	–
C5	V_{CC}	–
C6	V_{RST}	–
C7	D(1)	2903
C8	V_{SS}	–
C9	D(2)	4145
C10	D(3)	4596
C11	D(4)	5472
C12	V_{CC}	–
C13	RST_MODE	5292
C14	RST_SEL1	4536
C15	V_{SS}	--
C16	RST_A1	3418
C17	RST_$\overline{OE}$	3839
C18	RST_A0	3278
C19	RST_A2	2525
C20	RST_STB	3024
C21	V_{SS}	–
C22	V_{SS}	–
C23	V_{SS}	–
D1	V_{SS}	–
D2	V_{SS}	–
D3	TRC	632
D4	V_{OFFSET}	–
D5	V_{CC}	–
D6	SCTRL	2513
D7	V_{SS}	–
D8	LOADB	3270
D9	DCLK	4173
D10	D(9)	4471
D11	D(8)	5335
D12	V_{SS}	–
D13	D(7)	6171
D14	D(6)	6917
D15	V_{CC}	–
D16	D(5)	8145
D17	V_{SS}	–
D18	RST_SEL0	3564
D19	SACCLK	4515

Table 5. Package Trace Length Data (continued)

PIN NO.	PIN NAME	PACKAGE TRACE LENGTH (µm)
D20	V_{BIAS}	–
D21	SACBUS	716
D22	V_{SS}	–
D23	V_{SS}	–

Package Mechanical Characteristics

The mechanical characteristics of the DLP1700 are specified on the following pages.

Table 6. Revision History

REVISION	SECTION(S)	COMMENT
*	All	Initial release
A	All	Refined content
B	Table 4	Added table note "At a wavelength of 632.8 nm"

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLP1700FQA	LIFEBUY	LCCC	FQA	46		Green (RoHS & no Sb/Br)	Call TI	Level-1-NC-NC			

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

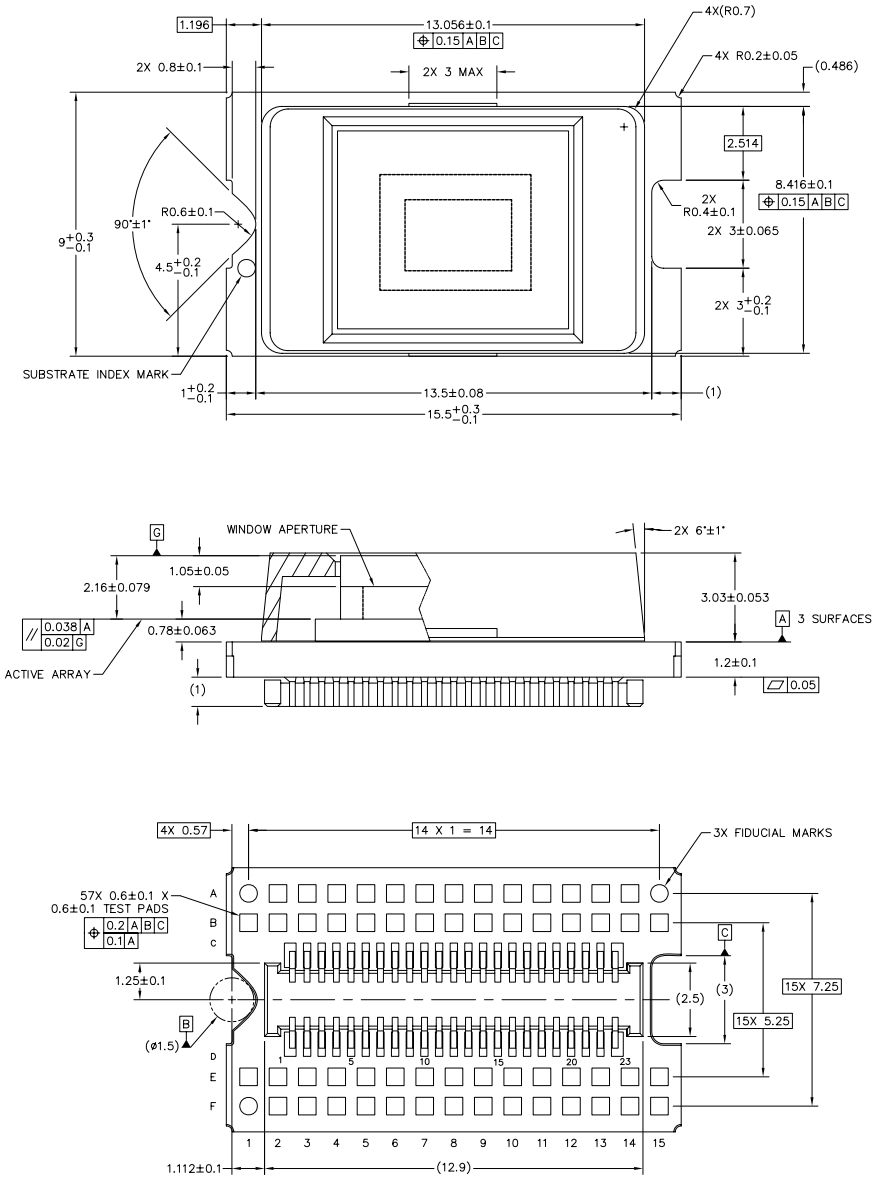
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

FQA (R–CLGA–N46) CERAMIC LAND GRID ARRAY PACKAGE



4210798/A 12/09

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Pins shall be gold plated.

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